INTEGRATED MICROWAVE RADIATOR AND GENERATOR

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to dipole radiators and, more particularly, to a hybrid integrated dipole radiator having a negative resistance semiconductor element mounted thereon and providing an impedance-transformation network for establishing oscillations for driving the radiator.

2. Description of the Prior Art

Heretofore in the prior art, much study has been made of microwave power generation by diode elements of the IMPATT (abbreviation for impatt ionization transit time, or avalanche transit time) types such as Read diodes, as well as those of the bulk effect, or GUNN type. Particular interest in the use of such devices for microwave applications results from the miniaturization capability thereby afforded.

Miniaturized radiating devices are adaptable for numerous microwave applications, such as use as elements of a large array for a radar system, in beacon service, and as active chaff. Array-type systems may be of two types, one in which all elements radiate independently to generate a multiplicity of spectral lines and in which the power is radiated into a solid angle characteristic of a dipole radiator, and another in which the elements are coupled and phase locked to produce coherent output radiation of the individual elements and form a directive beam. Prior art structures typically have required physical displacement or separation of the microwave oscillating source and the radiating element to enable the required closely spaced relationships of the radiating elements as required in a radar array. The oscillating source and the radiating element to enable the required closely spaced relationships of the radiating elements a required in a radar array. The oscillating source and the radiating element therefore required interconnection by a transmission line, inherently introducing transmission line losses, undue phase sensitivity, and additionally resulting in an undesirably large and complex system.

Where microwave systems are required for use as active chaff or in beacon applications, it is necessary that the oscillating and radiating structure be compact, of reasonable power output, and of minimum cost. Particularly, in beacon type applications, such as for homing systems, the expense of the oscillating and radiating devices must be such as to economically justify disposing of the radiation system once the lost object or person is located. Prior art devices fail to satisfy these combined requirements of size, low cost, and sufficiently high power output.

SUMMARY OF THE INVENTION

These and other defects and inadequacies of prior art systems and structures are overcome by the integrated microwave radiator of the invention.

In accordance with the invention, the microwave radiator comprises a hybrid integrated circuit including a dipole radiator on which is mounted a two terminal semiconductor element having negative resistance characteristics. The element may comprise an IMPATT type device or a GUNN type device capable of oscillation as a diode oscillator. The impedance-transforming network required for oscillations is provided by suitable forming of, and electrical connections to, the radiator and particularly includes lumped and distributed impedance elements and values. The hybrid-integrated structure therefore provides an impedance-transforming network for conjugate matching of the susceptance and negative conductance of the semiconductor element and the driving point impedance of the radiator to provide for generation of signal oscillations.

The semiconductor element is physically mounted on a portion of the radiator near the driving point thereof and preferably, as in one embodiment, disposed in the neutral plane of the radiator. The hybrid integrated structure may be

formed by the deposition and selective etching techniques on a suitable substrate which furthermore may be positioned in displaced relationship from a reflecting plane to afford control of the radiation pattern. In addition to providing certain of the conjugate impedance-matching elements, the radiating element may also provide thermal dissipation, or a heat sink, for the semiconductor element.

The hybrid integrated microwave radiator of the invention is physically compact in size, employs a minimum of components, and of relatively low cost. The radiator also is efficient in operation, particularly due to elimination of coupling transmission line losses between the semiconductor oscillating element and the radiating element.

The device of the invention is therefore ideally suited for numerous microwave applications. These and other features and advantages of the apparatus of the invention will become apparent and more fully understood from the following description of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a perspective view of a first embodiment of an integrated microwave radiator in accordance with the invention;

FIG. 2 is a cross-sectional view of a portion of the apparatus of FIG. 1 taken along the line 2—2;

FIG. 3 is a planar view of a second embodiment of an integrated microwave radiator in accordance with the invention; and

FIG. 4 is a schematic of an equivalent circuit of the integrated microwave radiator of the invention in accordance with either of the foregoing embodiments thereof.

DETAILED DESCRIPTION OF THE INVENTION

In FIG. 1 is shown a first embodiment of an integrated microwave radiator in accordance with the invention. The device 10 includes a substrate 12 on which are formed dipole-radiating elements 14 and 16, respectively having integral bias leads 18 and 20 oriented perpendicularly thereto and positioned at the central or driving points of the radiating elements 14 and 16. The substrate 12 may be of any suitable insulating material such as alumina or beryllia and the radiating elements and associated bias leads may be of any suitable conducting material such as chrome-gold. Preferably, the radiator elements and bias leads are formed by depositing a layer of chrome-gold on the substrate 12 which is thereafter operated upon by conventional photoresist techniques to produce the pattern shown in FIG. 1. The radiating elements 14 and 16 comprise a flat dipole of approximately one-half wavelength in physical length at the operating frequency.

The device 10, as noted, comprises a hybrid-integrated oscillator-radiator providing a single compact structure both he source of oscillations and the radiator or antenna, specifically the dipole elements 14 and 16 in FIG. 1. The active element of the oscillating circuit comprises a two terminal negative resistance semiconductor device 22 mounted on one of the dipole radiators and particularly on the radiator 14 preferably by ultrasonic bonding for mechanical and electrical connection thereto. Preferably, the element 22 comprises either an IMPATT (abbreviation for impatt ionization transit time, or avalanche transit time) device such as a Read diode, or a bulk effect semiconductor device, such as a GUNN diode. Hereinafter, the element 22 is referred to as a diode inclusive of any of the described types of devices. A lead wire or ribbon 24, typically gold, connects the exposed terminal of the diode 22 to the other element 16 of the radiator, or antenna, to which it is bonded as shown at 26.

An impedance-transforming network is required to satisfy conditions of oscillation of the diode 22 particularly due to the loading by the impedance of the antenna with which it is associated. The network includes tabs 30 and 32 formed preferably integrally with the radiating elements 14 and 16 and corresponding parts of a capacitive structure 34, the construction of which is described in detail hereinafter. The

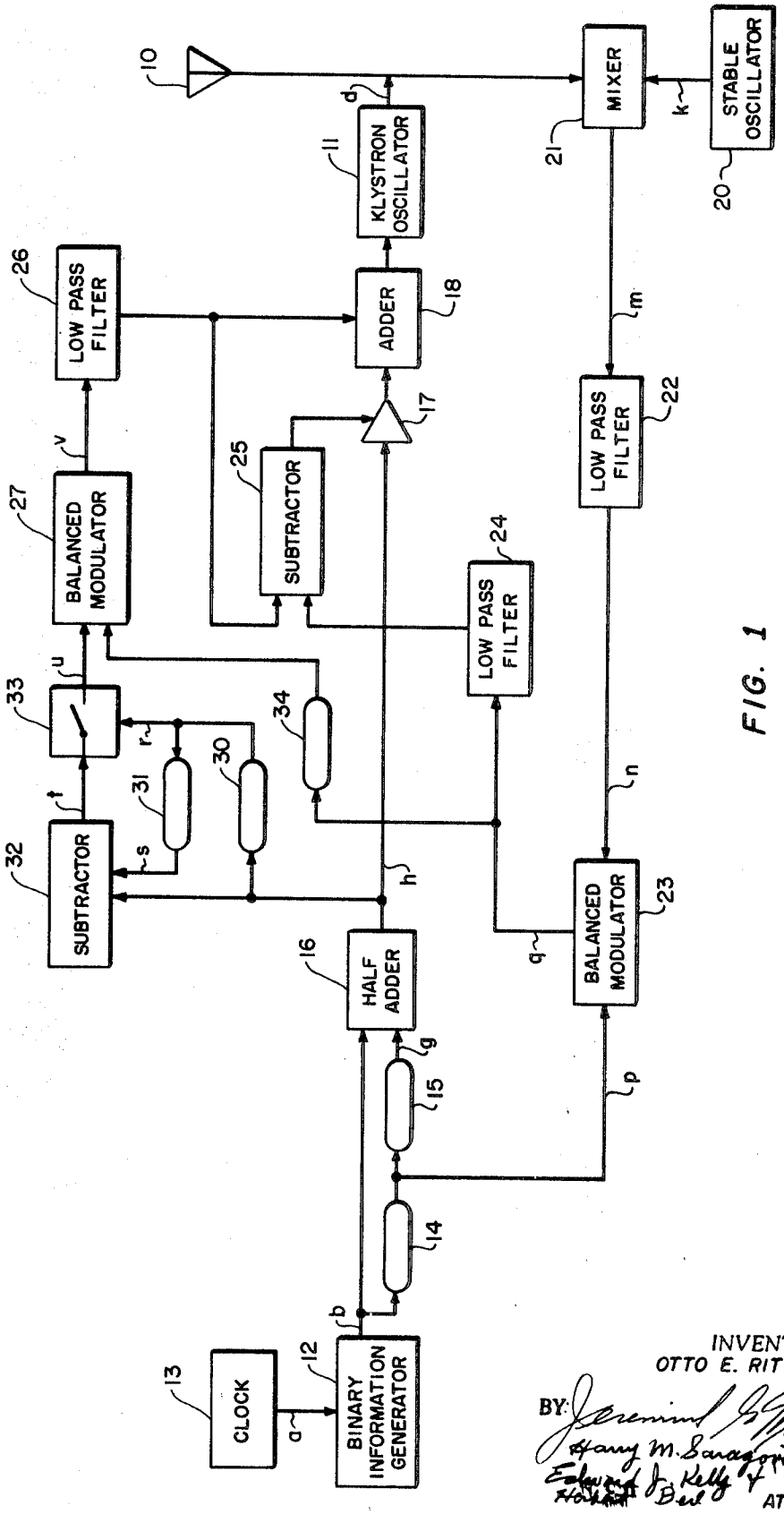


FIG. 1

INVENTOR,
OTTO E. RITTENBACH

BY: Jeremiah S. Mahoney AGENT
Harry M. Saragovitz,
Edward J. Kelly,
Herbert Berl
ATTORNEYS

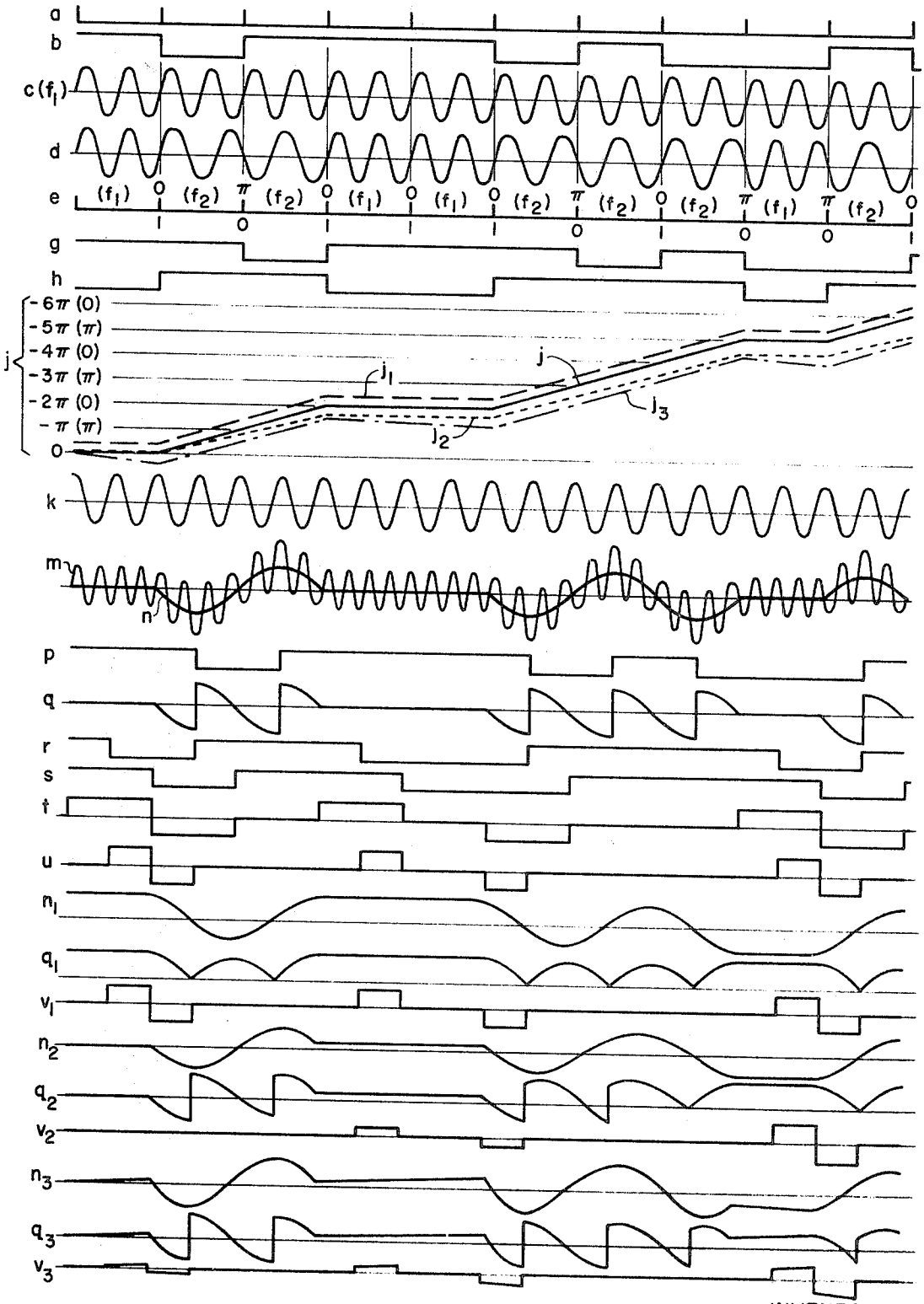


FIG. 2

INVENTOR:
OTTO E. RITTENBACH

BY: Jerome S. Mennemeyer AGENT
Harry M. Saragovitz,
Edmund J. Kelly &
Herbert Berl ATTORNEYS.

PHASE-MODULATED BINARY DATA TRANSMISSION SYSTEM EMPLOYING A VARIABLE FREQUENCY OSCILLATOR

The present invention relates to communication systems and more particularly to a binary transmission system for transmitting a phase-reversed carrier signal.

In the field of communications it has been the general practice to transmit binary information by periodically reversing the phase of a carrier signal in accordance with the information being transmitted. If the phase of the carrier signal is reversed instantaneously by, for example, balanced modulation, overtones and beat frequencies will be generated, thereby increasing substantially the bandwidth. However, if phase reversal of the carrier signal is accomplished gradually by instantaneously changing only the frequency of the carrier signal by a small amount, such that a proper phase reversal exists at the end of the clock period, then the bandwidth of the transmitted signal will be relatively narrow. A system for producing such a phase modulated signal is disclosed in my copending patent application, Ser. No. 872,969, filed Oct. 31, 1969, entitled Binary Transmission By Phase Modulation. That system derives from a highly stable oscillator two phase-related signals closely spaced in frequency. A switching circuit switches the output between these frequencies in accordance with the information to be transmitted. Of course, in order to produce high-power signals with this system, high-power amplifiers could be employed at obvious locations. However, to obtain both higher powers and higher frequency carrier signals, it becomes necessary to employ a less stable oscillator such as for example, the klystron oscillator. When using the klystron, minor instabilities in the output frequencies must be constantly detected and error signals must be generated such that the frequency of the klystron oscillator is changed such as to insure the proper phase relationships.

It is, therefore, the primary object of the present invention to provide a relatively narrow-band, high-power, phase-modulated communication system.

The exact nature of this invention as well as other objects and advantages thereof will be readily apparent from consideration of the following specification relating to the annexed drawing in which:

FIG. 1 shows a block diagram of a preferred embodiment of the invention; and

FIG. 2 shows waveforms useful in understanding the operation of the device of FIG. 1.

Referring now to the drawing there is shown in FIG. 1 a transmitter having an antenna 10 for radiating a phase-modulated signal generated by a high-power, variable frequency oscillator 11 such as a reflex klystron. A binary information generator 12 generates, in any well-known fashion, a binary signal in accordance with the information to be transmitted. The generator 12 operates under the influence and timing of a clock 13. The binary signal generated by generator 12 is modified by delays 14 and 15 and half adder 16 and then applied via variable gain amplifier 17 and adder 18 to the repeller of klystron oscillator 11 to vary the frequency thereof. The gain and bias of the delays 14 and 15, the half adder 16, the amplifier 17 and adder 18, are adjusted such that normally the klystron 11 will oscillate at either of two closely spaced frequencies depending on the level of the binary signal applied to the repeller thereof by adder 18. The exact nature and relationship of these two normal frequencies will be described later in greater detail. Generally, the frequency of the klystron 11 is switched such that the instantaneous phase of the output signal will normally reverse according to the information generated by generator 12 and at the rate of the clock signal 13. However, the output frequency of the klystron 11 may be slightly unstable due to excessive heating of the elements or variations in the bias voltages, etc. The instantaneous phase of the output as a result of such instabilities will gradually creep away from the normal or desired value and may, after several clock cycles, become intolerable if not corrected. Therefore, the phase of the output signal from klystron 11 is compared to the phase of an output signal from a stable oscillator 20 by a mixer 21 and a low pass filter 22. The output of filter 22, being an indication of the difference in phase between the oscillators 11 and 20, is then compared in balanced modulator 23 to the information signal generated by generator 12. If the detected difference in phase between oscillators 11 and 20 is not exactly correct at the right times i.e. in accordance with the information to be transmitted and at the clock rate, then feedback signals are generated which adjust the output of amplifier 17 and adder 18 which in turn will vary the bias on the repeller of klystron 11. The feedback signals are generated by first averaging the output of modulator 23 in filter 24 and by comparing in a subtractor 25 the output of filters 24 and 26. The output of subtractor 25 is used to adjust the gain of amplifier 17. Adder 18 adds the outputs of amplifier 17 and filter 26. The output of filter 26 is the average of the output of modulator 27. The output of half adder 16 is applied to a pair of delay elements 30 and 31. The output of delay 31 is subtracted from the output of half adder 16 in subtractor 32. The output of subtractor 32 is applied via normally closed switch 33 to modulator 27. Also applied to modulator 27 is the output of modulator 23 via delay 34.

The theory of operation will now be described with the aid of the waveforms shown in FIG. 2. Signal *a* represents the clock impulses generated by clock 13 that are applied to generator 12 which in turn generates, in any well known manner, a binary information signal such as signal *b* which represents a 1011101001. It is the purpose of the present transmitter to transmit a carrier signal *c* which is frequency modulated to cause phase differences of "0" and "π" radians at the clock time and in accordance with the information signal *b*. Therefore, ideally the output of klystron 11 may be represented by signal *d*, a relatively narrow band, frequency modulated wave having phase reversals at the clock rate and in accordance with the information signal *b*. The instantaneous phase of the waveform *d* with respect to waveform *c* at the clock rate *a* is shown just above line *e* and the corresponding binary information is shown below the phase. Waveform *d* is obtained by periodically changing the bias on the repeller of klystron 11, which is oscillating at a frequency f_1 (waveform *c*). As a result of the change in bias, the frequency of oscillation is slightly reduced to a frequency f_2. As can be seen from waveform *d*, f_2 is such that after one clock period or baud the phase of the modulated signal will be shifted π radians with respect to the carrier or reference signal f_1. In the example shown, f_1, is exactly twice the clock rate while f_2 is one and a half times the clock rate or three quarters of f_1. Of course, the closer f_1 and f_2 are to each other the narrower will be the bandwidth of waveform *d*, the transmitted signal. In general, f_1 and f_2 should differ in frequency by an odd multiple of one-half the clock rate.

Generation of signal *d* is accomplished by delaying in delays 14 and 15, the output of generator 12 (waveform *b*) one full clock period to obtain signal *g* and then applying signals *g* and *b* to half adder 16 to obtain signal *h*. Half adder 16 has a positive output when only one of the inputs *b* or *g* are positive. The output *h* of half adder 16 is then applied via variable gain amplifier 17 and adder 18 to the repeller of klystron 11 to vary the frequency thereof. For present, assume that the gain of amplifier 17 is unity and that the output of filter 26 is zero, so that the signal *h* passes through amplifier 17 and adder 18 unchanged. By comparing waveforms *h* and *d* it is seen that klystron 11 will normally oscillate at f_1 when *h* is equal to zero and will oscillate at f_2 when *h* is positive and equal to one unit. The instantaneous phase of the output signal *d* with respect to signal *c* will therefore advance linearly as shown by the solid line in waveforms *j*. However, because the klystron is subject to frequency and phase instabilities due to overheating or slight variations in the supply voltages, etc. the relative phase advancement might follow a path which is some combination of one of the paths j_1, j_2, and j_3. For example, if the frequencies f_1 and f_2 are correct but are out of phase slightly with respect to the reference signal *c*, then the relative phase advancement will follow the path shown by the long dashed line j_1. The short

dashed line j_2 represents the phase advancement, if f_1 is proper but f_2 is off slightly. Dashed line j_3 represents the phase advancement when f_2 is proper but f_1 is wrong. In order to correct these errors in phase, the klystron **11** output is constantly compared to the output k of the highly stable oscillator **20** which oscillates at f_1 and is displaced $\pi/2$ radians with respect to the carrier signal c.

For example, if signal d is proper and the phase is advancing along the solid line of j, then the output of mixer **21** may be represented by waveform m. Further the output n of filter **22** will then be the average value of m. Waveform b is delayed one-half the clock period by delay **14**, the output p of which is balanced modulated with n in modulator **23** to produce waveform q the average value of which is zero. Therefore, the output of filter **24** will be zero, if waveform d is properly phase related to oscillator **20** output k.

Also, signal h is delayed a half clock period in each delay **30** and **31** to produce signals r and s. Signal h is subtracted from s in subtractor **32** to give signal t. Signal t is switched by normally closed switch **33**, under the control of signal r, to produce an output signal u. Signal q is delayed a half clock period by delay **34** and then balanced modulated with signal u in modulator **27**. The output v of modulator **27** will be zero because signal q, after a delay of half a clock period, will line up with signal u such that u is zero when q is not and vice versa, thereby producing a zero output. Signal v is, of course, not shown in FIG. 2. It should now be clear that the output of modulator **27**, filter **26**, and subtractor **25** will be equal to zero when signal d is properly phase related with respect to signal k and the phase advancement of signal d is proceeding along the solid line j. In this case, therefore, the klystron **11** is stable and properly phased or, in other words, the signal h is providing the proper voltages to the repeller of klystron **11** to produce the correct output d and need not be altered by either amplifier **17** or adder **18**.

The output of klystron **11**, however, as explained above, may be in error thereby requiring adjustment of signal h. As indicated earlier, any error in the klystron output may be resolved into some combination of any one of three causes (1) only the phase is off and f_1 and f_2 are proper (path j_1), (2) f_2 is wrong and f_1 is proper (path j_2), and (3) f_1 is wrong and f_2 is proper (path j_3).

To illustrate the first case, assume that the phase of the output of klystron **11** is off by $\pi/2$ radians (worst case). In this case, the output of klystron **11** will be in phase with signal k and the average value of the output of mixer **21** will be of the form n_1. The output of modulator **23** will be q_1 which has an average value different from zero. Signal Q will be averaged by filter **24** the output of which will be proportional to the difference in phase between the actual output of klystron **11** and the desired output d. It is noted that an error in the phase of the klystron **11** output by $\pm\pi/2$ radians will produce the greatest outputs from filter **24**. The signal q_1 is also applied to modulator **27** via delay **34** producing a signal v_1, the average value of which is zero. Therefore, the output of filter **26** is zero in this case and, no correction to signal h will be made in adder **18**. However, the subtractor **25** which subtracts the output of filter **26** from the output of filter **24** will have an output which will vary the gain of amplifier **17**, thereby changing only the upper value of signal h. As a result, the repeller voltage of klystron **11** will be such that it will temporarily oscillate at a frequency slightly different then f_2, thereby slowly bringing the klystron **11** into proper phase.

To summarize, if the klystron **11** should be oscillating at the proper frequencies f_1 and f_2 but at the wrong phase the gain of the amplifier **17** will be varied such that only the high value of signal h will be correspondingly shifted thereby causing the klystron **11** to oscillate at a frequency slightly different then f_2 during those periods when it would otherwise be oscillating at f_2. It is during this period that the phase of the klystron **11** output signal will be corrected. When corrected of course, the error signal applied to amplifier **17** will also return to zero causing the gain of amplifier **17** to return to unity and the klystron **11** to again oscillate at f_2.

When f_1 is proper but f_2 is off (the second type of error listed above and illustrated by line j_2) the gain of amplifier **17** is again varied. In this case the output of filter **22** would be n_2. The output of modulator **23** is turn is q_2.

It can be seen by mere inspection that the average value of q_2 which appears at the output of filter **24**, will slowly increase as the relative phase of the klystron **11** output deviates more and more from the proper value due to the fact that klystron **11** is oscillating at a frequency different then f_2. Signal q_2 when delayed by delay **34** and modulated with signal u in modulator **27** will result in signal v_2 which has an average value of zero. Therefore, again the output of filter **26** is zero indicating that signal f_1 is correct. The output of filter **24** will be applied to amplifier **17** via subtractor **25**. As in the previous case, the gain of amplifier **17** will be correspondingly increased or decreased to raise or lower only the high voltage value of signal h. As before, this change will not alter the f_1 oscillations of klystron **11**, but will change the high value of the repeller voltage in a direction to correct the oscillations at f_2.

The third type of error is represented by line j_3 and occurs when f_1 is wrong and f_2 is correct. The output of filter **22** in this case will be n_3 and the output of modulator **23** will be q_3. It can be seen by inspection of q_3 that the output of filter **24** will slowly increase as the phase of the output of klystron **11** deviates from the proper value which is now a result of the error in f_1. Signal q_3 is also modulated with u after a delay in delay **34**. The output of modulator **27** will be v_3 and the average value thereof, as obtained from filter **26**, will in this case become slowly negative. This can be seen by inspection of v_3 where for every positive pulse there is a succeeding negative pulse which is slightly larger in absolute value. The output of filter **26** is then added to signal h to shift both the upper and lower values. The output of filter **26** is now subtracted from the output of filter **24** in subtractor **25** such that the upper value of signal h is shifted an amount equal and opposite to the amount it will be shifted in adder **18**. Therefore, the net result in this case will be to shift only the lower value of h an amount sufficient to correct for the error in only f_1. As a result, spurious fluctuations in the klystron **11** characteristics or in the power supplies and the bias voltages (not shown) will be immediately compensated for in amplifier **17** and adder **18**.

After transmission by antenna **10** and subsequent reception by a receiver the phase of signal d may be detected by any one of many well-known methods. For example, the slope of signal d could be measured in the receiver at the clock times as indicated on line e. Another method of detection of signal d is disclosed in my copending patent application, Ser. No. 875,682, filed Nov. 12, 1969, and entitled Binary Information Receivers for Detecting a Phase-Modulated Carrier Signal.

Obviously many modifications and variations of the present invention are possible in the light of the above teachings and the invention may be practiced otherwise than as specifically described.

What is claimed is:

1. A binary communication system for transmitting a carrier signal which is periodically of equal phase and of opposed phase with respect to a reference signal comprising; a clock means for generating a clock signal; a binary information generator means controlled by said clock means for generating a two-level information signal at the rate of said clock signal; control means connected to the output of said binary information generator means for shifting the levels of said two-level information signal; a variable frequency oscillator means for generating said carrier signal and having the frequency thereof shifted between first and second frequencies by the output of said control means; the difference between said first and second frequencies being equal to an odd multiple of one-half the rate of said clock signal; a stable oscillator means for generating a reference signal at said first frequency and at a fixed phase with respect to said clock signal; mixer means for comparing the outputs of each said oscillators to determine the difference in phases thereof; comparator means for comparing said two-level information signal to the output of said mixer means for generating first and

second error signals; said first error signal being a function of the phase differences detected by said mixer means and said second error signal being a function of the change in the difference in phase detected by said mixer means during the periods when said variable frequency oscillator should be operating at said first frequency; and means for applying said error signals to said control means for shifting the levels of said two-level information signal in accordance with said error signals.

2. The device according to claim 1 and wherein said control means includes; a subtractor means for generating a difference signal which is the difference between said first and second error signals; and a variable gain amplifier means being controlled by said difference signal for varying the difference between the levels of said two level information signal.

3. The device according to claim 2 and wherein said control means further includes an adder means for adding said second error signal to said two-level information signal.

4. The device according to claim 1 and wherein said variable frequency oscillator means is a klystron oscillator.