



(51) International Patent Classification:

G06F 13/42 (2006.01) G06F 13/40 (2006.01)

G06F 13/38 (2006.01) G06F 13/362 (2006.01)

(21) International Application Number:

PCT/US2019/026458

(22) International Filing Date:

09 April 2019 (09.04.2019)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

62/656,284 11 April 2018 (11.04.2018) US

16/000,733 05 June 2018 (05.06.2018) US

(71) Applicant: CYPRESS SEMICONDUCTOR CORPO-

RATION [US/US]: 198 Champion Court, San Jose, California 95134 (US).

(72) Inventors: **KHAMESRA, Arun**; #111-112, 9th Cross, BDS Garden, Hennur Main Road, Gedalahalli, Kothnur Main Road, Bangalore 560077 (IN). **NAYAK, Anup**; 43553 Southerland Way, Fremont, California 94539 (US). **MONDAL, Partha**; S/O-SUBODH CHANDRA MONDAL, KHUKURDAHA, PASCHIM MEDINIPUR, BENGAL 721641 (IN). **VISPUTE, Hemant P.**; Gopalan Grandeur Apartment, E-703, Near Hoodi Circle, Mahadevapura Post, Bangalore 560048 (IN). **KONDURU, Ravi**; Flat No: 310, A Block, Sreeja Tanisq Apartment, 2nd cross, Byrasandra Road, Bengaluru 560093 (IN).

(74) Agent: **DRAGANOFF, Stoycho**; 198 Champion Court, San Jose, California 95134 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN,

(54) Title: USB TYPE-C SIDEBAND SIGNAL INTERFACE CIRCUIT

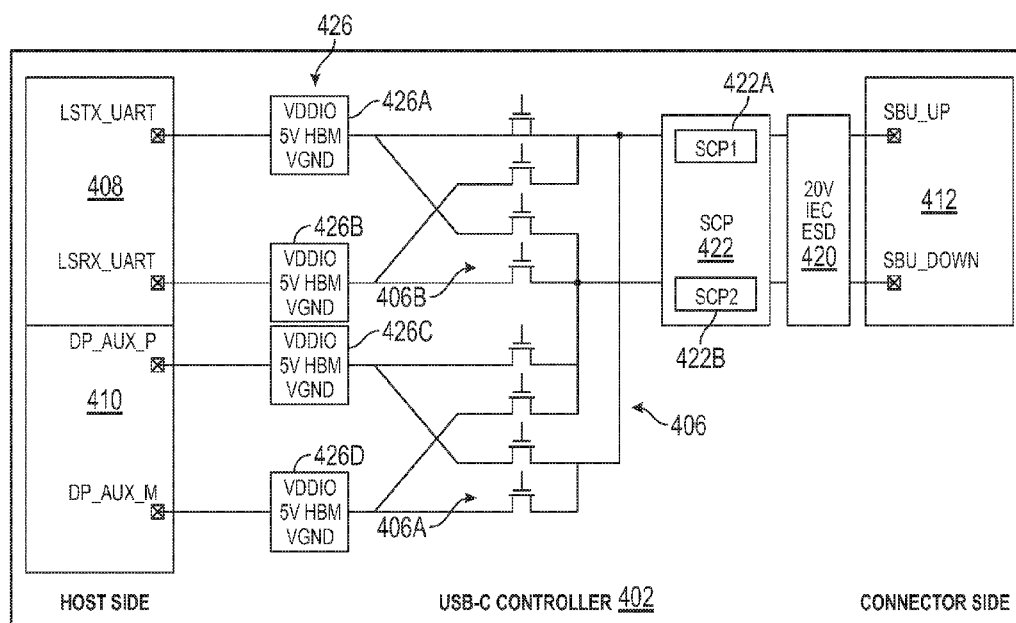


FIG. 4A

(57) Abstract: A device includes a USB-C controller instantiated as a first integrated circuit, the USB-C controller comprising a first pair of terminals to communicate with a first communication protocol that is other than USB, a second pair of terminals to communicate with a second communication protocol that is other than USB, and a third pair of terminals, each of which is to be coupled to a corresponding SBU1 terminal or SBU2 terminal of a type-C receptacle. The controller further includes a multiplexer to selectively couple the first pair of terminals to the third pair of terminals and the second pair of terminals to the third pair of terminals. The controller further includes a series of cascaded, low-voltage n-type field-effect transistors (LVNFETs) coupled between the multiplexer and each terminal of the third pair of terminals.



HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to the identity of the inventor (Rule 4.17(i))*

Published:

— *with international search report (Art. 21(3))*

USB TYPE-C SIDEBAND SIGNAL INTERFACE CIRCUIT

RELATED APPLICATIONS

[0001] This application is an International Application of U.S. Patent Application Number 16/000,733, filed on June 5, 2018, which claims the benefit of priority to U.S. Provisional Application No. 62/656,284, filed on April 11, 2018, which are herein incorporated by reference in their entirety.

TECHNICAL FIELD

[0002] The disclosure relates to the field of electronic circuits, in particular to a USB type-C sideband signal interface circuit.

BACKGROUND

[0003] Electronic circuits may include individual electronic components, such as resistors, transistors, capacitors, inductors, and diodes, among others, connected by conductive wires or traces through which electric current can flow. Electronic circuits may be constructed using discrete components, or more commonly integrated in an integrated circuit where the components and interconnections are formed on a common substrate, such as silicon.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] The disclosure is illustrated by way of example, and not of limitation, in the figures of the accompanying drawings.

[0005] **FIG. 1** is a block diagram of a USB type-C (USB-C) connector according an embodiment.

[0006] **FIG. 2A, FIG. 2B, and FIG. 2C** are portions of a circuit diagram of a single port Thunderbolt® (TBT) notebook power source/sink circuit, according to an embodiment.

[0007] **FIG. 3** is a circuit diagram of sub-portions of a USB-C controller according to an embodiment.

[0008] FIG. 4A is a circuit diagram illustrating a USB-C controller that integrates a USB type-C sideband signal interface according to another embodiment.

[0009] FIG. 4B is a circuit diagram illustrating a short circuit protection circuit of the USB-C controller of FIG. 4A according to an embodiment.

[0010] FIG. 4C is a circuit diagram of an IEC electrostatic discharge (ESD) protection circuit of the USB-C controller of FIG. 4A according an embodiment.

[0011] FIG. 4D and FIG. 4E are circuit diagrams of additional ESD protection circuitry on the system side of the USB-C controller of FIG. 4A according to an embodiment.

[0012] FIG. 5A is a circuit diagram of a test setup to measure a crosstalk parameter, and thus a level of isolation, between TBT transmit and receive control terminals (LSTX and LSRX) and sideband use terminals across the multiplexer of the USB-C controller of FIG. 4A according to an embodiment.

[0013] FIG. 5B is a graph illustrating results of the tests of FIG. 5A according to an embodiment.

[0014] FIG. 6A is a circuit diagram of a test setup to measure an isolation parameter as to isolation between negative auxiliary terminal (AUX_N) and first sideband use terminal (SBU1) through the multiplexer of the USB-C controller of FIG. 4A according to an embodiment.

[0015] FIG. 6B is a graph illustrating results of the tests of FIG. 6A according to an embodiment.

[0016] FIG. 7 is a flow chart for a method of designing a USB-C controller to form a type-C sideband interface circuit according to one embodiment.

DETAILED DESCRIPTION

[0017] A USB type-C receptacle, with capabilities of up-side down connection and accessible to external physical connectors, may access interface circuitry for reverse detection, multiplexers for flip correction, and IEC electrostatic discharge (ESD) protection. Sideband use (SBU) lines may be provided with additional short-circuit protection from accidental short to neighboring 20V VBUS terminal. There

is presently no one-die solution (e.g., a single integrated circuit chip) for these capabilities. Accordingly, a hardware manufacture that incorporates USB technology may need to use external components for one or another capability, which may degrade the high-speed signaling and increase costs, for example.

[0018] In various embodiments, a device includes a USB-C controller instantiated as a first integrated circuit, e.g., implemented as an instance on a single integrated circuit. The USB-C controller may include a first pair of terminals coupled to a first host controller to communicate with a first communication protocol that is other than USB, a second pair of terminals coupled to a second host controller to communicate with a second communication protocol that is other than USB, and a third pair of terminals, each of which is to be coupled to a corresponding SBU1 terminal or SBU2 terminal of a type-C receptacle. The SBU terminals allow communication in alternate mode, e.g., with a protocol other than USB. The USB-C controller may further include a multiplexer to selectively couple the first pair of terminals to the third pair of terminals and the second pair of terminals to the third pair of terminals. The controller may further include a series of cascaded, low-voltage n-type field-effect transistors (LVNFETs) coupled between the multiplexer and each terminal of the third pair of terminals. When terminals are referred to herein, reference is understood to be made to integrated circuit terminals, metal lines, pins, and to other input/output connectors, depending on implementation.

[0019] **FIG. 1** is a block diagram of a USB type-C (USB-C) connector 100 according an embodiment. Many of the terminals on the USB-C connector 100 are replicated on the top and on the bottom so that the USB-C connector may fit into a USB-C receptacle right side up or up-side down and still function. Those familiar with the USB-C standard will recognize these terminals, and with particular reference to the present disclosure, the sideband use terminals (SBU1, SBU2) and the configuration channel terminals (CC1, CC2).

[0020] The SBU terminals may be for communicating with other-than-USB protocols in alternate mode, such as selected from a group of protocols, which include the DisplayPort (DP) protocol, high-definition multimedia interface

(HDMI) protocol, the Thunderbolt[®] (TBT) protocol, the mobile high-definition link (MHL) protocol, and the Peripheral Component Interconnect Express (PCIe) protocol, and the like. The CC terminals may enable cable attach detection, cable orientation detection, role detection, and current-mode detection, e.g., standard mode or alternate mode. The unused CC terminal may become the VCONN terminal, which may supply power to USB-C controller chips in active cables or adaptors.

[0021] The VBUS terminals may be used for the cable bus power and are situated next to the SBU and CC terminals. For example, a first set of VBUS terminals are located adjacent the SBU1 and CC1 terminals (designated with box 101A) and a second set of VBUS terminals are located adjacent the SBU2 and CC2 terminals (designated with box 101B). As the sidewalls between the VBUS terminals and the sets of SBU and CC terminals wear down, the risk of a short circuit therebetween increases, thus causing a fault. Accordingly, switching circuitry in a USB-C controller on the SBU lines is to consider short-circuit and IEC electrostatic discharge (ESD) protections as will be discussed in more detail. Additional terminals include ground terminals (GND), D+/D- terminals to communicate over positive and negative data lines (DP/DM lines), and USB 3.1 transceiver/receiver terminals (TX/RX).

[0022] With additional reference to **FIG. 1**, the position of the SBU1 terminal and the SBU2 terminal on the one hand, and the position of the CC1 terminal and the CC2 terminal on the other hand, may each be flipped between the top and the bottom of the USB-C receptacle. This is due to the USB Type-C specification definition a Type-C port, which may be associated with a Type-C plug or a Type-C receptacle. For ease of use, the Type-C plug and the Type-C receptacle are designed as a reversible pair that operates regardless of the plug-to-receptacle orientation. Accordingly, a USB-C controller may include multiplexing between top and bottom duplicate terminals depending on the orientation of the USB-C connector placed therein. Further, a configuration channel (CC) signal may be transmitted through either of the CC1 or the CC2 terminals, which may follow CC

protocol for flip correction, so as to signal the multiplexers which set of terminals to select as will be discussed in detail.

[0023] FIG. 2 is a circuit diagram of a single port Thunderbolt® (TBT) notebook power source/sink circuit 200, according to an embodiment, for system context of where the disclosed type-C sideband signal interface circuit may be employed. The type-C sideband signal interface circuit may also be employed in other USB type-C devices and systems. In embodiments, the circuit 200 may include a type-C receptacle 201, a USB-C controller 202, a power subsystem 212, a TBT controller 222, an embedded controller 232, a USB host controller 242, and a proprietary host controller 252. In embodiments, the disclosed type-C sideband signal interface circuit may be employed as a part of or integrated within the USB-C controller 202. The power subsystem 212 may provide a five volt (5V) provider path 213, to generate VBUS_OUT for use by other USB-C circuitry, and a power consumer path 214 to power the power subsystem 212.

[0024] In various embodiments, the type-C receptacle 201 may contain terminals that correspond to the terminals of the USB-C connector 100 of FIG. 1, e.g., VBUS, SBU1, SBU2, D+/D- (top), D+/D- (bottom), CC2, CC1, and GND. These terminals may be coupled to corresponding terminals on the USB-C controller 202, respectively, the VBUS_C_CTRL, SBU2, SBU1, DPLUS_TOP, DMINUS_TOP, DPLU_BOT, DMINUS_BOT, CC2, and CC1 terminals. The USB-C controller 202 may be configured for alternate mode operation, which enables other communication protocols, which was just discussed.

[0025] As illustrated, the USB-C controller 202 may include a number of additional connections and circuitry, not all that are relevant here, and may be manufactured as a single integrated circuit. Note the additional negative auxiliary terminal (AUX_N), positive auxiliary terminal (AUX_P), TBT transmit control signal terminal (LSTX), and TBT receive control signal terminal (LSRX) on the USB-C controller 202 may be coupled to corresponding terminals on the TBT controller 222. The AUX_N, AUX_P terminals may provide auxiliary signals for DisplayPort signaling and the LSTX, LSRX terminals may provide TBT link management using Universal Asynchronous Receiver-Transmitter (UART)-based

technology, for example. Furthermore, a positive data system terminal (e.g., DPLUS_SYS) and a negative data system terminal (e.g., DMINUS_SYS) of the USB-C controller 202 may be coupled to DP/DM system lines that are routed to the USB host controller 242. A data transmitter terminal (e.g., UART_TX) and a data receiver terminal (e.g., UART_RX) may be coupled to the proprietary host controller 252. The proprietary host controller 252 may be a proprietary controller such as a test and debug controller of a host computing system in which the circuit 200 is located, e.g., the notebook or other computing system that hosts the USB-C controller 202.

[0026] In various embodiments, the embedded controller 232 may be coupled to the USB-C controller 202 through, for example, an inter-integrated circuit connection (I2C), e.g., a synchronous, multi-master, multi-slave, packet switched, single-ended, or a serial computer bus. The USB-C controller 202 may include an I2C address that is determined by the SWD_CLK terminal.

[0027] The USB-C controller 202 may communicate with the power subsystem 212 over I2C, which manages the power provided to the upstream type-C ports. The USB-C controller 202 may also update the TBT controller 222 over I2C based on the alternate mode negotiation to sink Thunderbolt® or USB or DisplayPort protocol data. The USB-C controller 202 may control the transfer of USB 2.0 D+/D- lines from the top and bottom of the type-C receptacle 201 to the D+/D- lines of the TBT controller 222. The USB-C controller 202 may also handle the routing of SBU1 and SBU2 lines from the type-C receptacle 201 to the TBT controller 222 for the link management. In embodiments, the USB-C controller 202 may offer on-chip ESD protection on D+/D- and SBU lines as well as on-chip VBUS Short protection on SBU and CC lines. Some of these capabilities will be discussed in more detail below.

[0028] **FIG. 3** is a circuit diagram of sub-portions of a USB-C controller 302, associated with a single port, according to an embodiment. In one embodiment, the USB-C controller 300 is the USB-C controller 202 of Figure 2. The USB-C controller 302 may include a configuration channel (CC) interface circuit 310, a

USB-C sideband signal interface circuit 330, and a USB-C D+/D- interface circuit 360.

[0029] In various embodiments, the CC interface circuit 310 may include a gate drive and 10V charge pump 311 and a pair of transistor switches 312 to enable VCONN functionality on CC1/CC2 depending on the connector direction. Either of CC1 or CC2 may be used for CC protocol and the other one may be connected to V5V using 312 switches to give power to the cable. The CC interface circuit 310 may further include reference circuitry 314 to compare and detect certain types of signals received through the CC1 and CC2 terminals, and to generate outgoing control signals over the CC1 and CC2 terminals.

[0030] In some embodiments, the USB-C sideband signal interface circuit 330 may include a four-by-two multiplexer 332 with resistance isolation on the inputs and having switches driven using a 5V charge pump 328. The four-by-two multiplexer 332 may selectively couple a first pair of terminals (e.g., AUX1, AUX2 terminals) to a pair of SBU terminals (e.g., SBU1, SBU2), and selectively couple a second pair of terminals (e.g., LSTX, LSRX terminals) to the pair of SBU terminals (e.g., SBU1, SBU2). The general purpose input/output (GPIO) boxes may be adapted to receive communication links of protocols other than USB. In one embodiment, the switches of the four-by-two multiplexer 332 are metal-oxide-semiconductor field-effect transistors (MOSFETs), e.g., specifically low-voltage n-type field effect transistors (LVNFETs). In one embodiment, the charge pump 328 may drive the gates of the LVNFETs such that the LVNFETs each operate in a linear region and exhibit less than a seven-ohm resistance.

[0031] The LVNFETs may be “low-voltage” in the sense of operating at the full operating voltage of the device (e.g., that includes the USB-C controller 302), as provided by the power subsystem 212. In some embodiments, this full operating voltage may be 5V, in another embodiment it is 3.3V, or another voltage that may be about 5V or less.

[0032] In some embodiments, a USB-C D+/D- interface circuit 360 may include a four-by-four multiplexer 362 that includes switches that are also driven by a 5V charge pump 358. The four-by-four multiplexer 362 may selectively couple the

positive data system terminal (DP_SYS) to one of the first and second positive data terminals (DP_TOP, DP_BOT), the data transmitter terminal (UART_TX) to one of the first and second positive data terminals (DP_TOP, DP_BOT), the negative data system terminal (DM_SYS) to one of the first and second negative data terminals (DM_TOP, DM_BOT), and the data receiver terminal (UART_RX) to one of the first and second negative data terminals (DM_TOP, DM_BOT).

[0033] In one embodiment, the switches of the four-by-four multiplexer 362 are MOSFETs, e.g., specifically n-type field effect transistors (NFETs). The 5V charge pump 528 may be a low-ripple charge pump (e.g., low-ripple 5V charge pump) coupled to gates of the MOSFETs of the four-by-four multiplexer 362. The low-ripple charge pump may drive the MOSFETs to operate in a linear region and such that each MOSFET exhibits less than seven-ohm resistance.

[0034] In embodiments, the high-speed operation of the disclosed USB-C controllers may meet USB2.0 high-speed data rates with signaling rates of 480 Mbps, USB2.0 full-speed data rates with signaling rates of 12 Mbps, may provide UART signaling, and provide access to a battery charger for USB devices.

[0035] **FIG. 4A** is a circuit diagram illustrating a USB-C controller 402 that integrates a USB type-C sideband signal interface according to another embodiment. In one embodiment, the USB-C controller 402 is the USB-C controller 202 of **FIG. 2** or the USB-C controller 302 of **FIG. 3**, and thus may be viewed as a part of the circuits of these Figures.

[0036] For example, the USB-C controller 402 may further include, on the host side, a first pair of terminals 408, including a data transmitter terminal (LSTX_UART) and data receiver terminal (LSRX_UART), e.g., to be coupled to the TBT controller 222 for communication with the TBT protocol. The USB-C controller 402 may further include, on the host side, the second pair of terminals 410, including a positive auxiliary terminal (DP_AUX_P) and a negative auxiliary terminal (DP_AUX_M), e.g., to be coupled to the TBT controller 222 for communication with the DisplayPort (DP) protocol according to the circuit 200 of **FIG. 2**. The TBT controller 222 may be a first host controller, and in another embodiment, the auxiliary terminals may be coupled to a second host controller

different than the TBT controller 222, to provide flexibility in choice of alternate mode communication.

[0037] In embodiments, the USB-C controller 402 may further include, on the connector side, a third pair of terminals 412, each of which is to be coupled to a corresponding SBU1 terminal or SBU2 terminal of the type-C receptable 201 (FIG. 1). Accordingly, the third pair of terminals may be a sideband use up terminal (SBU_UP) and a sideband use down terminal (SBU_DOWN), which terminals are respectively referred to as SBU1 and SBU2 in the USB-C controller 202 of **FIG. 2**.

[0038] In various embodiments, the USB-C controller 402 may further include a multiplexer 406 (e.g., a four-by-two multiplier), which may be made up of multiple low-voltage n-type field effect transistors (LVNFETs). For example, the multiplexer 406 may include a first set of four LVNFETs 406A and a second set of four LVNFETs 406B. The multiplexer 406 may selectively couple the first pair of terminals 408 to the third pair of terminals 412 and the second pair of terminals 410 to the third pair of terminals 412 in a way that enables flip correction between top and bottom terminals of the USB-C connector 100.

[0039] More specifically, the first set of LVNFETs 406A may couple the data transmitter terminal and the data receiver terminal to one of the SBU_UP terminal or the SBU_DOWN terminals, to provide flip correction in response to a configuration channel (CC) signal. Furthermore, the second set of LVNFETs 406B may couple the positive auxiliary terminal and the negative auxiliary terminal to one of the SBU_UP terminal or the SBU_DOWN terminal, to provide flip correction in response to the CC signal. In some embodiments, the data transmitter terminal may be a LSTX control terminal and the data receiver terminal may be a LSRX control terminal of the TBT protocol and the positive auxiliary terminal and the negative auxiliary terminal are control terminals of the DP protocol. Other protocols are envisioned as are coupling to different host controllers to support those other protocols. In this way, the multiplexer 406 may enable choice, based on the CC signal through one of the CC1 or CC2 terminals, of one or another possible communication protocol to use in alternate mode.

[0040] The USB-C controller 402 may further include an IEC electrostatic discharge (ESD) protection circuit 420 coupled between the multiplexer 406 and the third set of terminals 412, e.g., the SBU_UP and SBU_DOWN terminals. The 20V IEC ESD protection circuit 420, which will be discussed in detail with reference to **FIG. 4C**, may provide ± 8 KV of contact discharge protection and ± 15 KV of air gap discharge protection based on IEC61000-4-2 level 4C protection. The 20V IEC ESD protection circuit 420 may protect against electrostatic discharge and provide better signal integrity for high-speed signals, and avoid extra routing at board level, which would otherwise be required if located on a second integrated circuit chip from the chip on which the multiplexer 406 is disposed.

[0041] In various embodiments, the USB-C controller 402 may further include a short-circuit protection (SCP) circuit 422, e.g., a first SCP circuit 422A and a second SCP circuit 422B. The first SCP circuit 422A may be coupled to the SBU_UP terminal and the second SCP circuit 422B may be coupled to the SBU_DOWN terminal, of the third pair of terminals 412. The first SCP circuit 422A and second SCP circuit 422B may be identical, and will be discussed with reference to **FIG. 4B**. Note that, in alternate embodiments, locations of the 20V IEC ESD protection circuit 420 and the SCP circuit 422 may be swapped from that which is illustrated in **FIG. 4A**.

[0042] In some embodiments, the USB-C controller 402 further includes additional ESD protection circuitry 426 coupled to the host (or system) side of the multiplexer 406. The additional ESD protection circuitry 426 may include first ESD protection circuitry 426A, second ESD protection circuitry 426B, third ESD protection circuitry 426C, and fourth system ESD protection circuitry 426D. The 20V IEC ESD protection circuit 420 and the additional ESD protection circuitry 426 may provide ESD clamp protection.

[0043] **FIG. 4B** is a circuit diagram illustrating the first short circuit protection (SCP) circuit 422A of the USB-C controller 402 of **FIG. 4A** according to an embodiment. As the first SCP circuit 422A and the second SCP circuit 422B are identical, the first SCP circuit 422A is exemplary and is illustrated and discussed. Accordingly, the host terminal illustrated in **FIG. 4B** may be any one of the first

and second sets of terminals 410 and 412, as any one of these terminals may be coupled to the first SCP circuit 422A depending on a state of the multiplexer 406. Furthermore, the LVNFET labeled as S/W_M for “multiplexer switch” may represent any of the four LVNFETs of the multiplexer 406 that are coupled to the SBU_UP terminal.

[0044] In various embodiments, the first SCP circuit 422A may include a charge pump 428 (e.g., a 5V charge pump), a level shifter 429, a series of cascaded LVNFETs 430 having gates driven by the charge pump 428, and a bulk set of switches 432 (which may include firmware, state machine, or other logic) to selectively control the LVNFET switches of the multiplexer 406 based on an enabled mode signal (EN_M). The enabled mode signal may be or respond to the CC signal from one of the CC1 or CC2 terminals. The level shifter 429 may convert, based on an input control signal, the voltage from the charge pump 428 to a voltage level appropriate for the gate of the S/W_M LVNFET, e.g., the multiplexer LVNFET gate (“M” being for multiplexer).

[0045] With continued reference to **FIG. 4B**, the bulk set of switches 432 may switch the bulk connection of the S/W_M transistor between GND and the source of the S/W_M transistor based on the EN_M signal. This is done to avoid forward bias diode path from the host terminal to the SBU_UP terminal for the case when the host terminal is more than the signal on the SBU_UP terminal by one diode drop. Furthermore, use of the charge pump 428 to drive the gates of the LVNFETs may cause the LVNFETs (of the multiplexer 406 and of the series of cascaded LVNFETs 430) to operate in a linear region and exhibit less than seven-ohm resistance.

[0046] In embodiments, the first SCP circuit 422A may further include a first capacitor (C₁), a rail resistor (R₀), and a second capacitor (C₂) connected in series and coupled between the charge pump 428 and each of the gates of the series of cascaded LVNFETs 430. The series of LVNFETs 430 may provide isolation to avoid cross-talk issues between LSTX and LSRX terminals due to non-differential signaling. Furthermore, the SCP circuit 422A may include a series of resistors (R₁,

R₂, R₃, R₄) coupled between the gate of respective LVNFET of the series of cascaded LVNFETs 430 and the second capacitor.

[0047] In one embodiment, the series of cascaded LVNFETs 430 is a series of four cascaded LVNFETs, where the LVNEFTs of the multiplexer 406 and of the series of at least four cascaded LVNFETs are five-volt LVNFETs and provide at least 20 volts of short-circuit protection to circuitry of the USB-C controller 402 and host computing device. In an alternative embodiment, the series of cascaded LVNFETs 430 is a series of at least seven cascaded LVNFETs, where the LVNEFTs of the multiplexer 406 and the series of seven cascaded LVNFETs are three-volt LVNFETs and provide at least 20 volts of short-circuit protection to circuitry of the USB-C controller and host computing device.

[0048] In embodiments of normal operation (e.g., no VBUS short to SBU_UP), the voltages of the gates of the switches (S/W₁, S/W₂, S/W₃, and S/W₄) of the at least four cascaded LVNEFTs 430 are the same as the pump voltage of the charge pump 428, e.g., 5V. In such normal operation, when the enable mode line (EN_M) to the bulk set of switches 432 is low, the gate of the fifth switch (S/M_M) is at zero volts and no voltage signal is passed between the host terminal (e.g., LSTX or AUX pin) and the SBU_UP terminal. When the enable mode (EN_M) goes high and the all the switches (including the fifth switch) are at the pump voltage (e.g., 5V), then the voltage signal on the host terminal equals that of the SBU_UP voltage, whether low or high.

[0049] In an additional embodiment, the SCP circuit 422A may further include a self-bias circuit 433 coupled to the SBU_UP terminal to generate self-biased voltages on gates of the at least four LVNFETS 430, e.g., S/W₁, S/W₂, S/W₃, and S/W₄, in the case the 20V VBUS is shorted to the SBU_UP terminal. The voltage level of this self-biased voltage on each switch is illustrated in Table 1.

S/W ₁	16V	80% of VBUS
S/W ₂	12V	60% of VBUS
S/W ₃	8V	40% of VBUS
S/W ₄	4V	20% of VBUS

TABLE 1

[0050] Note that the voltage on the gate of each of the at least four LVNFETS 430 is the highest on the first switch (S/W₁) nearest the SBU_UP terminal at 16V, and progressively decreases with each switch (12V on S/W₂, 8V on S/W₃, and 4V on S/W₄) moving away from the SBU_UP terminal. In the case of a short on one or both of the SBU terminals, the fifth switch (S/W_M) is turned off and goes to zero volts. Additionally, the pump signal is also pulled to zero volts. Furthermore, the resistances of each of the series of resistors (R₁, R₂, R₃, R₄) enables the bias voltage at the gate of each of the LVNFET switches to be higher (at the self-biased voltage) while the pump voltage is kept at zero voltage, thus providing for resistance isolation during a short circuit.

[0051] **FIG. 4C** is a circuit diagram of the 20V IEC electrostatic discharge (ESD) protection circuit 420 of the USB-C controller of **FIG. 4A** according an embodiment. In this embodiment, the 20V ESD protection circuit 420 includes a 20V IEC RC snapback clamp 431A and 431B coupled between each of the third pair of terminals (e.g., each of SBU_UP and SBU_DOWN), respectively, and ground.

[0052] **FIG. 4D** and **FIG. 4E** are circuit diagrams of additional ESD protection circuitry on the system side of the USB-C controller of **FIG. 4A** according to an embodiment. In various embodiments, the additional ESD protection circuitry includes additional system ESD protection circuitry for each of the first set of terminals 410 coupled to the host controllers, e.g., for each of the data transmitter terminal (LSTX_UART) and the data receiver terminal (LSRX_UART) and for each of the second set of terminals 412, e.g., for each of the positive auxiliary terminal (DP_AUX_P) and the negative auxiliary terminal (DP_AUX_M).

[0053] More specifically, with reference to **FIG. 4D**, the first system ESD protection circuitry 426A may include a first human body model (HBM) snapback clamp 434A coupled to a ground and the data transmitter terminal (LSTX_UART). Further, the second system ESD protection circuitry 426B may include a second HBM snapback clamp 434B coupled to the ground and the data receiver terminal (LSRX_UART).

[0054] With additional reference to **FIG. 4E**, the third system ESD protection circuitry 426C may include a third HBM snapback clamp 434C coupled to the ground and the positive auxiliary terminal (DP_AUX_P). Further, the fourth system ESD protection circuitry 426D may include a fourth HBM snapback clamp 434D coupled to the ground and the negative auxiliary terminal (DP_AUX_M).

[0055] **FIG. 5A** is a circuit diagram of a test setup 500 to measure a crosstalk parameter, and thus a level of isolation, between TBT transmit and receive control terminals (LSTX and LSRX) and sideband use terminals (SBU1 and SBU2) across the multiplexer 406 of the USB-C controller 402 of **FIG. 4A** according to an embodiment. The test setup 500 may include a 50-ohm resistor connected across the LSTX and LSRX terminals on the outputs of the USB-C controller 402 and a network analyzer 504 connected across the SBU1 and SBU2 output terminals of the USB-C controller 402.

[0056] **FIG. 5B** is a graph illustrating results of the tests of **FIG. 5A** according to an embodiment. Note the isolation measured at 1 MHz was -63.18 decibel (DB), which is minimal crosstalk. Other measurements are illustrated inset within the graph of **FIG. 5B**.

[0057] **FIG. 6A** is a circuit diagram of a test setup 600 to measure an isolation parameter as to isolation between negative auxiliary terminal (AUX_N) and first sideband use terminal (SBU1) through the multiplexer 406 of the USB-C controller of **FIG. 4A** according to an embodiment. The test setup 600 may include a network analyzer 604 connected between the LSTX or the AUX_N terminal and the SBU1 terminal of the USB-C controller 402 of **FIG. 4A**.

[0058] **FIG. 6B** is a graph illustrating results of the tests of **FIG. 6A** according to an embodiment. Note the isolation measured at 1 MHz was -63.5 decibel (DB), which exhibits high off-switch isolation. Other measurements are illustrated inset within the graph of **FIG. 5B**.

[0059] **FIG. 7** is a flow chart for a method of designing a USB-C controller to form a type-C sideband interface circuit according to one embodiment. The method 700 may be performed by processing logic that comprises hardware (e.g., circuitry, dedicated logic, programmable logic, microcode, etc.). In some embodiments, the

method 700 is performed wholly or in part by one of the USB-C controllers discussed herein.

[0060] In various embodiments, the method 700 may begin by operating a USB-C controller instantiated as a first integrated circuit, wherein the USB-C controller comprises a multiplexer, a series of cascaded, low-voltage n-type field-effect transistors (LVNFETs), a first pair of terminals, a second pair of terminals, and a pair of sideband use (SBU) terminals (710). The operating the USB-C controller may be performed as illustrated in any of blocks 720, 730, and/or 740. For example, the method 700 may continue with selecting, by the multiplexer, the first pair of terminals (associated with a first non-USB communication protocol) or a second pair of terminal (associated with a second non-USB communication protocol) (720). The method 700 may continue with coupling, by the multiplexer, the selected pair of terminals to the pair of SBU terminals (730). The selecting and coupling by the multiplexer of the selected pair of terminals to the pair of SBU terminals may be performed in response to, or after, connection orientation is determined based on CC signal(s) on the CC channel of the USB-C controller.

[0061] With additional reference to FIG. 7, the method 700 may continue with coupling the series of cascaded (LVNFETs) between the multiplexer and each of the pair of SBU terminals to provide short-circuit protection (740). The short circuit protection may be provided in response to detecting a short between an adjacent VBUS terminal and one of the pair of SBU terminals.

[0062] In the above description, numerous details are set forth. It will be apparent, however, to one of ordinary skill in the art having the benefit of this disclosure, that embodiments of the present disclosure may be practiced without these specific details. In some instances, well-known structures and devices are shown in block diagram form, rather than in detail, in order to avoid obscuring the description.

[0063] Some portions of the detailed description are presented in terms of algorithms and symbolic representations of operations on data bits within a computer memory. These algorithmic descriptions and representations are the means used by those skilled in the data processing arts to most effectively convey

the substance of their work to others skilled in the art. An algorithm is here and generally, conceived to be a self-consistent sequence of steps leading to a desired result. The steps are those requiring physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared and otherwise manipulated. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, values, elements, symbols, characters, terms, numbers or the like.

[0064] It should be borne in mind, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities. Unless specifically stated otherwise as apparent from the above discussion, it is appreciated that throughout the description, discussions utilizing terms such as “receiving,” “adjusting,” or the like, refer to the actions and processes of a computing system, or similar electronic computing device, that manipulates and transforms data represented as physical (e.g., electronic) quantities within the computing system's registers and memories into other data similarly represented as physical quantities within the computing system memories or registers or other such information storage, transmission or display devices.

[0065] The words “example” or “exemplary” are used herein to mean serving as an example, instance or illustration. Any aspect or design described herein as “example” or “exemplary” is not necessarily to be construed as preferred or advantageous over other aspects or designs. Rather, use of the words “example” or “exemplary” is intended to present concepts in a concrete fashion. As used in this application, the term “or” is intended to mean an inclusive “or” rather than an exclusive “or.” That is, unless specified otherwise, or clear from context, “X includes A or B” is intended to mean any of the natural inclusive permutations. That is, if X includes A; X includes B; or X includes both A and B, then “X includes A or B” is satisfied under any of the foregoing instances. In addition, the articles “a” and “an” as used in this application and the appended claims should generally be construed to mean “one or more” unless specified otherwise or clear

from context to be directed to a singular form. Moreover, use of the term “an embodiment” or “one embodiment” or “an embodiment” or “one embodiment” throughout is not intended to mean the same embodiment or embodiment unless described as such.

[0066] Embodiments described herein may also relate to an apparatus for performing the operations herein. This apparatus may be specially constructed for the required purposes, or it may comprise a general-purpose computer selectively activated or reconfigured by a computer program stored in the computer. Such a computer program may be stored in a non-transitory computer-readable storage medium, such as, but not limited to, any type of disk including floppy disks, optical disks, CD-ROMs and magnetic-optical disks, read-only memories (ROMs), random access memories (RAMs), EPROMs, EEPROMs, magnetic or optical cards, flash memory, or any type of media suitable for storing electronic instructions. The term “computer-readable storage medium” should be taken to include a single medium or multiple media (e.g., a centralized or distributed database and/or associated caches and servers) that store one or more sets of instructions. The term “computer-readable medium” shall also be taken to include any medium that is capable of storing, encoding or carrying a set of instructions for execution by the machine and that causes the machine to perform any one or more of the methodologies of the present embodiments. The term “computer-readable storage medium” shall accordingly be taken to include, but not be limited to, solid-state memories, optical media, magnetic media, any medium that is capable of storing a set of instructions for execution by the machine and that causes the machine to perform any one or more of the methodologies of the present embodiments.

[0067] The algorithms and displays presented herein are not inherently related to any particular computer or other apparatus. Various general-purpose systems may be used with programs in accordance with the teachings herein, or it may prove convenient to construct a more specialized apparatus to perform the required method steps. The required structure for a variety of these systems will appear from the description below. In addition, the present embodiments are not described with reference to any particular programming language. It will be appreciated that a

variety of programming languages may be used to implement the teachings of the embodiments as described herein.

[0068] The above description sets forth numerous specific details such as examples of specific systems, components, methods and so forth, in order to provide a good understanding of several embodiments of the present disclosure. It will be apparent to one skilled in the art, however, that at least some embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known components or methods are not described in detail or are presented in simple block diagram format in order to avoid unnecessarily obscuring the present disclosure. Thus, the specific details set forth above are merely exemplary. Particular embodiments may vary from these exemplary details and still be contemplated to be within the scope of the present disclosure.

[0069] It is to be understood that the above description is intended to be illustrative and not restrictive. Many other embodiments will be apparent to those of skill in the art upon reading and understanding the above description. The scope of the disclosure should, therefore, be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

[0070] In the above description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the present disclosure. It will be evident, however, to one skilled in the art that the present disclosure may be practiced without these specific details. In other instances, well-known circuits, structures, and techniques are not shown in detail, but rather in a block diagram in order to avoid unnecessarily obscuring an understanding of this description.

Reference in the description to “one embodiment” or “an embodiment” means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the disclosure. The phrase “in one embodiment” located in various places in this description does not necessarily refer to the same embodiment.

CLAIMS

What is claimed is:

1. A device comprising a USB-C controller instantiated as a first integrated circuit, the USB-C controller comprising:
 - a first pair of terminals to communicate with a first communication protocol that is other than USB;
 - a second pair of terminals to communicate with a second communication protocol that is other than USB;
 - a third pair of terminals, each of which is to be coupled to a corresponding SBU1 terminal or SBU2 terminal of a type-C receptacle;
 - a multiplexer to selectively couple the first pair of terminals to the third pair of terminals and the second pair of terminals to the third pair of terminals; and
 - a series of cascaded, low-voltage n-type field-effect transistors (LVNFETs) coupled between the multiplexer and each terminal of the third pair of terminals.
2. The device of claim 1, wherein one of the first communication protocol or the second communication protocol is selected from a group of protocols comprising the DisplayPort (DP) protocol, the high-definition multimedia interface (HDMI) protocol, the Thunderbolt® (TBT) protocol, the mobile high-definition link (MHL) protocol, and the Peripheral Component Interconnect Express (PCIe) protocol.
3. The device of claim 1, wherein the multiplexer comprises a plurality of LVNFETs, the series of cascaded LVNFETs comprises a series of at least four cascaded LVNFETs, and wherein the LVNFETs of the plurality of LVNFETs and the series of at least four cascaded LVNFETs are five-volt LVNFETs.
4. The device of claim 3, wherein the device is to provide at least 20 volts of short-circuit protection to circuitry of the USB-C controller and host computing device.
5. The device of claim 1, wherein the first pair of terminals comprises a data transmitter terminal and a data receiver terminal, the second pair of terminals comprises a

positive auxiliary terminal and a negative auxiliary terminal, the third pair of terminals comprises an SBU_UP terminal to be coupled to the SBU1 terminal and an SBU_DOWN terminal to be coupled to the SBU2 terminal, and wherein the multiplexer comprises:

a first set of NVFETs to couple the data transmitter terminal and the data receiver terminal to one of the SBU_UP terminal or the SBU_DOWN terminals and to provide flip correction in response to a configuration channel (CC) signal; and

a second set of NVFETs to couple the positive auxiliary terminal and the negative auxiliary terminal to one of the SBU_UP terminal or the SBU_DOWN terminal and to provide flip correction in response to the CC signal.

6. The device of claim 5, wherein the data transmitter terminal is a LSTX control terminal and the data receiver terminal is a LSRX control terminal of the Thunderbolt® (TBT) protocol, and the positive auxiliary terminal and the negative auxiliary terminal are control terminals of the DisplayPort (DP) protocol.

7. The device of claim 1, wherein the multiplexer comprises a first set of four LVNFETs, and wherein the USB-C controller further comprises:

a charge pump coupled to gates of each of the first set of four LVNFETs and of the series of cascaded LVNFETs, which LVNFETs are to exhibit less than a seven-ohm resistance; and

first logic to control the gates of each of the first set of four LVNFETs according to a mode enabled within a configuration channel (CC) signal.

8. The device of claim 1, wherein the USB-C controller further comprises a 20V IEC RC snapback clamp coupled between each of the third pair of terminals and ground.

9. The device of claim 1, wherein the USB-C controller further comprises a human body model (HBM) snapback clamp coupled between each of the first pair of terminals and ground.

10. A system comprising:
a first host controller to communicate with a first communication protocol;
a second host controller to communicate with a second communication protocol,
wherein the first and second communication protocols are other than USB;
a USB type-C receptacle; and
a USB-C controller instantiated as a first integrated circuit and comprising:
a first pair of terminals coupled to the first host controller to communicate with the first communication protocol that is other than USB;
a second pair of terminals coupled to the second host controller to communicate with the second communication protocol that is other than USB;
a third pair of terminals, each of which is to be coupled to a corresponding SBU1 terminal or SBU2 terminal of a type-C receptacle;
a multiplexer to selectively couple the first pair of terminals to the third pair of terminals and the second pair of terminals to the third pair of terminals;
and
a series of cascaded, low-voltage n-type field-effect transistors (LVNFETs) coupled between the multiplexer and each terminal of the third pair of terminals to provide short-circuit protection.
11. The system of claim 10, wherein one of the first communication protocol or the second communication protocol is selected from a group of protocols comprising the DisplayPort (DP) protocol, the high-definition multimedia interface (HDMI) protocol, the Thunderbolt[®] (TBT) protocol, the mobile high-definition link (MHL) protocol, and the Peripheral Component Interconnect Express (PCIe) protocol.
12. The system of claim 10, wherein the multiplexer comprises a plurality of LVNFETs, the series of cascaded LVNFETs comprises a series of at least four cascaded LVNFETs, and wherein the LVNFETs of the plurality of LVNFETs and the series of at least four cascaded LVNFETs are five-volt LVNFETs.

13. The system of claim 12, wherein the first integrated circuit is to provide at least 20 volts of short-circuit protection to circuitry of the USB-C controller and host computing device.

14. The system of claim 10, wherein the first pair of terminals comprises a data transmitter terminal and a data receiver terminal, the second pair of terminals comprises a positive auxiliary terminal and a negative auxiliary terminal, the third pair of terminals comprises an SBU_UP terminal coupled to the SBU1 terminal and an SBU_DOWN terminal coupled to the SBU2 terminal, and wherein the multiplexer comprises:

a first set of NVFETs to couple the data transmitter terminal and the data receiver terminal to one of the SBU_UP terminal or the SBU_DOWN terminals and to provide flip correction in response to a configuration channel (CC) signal; and

a second set of NVFETs to couple the positive auxiliary terminal and the negative auxiliary terminal to one of the SBU_UP terminal or the SBU_DOWN terminal and to provide flip correction in response to the CC signal.

15. The system of claim 10, wherein the multiplexer comprises a first set of four LVNFETs, and wherein the USB-C controller further comprises:

a charge pump coupled to gates of each of the first set of four LVNFETs and of the series of cascaded LVNFETs, which LVNFETs are to exhibit less than a seven-ohm resistance; and

first logic to control the gates of each of the first set of four LVNFETs according to a mode enabled within a configuration channel (CC) signal.

16. The system of claim 10, wherein the USB-C controller further comprises a 20V IEC RC snapback clamp coupled between each of the third pair of terminals and ground.

17. The system of claim 10, wherein the USB-C controller further comprises a human body model (HBM) snapback clamp coupled between each of the second pair of terminals and ground.

18. A method comprising:

operating a USB-C controller instantiated as a first integrated circuit, wherein the USB-C controller comprises a multiplexer, a series of cascaded, low-voltage n-type field-effect transistors (LVNFETs), a first pair of terminals, a second pair of terminals, and a pair of sideband use (SBU) terminals, and wherein operating the USB-C controller comprises:

selectively coupling, by the multiplexer, the first pair of terminals, associated with a first communication protocol, to the pair of SBU terminals and the second pair of terminals, associated with a second communication protocol, to the pair of SBU terminals; and

coupling the series of cascaded (LVNFETs) between the multiplexer and each of the pair of SBU terminals to provide short-circuit protection.

19. The method of claim 18, wherein the first integrated circuit provides at least 20 volts of short-circuit protection to circuitry of the USB-C controller and a host computing device.

20. The method of claim 18, wherein the multiplexer comprises a first set of four LVNFETs, the USB-C controller further comprises a charge pump, and the method further comprising:

coupling the charge pump to gates of each of the first set of four LVNFETs and of the series of cascaded LVNFETs; and

employing first logic to control the gates of each of the first set of four LVNFETs according to a mode enabled within a configuration channel (CC) signal.

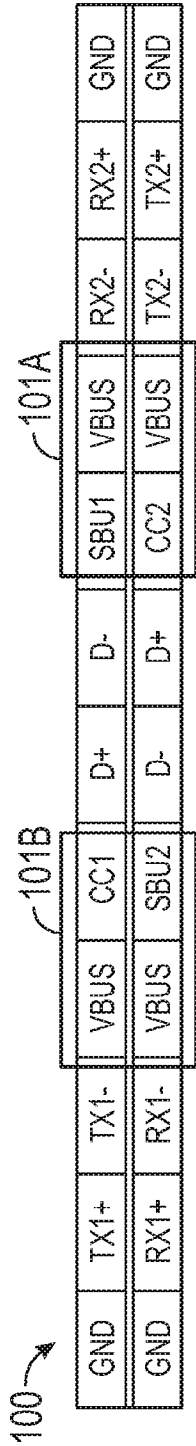


FIG. 1

200

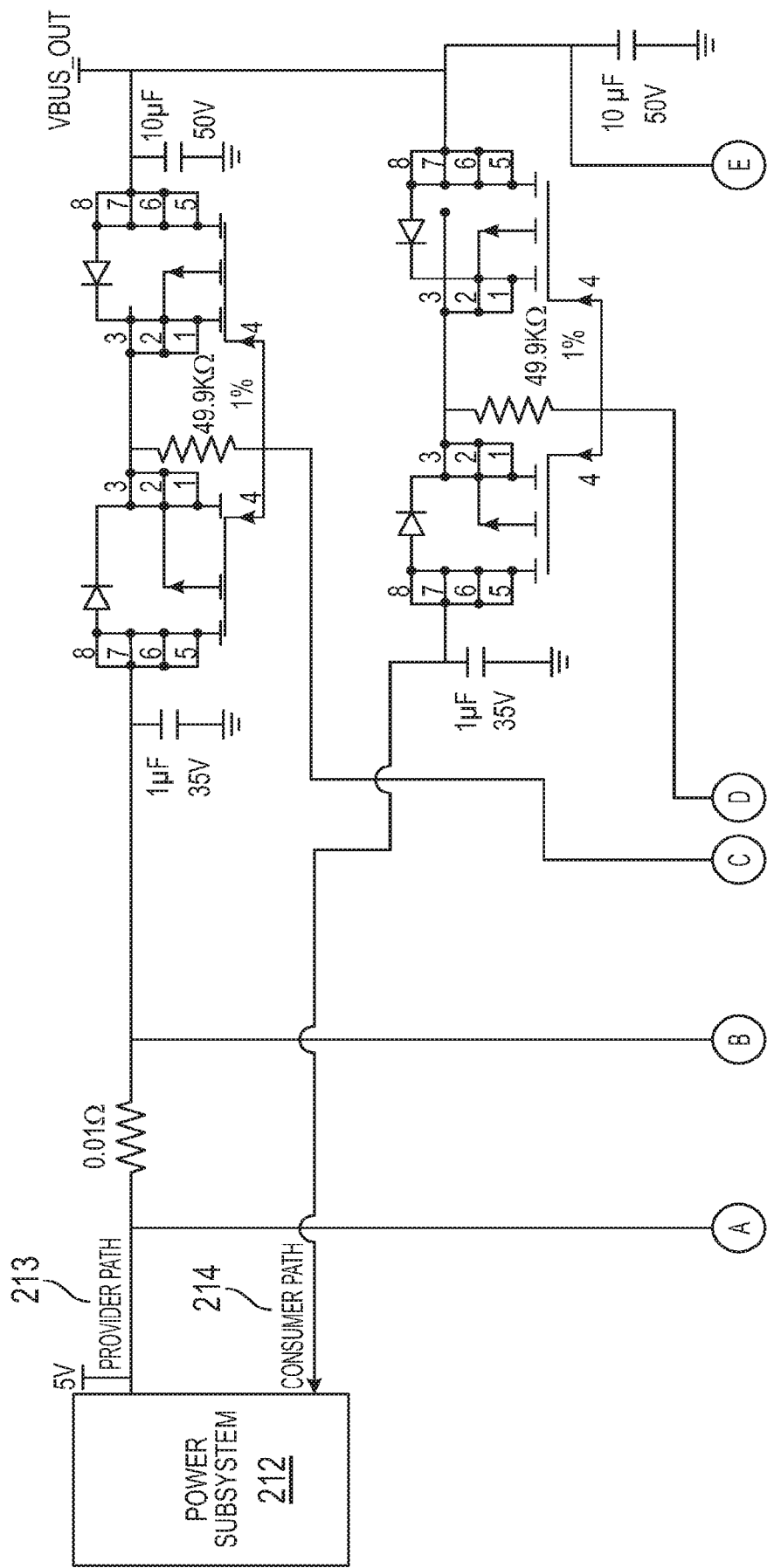


FIG. 2A

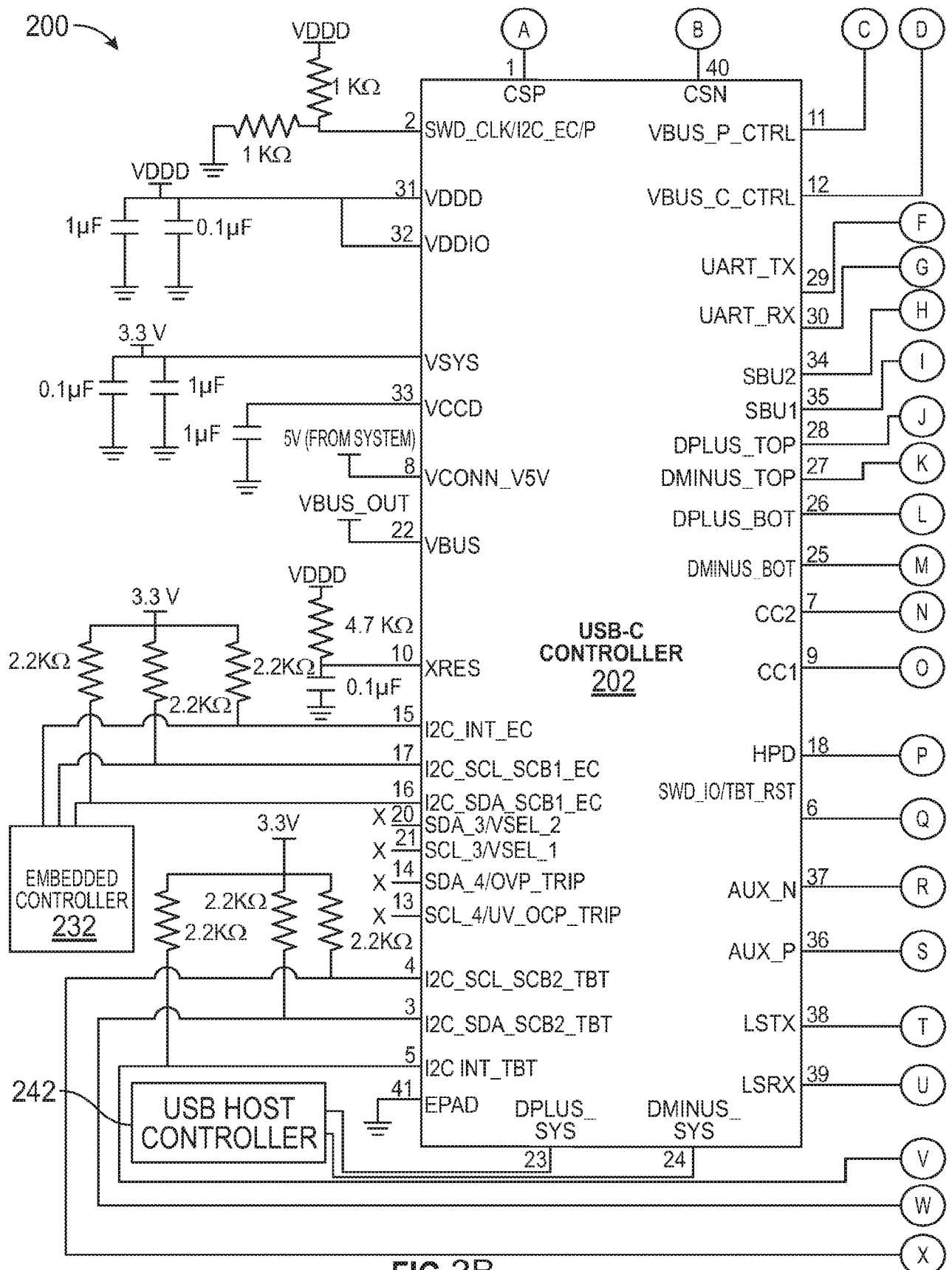


FIG.2B
(Continued)

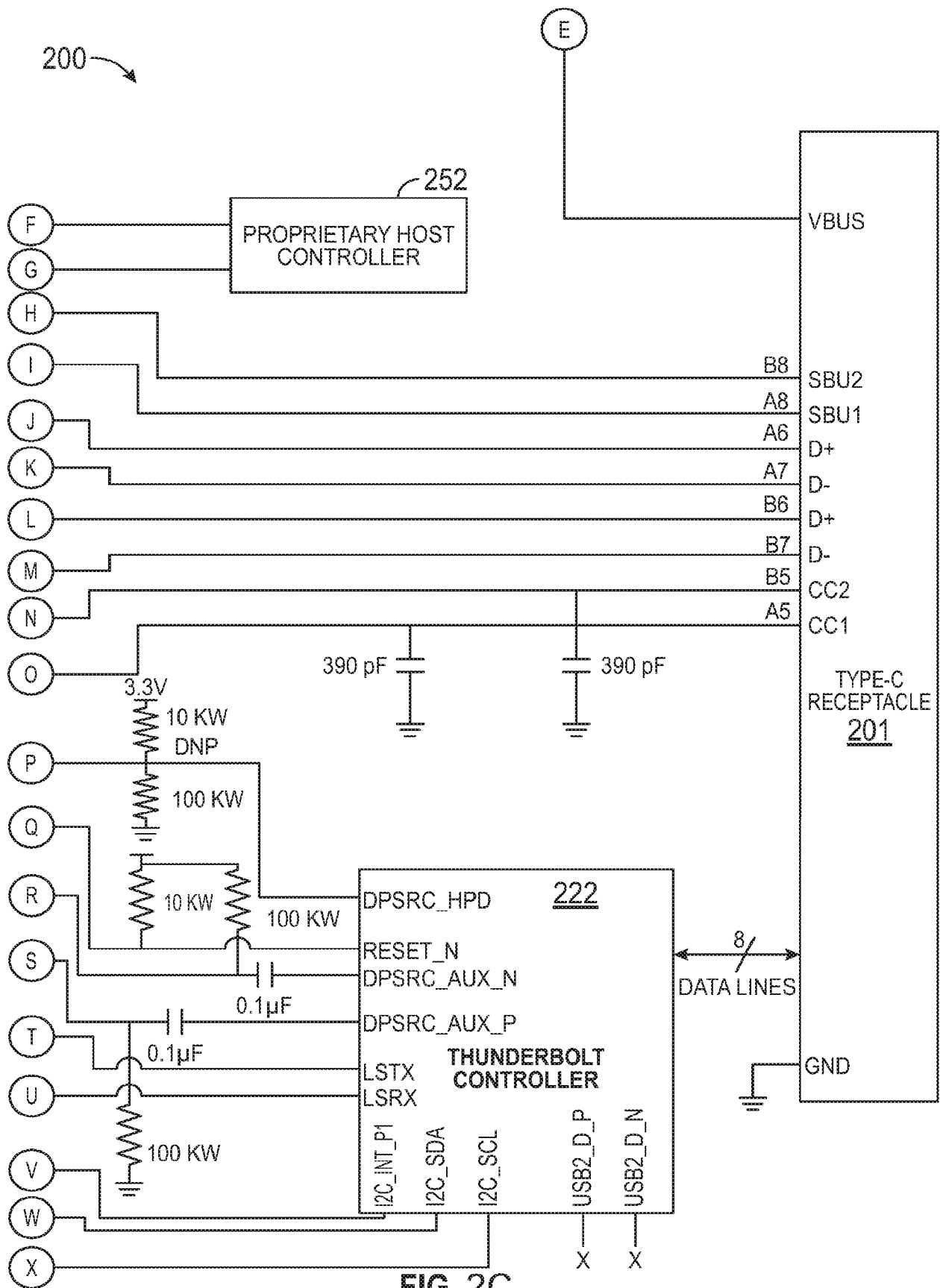


FIG. 2C
(Continued)

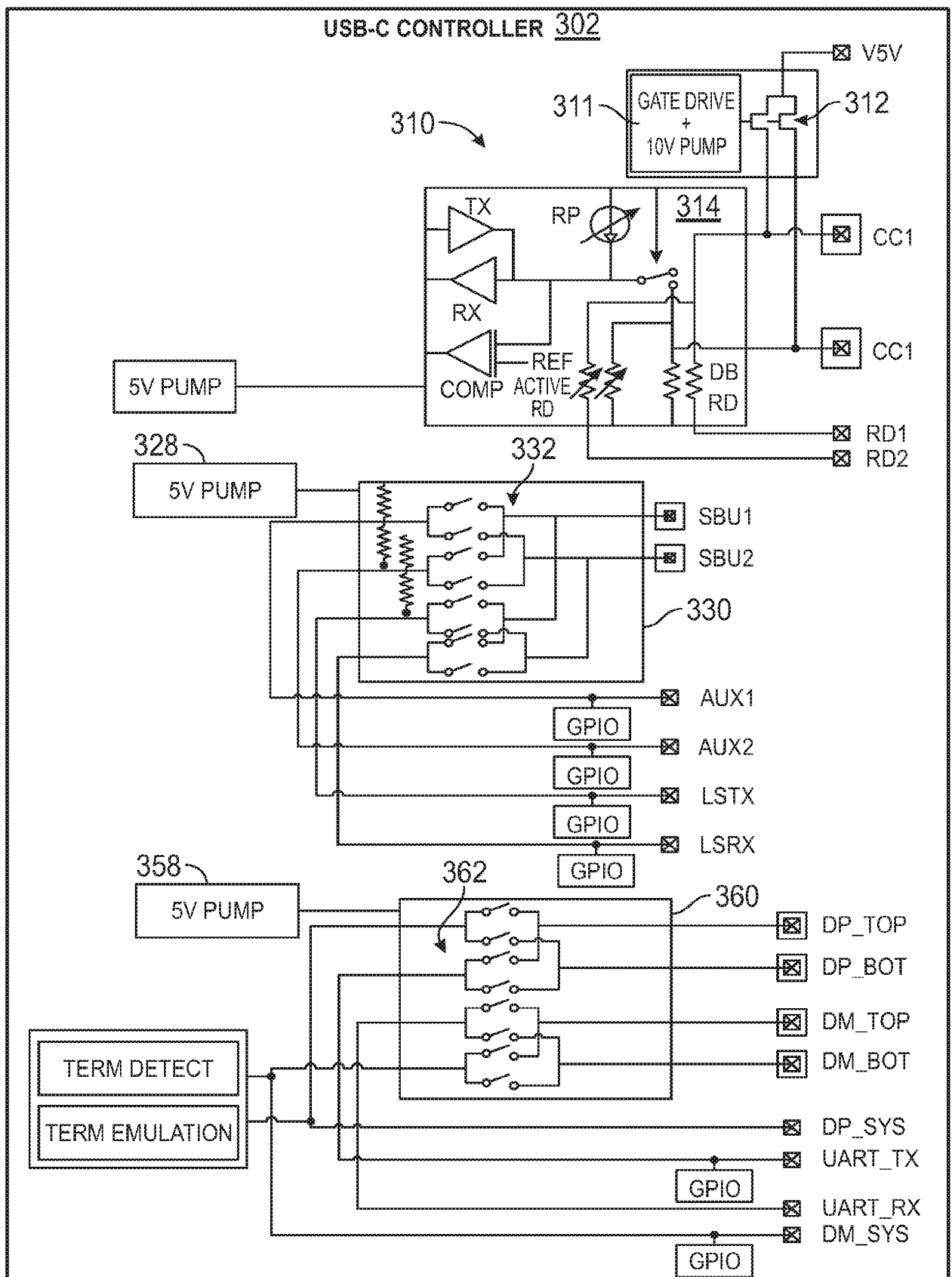


FIG. 3

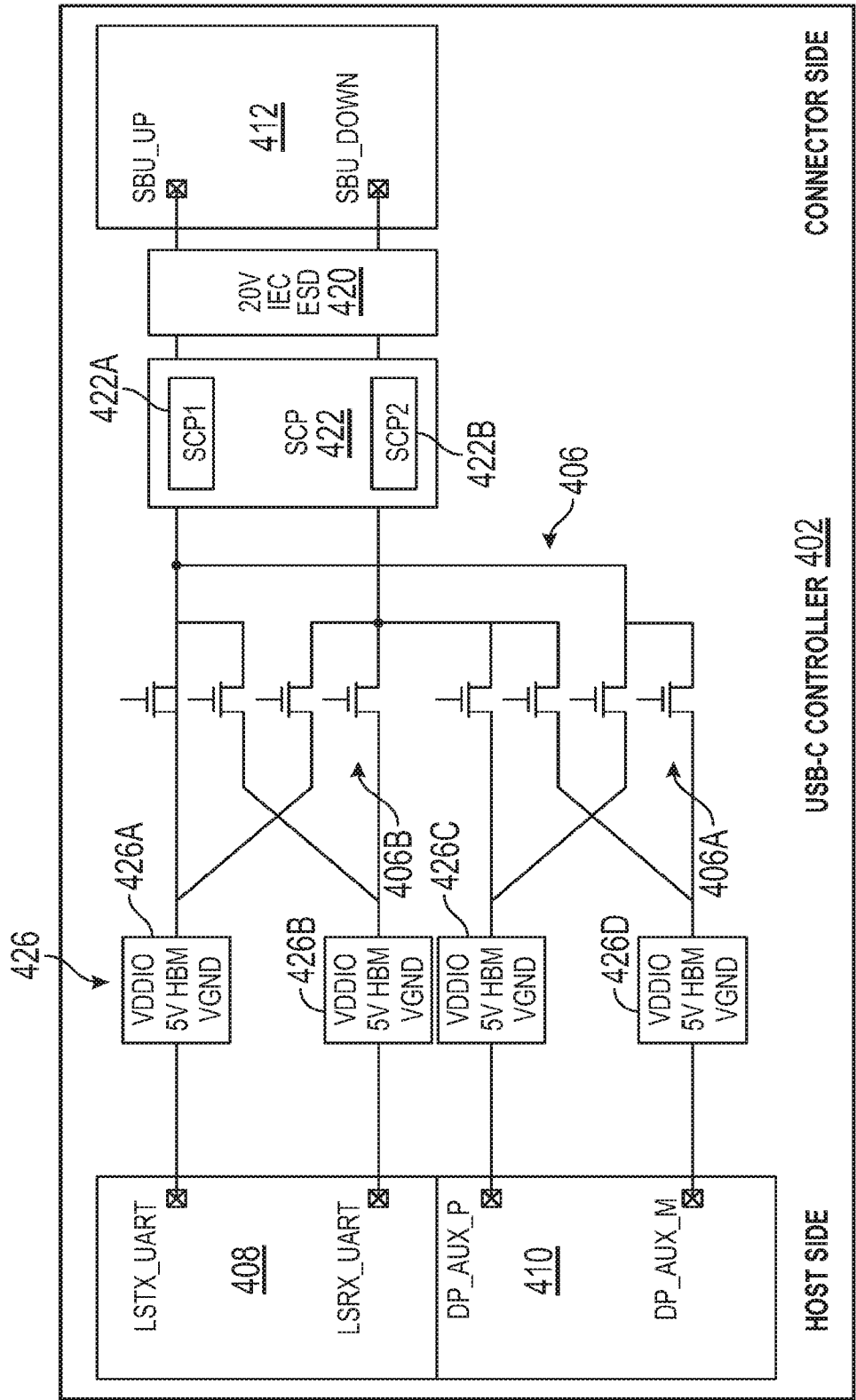


FIG. 4A

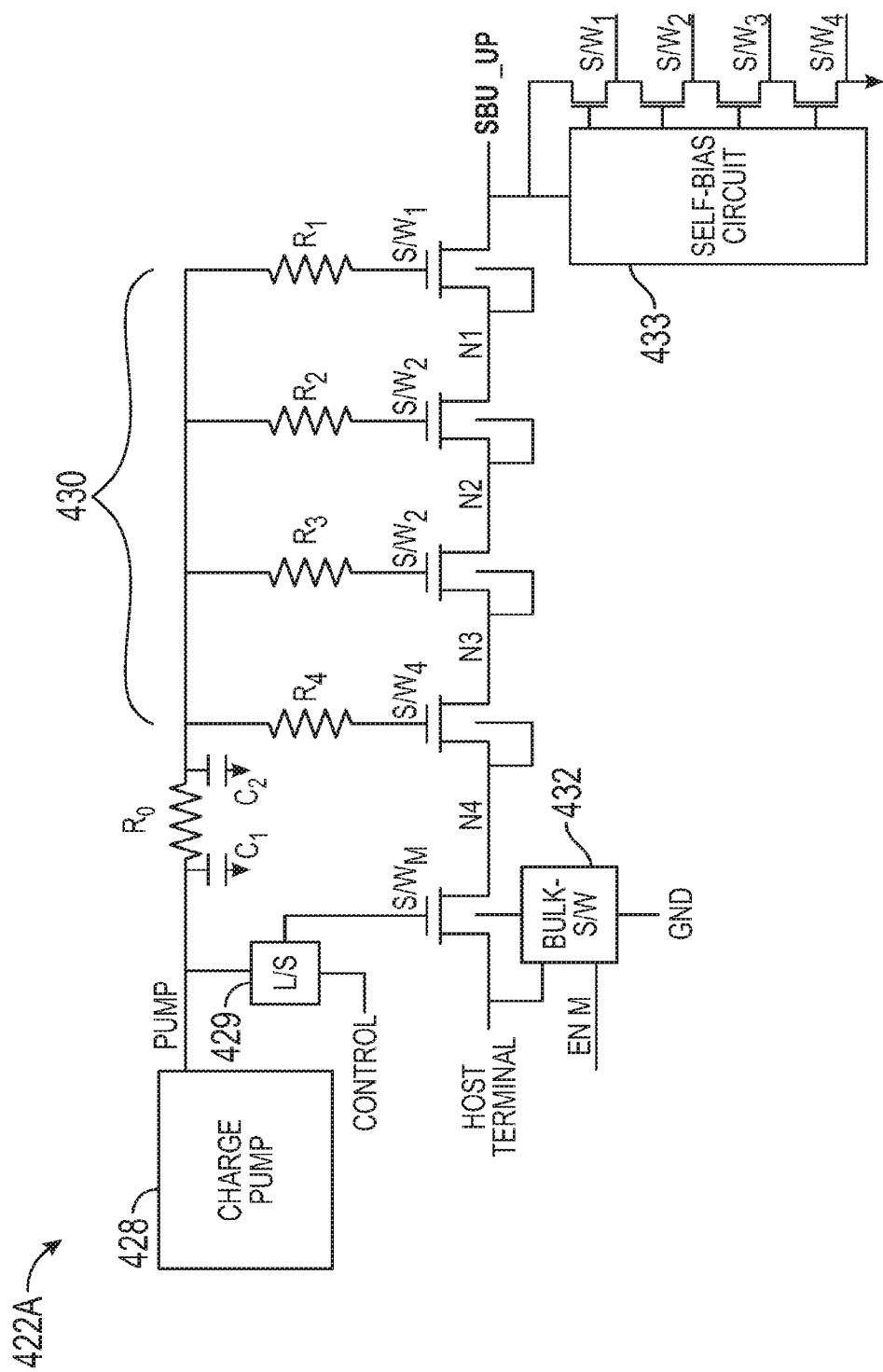


FIG. 4B

420

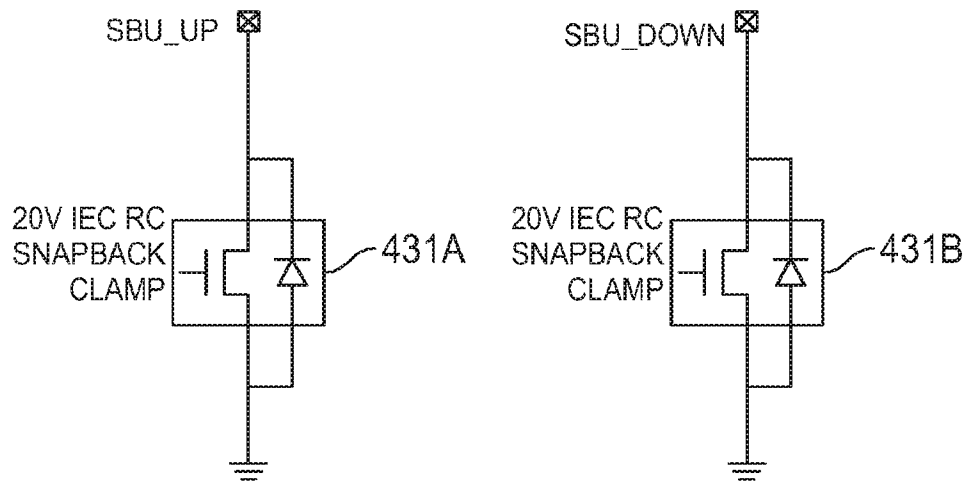


FIG. 4C

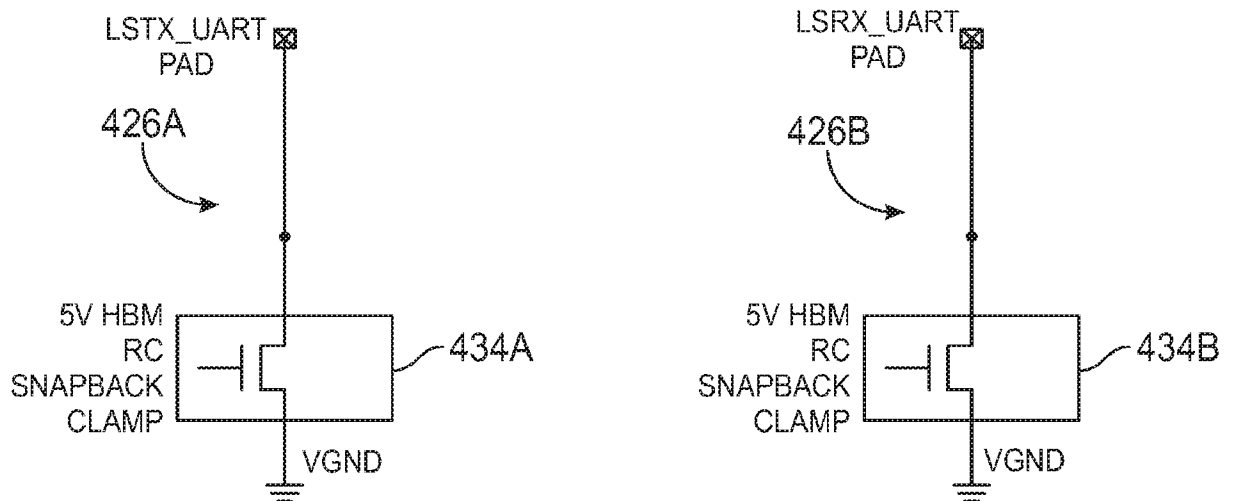


FIG. 4D

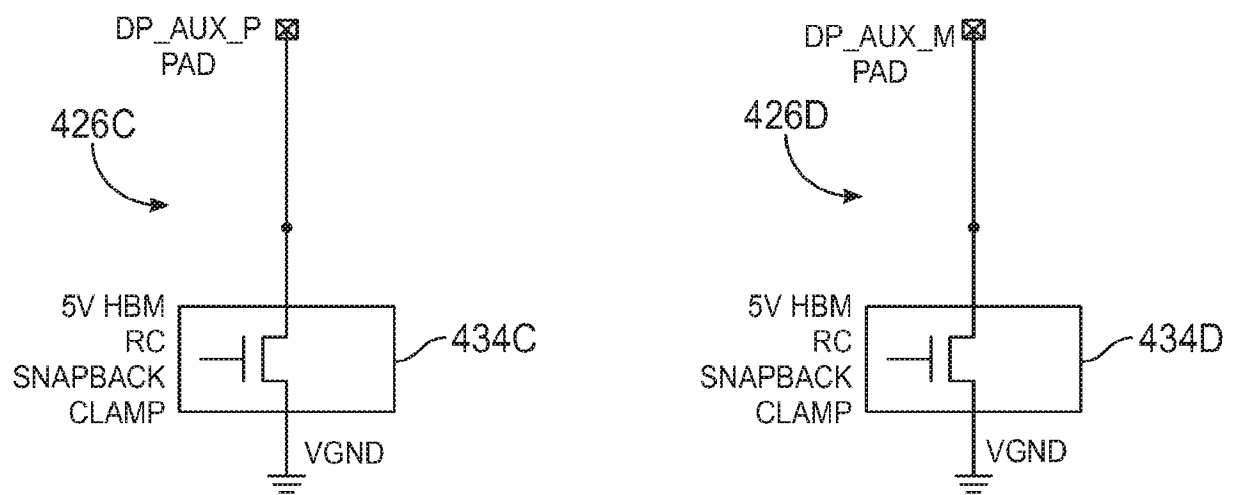


FIG. 4E

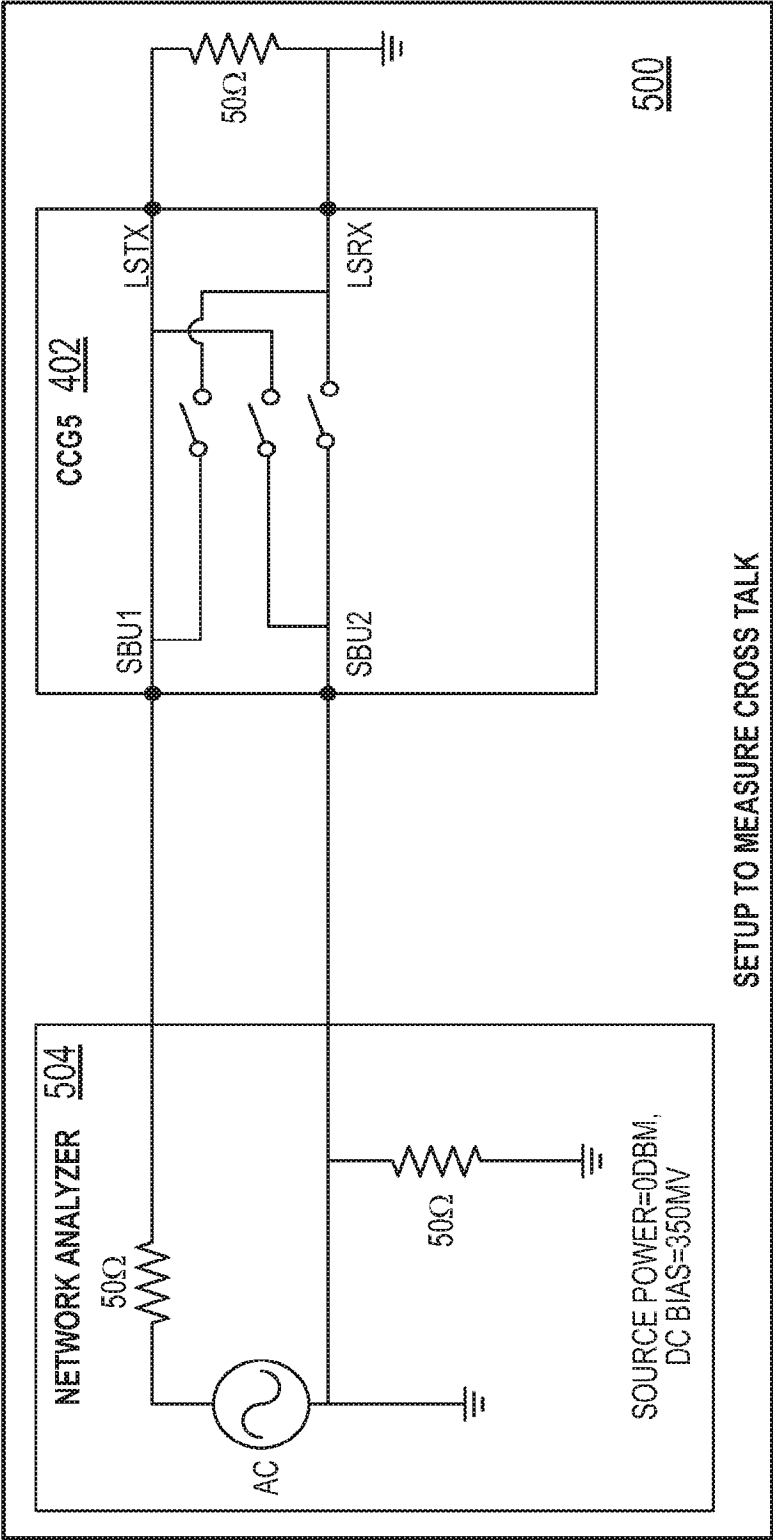


FIG. 5A

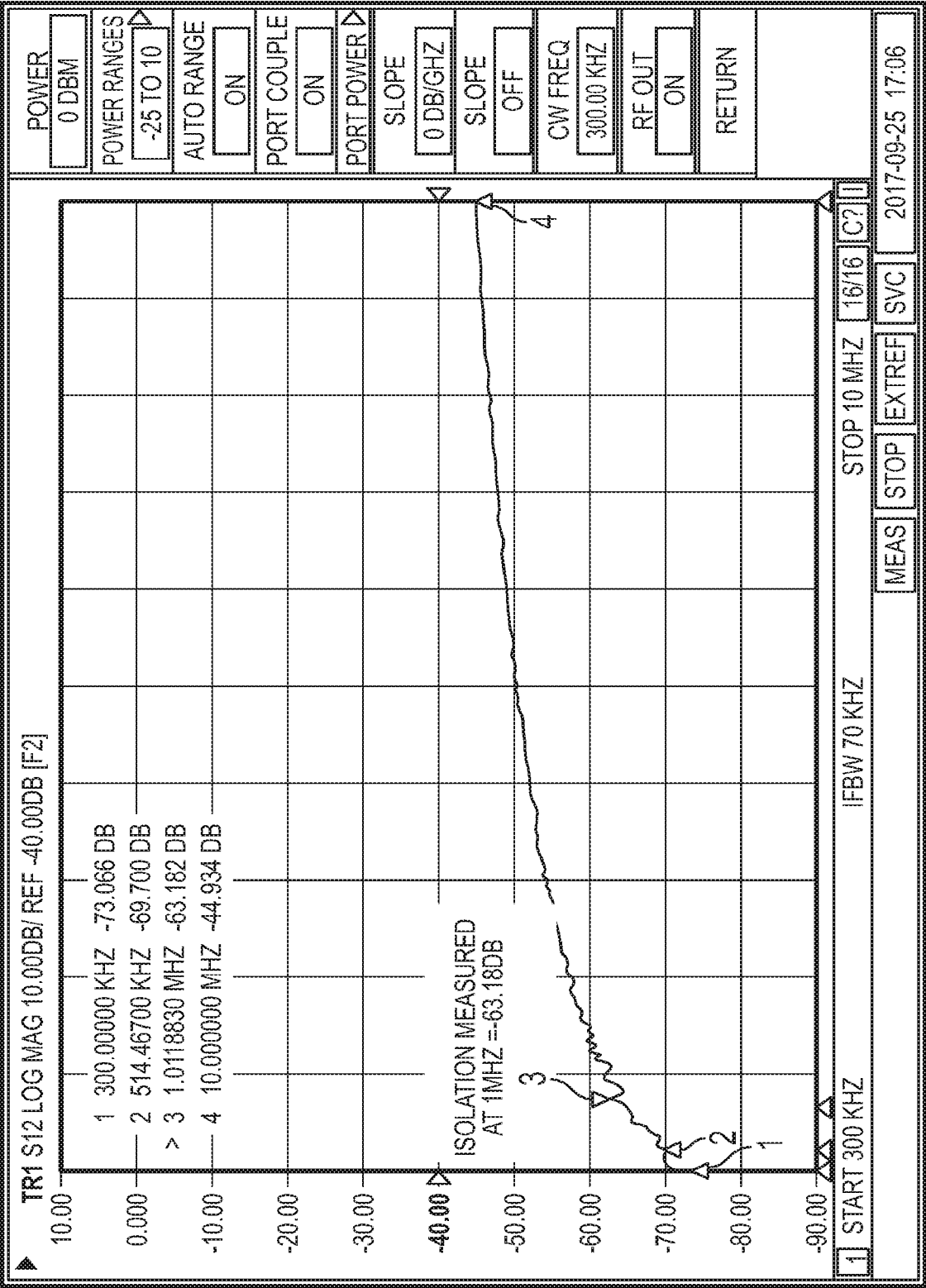


FIG. 5B

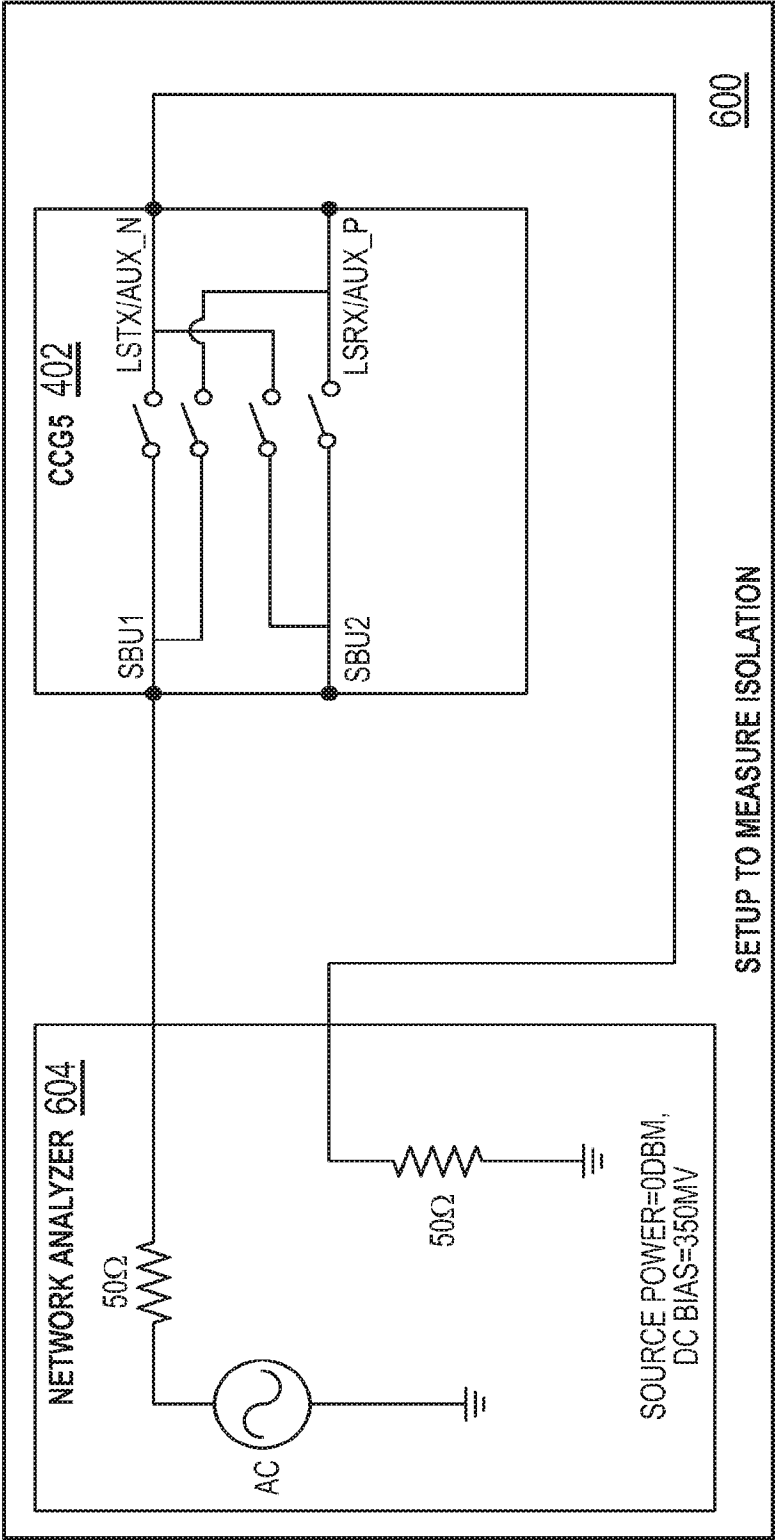


FIG. 6A

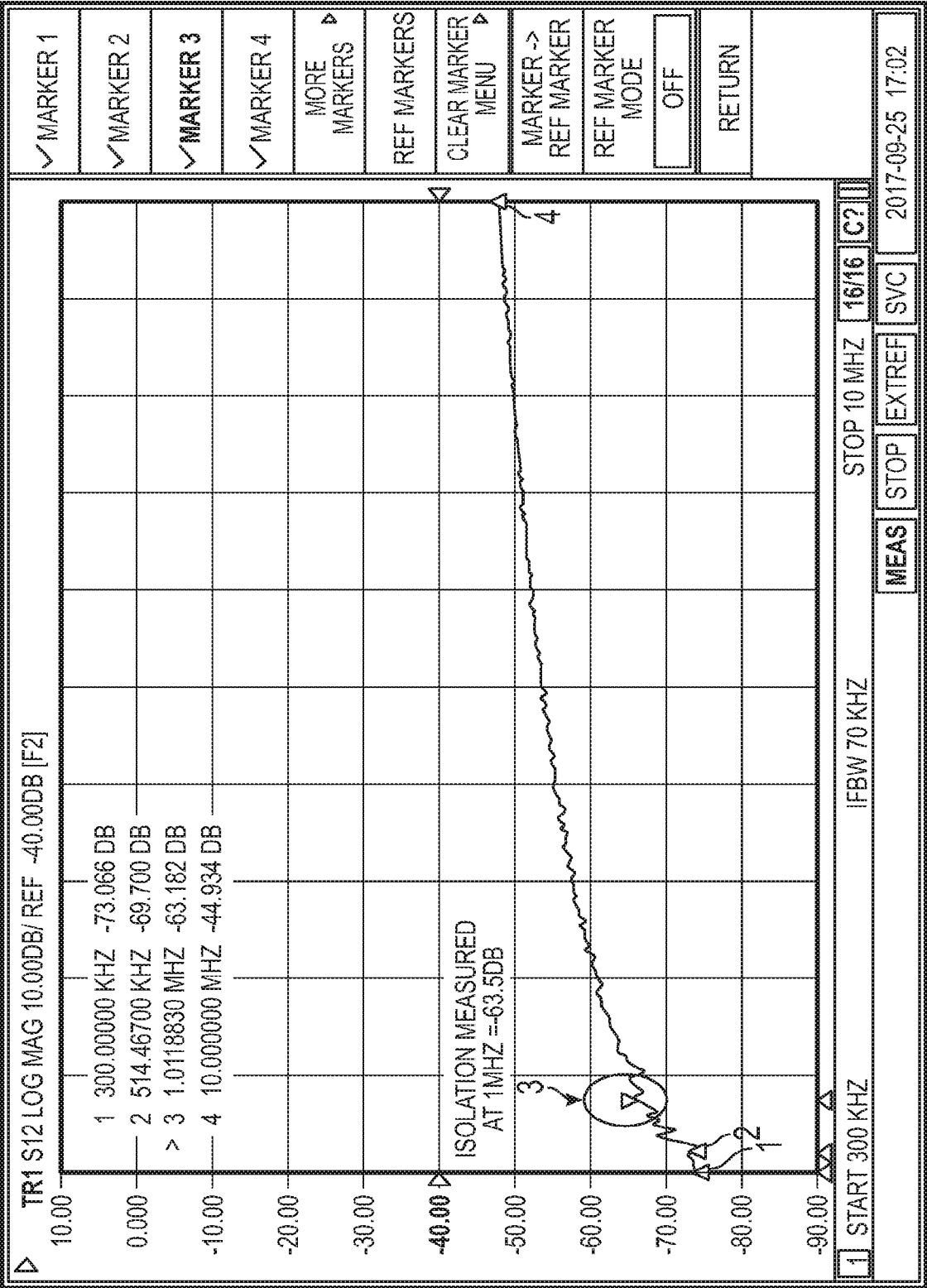


FIG. 6B

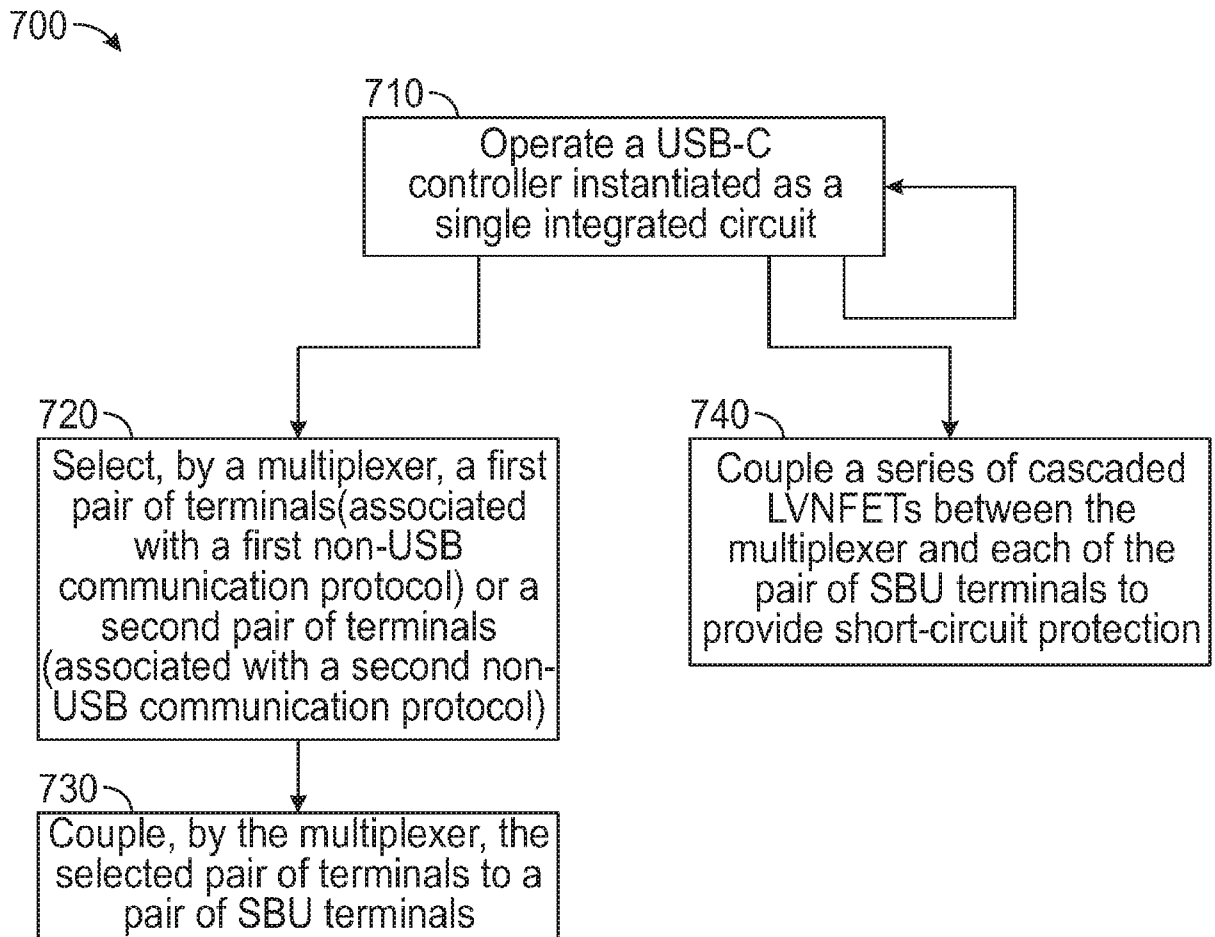


FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2019/026458

A. CLASSIFICATION OF SUBJECT MATTER

IPC: G06F 13/42, 13/38, 13/40, 13/362
CPC: G06F 13/4282

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

CPC: G06F 13/4282; H01L 2924/00, 2924/0002, 2224/131, 2924/014, 23/3737; USPC: 257/392, E21.689, E27.081; 438/479; 710/313

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EAST: US-PGPUB; USPAT; Search Terms: usbc, usb, c, controller, sideband, use, sbu 1, non, displayport, hdmi, thunderbolt, mhl, pcie, switch\$3, multiplex\$3, select\$3, mux, low, voltage, type, field, effect, transistor, multiplex?r, protection, cascaded\$3, plural\$3, several, many, multiple, two, three, short, human, body, snapback, model

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2016/0170932 A1 (LIN) 16 June 2016 (16.06.2016) , entire document.	1-20
Y	US 2013/0249514 A1 (HUANG ET AL.) 26 September 2013 (26.09.2013) , entire document.	1-20

☐ Further documents are listed in the continuation of Box C.☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

08 May 2019 (08.05.2019)

Date of mailing of the international search report

14 MAY 2019

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HARRY C. KIM

Telephone No. 571-272-4300