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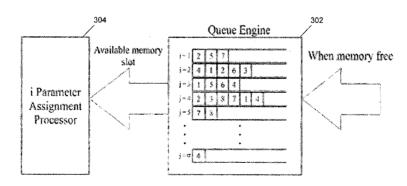
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(54) Title: METHODS FOR MEMORY ASSIGNMENT SCHEMES AND ARCHITECTURE FOR SHAREABLE PARALLEL MEMORY MODULE BASED INTERNET SWITCHES



(57) Abstract: System and methods are described for high-speed memory assignment schemes for routing packels in a sharable parallel memory module based switch system (Fig. 3). A method includes receiving a parameter, determining availability of memory location, determining if an available memory location is pre-assigned, and assigning a packet a parameter if the memory location is available (302). Systems of present invention provides hardware and/or software based components for implementing the steps of receiving a parameter, determining available memory location, determining if available memory location is pB-assigned, and assigning a packet a parameter if the memory location is available (304, 302).





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	UMENTS CONSIDERED TO BE RELEVANT		
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Α	US 20040143710 A1 (Walmsley) 22 July 2004 (22.0	07.2004), entire reference	1-20
Α	US 6687247 B1 (Wilford et al.) 3 February 2004 (03.02.2004), entire reference		1-20
A	6011775 (Bonomi et al.) 4 January 2000 (04.01.2000), entire reference		1-20
A	5887146 (Baxter et al.) 23 March 1999 (23.03.1999), entire reference		1-20
A	6014690 (VanDoren et al.) 11 January 2000 (11.01.2000), entire reference		1-20
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