(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
18 June 2009 (18.06.2009)

PCT

(10) International Publication Number
WO 2009/076563 A2

(51) International Patent Classification:
*H04L 25/06* (2006.01)

(21) International Application Number:
PCT/US2008/086489

(22) International Filing Date:
11 December 2008 (11.12.2008)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
11/955,159 12 December 2007 (12.12.2007) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

**Declarations under Rule 4.17:**

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

**Published:**

— *without international search report and to be republished upon receipt of that report*

(54) **Title:** METHOD AND APPARATUS FOR COMPENSATING DC OFFSETS IN COMMUNICATION SYSTEMS

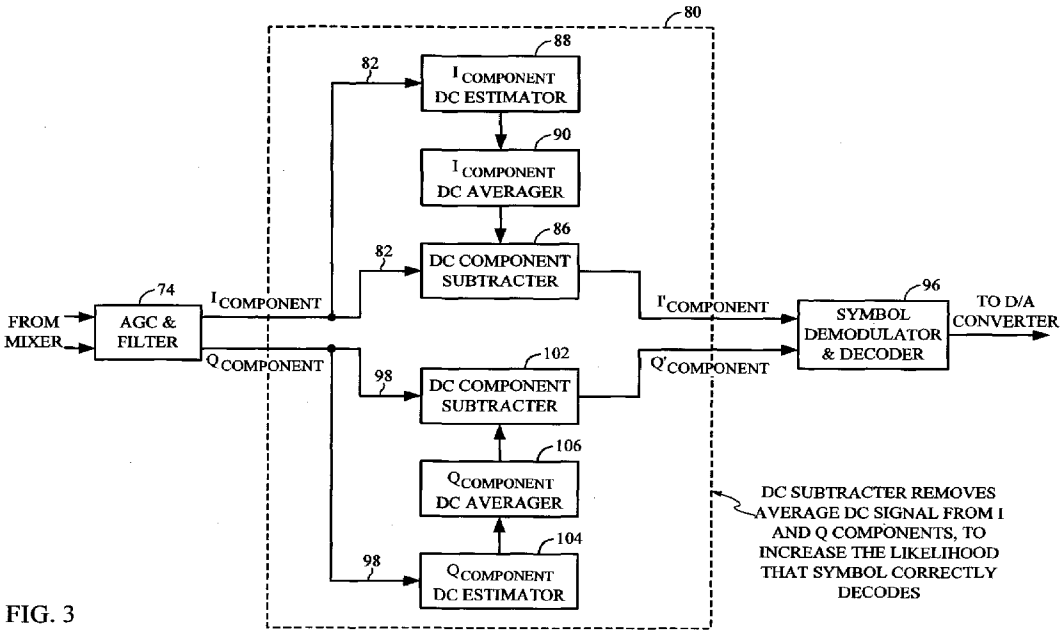


FIG. 3

(57) **Abstract:** A communications system receiver incorporates a time-averaged DC component subtracter to subtract a time-averaged DC offset component from a received, processed signal. The time-averaged DC offset is selectably calculated from a moving average or a running average. The selection of the time-averaged DC offset can be done depending on whether the receiver operates in a frequency hop mode or not.

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# METHOD AND APPARATUS FOR COMPENSATING DC OFFSETS IN COMMUNICATION SYSTEMS

## RELATED APPLICATIONS

**[0001]** This application is a continuation-in-part of copending U.S. patent application serial number 10/722,229, filed November 25, 2003, which is a continuation-in-part of U.S. patent application serial number 10/600,499, filed June 19, 2003, which claims priority to U.S. provisional patent application serial number 60/390,585, filed on June 20, 2002, the full disclosures of which are incorporated herein by reference in their entireties.

## BRIEF DESCRIPTION OF THE FIGURES

**[0002]** Figure 1 illustrates a high-level block diagram of a wireless data communication system incorporating a subtracter.

**[0003]** Figure 2A illustrates a signal map of in-phase (I) and quadrature-phase (Q) inputs to a symbol decoder in an "ideal" or theoretical system.

**[0004]** Figure 2B illustrates a signal map of I and Q inputs to a symbol decoder in the presence of direct current (DC) offsets.

**[0005]** Figure 3 illustrates a block diagram of a receiver incorporating a DC component subtracter.

## DETAILED DESCRIPTION

**[0006]** Figure 1 is a block diagram of a wireless data communications system 10, which includes a transmitter 12 and a receiver 14. At the transmitter 12, as a user 16 speaks into a microphone 18, it converts the sound energy of the user's voice into analog electrical signals having a real-time voltage waveform 20. Although the example shown is described in terms of converted sound energy of a user's voice, the operation of the transmitter 12 is the same, or substantially the same, with respect to other types of signals as well. With appropriate modifications, the transmitter 12, as well as the receiver described below, may also be used to transmit and receive digital signals, the analog embodiment being shown only by way of example.

**[0007]** With reference again to the analog embodiment, a sampler 22 converts the analog electrical signals into discrete electrical signals to provide a sampled waveform 24. A quantizer 26 quantizes the discrete electrical signals into pulse amplitude modulation voltages, representing a quantized waveform version of the sampled waveform 28. An encoder 30 encodes the quantized discrete electrical signal into a string of bits, for example, represented by a stream of eight bit words, or octets 32. The octets are encoded by a symbol encoder 34 according to a symbol encoding scheme. Thus, for example, the symbol encoder 34 encodes each successive two bits of each octet to provide a stream of two bit symbols.

**[0008]** The symbols produced by the symbol encoder 34 represent the values of $I_{component}$ and $Q_{component}$ vectors such that their vector sum results in an appropriate value under the defined signal scheme. The $I_{component}$ vector is multiplied in multiplier 38 by a first sine wave produced by oscillator 40 to produce a modulated "in-phase" (I) signal. On the other hand, the $Q_{component}$ vector is multiplied in multiplier 42 by a second sine wave produced by the oscillator 40 that has been shifted $90^{o}$ by a $90^{o}$ phase shifter 44 to produce a modulated "quadrature-phase" (Q) signal. The I and Q modulated signals are added by an adder 46 together with the sine wave produced by oscillator 40 to produce a composite signal, which is received by modulator 48 to modulate a carrier sine wave. The modulator 48 includes an oscillator 50 and multiplier 52, which multiplies the composite and the oscillator signals to produce the modulated carrier signal, which is then transmitted by an antenna 54.

**[0009]** At the receiver 14, the transmitted signal is received by an antenna 60, which feeds the received signal into a low noise amplifier (LNA) 62, the output of which is connected to a mixer 64, also known as a demodulator. The mixer 64 includes a multiplier 66 and oscillator 68 arranged to produce quadrature output signals on lines 70 and 72. The signals on lines 70 and 72 are connected to a filter and automatic gain control unit (AGC) 74. The filter and AGC unit 74 automatically adjusts the gain applied to the output signals from the AGC 74 as a function of the strength of the modulated carrier received via antenna 60, in order to maintain a relatively constant output signal level.

**[0010]** The quadrature output signals from the filter and AGC unit 74 are connected through a subtracter 80, below described in detail, to a symbol demodulator 76, which demodulates the automatic gain controlled version of the received signal to produce

both the in-phase (I) signal and the quadrature-phase (Q) signals, which respectively represent the received values of the $I_{component}$ vector and $Q_{component}$ vector signals. Thereafter, a symbol decoder 78, which may be a quadrature phase shifted keyed (QPSK) decoder, uses the two bit values of the $I_{component}$ and $Q_{component}$ vectors to produce the decoded successive symbol bits in a stream of reconstructed octet words. The reconstructed octet words are then passed to D/A converter 79, which outputs an analog electrical signal which is converted into sound energy by speaker 81. In processing a digital signal, the output from the signal decoder may be separately processed, without need for the D/A converter 80.

**[0011]** Referring additionally now to Figure 2a, a map of the I and Q inputs to the symbol decoder 76 in an "ideal," or theoretical, system, are shown. In the ideal system, both the I and Q components are always detected correctly by the symbol decoder 78. For instance, in the example shown, respective I and Q values “0” and “1” are properly decoded as “01”.

**[0012]** However, in an actual, physical system, an example of the signal map of which is shown in Figure 2b, without the use of the subtracter 80 system irregularities give rise to direct current (DC) offset voltages on either or both the I and Q components. Factors that may cause the values of the I and Q value to contain a DC offset, for example, include the presence of noise and variations of the signal strength of the received signal, as well as component and circuit imbalances and designs in the receiver system. Moreover, due to the effects of the AGC 74, the DC offsets will tend to vary over time. Such time-varying DC offsets may be difficult to compensate.

**[0013]** Insofar as symbol decoder 78 relies upon both the sign and magnitude of the detected voltages of the respective I and Q components in order to correctly decode a received symbol, the presence of DC offset voltages can result in symbol decoder 78 incorrectly decoding a received symbol. In the example shown, for example, the respective values for I and Q of “0” and “1” shown in Figure 2a have erroneously been detected as “00”, shown in Figure 2b.

**[0014]** The DC offsets which may be present in the received signals, however, can be substantially reduced or eliminated, regardless of whether AGC 74 is causing such DC offsets to change over time, through the use of the subtracter 80 and methods illustrated in the block diagram of Figure 3, to which reference is now additionally made.

**[0015]** The subtracter 80 is placed between the filter & AGC 74 and the symbol demodulator 76 and symbol decoder 78 in the receiver portion of the system 10 (the symbol demodulator 76 and symbol decoder 78 being represented for convenience as a single block 96). Briefly, in the subtracter 80, a time-averaged value of the DC offsets of both I and Q components are substantially removed or eliminated before symbol decoding is performed.

**[0016]** In the subtracter 80, the demodulated in-phase $I_{component}$ signal on line 82 is fed into an $I_{component}$ DC estimator 88. The DC estimator 88 determines an instantaneous DC level in the $I_{component}$ signal, such as through low pass filtering techniques, or the like. The output of the $I_{component}$ DC estimator 88 is fed into an $I_{component}$ DC averager 90, which calculates a time-average of its DC input. The average may be calculated and updated periodically.

**[0017]** In an embodiment, the average may be updated whenever a new output value of the $I_{component}$ DC estimator 88 is made available. In this specification and in the claims, such an average is termed a "moving average." A DC averager calculating a moving average is termed to be in a "moving average mode." The moving average may be calculated as the average of the $I_{component}$ DC estimator 88 output over a predetermined number of values.

**[0018]** In an alternative embodiment, the average may be updated once every predetermined time interval. In this specification and in the claims, such an average is termed a "running average." A DC average calculating a running average is termed to be in a "running average mode." The running average may be calculated as the average of the $I_{component}$ DC estimator 88 over the predetermined time interval. For example, the predetermined time interval may encompass a plurality of DC estimator output values.

**[0019]** In an alternative embodiment, the average may be calculated by another averaging technique.

**[0020]** According to the present disclosure, the DC averager 90 may switch from a moving average mode to a running average mode if the DC offset in the $I_{component}$ signal is expected to change discontinuously, and vice versa. In an embodiment, the $I_{component}$ DC averager 90 may switch between moving average mode and running average mode based on an operating mode of the receiver. For example, if the operating mode of the receiver is a frequency hop mode, the DC averager 90 may be configured to operate in a running average mode. The predetermined time period of the running average mode

may be configured such that only DC estimate values corresponding to a single frequency hop are averaged together. In contrast, if the operating mode of the receiver is a non-frequency hop mode, the DC averager 90 may be configured to operate in a moving average mode.

**[0021]** The output of the $I_{component}$ DC averager 90 is fed into the DC component subtracter 86, which subtracts the time-averaged DC component from the demodulated in-phase $I_{component}$ signal on line 82. The output of the DC component subtracter 86 $I'_{component}$, which represents the $I_{component}$ value having any DC offset that may be contained therein substantially removed, then is fed into the symbol demodulator and decoder 96.

**[0022]** At the same time, in the quadrature signal channel, the demodulated quadrature-phase $Q_{component}$ signal on line 98 is fed into a $Q_{component}$ DC estimator 104. The DC estimator 104 determines an instantaneous DC level in the $Q_{component}$ signal, using techniques described above with respect to the $I_{component}$ DC estimator 88. The output of the $Q_{component}$ DC estimator 104 is fed into a $Q_{component}$ DC averager 106, which calculates a time-average of its DC input using, for example, techniques described above with respect to the $I_{component}$ DC averager 90.

**[0023]** The output of the $Q_{component}$ DC averager 106 is fed into the DC component subtracter 102, which subtracts the time-averaged DC component from the demodulated quadrature-phase $Q_{component}$ signal on line 98. The output of the DC component subtracter 102 $Q'_{component}$, which represents the $Q_{component}$ value having any DC offset that may be contained therein substantially removed, then is fed into the symbol demodulator and decoder 96.

**[0024]** The systems, functions, and operations described in the block diagrams, graphs, or examples above may be implemented, individually or collectively, in hardware, software, firmware, or a combination thereof. For example, the functions may be implemented in application specific integrated circuits (ASICs), standard integrated circuits, as one or more computer programs running on a computer, computer system, one or more controllers (e.g., microcontrollers), one or more processors (e.g., microprocessors), or any combination thereof. In addition, the processes, methods, or techniques of the invention may be distributed as a program product in a variety of forms, such as may be incorporated in a digital storage medium, or the like.

## CLAIMS

1. An apparatus for use in a communications system, the apparatus comprising:

a DC estimator to receive an input signal and generate estimate values of the input signal's DC level;

a DC averager to receive the estimate values and generate a DC average, the DC average selectable from a moving average of the estimate values or a running average of the estimate values; and

a subtracter unit to subtract the DC average from the input signal.

2. The apparatus of claim 1, the DC averager configured to select from a moving average or a running average based on an operating mode of the receiver.

3. The apparatus of claim 2, the DC averager configured to select a moving average if the receiver is in a frequency hop mode, the DC averager further configured to select a running average if the receiver is not in a frequency hop mode.

4. The apparatus of claim 3, the input signal comprising an in-phase (I) component and a quadrature (Q) component, the DC estimator configured to generate estimate values for each of the I and Q components, the DC averager configured to generate DC averages for the estimate values generated for each of the I and Q components, and the subtracter unit configured to subtract a DC average from each of the I and Q components.

5. The apparatus of claim 3, further comprising:

an automatic gain correction unit to receive an uncorrected modulated composite signal, provide gain correction, and output a corresponding gain corrected modulated composite signal to the demodulator; and

a symbol decoder to receive the demodulated component output from the subtracter unit and output a corresponding plurality of symbol bits.

6. The apparatus of claim 5, wherein the apparatus is a handset in a wireless communication system, further comprising:

an antenna to communicate a wireless signal to the automatic gain correction unit;

a converter unit to convert the plurality of symbol bits output from the symbol decoder into a corresponding analog signal; and

a transducer for converting the analog signal from the converter unit into an acoustic signal.

7. The apparatus of claim 5, wherein the apparatus is an integrated circuit adapted for use in a handset, the handset comprising:

an antenna to communicate a wireless signal to the automatic gain correction unit;

a converter unit to convert the plurality of symbol bits output from the symbol decoder into a corresponding analog signal; and

a transducer for converting the analog signal from the converter unit into an acoustic signal.

8. The apparatus of claim 7, wherein the communication system further comprises a transmitter to transmit the wireless signal to the antenna.

9. The apparatus of claim 3, wherein the apparatus is a programmable microprocessor running executable code in a handset configured to operate within the communications system.

10. The apparatus of claim 3, wherein the uncorrected modulated composite signal is a quadrature phase shift keying signal.

11. A method for use in a communication system, the method comprising:

receiving an input signal and generating estimate values of the input signal's DC level using a DC estimator;

receiving the estimate values using a DC averager to generate a DC average, the DC average selectable from a moving average of the estimate values or a running average of the estimate values; and

subtracting the DC average from the input signal.

12. The method of claim 11, further comprising selecting from a moving average or a running average based on an operating mode of the receiver.

13. The method of claim 12, further comprising selecting a moving average if the receiver is in a frequency hop mode, and selecting a running average if the receiver is not in a frequency hop mode.

14. The method of claim 13, the input signal comprising an in-phase (I) component and a quadrature (Q) component, the DC estimator configured to generate estimate values for each of the I and Q components, the DC averager configured to generate DC averages for the estimate values generated for each of the I and Q components, and the subtracting comprising subtracting a DC average from each of the I and Q components.

15. The method of claim 13, further comprising:

receiving an uncorrected modulated composite signal, providing gain correction, and outputting a corresponding gain corrected modulated composite signal as the input signal; and

symbol demodulating the output of said subtracting.

16. The method of claim 15, further comprising:

decoding the demodulated symbols;

converting the decoded symbols into a corresponding analog signal; and

converting the analog signal from the converter unit into an acoustic signal.

17. An apparatus for use in a communications system, the apparatus comprising:

DC estimator means for receiving an input signal and generating estimate values of the input signal's DC level;

DC averager means for receiving the estimate values to generate a DC average, the DC average selectable from a moving average of the estimate values or a running average of the estimate values; and

subtracter means for subtracting the DC average from the input signal.

18. The apparatus of claim 17, further comprising means for selecting from a moving average or a running average based on an operating mode of the receiver.

19. The apparatus of claim 18, further comprising means for selecting a moving average if the receiver is in a frequency hop mode, and selecting a running average if the receiver is not in a frequency hop mode.

20. The apparatus of claim 19, the input signal comprising an in-phase (I) component and a quadrature (Q) component, the DC estimator means configured to generate estimate values for each of the I and Q components, the DC averager means configured to generate DC averages for the estimate values generated for each of the I and Q components, and the subtracter means comprising subtracting a DC average from each of the I and Q components.

21. The apparatus of claim 19, further comprising:

means for receiving an uncorrected modulated composite signal, providing gain correction, and outputting a corresponding gain corrected modulated composite signal as the input signal; and

means for symbol demodulating the output of said subtracting.

22. The apparatus of claim 21, further comprising:

means for decoding the demodulated symbols;

means for converting the decoded symbols into a corresponding analog signal; and

means for converting the analog signal from the converter unit into an acoustic signal.

23. The apparatus of claim 19, wherein the communication system further comprises a transmitter to transmit the wireless signal to the antenna.

24. The apparatus of claim 19, wherein the apparatus is a programmable microprocessor running executable code in a handset configured to operate within the communications system.

25. The apparatus of claim 19, wherein the uncorrected modulated composite signal is a quadrature phase shift keying signal.

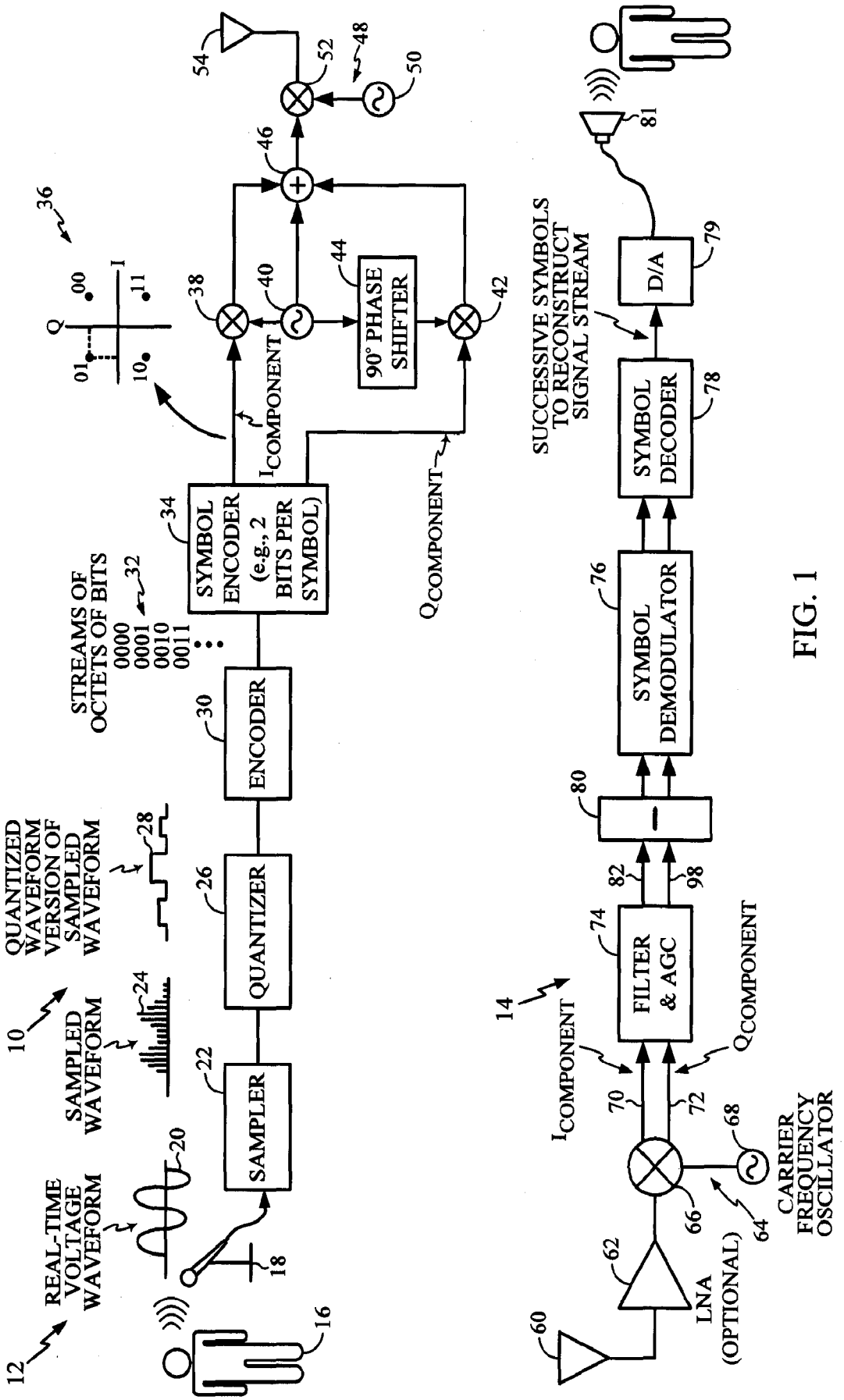
12
REAL-TIME VOLTAGE WAVEFORM
10
SAMPLED WAVEFORM
QUANTIZED WAVEFORM VERSION OF SAMPLED WAVEFORM
STREAMS OF OCTETS OF BITS
0000
0001
0010
0011
SAMPLER
QUANTIZER
ENCODER
SYMBOL ENCODER (e.g., 2 BITS PER SYMBOL)
I COMPONENT
Q COMPONENT
90° PHASE SHIFTER
16
18
20
22
24
26
28
30
32
34
36
38
40
42
44
46
48
50
52
54
14
I COMPONENT
Q COMPONENT
FILTER & AGC
SYMBOL DEMODULATOR
SYMBOL DECODER
SUCCESSIVE SYMBOLS TO RECONSTRUCT SIGNAL STREAM
D/A
LNA (OPTIONAL)
CARRIER FREQUENCY OSCILLATOR
60
62
64
66
68
70
72
74
76
78
79
80
81
82
98

FIG. 1

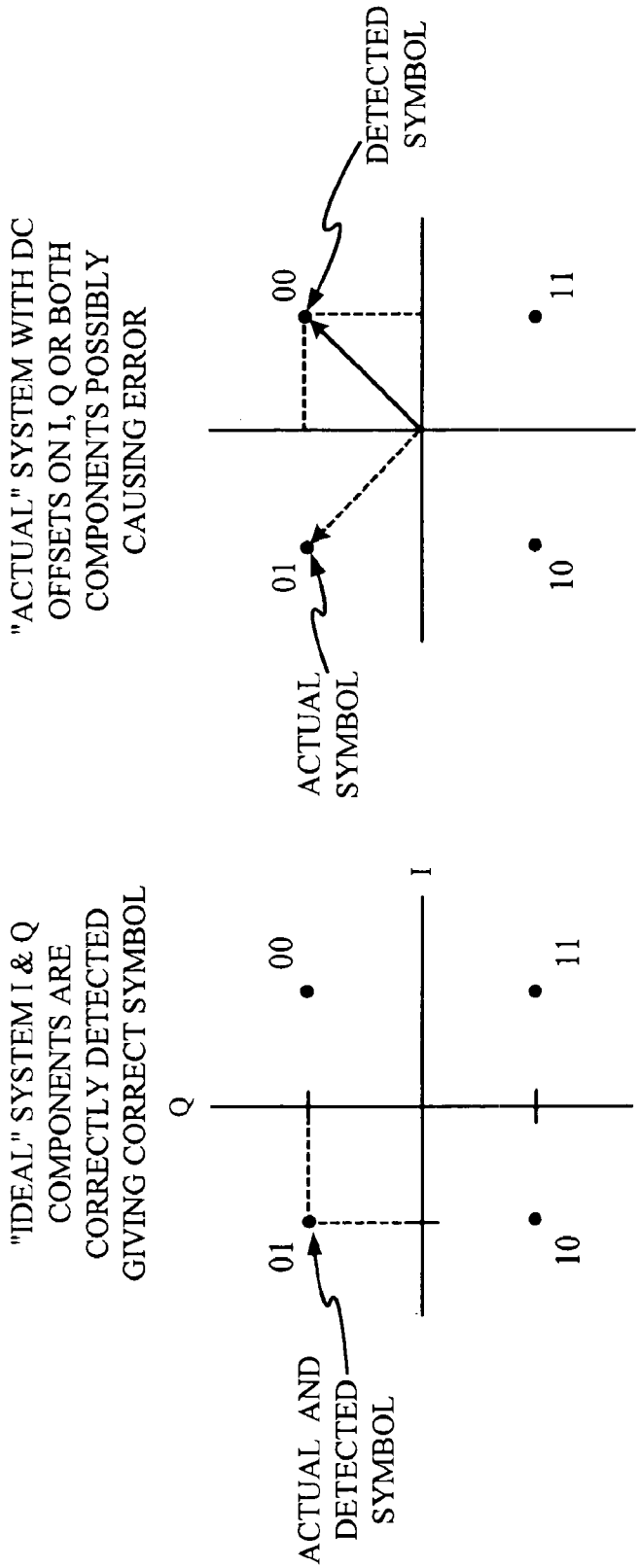
"IDEAL" SYSTEM I & Q COMPONENTS ARE CORRECTLY DETECTED GIVING CORRECT SYMBOL
Q
I
00
01
10
11
ACTUAL AND DETECTED SYMBOL
"ACTUAL" SYSTEM WITH DC OFFSETS ON I, Q OR BOTH COMPONENTS POSSIBLY CAUSING ERROR
DETECTED SYMBOL
ACTUAL SYMBOL

FIG. 2A

FIG. 2B

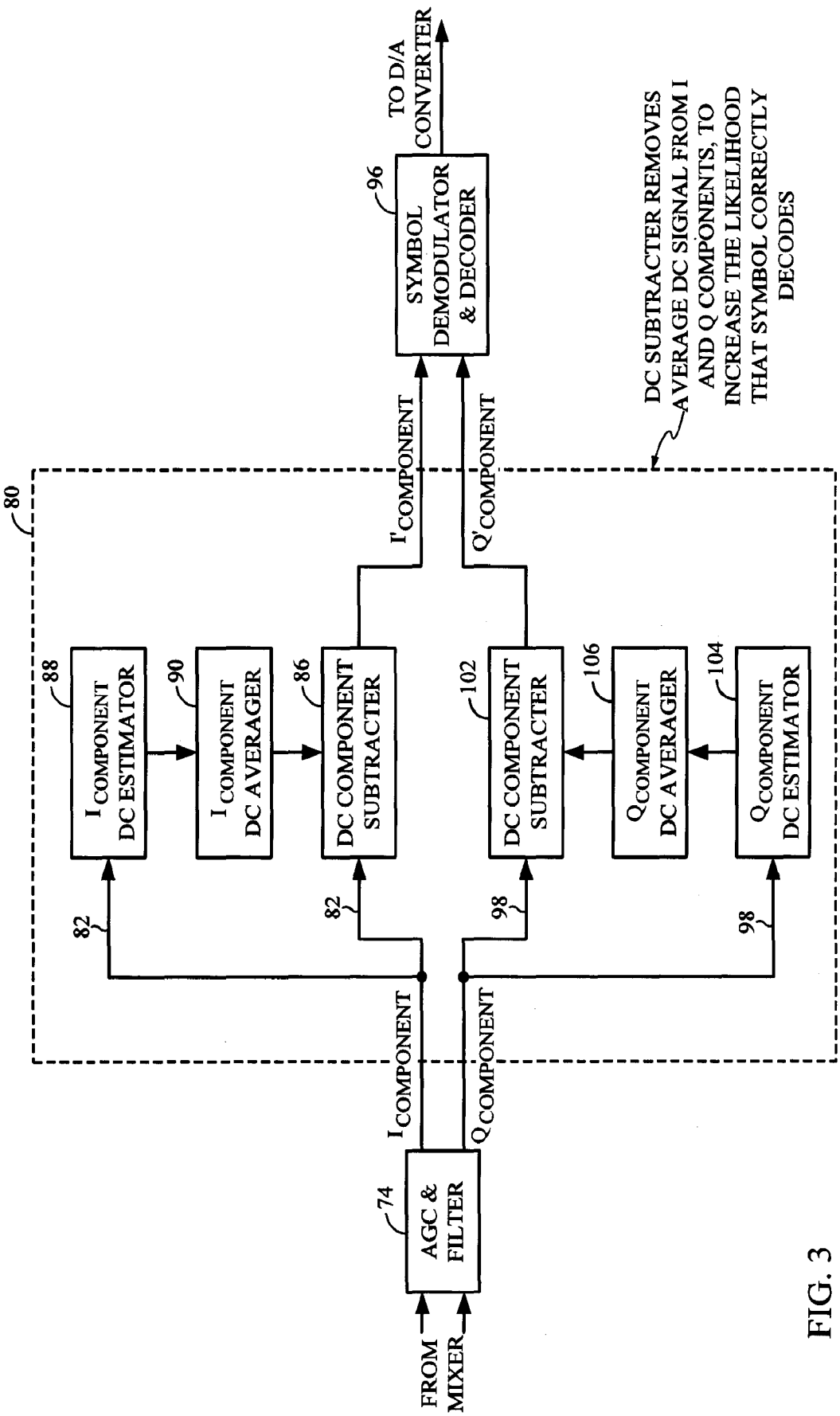
FROM MIXER
74
AGC & FILTER
I COMPONENT
Q COMPONENT
80
82
98
I COMPONENT DC ESTIMATOR
88
I COMPONENT DC AVERAGER
90
DC COMPONENT SUBTRACTER
86
Q COMPONENT DC ESTIMATOR
104
Q COMPONENT DC AVERAGER
106
DC COMPONENT SUBTRACTER
102
I' COMPONENT
Q' COMPONENT
SYMBOL DEMODULATOR & DECODER
96
TO D/A CONVERTER
DC SUBTRACTER REMOVES AVERAGE DC SIGNAL FROM I AND Q COMPONENTS, TO INCREASE THE LIKELIHOOD THAT SYMBOL CORRECTLY DECODES

FIG. 3