

Oct. 14, 1969

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3,473,082

INTENSITY CONTROL FOR CRT DISPLAY

Filed Sept. 20, 1968

5 Sheets-Sheet 1

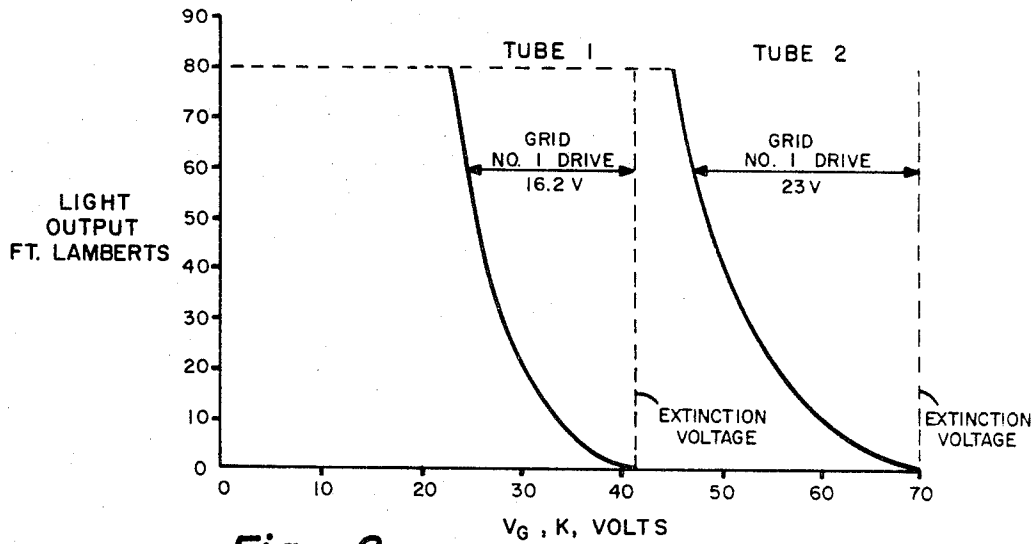


Fig. 2

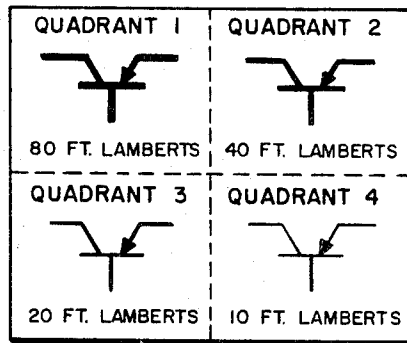


Fig. 3

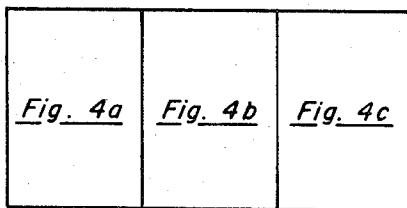


Fig. 4

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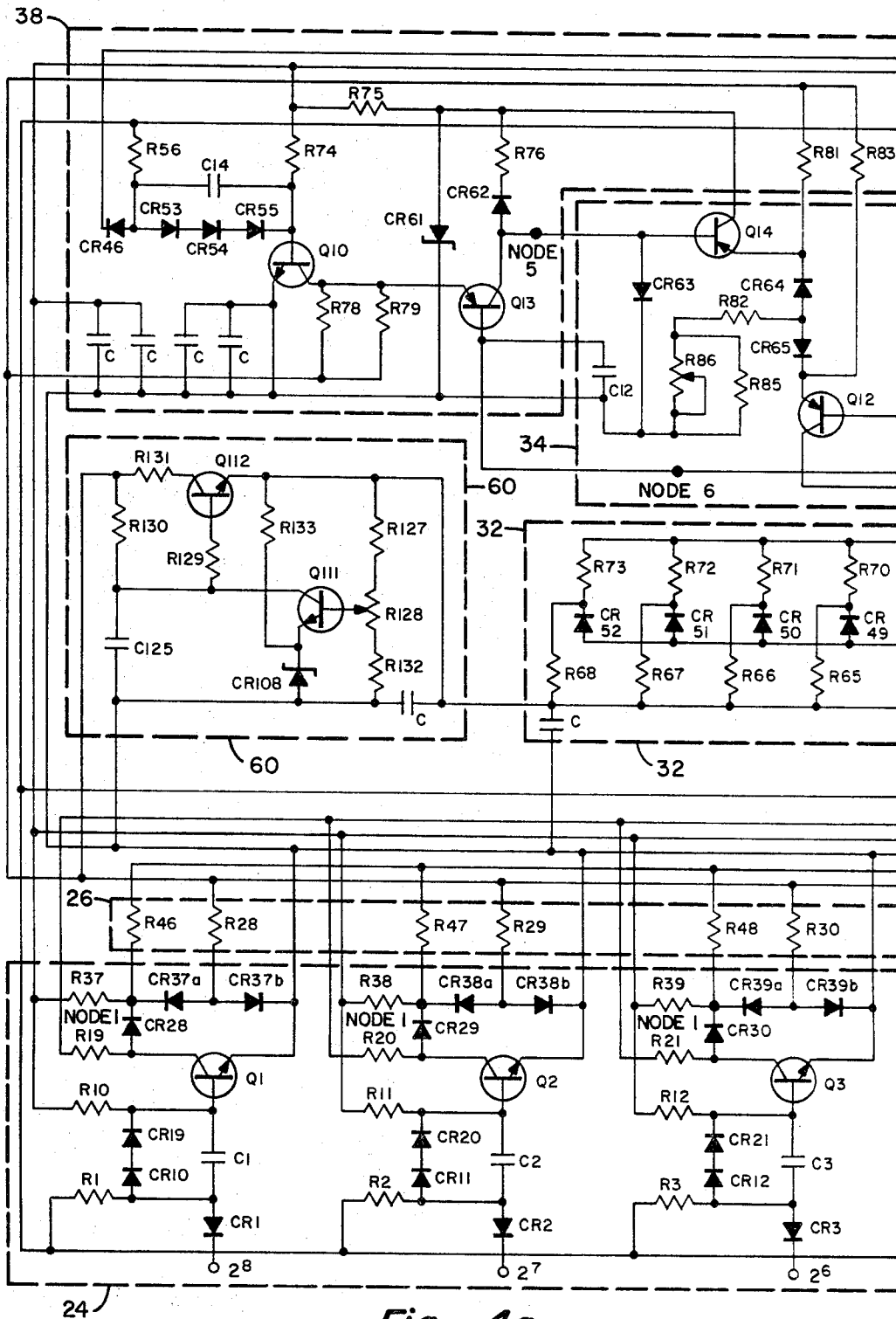


Fig. 4a

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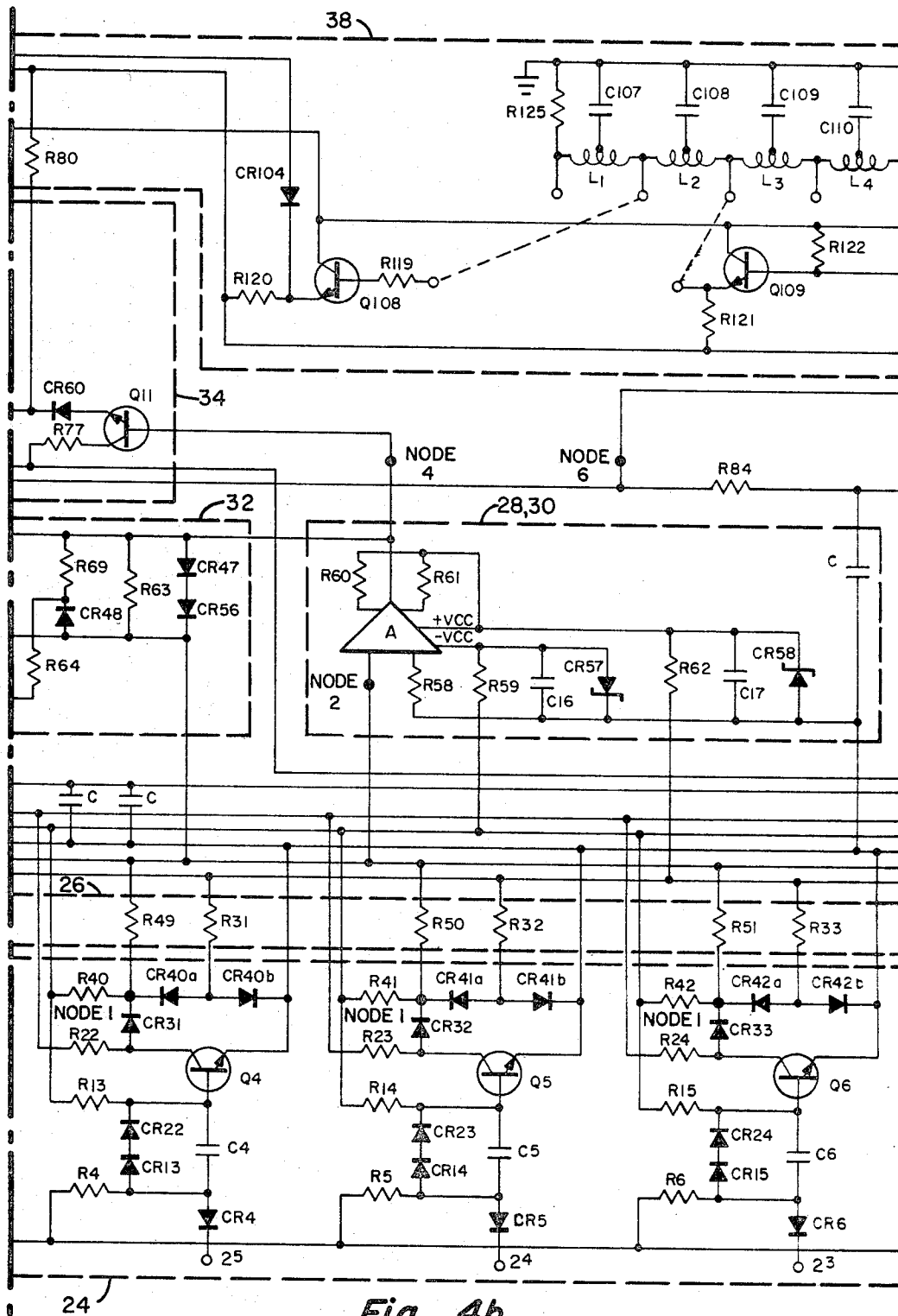
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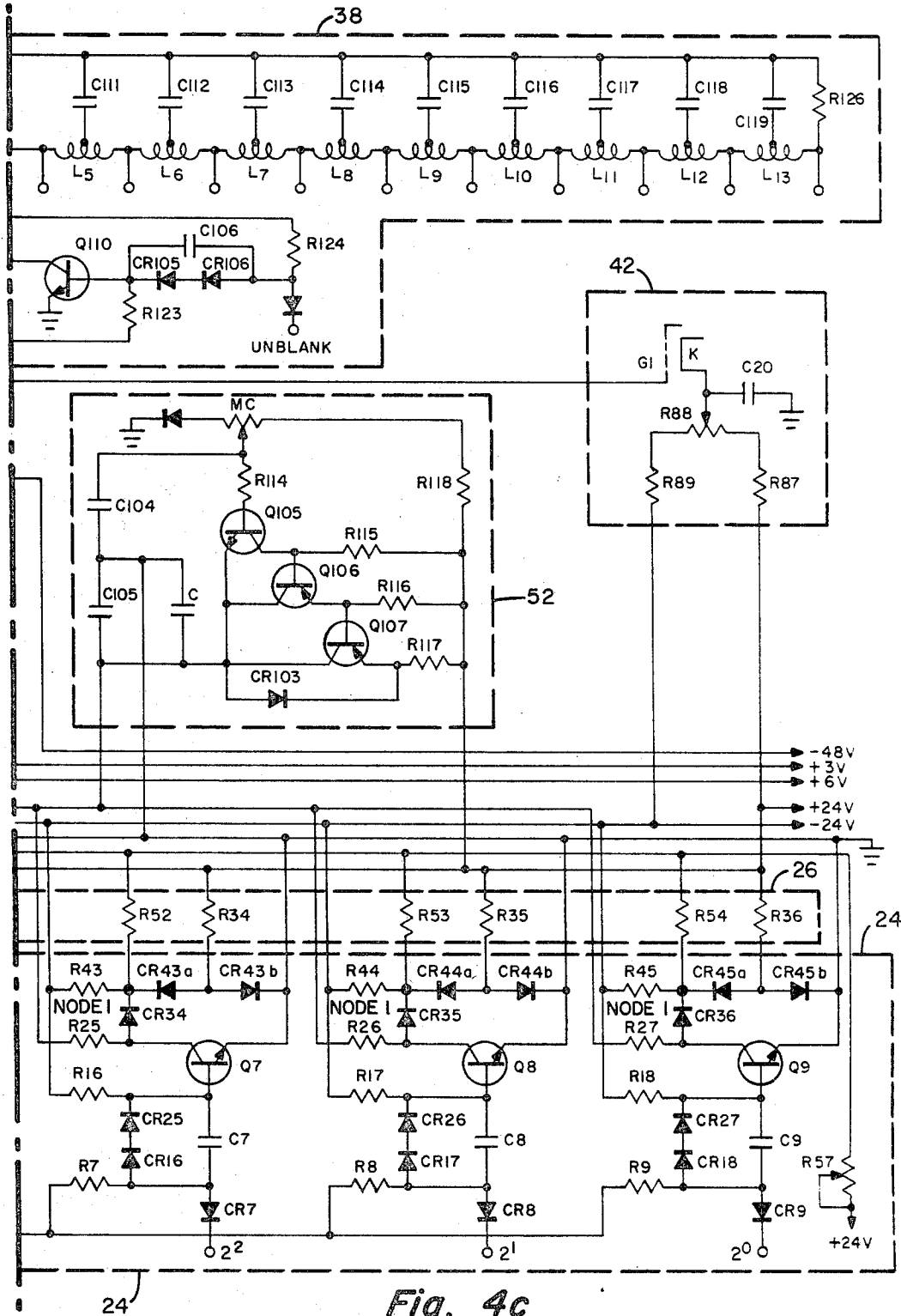
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3,473,082

INTENSITY CONTROL FOR CRT DISPLAY

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10 Claims

ABSTRACT OF THE DISCLOSURE

An improved image intensity control circuit for use with cathode ray tube display is described. The intensity control system described provides for permitting the changing of the intensity of n gradations differentiated by a factor of 2, while permitting the intensities of images in different portions of the screen to be different with respect to other selected portions of the screen. The image intensity control circuit responds to externally applied digital-data intensity-defining signals for providing the selected image intensity of the displayed image automatically. An auxiliary manual intensity control device is described for selecting a base level of intensity for use in conjunction with the externally applied digital-data intensity-defining signals. The image intensity control circuit operates to control the cathode-to-grid bias voltage for controlling the intensity of the electron beam.

BACKGROUND OF THE INVENTION

Field of the invention

This invention relates generally to the field of cathode ray tube displays, and has particular application for those cathode ray tube display devices having capability of displaying vectors and characters. The invention is particularly applicable to those cathode ray tube display devices that are utilized in data processing systems.

Description of the prior art

Prior art cathode ray tube display devices have had several problems in the control of the beam intensity. One problem has been in arriving at a linear approximation of the relationship between the resulting intensity of the electron beam based on the bias voltage applied to the cathode ray tube. Such non-linearity provides the disadvantage of having the intensity change by differing amounts for incremental changes in the bias voltage. Another problem in the prior art was the lack of the ability for a given image intensity control circuit to respond to a plurality of programmable levels of intensity as determined by a programmable control device such as the data processor. While cathode ray tube display devices have been developed that will provide for one or two image intensity levels, no known prior art display systems have been made capable of providing programmable image intensity levels, nor have they provided for an image intensity control circuit that will allow selected images or portions of the face of the cathode ray tube to exhibit different image intensities. While the prior art display devices have provided one form or another of manual intensity control, there are no known prior art devices that combine a programmable image intensity level control with a manual intensity control, whereby the entire display can be manually altered in intensity while maintaining the programmable difference of image intensity of selected images. Yet another problem of the prior art, is

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the matching of the response of beam deflection system with the image intensity control circuit response.

SUMMARY

With the foregoing mentioned problems of the prior art in mind, and with the object of providing an overall improved image intensity control circuit, the subject invention was made. The image intensity control circuit of this invention includes a cathode ray tube display control portion for receiving programmable commands from an associated processor. The cathode ray tube control portion provides the overall control for the cathode ray tube device, and provides the digital image intensity control signals that are utilized to drive the image intensity control circuit. Ultimately, the digital image intensity control signals are converted to a voltage level by the image intensity control circuit, and applied to grid number 1 of a cathode ray tube for establishing a cathode-to-grid bias voltage that will determine the image intensity of the light output from the cathode ray tube. The image intensity control circuit utilizes a transistor switching network at the input for receiving the digital image intensity signals for driving a weighted input resistor network for developing current levels to an amplifier. Associated with the amplifier is an automatically variable feed back network that responds to the various current level inputs for controlling the voltage change at the output of the amplifier. A control amplifier responds to this voltage and to a blank/unblank signal for providing a resultant bias voltage to grid 1 of the cathode ray tube when the control amplifier is unblanked. A manual intensity control circuit is coupled to the transistor switching network for providing a uniform bias level for the images on the entire face of the cathode ray tube.

In view of the foregoing, it can be seen that a primary object of this invention is to provide an improved cathode ray tube display system. Yet another object of this invention is to provide an improved image intensity control circuit capable of responding to programmable digital-data intensity-defining signals for establishing programmably alterable image intensity levels on the screen of the cathode ray tube. Still a further objective of this invention, is to provide an image intensity control system for controlling the image intensity in a continuous manner in response to digital-data intensity-defining input signals. Yet a further objective of this invention is to provide an improved image intensity control circuit wherein the over-all image intensity can be manually controlled while maintaining programmed image-intensity differences in the same ratios. Still a further objective of this invention, is to provide an improved image intensity control circuit utilizing a plurality of weighted input resistors in conjunction with an amplifier and an automatically variable feed back network for providing digital-to-analog conversion for providing a controlled cathode-to-grid bias voltage for a cathode ray tube.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and more detailed objectives will become apparent when considering the following specification in light of the drawings in which: FIGURE 1 is a block diagram of the improved image intensity control circuit of this invention; FIGURE 2 are characteristic plots of the light output in foot lamberts in response to changes in the cathode-to-grid voltage changes for a pair of cathode ray tubes; FIGURE 3 is a characteristic view of the face of the cathode ray tube wherein the programmable intensity levels are presented as factors of

two in the four quadrants of the face of the cathode ray tube; and FIGURES 4a through 4c, when arranged as shown in FIGURE 4 are a circuit schematic diagram of the inventive image intensity control circuit.

DESCRIPTION OF THE PREFERRED EMBODIMENT

In modern day cathode ray tube display systems, it has been found desirable to intensify one or more images that appear on the face of the cathode ray tube to emphasize the image by causing it to appear more brightly. The image intensity control circuit of this invention provides for changing the intensity of the image to n gradations differentiated by the factor of two as well as permitting different images to be different in intensity with respect to each other. For example, referring briefly to FIGURE 3, it can be seen that this system has been established wherein each quadrant is illuminated to a different degree, for example, when quadrant one is illuminated to 80 foot lamberts, quadrant two can be illuminated to 40 foot lamberts, quadrant 3 to 20 foot lamberts, and quadrant 4 to 10 foot lamberts. In the drawing, image intensity is depicted by correspondingly heavier lines. To accomplish the variable image intensity, image intensity control circuitry is utilized to respond to digital-data image-intensity control signals for generating an appropriate cathode-to-grid bias voltage for the cathode ray tube. Referring to this bias voltage as V_b , it will be apparent that the image intensity I will be a function of the bias voltage V_b . Therefore, by appropriately controlling the bias voltage V_b , the intensity I of the images on the cathode ray tube face will be controlled.

Turning now to a consideration of FIGURE 1, which is a block diagram of the image intensity control circuit of this invention, there is shown a digital data processor 10 for providing control signals over path 12 to the display control 14 of the cathode ray tube display device. The signals provided by processor 10 will include the designation of vector or character images that are to be displayed on the cathode ray tube 16. Also, the processor will at least in part determine the intensity levels to be applied to the cathode ray tube 16. The display control 14 will operate to evaluate the signals received from processor 10 and will provide further manipulation of the digital-data image-intensity control signals. It will be noted that in some cathode ray tube display devices, fixed time-increments are provided for displaying images of varying lengths and sizes. Accordingly, in order for the various images to appear at uniform intensity, it is necessary to increase the bias voltage V_b for the time interval that a relatively long vector image is to be displayed, over the level of the bias voltage V_b that would be required for a shorter vector image. This factor is taken into account by the display control 14 as one element in the determination of the digital image-intensity control signals. Yet another factor in determining the image intensity, is the intensity level specified by the processor 10. Taking all of the various factors required for the determination of the image intensity for any given image into account, the display control 14 sends a grouping of digital image-intensity control signals over lines 18 to shift register 20. The shift register 20 is then controlled by the display control 14 for providing the appropriate digital numerical value for input to the image intensity control circuit. For sake of definition, it will be assumed that a predetermined minimum image intensity will result with the digital image-intensity control signals in an unshifted position in shift register 20. In order to change the intensity by a factor of 2, the digital image-intensity control signals are shifted upward in significance one position in order of magnitude. It will be understood that this relationship of a factor of 2 is purely arbitrary and that different gradations can be achieved by adjusting the circuitry in the image intensity control circuit such that the relationship of the shifting in the shift register will have

some other predetermined relationship to a change of intensity of the image on the face of the cathode ray tube 16.

The digital image-intensity control signals held in the shift register 20 are then applied over lines 22 to respective stages of a transistor switching network 24. The combination of digital image-intensity control signals will cause selected ones of the transistor switches in the transistor switching network 24 to switch and drive currents through respectively associated weighted input resistors in weighted input resistor network 26. The weighted input resistor network 26 drives node 2, which is coupled to an input of a high input-impedance amplifier 28, and node 2 will be seen to be a virtual ground. The weighted input resistor 26 will determine the current flow at node 2. The summed current of node 2 is also applied to the automatically variable feedback network 32. The amplifier 28 receives a reference level 30 and is coupled to the automatically variable feedback network 32. The automatically variable feedback network 32 sees the same current flow from the summing resistors as the high input-impedance amplifier 28. As different current increments are provided in response to different selections made by the digital image-intensity control signals, the impedance of the automatically variable feedback network 32 will be varied. The interaction of the automatically variable feedback network 32 and amplifier 28 will determine the potential V_4 at node 4.

The potential V_4 is applied to the control amplifier 34. This control amplifier also receives the blank/unblank control signal from the display control 14 by way of control line 36, the delay line with transmission drivers 38, and control line 40. If the potential at node 4 is higher than the potential V_5 at node 5, the potential V_6 at node 6 will be driven accordingly. The potential V_6 at node 6 in combination with a potential at the cathode K of the cathode ray tube determine V_b , the tube bias. To blank the tube, the display control 14 provides a signal through the delay line transmission drivers 38 for holding the potential V_5 more positive than the potential V_4 . To unblank the cathode ray tube, potential V_5 is dropped below the level of V_4 and the image is unblanked and allowed to establish a bias at node 6 that will cause the image to be displayed. A cathode voltage control 42 is coupled via line 44 to the cathode K of tube 16. Tube 16 also has power source 46 coupled to grid G2 via line 48 and to tube via line 50. As will be described in more detail below, the delay line with transmission drivers 38, is utilized to synchronize the deflection signals and the image intensity signals.

It will be recalled that the voltage V_1 at node 1 basically determines the ultimate image intensity by controlling the voltage applied to grid G1. A manual intensity control 52 is coupled to a voltage source V_1 and directed over line 54 to the transistors switching network 24. The manual intensity control 52 operates to establish a base level of image intensity. By way of example, let it be assumed that the manual intensity control 52 is at a predetermined image intensity level. The display control 14 then provides shifted digital image intensity control signals to the transistor switching network 24, whereby the image will be displayed at 80 foot lamberts. Then let it be assumed that another image is displayed by the display control 14 at 40 foot lamberts, with the same manual intensity control setting. The system is so arranged that under these conditions, changing the manual intensity control 52 such that the 80 foot lambert image is displayed at 60 foot lamberts, the second image will be correspondingly reduced in illumination to maintain the same illumination ratio. Therefore it can be seen that for any combination of intensities of images, the manual intensity control 52 will operate to either increase or decrease the image intensity for the entire display.

Next turning to a consideration of FIGURE 2, it will be seen that it is a plot of the light output in foot lamberts for

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two cathode ray tubes based on the cathode-to-grid voltage differentials. This figure is intended to show that different tubes will have different extinction voltages. In order to accommodate these different extinction voltages characteristics, a cathode voltage control 42 is utilized in the image intensity control circuit of this invention. The adjustment is made to accommodate the characteristic of the given tube and will be discussed in somewhat more detail below in the consideration of the detail circuitry.

Turning now to a consideration of FIGURES 4a through 4c, which when arranged as shown in FIGURE 4, are a detailed circuit diagram of the image intensity control circuit of this invention. The various components utilized in the preferred embodiment are set forth in Table I. It should be understood that these components are available commercially, and that while the particular circuit diagram shown has been found to be advantageous in performing the desired functions, it is recognized that various circuit modifications could be made without departing from the scope and spirit of the invention.

In this discussion, the circuit components that are included within the block representations referred to in FIGURE 1 will be enclosed in dashed-line blocks and will bear similar reference numerals. Reference to the particular circuit components will be by way of specific component reference designation.

The transistors switching network is shown enclosed within dashed block 24, and for this embodiment comprises stages 2⁹ through 2⁸. These input terminals are coupled to the shift register 20 mentioned with regard to FIGURE 1. For this embodiment, ground (a substantial zero volt signal) will represent a logical 1; and a plus voltage (for example +6 volts), will represent a logical 0. The circuit arrangement is such each of the stages operate in a similar fashion, so a consideration of an example stage will be sufficient for understanding of the circuit operation. Considering the lowest ordered stage for bit position 2⁰, it will be seen that transistor Q9 has a pair of matched diodes CR45a and CR45b coupled anode-to-anode across the collector-emitter circuit of transistor Q9. The selection of the resistor, capacitor, and diode values for the remainder of the circuit, as shown in Table I, and is such that when the digital input signal is such that transistor Q9 is switched to a conducting state, the voltage at node 1 for the stage will be zero. Alternatively, if the digital input signal to the stage is such that transistor Q9 is switched to a nonconducting state, the potential level at node 1 for the stage will be at a positive level. With the transistor Q9 switched to conduct, a portion of the current flow will be through resistor R27 and the resistor to ground, at a portion will be through resistor R36 and diode CR45b to ground. This will result, as mentioned above, in substantially a zero voltage at node 1 for the stage. However, when the transistor Q9 is switched off, the current flow will be partially through resistor R36 and CR45b to ground, and partially through CR45a to node 1 and then to resistor R54.

The weighted input resistor network 26 is comprised of resistors R46 through R54. These weighted resistors have a resistive value relationship of a power of 2. That is, R46 has a nominal resistor value R. For this embodiment, the value R is of 9530 ohms. Resistor R47 is twice this value; R48 is four times this value; R49 is eight times this value; R50 is sixteen times this value; R51 is thirty-two times this value; R52 is sixty-four times this value; R53 is one hundred twenty-eight times this value; and R54 is two hundred fifty-six times this value. From this it can be seen that the least significant digit position 2⁰ has the largest resistor value and will provide the smallest increment of current. Alternatively, stage 2⁸ has the smallest resistive value and will provide the largest increment of current. These weighted input resistors are coupled to a common point and then to node 2 for amplifier A in the circuit diagram. The same common point is coupled

as an input to the automatically variable feedback network 32.

The circuitry enclosed within dashed block 28, 30 comprises the amplifier 28 and the reference 30, referred to in FIGURE 1. In this circuitry representation the amplifier 28 is referred to as A, and the remainder of the circuitry is utilized to establish the reference for one of the inputs to the amplifier.

Amplifier A has a high input impedance. The summing resistors R46 through R54 will determine the current flow to node 2, as mentioned above. This same current flow will be provided to the automatically variable feedback network 32. This automatically variable network is coupled across the amplifier A, and receives the same current flow as provided at node 2. A voltage regulator, shown enclosed in dashed block 60, provides the regulated 12 volt level to the common point of resistors R64 through R68. The summed current is provided to a common point of diodes CR46, CR48 through CR52, and resistor R63. A common point for resistors R63, R69 through R73, and diode CR47 is coupled to line common with node 4. The arrangement of diodes and resistors, as shown, results in an automatically variable resistive value for the total network that is dependent upon the current level applied thereto. That is, as additional increments of current are added by appropriately selecting higher valued digital-data image-intensity defining signals, the total resistive value of the network will be altered. Therefore, the combination of the automatically variable feedback network 32 and the amplifier circuit arrangement 28, 30 as controlled by the current level in the summing resistors, will determine the potential V4 at node 4.

Node 4 is coupled as input to the control amplifier section, shown enclosed in dashed block 34. The control amplifier provides an output at node 6 that is directed to grid 1 of the cathode ray tube. Control amplifier 34 also receives the blank/unblanked control signal. The circuitry shown enclosed within dashed block 38 includes the delay line with the transmission drivers and controls for the blanking and unblanking of the cathode ray tube in accordance with the signal received from the display control 14 at the diode CR107. The blank or unblank signal so applied, is passed through the amplifiers including transistors Q109 and Q110 and to a selected tap on the delay line, such as the input tap to L2. Another selected tap is coupled to a terminal of resistor R119 where the signal is utilized to drive another amplifier that determines the voltage level at node 5. When the appropriate unblank signal is received at CR107, a predetermined time later, transistor Q10 is switched to saturation and operates to drive transistor Q13 to a mode of operation for providing a voltage level at node 5 lower than the voltage level at node 4. Under such a condition, the cathode ray tube is unblanked and the voltage level in control amplifier 34, as determined by the current sum resulting from the weighted input resistor network 26, will be passed to the cathode ray tube grid 1. Alternatively, when the blank signal is received at CR107, transistor Q10 will be switched off, and in turn, will cause Q13 to put node 5 at a voltage level higher than the voltage level of node 4.

The delay line is utilized to match the propagation time for the deflection amplifier to the image intensity control circuit.

It will be recalled from the consideration of FIGURE 2, that various cathode ray tubes have different voltage ranges required for the cathode-to-grid bias to cause extinction. To accommodate varying parameter tubes, the circuitry enclosed within dashed block 42 is used for providing a variable voltage drive to the cathode ray tube. It can be seen that a voltage divider network comprised of resistors R87 together with potentiometer R88 are coupled intermediate plus 24 volt and minus 24 volt supplies. It will be noted that -48 volts is the most negative that grid 1 can be driven. For those tubes requiring a greater volt-

age difference for the cathode-to-grid potential difference, the potentiometer R88 can be adjusted to provide this necessary potential difference. These adjustments are normally made to accommodate the image intensity control circuits to a particular tube.

The manual intensity control is shown enclosed in dashed block 52. The manual control, labeled MC, is provided at the operators console. This manual control is a potentiometer coupled between a ground level and +24 volts. The wiper of the potentiometer is coupled to the input of amplifier stage Q105 which in turn drives transistors Q106 and Q117. The collector of transistor

Q117 is coupled to the common points of the collector-resistors R19 through R27 for the transistor switching network 24. This potential in conjunction with the ground potential coupled to the emitter circuits provides the operational parameters for the transistors switching network, and allow the intensity of images applied on the cathode ray tube to be changed in intensity by the manipulation of control MC. As described above, the operation of the manual control is over and above the operation that is provided by the application of the digital-data intensity-defining signals to the input terminals of the transistor switching network.

TABLE I

C.	Capacitor, 75 V., 2.2 μ f. $\pm$ 20%.
R85.	Resistor, 200 ohm $\pm$ 1%.
R70.	Resistor, 750 ohm $\pm$ 1%.
R22.	Resistor, 1,300 ohm $\pm$ 1%.
R23.	Resistor.
R24 through R27.	Resistor, 1,500 ohm $\pm$ 1%.
R82.	Resistor, 200 ohm $\pm$ 2%.
R84.	Resistor, 910 ohm $\pm$ 2%.
R19.	Resistor, 1,050 ohm $\pm$ 1%.
R20.	Resistor, 1,150 ohm $\pm$ 1%.
R21.	Resistor, 1,240 ohm $\pm$ 1%.
R73.	Resistor, 2,370 ohm $\pm$ 1%.
R71.	Resistor, 5,110 ohm $\pm$ 1%.
R37 through R45.	Resistor, 11,800 ohm $\pm$ 1%.
R68.	Resistor, 5,900 ohm $\pm$ 1%.
R67.	Resistor, 7,150 ohm $\pm$ 1%.
R46.	Resistor, 9,530 ohm $\pm$ 1%.
R70.	Resistor, 9,750 ohm $\pm$ 1%.
R69.	Resistor, 10,500 ohm $\pm$ 1%.
R28 through R36.	Resistor, 5,750 ohm $\pm$ 1%.
R47.	Resistor, 19,100 ohm $\pm$ 1%.
R66.	Resistor, 24,300 ohm $\pm$ 1%.
R48.	Resistor, 38,300 ohm $\pm$ 1%.
R63.	Resistor, 61,900 ohm $\pm$ 1%.
R65.	Resistor, 68,100 ohm $\pm$ 1%.
R49.	Resistor, 76,800 $\pm$ 1%.
R50.	Resistor.
R64.	Do.
R51.	Do.
R78, R79.	Resistor, 1.5K ohm $\pm$ 2%.
R75.	Resistor, 160 ohm $\pm$ 2%.
CR57, CR58.	Diode, V.R., 1 watt, 15.0 volt.
R77.	Resistor, 160 ohm $\pm$ 5%.
R87.	Resistor, 510 ohm $\pm$ 5%.
R80.	Resistor, 3.0K ohm $\pm$ 5%.
R89.	Resistor, 1.2K ohm $\pm$ 5%.
R58, R60, R61, R81, R83.	Resistor, 45K ohm $\pm$ 5%.
R55.	Resistor, 430K ohm $\pm$ 5%.
R52.	Resistor, 620K ohm $\pm$ 5%.
R53.	Resistor, 1.2M ohm $\pm$ 5%.
R54.	Resistor, 2.4M ohm $\pm$ 5%.
R59, R62.	Resistor, 240 ohm $\pm$ 2%.
C10.	Capacitor, 35 volt, 2.2 μ f. $\pm$ 20%.
CR61.	Diode, Zener, 12 volt.
R1 through R9.	Resistor, 750 ohm $\pm$ 2%.
R10 through R18, R74.	Resistor, 16K ohm $\pm$ 2%.
R56.	Resistor, 560 ohm $\pm$ 2%.
R86.	Resistor, variable, 200 ohm $\pm$ 10%.
R88.	Resistor, variable, 5,000 ohm $\pm$ 10%.
R57.	Resistor, variable, 1 megohm, $\pm$ 10%.
Q13, Q14.	Transistor, PNP.
R72.	Resistor, 2,320 ohm, $\pm$ 1%.
C1 through C9, C14.	Capacitor, 1 cov, 100 μ f., $\pm$ 2%.
CR1 through CR36, CR46 through CR56, CR59, CR60.	Diode, 250 mw., 40 v.
CR62, CR63 through CR65.	Diode, 250 mw., 40 v.
C16, C17, C20.	Capacitor, 25 volt., .01 μ f. $\pm$ 20%.
CR37 through CR45.	Diodes, matched dual-silicon.
Q1 through Q11.	Transistor, NPN, switching, 360 mw., 40 v.
Q110.	Transistor-NPN, 360 mw., 40 v.
R117.	Resistor, 12 ohm $\pm$ 2%.
R125, R126.	Resistor, 200 ohm, $\pm$ 2%.
R127, R131.	Resistor, 360 ohm $\pm$ 2%.
R132.	Resistor, 560 ohm $\pm$ 2%.
R120.	Resistor, 1.6K ohm $\pm$ 2%.
R121.	Resistor, 27K ohm $\pm$ 5%.
L1 through L9.	Delay line—4 μ H.
L10 through L13.	Delay line—1 μ H.
R114, R118, R130, R133.	Resistor, 2.0K ohm $\pm$ 5%.
R115.	Resistor, 3.0K ohm $\pm$ 5%.
C104.	Capacitor, 35 volt, 2.2 μ F $\pm$ 20%.
C105.	Capacitor, 35 volt, 22 μ F $\pm$ 20%.
R122.	Resistor, 360 ohm $\pm$ 2%.
R124.	Resistor, 750 ohm $\pm$ 2%.
R123.	Resistor, 16K ohm $\pm$ 2%.
R128.	Resistor, variable, 500 ohm, $\pm$ 10%.
Q108, Q109.	Transistor, NPN, 360 mw., 40 v.
C125.	Capacitor, 100 v., 4,700 pf. 20%.
Q106.	Transistor-PNP.
C116 through C119.	Capacitor, 100 volt, 25 μ F. $\pm$ 2%.
C106 through C115.	Capacitor, 100 v., 100 μ F., $\pm$ 2%.
CR104 through CR107.	Diode, 250 mw., 40 v.
Q107.	Transistor-PNP, power.
Q111, Q112.	Transistor, NPN, 360 mw., 40 V.
R119.	Resistor, 1.3K ohm $\pm$ 2%.
R129.	Resistor, 200 ohm, $\pm$ 5%.
R116.	Resistor, 300 ohm $\pm$ 5%.
Q105.	Transistor—NPN, 500 mw., 60 v.

SUMMARY

From the foregoing description of the detailed circuit diagram, and the discussion of the general circuit arrangement, it can be seen that an improved image intensity control circuit has been described for use with a cathode ray tube display system. The use of the transistor switching network allows a display control to provide appropriately positioned digital-data intensity-defining signals for establishing the predetermined programmable level of image intensity for any image that is being displayed. The image intensity can be programmably altered by shifting the digital-data intensity-defining signals prior to their application to the transistor switching network. The weighted resistor network then provides a current sum that is utilized by the high input-impedance amplifier and the automatically variable feedback network to provide a voltage level for driving the control amplifier in a manner to change the bias voltage on grid 1 of the cathode ray tube. The manual intensity control operates to provide controlled levels of intensity for the entire cathode ray tube.

Having then described a preferred embodiment of this invention, it being apparent that various modifications will become apparent to those skilled in the art without departing from the spirit and scope of the invention, what is intended to be protected by Letters Patent is set forth in the appended claims.

I claim:

1. An image intensity control circuit for use with a cathode ray tube display device comprising:
 - switching means for receiving programmably alterable digital-data image-intensity defining signals;
 - weighted resistor network means coupled to said switching means for providing current sums indicative of the intensity values of said digital-data image-intensity defining signals;
 - automatically variable impedance means coupled to said weighted resistor network means for providing voltage levels in response to said current sums; and
 - output means coupled to said automatically variable impedance means for providing bias voltages to a grid in a cathode ray tube in response to said voltage levels.
2. An image intensity control circuit as in claim 1 wherein said switching means includes a plurality of transistor-switch stages, each of said stages including a transistor having emitter, collector, and base electrodes, a pair of matched diodes having terminals coupled in opposed directions of current flow, one of said pair of matched diodes having another terminal coupled to said emitter electrode, and the other of said pair of matched diodes having another terminal for coupling to a first source of potential, said terminals coupled in common further coupled to load resistor means for coupling to a second source of potential, and resistor means coupled to said collector terminal for coupling to a variable source of potential.
3. An image intensity control circuit as in claim 2 and further including variable potential means coupled to said resistor means of each of said stages for establishing a desired level of intensity of images displayed.
4. An image intensity control circuit as in claim 3 wherein said variable potential means includes manually

operable control means for coupling to a third source of potential for providing manually selectable potential levels to said resistor means, thereby establishing said desired level of intensity.

5. In image intensity control circuit as in claim 1 and further including manual intensity control means for providing manually controlled levels of said bias voltages for controlling the intensity of images on said cathode ray tube in conjunction with said digital-data image-intensity defining signals.

6. An image intensity control circuit as in claim 1 and further including cathode control means for coupling to the cathode of said cathode ray tube for controlling the potential on said cathode, the potential on said cathode and said bias voltages determining the intensity of images on said cathode ray tube.

7. An image intensity control circuit as in claim 1 wherein said output means includes blanking means having input means for alternatively receiving blanking and unblanking signals, said blanking means including means for passing said bias voltage to said grid in response to said unblanking signal and for preventing said bias voltage from passing to said grid in response to said blanking signal.

8. An image intensity control circuit as in claim 7 wherein said blanking means includes signal delay means for synchronizing the application of said bias voltages to said grid with the operation of deflection circuits in the cathode ray tube display device.

9. An image intensity control circuit as in claim 1 wherein said weighted resistor network means includes n resistor means having resistive values for any i^{th} of said resistor means of $2^i R$, where R is a predetermined basic resistive value, n and i are integers, and each of said resistor means is associated with a predetermined one of digital-data image-intensity defining signals.

10. An image intensity control circuit as in claim 1 wherein said automatically variable impedance means includes a high input-impedance amplifier means having an output terminal and an input terminal coupled to said weighted resistor network means for receiving said current sums, reference means coupled to said high input-impedance amplifier means, and automatically variable feedback network means having a first input terminal for coupling to a source of regulated potential, a second input terminal coupled to said weighted resistor network means for receiving said current sums, and output means coupled to said output terminal, said automatically variable feedback network means providing differing levels of impedance in response to said current sums.

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