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(54) **METHODS OF FORMING DYNAMIC RANDOM ACCESS MEMORY TRENCH CAPACITORS**

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(60) Provisional application No. 60/311,801, filed on Aug. 13, 2001.

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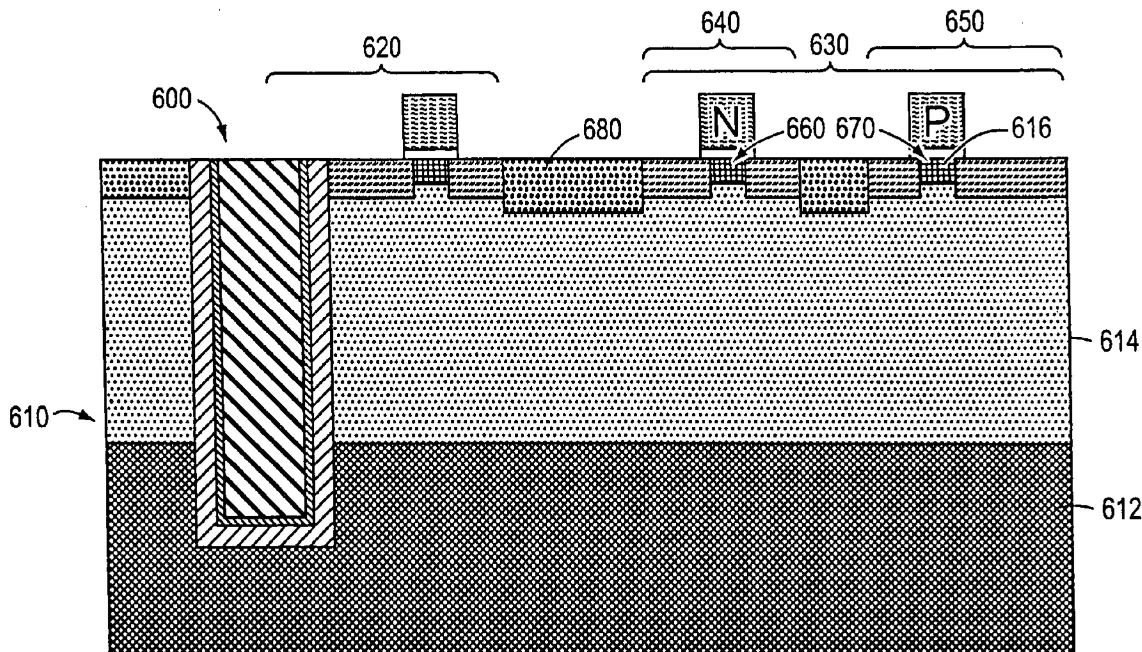
(57) **ABSTRACT**

DRAM trench capacitors formed by, inter alia, deposition of conductive material into a trench or doping the semiconductor region in which the trench is defined.



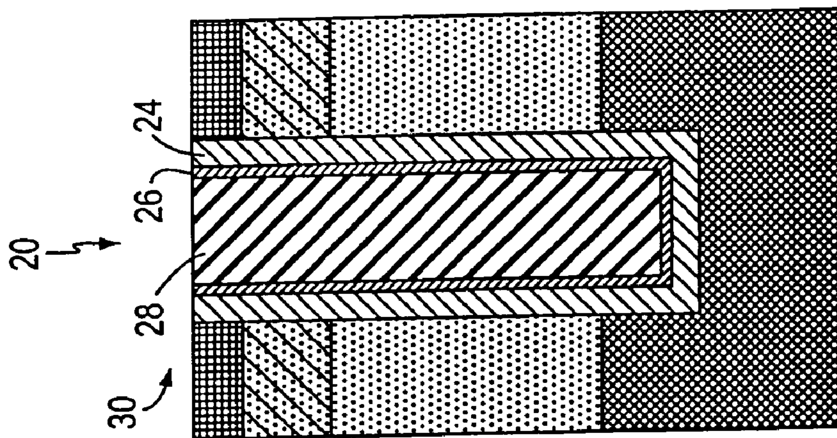


FIG. 1C

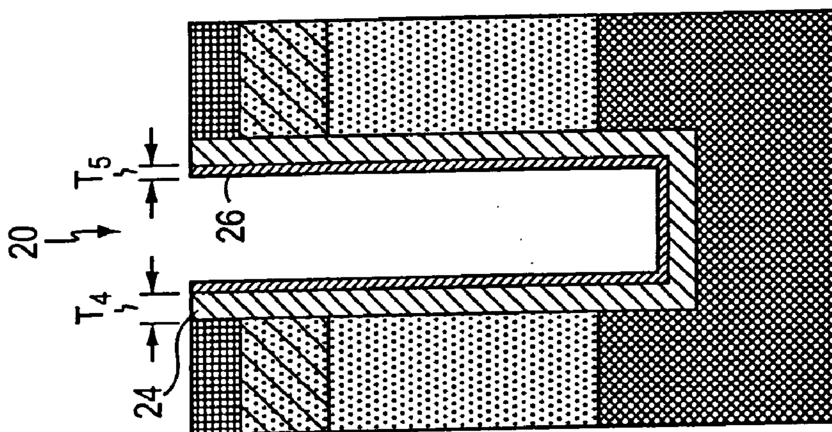


FIG. 1B

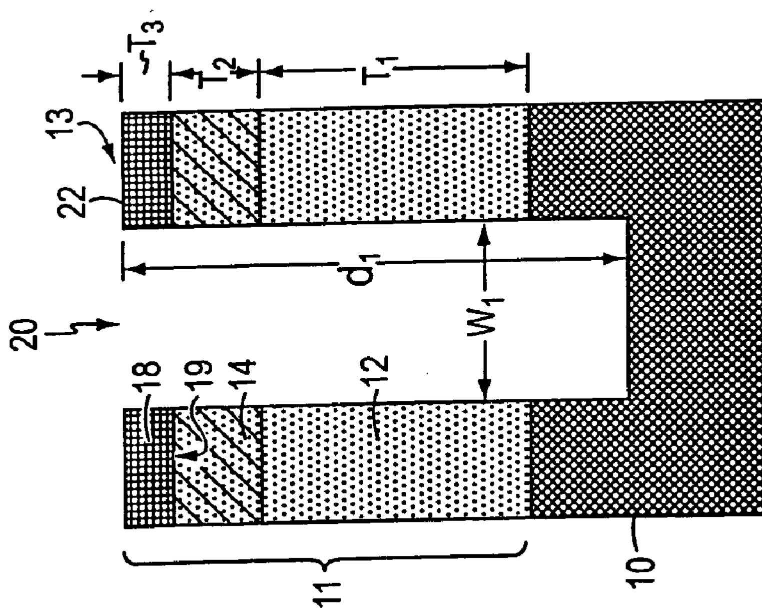


FIG. 1A

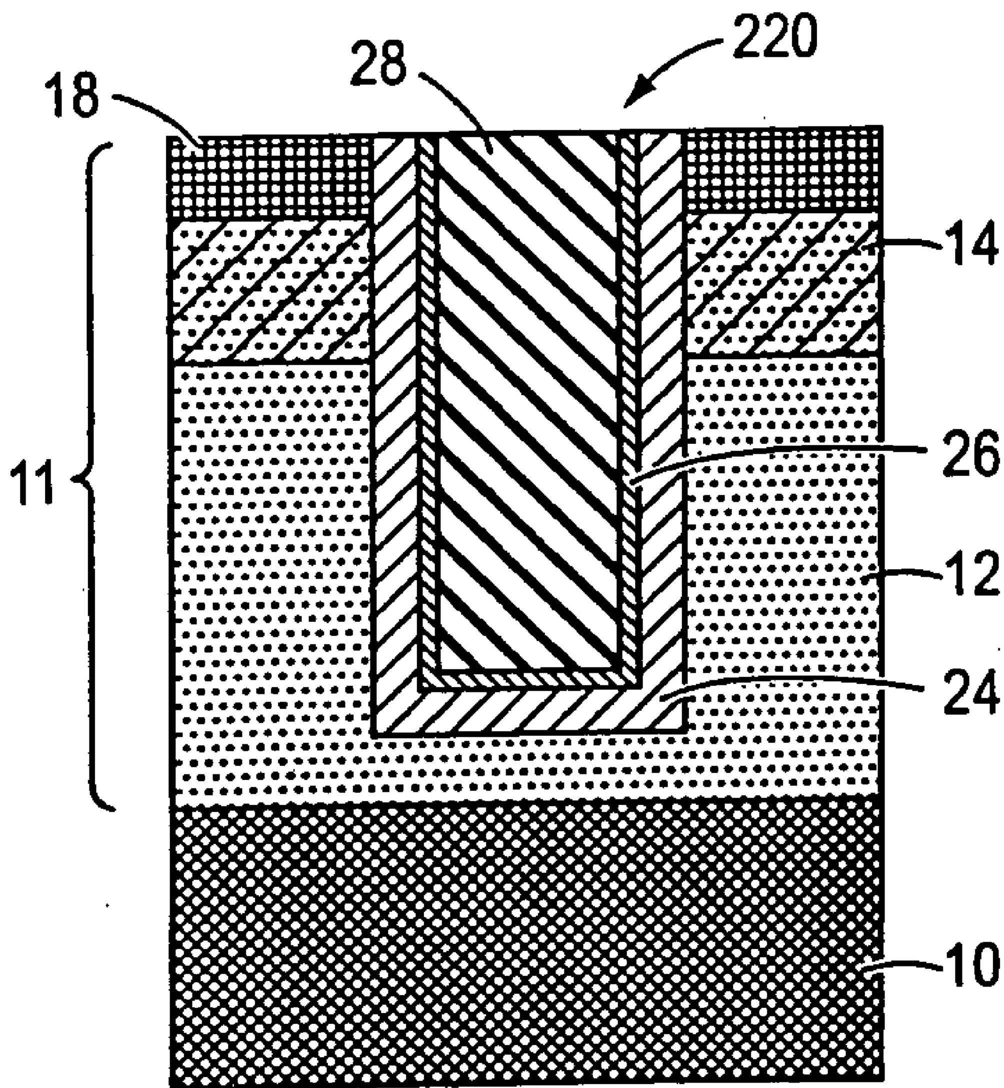


FIG. 2

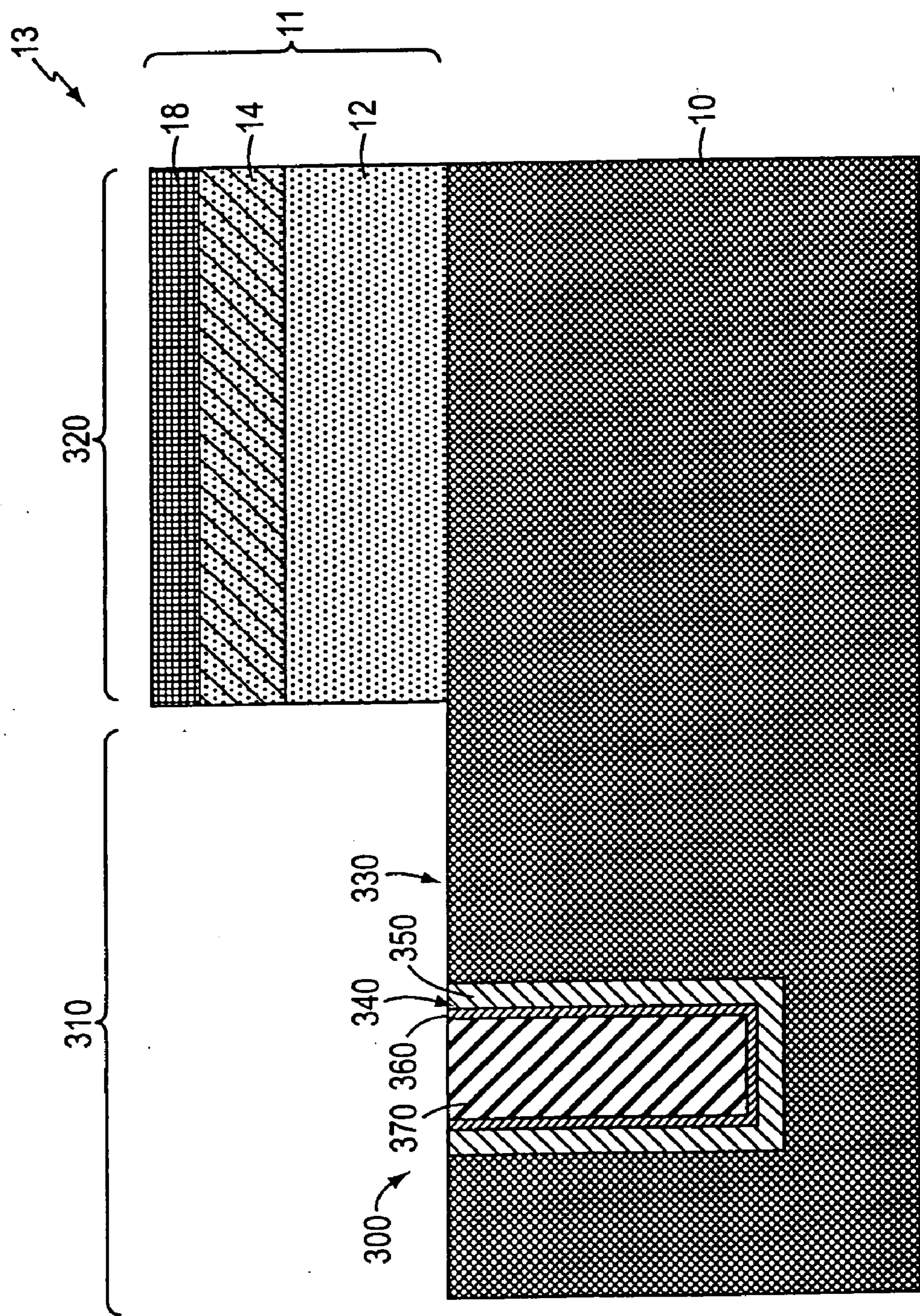


FIG. 3

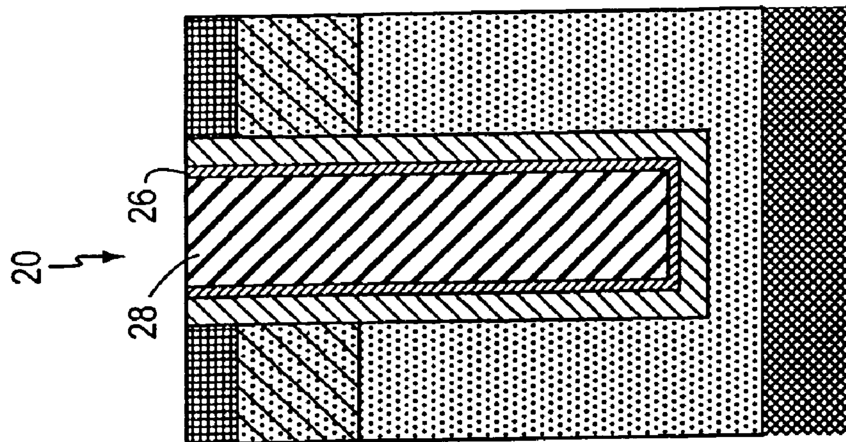


FIG. 4C

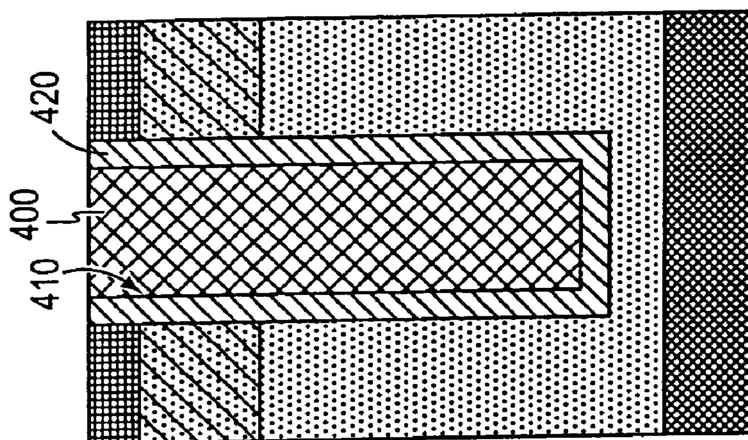


FIG. 4B

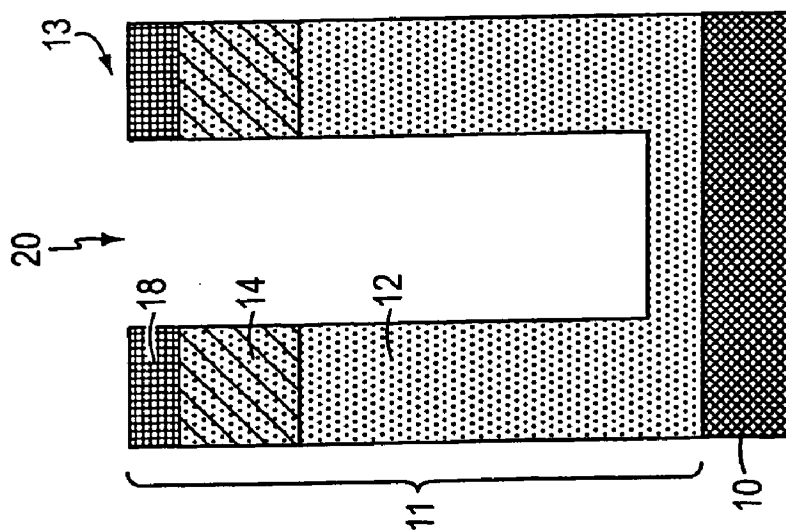


FIG. 4A

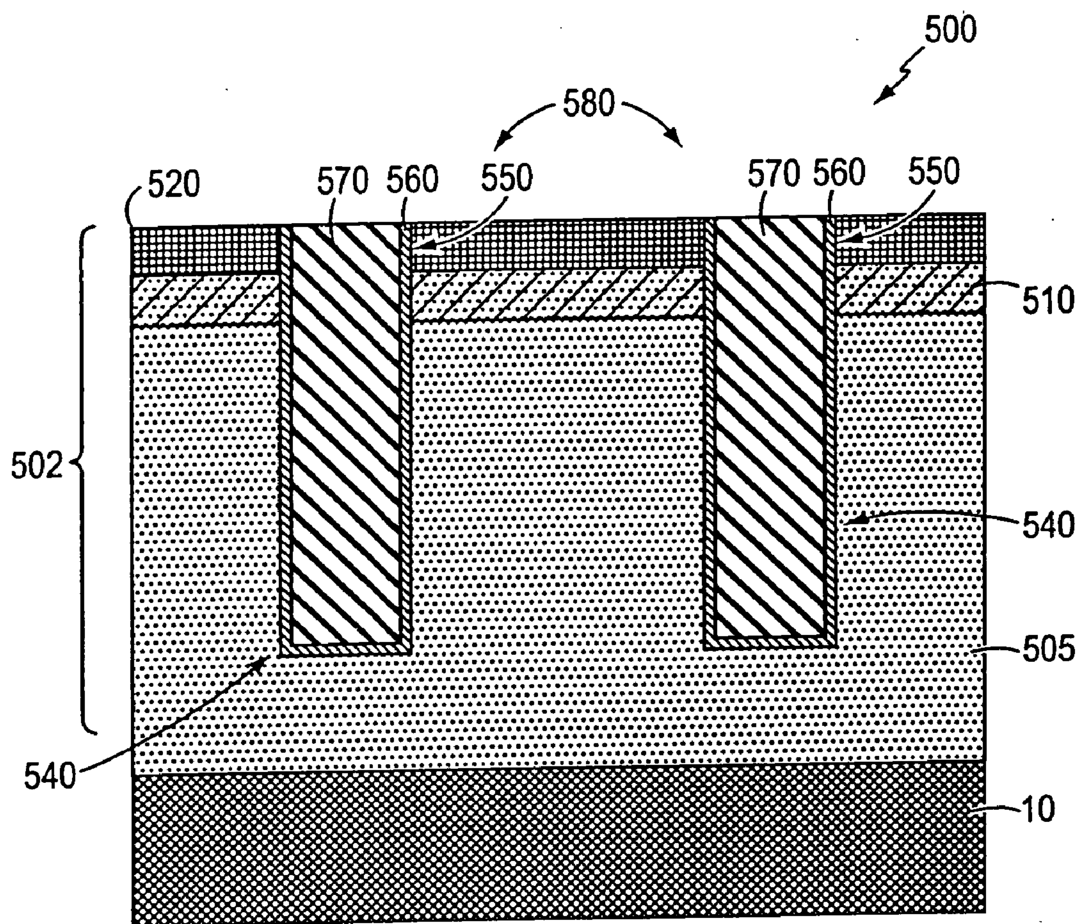


FIG. 5

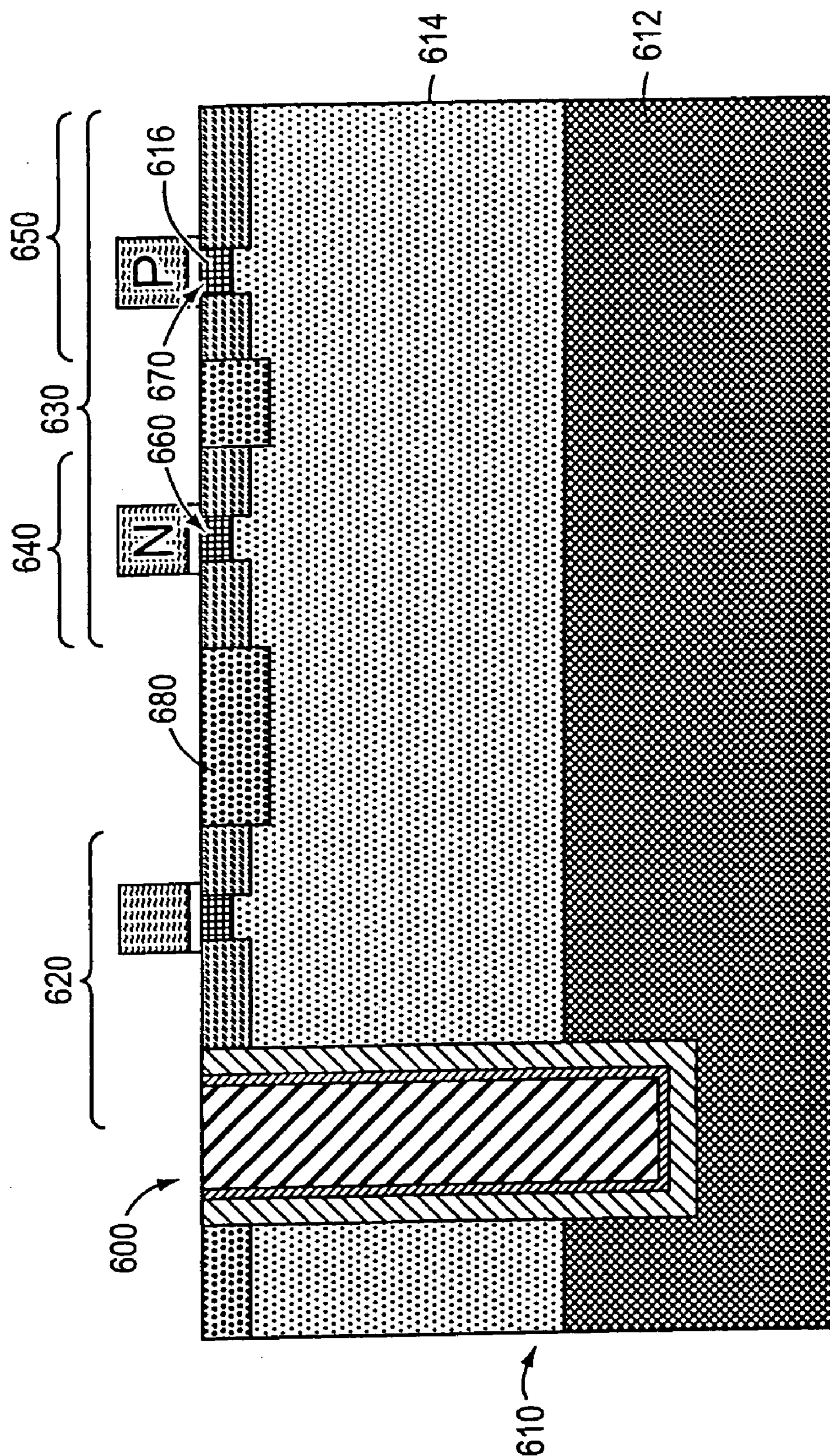


FIG. 6

METHODS OF FORMING DYNAMIC RANDOM ACCESS MEMORY TRENCH CAPACITORS

RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application 60/311,801 filed Aug. 13, 2001, the entire disclosure of which is hereby incorporated by reference.

FIELD OF THE INVENTION

[0002] This invention relates generally to semiconductor structures and particularly to semiconductor structures formed on strained semiconductor layers.

BACKGROUND

[0003] Relaxed silicon-germanium (SiGe) virtual substrates, including a tensilely strained layer and a relaxed underlying layer, enable the production of novel silicon (Si)-, germanium (Ge)-, and SiGe-based devices such as field-effect transistors (FETs). A "virtual substrate" includes a layer of SiGe that has been relaxed to its equilibrium lattice constant (i.e., one that is larger than that of Si). This relaxed SiGe layer can be directly applied to a Si substrate (e.g., by wafer bonding or direct epitaxy) or atop a graded SiGe layer, in which the lattice constant of the SiGe material has been increased gradually over the thickness of the layer. The SiGe virtual substrate can also incorporate buried insulating layers, in the manner of a silicon-on-insulator (SOI) wafer. In order to fabricate high-performance devices on these platforms, thin strained layers of Si, Ge, or SiGe are grown on the relaxed SiGe virtual substrates. The resulting biaxial tensile or compressive strain alters the carrier mobilities in the layers, enabling the fabrication of high-speed and/or low-power devices. Utilizing both strain and bandgap engineering, modulation-doped FETs (MODFETs) and metal-oxide-semiconductor FETs (MOSFETs) may be tailored for enhanced performance analog or digital applications. However, because these devices are fabricated on Si/SiGe virtual substrates rather than the Si substrates commonly utilized for complementary MOS (CMOS) technologies, they present new processing challenges.

[0004] One processing challenge to device fabrication on Si/SiGe virtual substrates is the definition of dynamic random access memory (DRAM) trench storage capacitors. DRAM storage capacitors require high quality insulating layers for storing charge. A conventional RAM trench storage capacitor formed on, for example, a p-type Si substrate may include an outer plate of, e.g., n-type doped Si substrate material (also referred to as the buried plate), a high-quality insulator grown on the outer plate, and an inner plate of, e.g., n-type doped polysilicon. Thus, two conducting plates are separated by an insulating plate. Traditionally, in DRAM trench capacitors fabricated in bulk Si substrates, the insulator is a thermally-grown silicon dioxide layer or nitrided silicon dioxide.

[0005] A conventional DRAM trench storage capacitor structure ordinarily is not suitable for fabrication on SiGe virtual substrates. The trench for this structure may be 5-10 micrometers (μm) deep, and would, therefore, extend into the relaxed SiGe layer. This layer may have many defects due to a high density of dislocations necessary to relax the strain in this layer. This high defect density, in turn, may interfere with subsequent efforts to create an insulator. In particular, thermal growth may be hampered by the defects and may result in a leaky insulator with many imperfections. Thus, the high defect density of the relaxed SiGe prevents the formation of the good-quality thermal dielectric incorporated in conventional DRAM trench capacitors. Furthermore, the nature of the insulator produced by thermal oxidation of SiGe is not well understood, so that even if the trench is etched in a defect-free SiGe region, in some applications, the thermal oxide may not be of sufficiently good quality for DRAM charge storage.

[0006] An additional challenge to the formation of DRAM trench capacitors in SiGe virtual substrates pertains to the formation of the outer plate. In conventional processes, the outer or buried plate is created for electrical isolation, either by implantation or by out-diffusion from a sacrificial dopant source deposited in the trench, prior to trench sidewall oxidation and inner-plate deposition. For either method of outer plate formation, the thermal steps used in conventional trench-capacitor processes for proper distribution of dopants may employ temperatures too high for use with Si/SiGe substrates.

[0007] Despite the inherent challenges, a DRAM trench capacitor is generally a better design choice for Si/SiGe substrates than, for example, stacked capacitor structures. First, the trench capacitor is more compatible with front-end CMOS device fabrication processes, because the alternative stacked capacitor is traditionally fabricated using chemical vapor deposition (CVD) processes at temperatures potentially high enough to degrade high-performance transistors. The trench capacitor is also more compatible with a back-end process involving many levels of metal interconnect, because it is inherently more planar than the stacked capacitor. These issues may be critical for applications which require CMOS performance on par with leading-edge microprocessors.

SUMMARY

[0008] In accordance with the present invention, DRAM trench capacitors are formed in substrates including materials other than Si, such as SiGe. These materials may be relaxed or strained, and may have dislocation defects. The challenges associated with forming a good quality thermal dielectric on trench sidewalls having many defects are addressed by forming an outer plate, an insulating layer, and an inner plate by deposition processes. In some embodiments, the quality of the deposited outer plate is sufficient for the thermal growth of the insulating layer. Alternatively, an outer plate may be formed in a trench sidewall by diffusion of dopants from a sacrificial source. Subsequently, an insulating layer may be thermally grown or deposited on the outer plate. In some other embodiments, the outer plate is formed by doping the substrate region proximate the trench, either prior to or after trench formation. This doping may be performed, for example, by an implantation process (e.g., ion implantation). Alternatively, substrate layers may be doped during epitaxial formation.

[0009] In one aspect, therefore, the invention features a method for forming a trench capacitor in a semiconductor substrate. A trench is defined extending into the semiconductor substrate from a top surface of the substrate. A first conductive material is deposited in the trench to define an outer plate, and an insulating layer is formed on the outer

plate. A second conductive material is deposited in the trench to define an inner plate.

[0010] One or more of the following features may also be included. The semiconductor substrate may include a layer containing germanium, with the trench extending into the germanium-containing layer. The step of forming the insulating layer may include deposition, such as chemical vapor deposition, or the insulating layer may be grown. The semiconductor substrate may include a tensilely strained layer disposed over a relaxed layer.

[0011] In another aspect, the invention features a method for forming a trench capacitor in a semiconductor substrate, in which the semiconductor substrate includes germanium. A trench is defined extending into the semiconductor substrate from a top surface of the substrate. A material including dopants is introduced into the trench. The dopants are diffused into a sidewall of the trench to define an outer plate. The material is removed from the trench, and an insulating layer is formed on the outer plate. A conductive material is deposited on the insulating layer to define an inner plate.

[0012] One or more of the following features may also be included. The material may be introduced into the trench by deposition. The material may include polysilicon. The step of removing the material comprises may include a wet etch. The step of forming the insulating layer may include thermal growth and/or deposition.

[0013] In another aspect of the invention, a method for forming a trench capacitor in a semiconductor substrate includes providing the semiconductor substrate, with the substrate having a layer containing germanium. Dopants are introduced into a region of the substrate. A trench is defined in the substrate region, with the trench extending into the germanium-containing layer and the region including the dopants defining an outer plate along a sidewall of the trench. An insulating layer is formed in the trench proximate the outer plate, and a conductive plate is deposited on the insulating layer to define an inner plate.

[0014] One or more of the following features may also be included. The step of forming the insulating layer may include deposition, or the insulating layer may be grown.

[0015] In another aspect of the invention, a semiconductor structure includes a trench capacitor, with the trench capacitor including a trench formed in a semiconductor substrate, the trench extending into a region of the substrate including germanium. A first conductive material is disposed in the trench, defining an outer plate. An insulating layer is disposed proximate the outer plate. A second conductive material is disposed in the trench proximate the insulating layer, the second conductive material defining an inner plate.

[0016] One or more of the following features may also be included. The semiconductor substrate may include a strained layer disposed over a relaxed layer. The relaxed layer may include germanium. The strained layer may include at least one of silicon, germanium, a group II element, a group III element, a group V element, and a group VI element. The strained layer may be tensilely strained and may include silicon.

[0017] The trench may be formed on a first region of the semiconductor substrate. The structure may also include a logic circuit disposed on a second region of the semiconductor substrate, the second region of the semiconductor substrate being electrically isolated from the first region, and the logic circuit including at least one transistor.

[0018] In another aspect of the invention, a semiconductor structure includes a trench capacitor, which itself includes a trench formed in a semiconductor substrate, the trench having an interior surface and extending into a region of the substrate. A first conductive material is deposited on the interior trench surface, defining an outer plate. An insulating layer is disposed proximate the outer plate, and a second conductive material may be disposed in the trench proximate the insulating layer, with the second conductive material defining an inner plate.

[0019] One or more of the following features may also be included. The trench may extend into a region of the substrate including germanium. The first conductive material may include polysilicon. The trench may be formed on a first region of the semiconductor substrate, and the structure may also include a logic circuit disposed on a second region of the semiconductor substrate, with the second region of the semiconductor substrate being electrically isolated from the first region, and the logic circuit including at least one transistor.

[0020] In another aspect, the invention features a semiconductor structure including a substrate having a first region substantially free of germanium and a second region having a layer including germanium. The structure also includes a trench capacitor disposed in the first region, the trench capacitor including an outer plate, an insulator disposed proximate the outer plate, and an inner plate disposed proximate the insulator.

[0021] One or more of the following features may be included. The second region may include a strained layer disposed over a relaxed layer. The relaxed layer may include germanium. The strained layer may include at least one of silicon, germanium, a group II element, a group III element, a group V element, and a group VI element.

[0022] In another aspect, the invention features a semiconductor structure including a trench capacitor, which itself includes a trench formed in a semiconductor substrate, the trench extending into a region of the substrate including germanium. A conductive trench sidewall has a conductivity imparted by dopants disposed therein and defining an outer plate. An insulating layer is disposed proximate the outer plate. A second conductive material is disposed in the trench proximate the insulating layer, with the second conductive material defining an inner plate.

[0023] One or more of the following features may also be included. The dopants may be diffused into the trench sidewall. The dopants may be implanted into the trench sidewall.

[0024] In another aspect, a semiconductor structure includes a trench capacitor, which itself includes a trench formed in a semiconductor substrate, with the trench extending into a region of the substrate including germanium and dopants. A conductive trench sidewall has a conductivity imparted by the dopants disposed in the region of the substrate and defining an outer plate. An insulating layer is disposed proximate the outer plate, and a second conductive material is disposed in the trench proximate the insulating layer, the second conductive material defining an inner plate.

[0025] One or more of the following features may also be included. The substrate may include a relaxed layer including germanium and dopants, and the trench may extend into the relaxed layer. The substrate may include a strained layer and the trench may extend into the strained layer.

BRIEF DESCRIPTION OF THE FIGURES

[0026] FIGS. **1**(*a*)-**1**(*c*) are a series of schematic cross-sectional views of a semiconductor substrate illustrating a process for fabricating a semiconductor structure on the substrate;

[0027] **FIG. 2** is a schematic cross-sectional view of a semiconductor structure formed on an alternative substrate;

[0028] **FIG. 3** is a schematic cross-sectional view of an alternative semiconductor structure;

[0029] FIGS. **4**(*a*)-**4**(*c*) are a series of schematic cross-sectional views of a semiconductor substrate illustrating an alternative process for fabricating a semiconductor structure on the substrate;

[0030] **FIG. 5** is a schematic cross-sectional view of a semiconductor substrate illustrating an alternative semiconductor structure; and

[0031] **FIG. 6** is a schematic cross-sectional view of a semiconductor substrate illustrating several semiconductor structures formed on the substrate.

DETAILED DESCRIPTION

[0032] The invention provides improved semiconductor structures, including improved DRAM trench capacitors. Various features of the invention are well suited to applications utilizing MOS devices that include, for example, Si, $Si_{1-x}Ge_x$ and/or Ge layers in and or on a substrate.

[0033] The term "MOS" is here used to refer generally to semiconductor devices that include a conductive gate spaced at least by an insulating layer from a semiconducting channel layer. The terms "SiGe" and "$Si_{1-x}Ge_x$" refer to silicon-germanium alloys.

[0034] Referring to FIGS. **1**(*a*)-**1**(*c*), a substrate **10** comprises a semiconductor, such as silicon. Several layers collectively indicated at **11** are formed on substrate **10**. Layers **11** may be grown, for example, in a CVD system, including atmospheric pressure CVD (APCVD) or low pressure CVD (LPCVD). Layers **11** and substrate **10** may be referred to together as "semiconductor substrate **13**."

[0035] Layers **11** include a graded layer **12** disposed over substrate **10**. Graded layer **12** may include SiGe with a grading rate of, for example, 10% Ge/μm of thickness, with a thickness T_1 of, for example, 2-9 μm, and grown, for example, at 600-1100° C. A relaxed layer **14** is disposed over graded layer **12**. Relaxed layer **14** may include, for example, $Si_{1-x}Ge_x$ with a uniform composition containing, for example, 20-90% Ge, (i.e., $0.2 \leqq x \leqq 0.9$) having a thickness T_2 of, e.g., 0.2-2 μm. In an alternative embodiment, relaxed layer **14** may be formed directly on substrate **10**, without graded layer **12**.

[0036] A tensilely strained layer **18** is disposed over relaxed layer **14**, sharing an interface **19** with relaxed layer **14**. In an embodiment, tensilely strained layer **18** is formed of silicon. In other embodiments, tensilely strained layer **18** may be formed of SiGe, or at least one of a group II, a group III element, a group V, and a group VI element. Tensilely strained layer **18** may have a starting thickness T_3 of, for example, 50-300 Å.

[0037] In some embodiments, a compressively strained layer (not shown) may be disposed between relaxed layer **14** and tensilely strained layer **18**. In an embodiment, the compressively strained layer includes $Si_{1-y}Ge_y$ with a Ge content (y) higher than the Ge content (x) of relaxed $Si_{1-x}Ge_x$ layer **14**. The compressively strained layer may contain, for example 40-100% Ge and have a thickness of, e.g., 10-200 angstroms (Å).

[0038] A trench **20** is defined in layers **11**, extending into semiconductor substrate **13** from a top surface **22** of semiconductor substrate **13**. Trench **20** may be defined by, e.g., reactive ion etching (RIE). Trench **20** may have an aspect ratio of 40:1, with a width w_1 of, e.g., 0.3 μm and a depth d_1 of, e.g., 12 μm. In the illustrated embodiment, trench **20** extends through layers **11** into substrate **10**.

[0039] Referring to **FIG. 1**(*b*), a first conductive material is deposited in trench **20** to define an outer plate **24**. First conductive material may be, for example, n-type doped polysilicon, having a thickness T_4 of, e.g., 100-500 Å. Outer plate **24** may be formed by deposition, such as by CVD or physical vapor deposition (PVD). Subsequently, an insulating layer **26** is formed on outer plate **24**. Insulating layer **26** may be a thermally-grown material, such as silicon dioxide or nitrided silicon dioxide. Alternatively, insulating layer **26** may be deposited by, for example, plasma enhanced CVD (PECVD), LPCVD, or APCVD. In an embodiment in which insulating layer **26** is deposited, the composition of the sidewall of trench **20**, e.g., outer plate **24**, may not affect the quality of insulating layer **26**. The deposited insulating material may be, for example, a material with a dielectric constant higher than that of silicon dioxide, such as tantalum oxide (Ta_2O_5) or silicon nitride (Si_3N_4). Insulating layer **26** may have a thickness T_5 of, e.g., 15-50 Å.

[0040] Referring to **FIG. 1**(*c*), a second conductive material is deposited in trench **20** proximate insulator **26** to define an inner plate **28**. Second conductive material may be, for example, n-doped polysilicon. A DRAM trench capacitor **30** includes outer plate **24**, insulator **26**, and inner plate **28**.

[0041] Referring to **FIG. 2**, in an alternative embodiment, layers **11**, i.e., tensilely strained layer **18**, relaxed layer **14**, and graded layer **12**, are sufficiently thick to completely accommodate a DRAM trench capacitor **220** including outer plate **24**, insulator **26**, and inner plate **28**. In this embodiment, insulator **26** may be thermally grown or deposited. Relaxed layer **14** has a low density of threading dislocations, but may be substantially free of misfit dislocations. Graded layer **12**, on the other hand, may have a high density of misfit dislocations. Misfit dislocations hinder the growth of good quality dielectrics on trench sidewalls, but threading dislocations have a minimal affect on thermal growth on sidewalls. Thermal growth of insulator **26** may be performed with adequate results, therefore, in some embodiments in which DRAM trench capacitor **220** is disposed primarily in relaxed layer **14**.

[0042] In some embodiments, a semiconductor substrate includes a region substantially free of Ge and another region including a layer containing Ge, with a DRAM trench

capacitor formed in the region substantially free of Ge. For example, referring to **FIG. 3**, a semiconductor substrate includes layers **11** disposed over silicon substrate **10**, with layers **11** including graded layer **12**, relaxed layer **14**, and tensilely strained layer **18**, as described with reference to **FIG. 1**(*a*). A DRAM trench capacitor **300** is formed in a first region **310** of semiconductor substrate **13**. A second region **320** of semiconductor substrate **13** is allocated for the formation of other electronic or opto-electronic semiconductor devices (not shown). Portions of layers **11** disposed in first region **310** are removed by, e.g., a wet etch, a dry etch, or a thermal oxidation followed by wet or dry etch of the resulting oxide, such as silicon-germanium oxide, to expose a top surface **330** of Si substrate **10**. DRAM trench capacitor **300** is formed by the etching of a trench **340** in Si substrate **10**, and doping the sidewalls of trench **340** with, for example, n-type dopants to define an outer plate **350** by either ion implantation or, as described below, out-diffusion from a sacrificial dopant source deposited in trench **340**. In the case of ion implantation, n-type ions, such as phosphorus or arsenic, may be implanted into trench **340**. Subsequently, an insulator **360** such as silicon dioxide or nitrided silicon dioxide is thermally grown on outer plate **350**, and an inner plate **370** of, e.g., n-type doped polysilicon is deposited. Semiconductor devices may be formed in region **320** prior or subsequent to DRAM trench capacitor **300** formation.

[**0043**] FIGS. **4**(*a*)-**4**(*c*) illustrate fabrication of the outer plate by introduction of a sacrificial doping source and out-diffusion. Referring to **FIG. 4**(*a*) as well as to **FIG. 1**(*a*), trench **20** is etched in semiconductor substrate **13**, with layers **11**, including graded layer **12**, relaxed layer **14**, and tensilely strained layer **18**, being sufficiently thick to accommodate all of trench **20**.

[**0044**] Referring to **FIG. 4**(*b*) as well as to **FIG. 4**(*a*), trench **20** is filled with a sacrificial dopant source **400** containing dopants of the desired type. Dopant source **400** may be, for example, phosphor-silicate glass (PSG) as an n-type dopant source or boron-silicate glass (BSG) as a p-type dopant source. Dopant source **400** may be, for example, deposited by CVD. After formation of dopant source **400**, a thermal anneal is performed to out-diffuse dopants from dopant source **400** into a sidewall **410** of trench **400** to define an outer plate **420**. In embodiments in which layers **11** contain Ge, this thermal anneal may be performed at a temperature lower than conventionally used in silicon processing because of the greater diffusivity of n-type carriers in germanium-containing layers. The anneal may be performed, for example, at 800-900° C. for 30 minutes.

[**0045**] Referring to **FIG. 4**(*c*) as well as to **FIG. 4**(*b*), dopant source **400** is removed by, for example, a wet etch such as a mixture of hydrofluoric acid and water. Subsequently, insulating layer **26** is formed on outer plate **420**. As discussed above with reference to **FIG. 1**(*b*), insulating layer **26** may be thermally-grown silicon dioxide or nitrided silicon dioxide. Alternatively, insulating layer **26** may be deposited by, for example, PECVD, LPCVD, or APCVD. The deposited insulating material may be, for example, a material with a dielectric constant higher than that of silicon dioxide, such as Ta_2O_5 or Si_3N_4.

[**0046**] A conductive material is deposited on insulating layer **26** to define inner plate **28**. The conductive material may be, for example, n-type doped polysilicon.

[**0047**] As shown in **FIG. 5**, portions of SiGe virtual substrate layers may be doped to define the outer plate of a DRAM trench capacitor. In this embodiment, a semiconductor substrate **500** includes a plurality of layers **502** disposed over substrate **10**. Layers **502** include a graded layer **505** disposed over substrate **10**. Graded layer **505** may be doped and may include SiGe with a grading rate of, for example, 10% Ge/μm of thickness. During epitaxial growth, graded layer **505** may be doped with n-type dopants, such as phosphorus or arsenic. In an alternative embodiment, graded layer **500** may be doped with p-type dopants such as boron or gallium. A relaxed layer **510**, disposed over doped graded layer **500**, may include, for example, $Si_{1-x}Ge_x$, that may be doped with the same type of dopants as are incorporated in graded layer **500**, i.e., n-type or p-type dopants. A tensilely strained layer **520** is disposed over relaxed layer **510**. In an embodiment, tensilely strained layer **520** is formed of silicon. In other embodiments, tensilely strained layer **520** may be formed of SiGe, or at least one of a group II, a group III, a group V, and a group VI element. The doped layer(s), e.g., at least one of tensilely strained layer **520**, relaxed layer **510**, and graded layer **505**, form an outer plate **540** for a subsequently formed DRAM trench capacitor (as discussed below).

[**0048**] A trench capacitor may be formed in a doped region, so that the doped region defines the outer plate of the trench capacitor. A trench **550** is formed by, e.g., RIE in tensilely strained layer **520**, relaxed layer **510**, and graded layer **505**. As illustrated, more than one trench **550** may be etched in semiconductor substrate **500**. In these embodiments, outer plate **540** does not line individual trenches, but is a larger region of high doping into which one or more trenches **550** may be etched. An insulating layer **560** is formed in trench **550** proximate outer plate **540**. Insulating layer **560** may be deposited, for example, by CVD. In some embodiments, insulating layer **560** may be grown by a thermal process. Insulating layer **560** may be formed of a dielectric like silicon dioxide or nitrided silicon dioxide. A conductive material is deposited on insulating layer **560** to define an inner plate **570**. The conductive material may be, for example, doped polysilicon deposited by CVD. DRAM trench capacitor **580** includes outer plate **540**, insulating layer **560**, and inner plate **570**.

[**0049**] In an alternative embodiment, dopants are introduced into layers **502** not during epitaxial growth, as described above, but by ion implantation. Here, dopants are selectively introduced into a portion of semiconductor substrate **500** in which trenches **550** are formed. The dopants may be introduced either before or after trench **550** formation. A post-implant anneal is generally performed to activate the dopants and to re-distribute the dopant concentration. In an embodiment, layers **502** contain SiGe, a material in which the diffusivity of n-type dopants is enhanced. Here, the anneal may be performed at a relatively low temperature, e.g., 800-900° C.

[**0050**] In an embodiment wherein it may not be practical to implant deeply enough to create a sufficiently thick outer plate **540**, a two-step implant may be utilized. Here, a deep implant may be followed by epitaxial growth, and then a second implant may be performed.

[**0051**] As shown in **FIG. 6**, trench capacitors formed in accordance with the present invention may be utilized in

conventional CMOS logic circuits. A DRAM trench capacitor **600** is formed on a semiconductor substrate **610** in accordance with any of the methods described above. Semiconductor substrate **610** includes a substrate **612** formed of, e.g., Si, and a layer **614** including, for example, graded and relaxed SiGe layers. A tensilely strained layer **616** is disposed over layer **614**. DRAM trench capacitor **600** is in electrical communication with access transistor **620**. A CMOS logic circuit **630** is also formed on semiconductor substrate **610**. CMOS logic circuit **630** may include an NMOS transistor **640** and a PMOS transistor **650**, with each transistor having a channel **660**, **670** disposed in tensilely strained layer **616**. CMOS logic circuit **630** is electrically isolated from DRAM trench capacitor **600** and access transistor **620** by an isolation region **680** formed from, for example, a dielectric material such as silicon dioxide.

[**0052**] In alternative embodiments, the trench capacitors described above may be formed in layers which are either all SiGe, or are various combinations of SiGe and Si. The SiGe layers may include graded SiGe, relaxed SiGe, and/or compressively strained SiGe.

[**0053**] The invention may be embodied in other specific forms without departing from the spirit of essential characteristics thereof. The foregoing embodiments are therefore to be considered in all respects illustrative rather than limiting on the invention described herein. Scope of the invention is thus indicated by the appended claims rather than by the foregoing description, and all changes which come within the meaning and range of equivalency of the claims are intended to be embraced therein.

1-37. (canceled)

38. A method for forming a semiconductor structure, the method comprising:

forming a trench capacitor, including the steps of:

defining a trench in a portion of a semiconductor substrate, the trench having an interior surface and extending into a region of the substrate substantially free of germanium,

introducing a first conductive material into the trench to define an outer plate,

forming an insulating layer on the outer plate, and

introducing a second conductive material into the trench to define an inner plate; and

forming a device on the substrate, the device comprising a strained channel.

39. The method of claim 38, wherein the strained channel comprises strained silicon.

40. The method of claim 38, wherein the strained channel is disposed proximate a material including SiGe.

41. The method of claim 38, wherein the device comprises a transistor.

42. The method of claim 41, wherein the transistor comprises an access transistor.

43. The method of claim 41, wherein the transistor comprises an NMOS transistor.

44. The method of claim 41, wherein the transistor comprises a PMOS transistor.

45. The method of claim 38, further comprising:

providing a strain-inducing material over the substrate, the strain-inducing material comprising silicon,

wherein strain in the strained channel is induced by the strain-inducing material.

46. The method of claim 45, wherein providing the strain-inducing material comprises deposition.

47. The method of claim 46, wherein deposition comprises chemical vapor deposition.

48. The method of claim 45, further comprising:

defining an isolation region proximate the strain-inducing material.

49. The method of claim 48, wherein the isolation region comprises silicon dioxide.

50. The method of claim 38, further comprising:

providing a strain-inducing material over the substrate, the strain-inducing material comprising germanium,

wherein strain in the strained channel is induced by the strain-inducing material.

51. The method of claim 50, wherein providing the strain-inducing material comprises deposition.

52. The method of claim 51, wherein deposition comprises chemical vapor deposition.

53. The method of claim 50, wherein the strain-inducing material is at least partially relaxed.

54. The method of claim 50, further comprising:

defining an isolation region proximate the strain-inducing material.

55. The method of claim 54, wherein the isolation region comprises silicon dioxide.

56. The method of claim 38, further comprising:

forming a second insulating layer, wherein the second insulating layer is disposed beneath the strained channel.

57. The method of claim 38, wherein the insulating layer comprises silicon dioxide.

58. The method of claim 38, wherein the insulating layer comprises nitrided silicon dioxide.

59. The method of claim 38, wherein the insulating layer comprises an insulating material having a dielectric constant higher than a dielectric constant of silicon dioxide.

60. The method of claim 59, wherein the insulating material comprises at least one of tantalum oxide and silicon nitride.

61. The method of claim 38, wherein the first conductive material comprises polysilicon.

62. The method of claim 38, wherein the second conductive material comprises polysilicon.

63. The method of claim 38, wherein the outer plate comprises a conductive trench sidewall.

64. The method of claim 63, wherein introducing the first conductive material into the trench to define an outer plate comprises defining the conductive trench sidewall by diffusing dopants into the trench sidewall.

65. The method of claim 64, further comprising:

at least partially filling the trench with a sacrificial dopant source prior to diffusion;

and at least partially removing the sacrificial dopant source from the trench after diffusion.

66. The method of claim 65, wherein the step of removing the dopant source comprises using a wet etch.

67. The method of claim 65, wherein the dopant source comprises at least one of boron-silicate glass and phosphor-silicate glass.

68. The method of claim 63, wherein introducing the first conductive material into the trench to define an outer plate comprises defining the conductive trench sidewall by implanting dopants into the trench sidewall.

69. The method of claim 63, wherein defining the outer plate comprises forming the conductive trench sidewall by introducing dopants into the semiconductor substrate portion before defining the trench.

70. The method of claim 38, wherein the strained channel is tensilely strained.

71. The method of claim 38, wherein the strained channel is compressively strained.

72. The method of claim 38, wherein the strained channel is proximate a material comprising strained SiGe.

73. The method of claim 38, wherein forming the insulating layer comprises deposition.

74. The method of claim 73, wherein deposition comprises chemical vapor deposition.

75. The method of claim 38, wherein forming the insulating layer comprises growing the insulating layer.

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