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[54] **REMOTE TIME CLOCK SYSTEM WITH STANDBY POWER MEANS**

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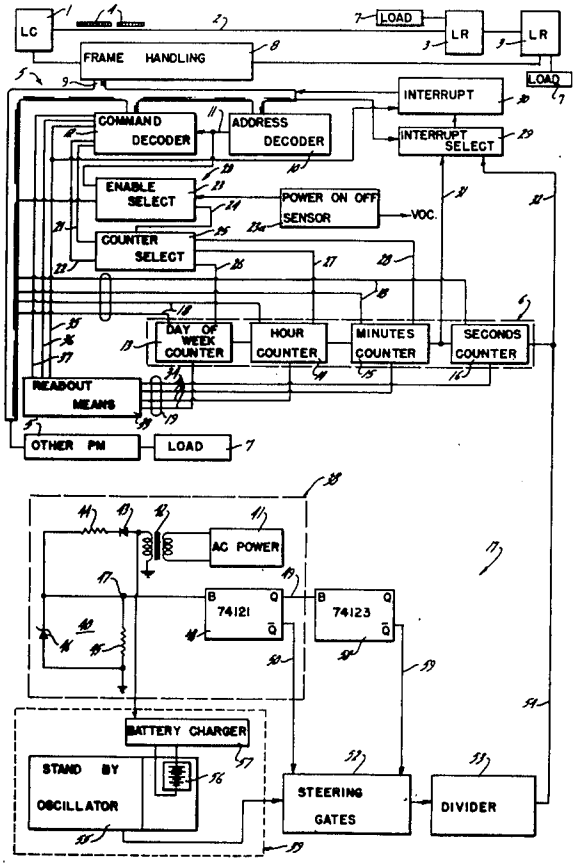
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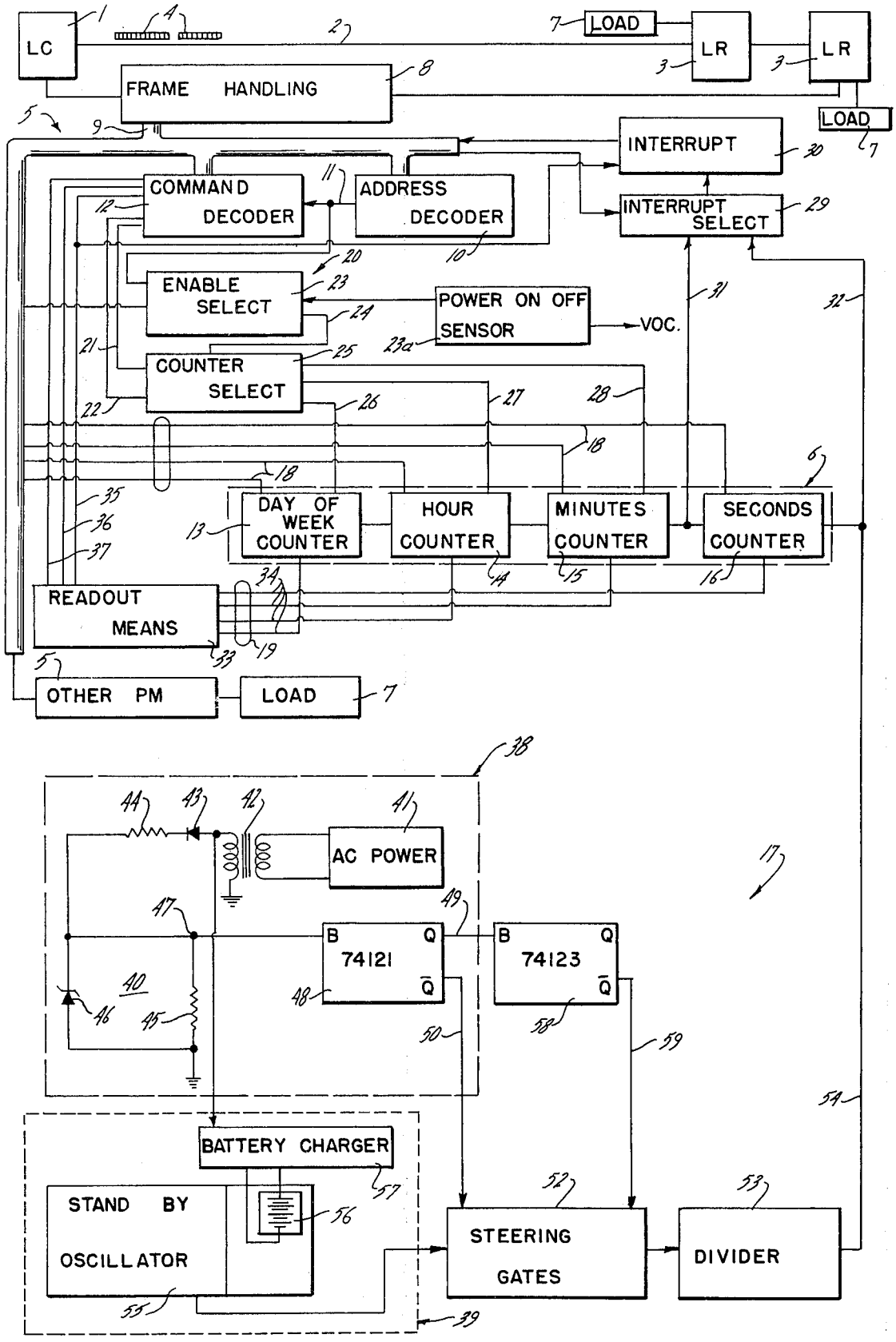
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[57] **ABSTRACT**

A remote time clock unit is connected as a part of one remote station of several in a data communication system having a controller to generate message frames for reading and resetting of the clock. The clock unit is a digital type having individual day, hour, minute and second counters, with binary coded decimal paralleled input and outputs connected for direct transfer of the input setting to the outputs. The clock outputs, through the loop controller, actuate time operated loads at loop remotes in response to programs at the loop controller. The clock unit is connected to the system by a module address decoder and a command decoder to read the message frames and provide for setting of the day, hour and minute counters. The clock unit is read by message frames with a pair of succeeding frames reading the three BCD bits for the day while simultaneously reading the hour data and the minutes or seconds data. The system is automatically updated each minute or second by an interrupt signal device connected to the input of the minute and second counters. The interrupt device normally connects the minute selection to control updating, but is connected to the system for response to a message frame signal to select the second interrupt interval.

5 Claims, 1 Drawing Figure




LC
1
4
2
7
LOAD
LR
3
LR
3
FRAME HANDLING
8
LOAD
7
5
9
INTERRUPT
30
COMMAND DECODER
12
11
ADDRESS DECODER
10
INTERRUPT SELECT
29
20
ENABLE SELECT
23
24
POWER ON OFF SENSOR
23a
VOC.
31
32
21
COUNTER SELECT
25
22
26
27
28
18
18
6
35
36
37
13
DAY OF WEEK COUNTER
HOUR COUNTER
MINUTES COUNTER
SECONDS COUNTER
14
15
16
34
READOUT MEANS
33
19
5
OTHER PM
LOAD
7
38
44
43
42
41
AC POWER
17
47
49
B
Q
74121
Q̄
B
Q
74123
Q̄
40
46
45
48
50
58
59
54
BATTERY CHARGER
57
STAND BY OSCILLATOR
56
55
52
STEERING GATES
53
DIVIDER
39

REMOTE TIME CLOCK SYSTEM WITH STANDBY POWER MEANS

This is a division of application, Ser No. **315,568,** filed Dec. **15, 1972** which is now U.S. Pat. No. **3,861,134.**

BACKGROUND OF THE INVENTION

This invention relates to a remotely controlled time clock having standby power means and in particular to such a time clock forming a part of a remote control system.

In automated control systems, various functions are to be completed in accordance with a predetermined real time program. For example, in automated environmental control systems a real time clock may be employed to provide automatic activation of certain equipment, read-outs, and displays with respect to the system at a particular time of day on a particular day within any given week. In local systems, the time clock is readily hard-wired directly into the processing and control unit. The clock is manually resettable and directly driven from a power supply system forming a part of a total public utility power system. Standby power operations are normally provided through a battery controlled system or the like. However, the basic clock system is normally constructed without specific consideration of the power drawn and the battery supplies will only control it for a relatively short period of time.

Further, the timing signals are normally obtained from a suitable crystal oscillator which inherently may result in an accumulated error which limits the applicability of the clock in primary-secondary related time systems.

In control systems having remotely located activated devices, the real time clock at the remote station should be reliably driven from a standby supply and the system should provide for remote checking and updating of the clock to insure proper timed operation of the various pieces of hardware and coupling means in accordance with a predetermined time programming pattern.

Thus, the copending application of Buchanan et al entitled DATA COMMUNICATION SYSTEM EMPLOYING A SERIES LOOP, which was filed on the same day as this application and which is assigned to the same assignee, disclosed a loop control system employing actuated control stations and a plurality of remote stations. A serial data loop connects the stations by loop communication therebetween to permit the central station to not only control the hardware at the remote stations but to receive information regarding the functioning of such hardware. Digitally information in binary code form is transmitted to and from the remote stations under the control of a loop controller at the central station, with the data information carried in discrete multiple bit frames. Each frame includes a plurality of bytes related successively to a remote station address, point module address, command and data information, in multiple bit form.

SUMMARY OF INVENTION

The present invention is particularly directed to a remote time clock means which can be coupled into a communication or processing system such as in the Buchanan et al application without being directly wired thereto and which permits the automatic remote resetting and readout.

Generally in accordance with the present invention, the time clock means which is preferably a digital type which includes separate time units or elements for recording the several divisions of time; for example, the day, the hour, the minute and the second of real time. The clock elements are connected to to form an interrelated time unit connected to a processing point module having a common coded address for remote communication to a central controller station or means. The module is provided with a unique interlock means including a command decoding means responsive to a command section of a message frame permitting selective transfer of information to set the clock means and also to read the clock means for control station verification and the like. The several time elements of a digital clock are perferably provided with paralleled preset input and paralleled outputs which are in binary coded decimals (BCD) and which are directly transferable from the inputs to outputs. With the appropriate strobing signals received from the message frames and the like, the information is transferred through the counters to their outputs without the rapid pulse and compare technique normally encountered in many systems. Consequently, there is no need to terminate the clock operation for other than a relatively brief period during which the information is strobed through the clock and into the clock's counters or the like. The paralleled circuitry also minimizes the required interconnecting circuitry.

The novel apparatus also preferably includes a second's interrupt and a minute's interrupt to provide for updating the system at selected intervals. The information is fed into the clock from successive frame elements by individual introduction of the time information for the several time units.

In accordance with one aspect of this invention, only the unit of time set is the minutes counter. The information is read out of the time clock by reading of all of the several time units or counters.

The command section or byte of a first message frame is employed to initiate the setting of information from the data byte into the properly addressed time clock module, with the day set by the initiating frame and with subsequent write frames providing for the writing of the minutes and the hours into the clock. The data byte also includes information as to whether a minute or second interrupt updating is to be established. The command decoding means further provides for the reading of the day, hour, minutes and seconds by three successive frames, with the first frame receiving the first digit of the day information and the 7 hour bits, the second frame providing for final introduction of the last two day bits required for the day address and the reading for the minutes or seconds information. The final frame receives the seconds or minutes, depending upon the decoding of its command section or byte. A readout can be taken in any sequence or order.

The time clock may derive power principally from line power. An auxiliary novel standby power system with minimum power consumption, particularly in standby conditions, is preferably provided for maintaining operation in response to a main power failure.

The real time clock is, in accordance with a particularly novel construction, a solid state counter having the input connected to be driven from a suitable alter-

nating current power supply, such as a conventional 60 Hz or 50 Hz public utility system. A line-powered synchronization circuit includes a triggered circuit means which maintains a continuous source of clock pulses for normal operation which are connected directly to the seconds or lowest-reading unit of the clock through a suitable dividing network to generate the appropriate clock signal for the counter. The circuit preferably includes a rectifier and voltage limiter connecting a power line transformer to drive a suitable one-type circuit, the output of which is connected to generate the clock signal. An auxiliary battery-operated power and oscillator is provided for replacing of the line-powered synchronizing circuit. The standby power system preferably includes a battery drive having a charging circuit connected to the incoming line circuit to provide continuous charging during normal operation. The output of the standby oscillator is coupled to a steering or switching network to provide an alternate source of clock signals to the dividing network. The switching network may advantageously employ solid state gates. The normal synchronizing pulses are also connected through a timing means such as a retriggerable one-shot to control the gates after a selected time period. The second timing device remains active for a relatively long period when compared with that of the first device. Thus, as long as the first trigger means continuously generates the necessary clock signals, the second timing means will be held in the normal standby position. If power fails, the first timing means will not generate the required timing signals. The second timing means, which has a longer time period, however, will sense the power failure and generate a logic signal to the steering gates and automatically actuate the gates to connect the clock circuit to the standby oscillator. The system will thus respond with the auxiliary circuit replacing the normal clock synchronizing pulses in such that no more than two timing pulses will be missed by the clock in response to such power failure.

The time clock and particularly the standby circuitry is designed to use the integrated circuitry such as that conventionally identified as C/MOS or COS-MOS type to reduce the power consumption, particularly in the standby operating mode. The standby oscillator is selected to operate continuously, but the output or loading thereof is only in response to main power failure. Thus, the load requirements on the system are minimized and the total design of the system minimizes the power requirements.

The present invention thus provides an improved digital type clock which is particularly adapted for remote control systems such as the serial data loop control and monitoring system previously discussed wherein all communication is through a common communication cable which minimizes the wiring of the system while maintaining a highly flexible and rapidly responding clock unit. Further, the clock can be built as an integrated circuit module for direct addition to any properly terminated communication network.

BRIEF DESCRIPTION OF DRAWING

The drawing furnished herewith illustrated a preferred consturction of the present invention in which the above advantages and features are clearly disclosed as well as others which will be readily understood from the subsequent description of such illustrated embodiment.

The drawing furnished herewith is a diagrammatic illustration of a real time clock constructed in accordance with the present invention and interconnected into a loop communication system for remote control.

DESCRIPTION OF ILLUSTRATED EMBODIMENT

Referring to the drawing and particularly to FIG. 1, the present invention is shown applied to a data communication loop system employing a central loop controller 1 serially coupled by a loop communication cable 2 to a plurality of remote stations 3, generally as more fully disclosed in the previously referred to Buchanan et al. application. The central controller 1 generates a series of message frames 4, each of which includes a plurality of digital logic bits. The message frames 4 are circulated in serial fashion throughout the loop to establish communication with the several remote stations 3 in a selected manner. Each of the remote stations 3 controls various load means for producing various controlling and monitoring functions. Thus, a heating, ventillating and air-conditioning system for a building or complex of buildings may include various contact and drive means for controlling the operating means as well as sensing devices for monitoring the conditions and system operation. Some of the load means may be operated at a predetermined time during the week and day under control of a time program at the loop controller. The several remote staions 3 are each arranged to control and monitor selected operating groups, which are further divided at each station into related functional groups. The groups are defined as point modules 5 which are selectively activated by the message frame, as more fully disclosed in the Buchanan et al application. The present invention is particularly related to the reading and setting of a real time clock unit 6 which is interconnected at a point module 5 at a remote station 3 for automatic activation of time program functions, operator display and the like. The time clock unit 6, by means of its time point module 5, converses with the loop controller 1 to actuate load means 7 at selected times at the various loop remotes 3. In a remote time clock system, the clock unit 6 should be periodically checked by readout of the setting and reset to update the setting and ensure continued proper programming of the load means.

The remote station 3, which includes a time clock unit 6 and its assorted time point modules, is shown in detail for purposes of clearly describing the embodiment of the present invention. All remote stations 3 may include time actuated loads 7, and the same time clock may be employed for load control in several loops.

The last remote station 3 connected to receive the frame 4 and return it to the loop controller 1 is shown and includes a frame logic handling means 8 which is connected via a common bus 9 to point modules 5 for selectively activating one of the modules for receiving and processing the particular message frame 4. Each point module 5 is generally constructed with an address decoder 10 which produces a point enable signal at its output line 11 and a command decoder 12. The decoders 10 and 12 are connected to bus 9, as shown, to receive binary coded logic messages.

The, the central controller 1 generates the message frames 4 in the time spaced sequence. The frames 4 are divided into a plurality of coded bytes each having multiple bits as disclosed in the Buchanan et al application

and particularly including a station address byte, a point module address byte as well as command and status check bytes and a final function or data byte. The frame handling means **8** will detect the initial byte of the message frame **4** and, if appropriate, couples the message frame to the appropriate point modules **10 – 12,** for processing of each bit of the message. The associated point module hardware is activated in accordance with the multiple bit instructions or command of the message frame **4,** which is decoded by the command decoder **12.** The decoders **10** and **12** may be of any suitable construction. As applied to the system described, a satisfactory construction is shown in the copending application of L. J. Strojny entitled "REMOTE CODED DUAL STATE CONTROLLER APPARATUS" which was filed on the same day as this application and is assigned to the same assignee.

Generally, the time point module **5,** in the illustrated embodiment of this invention, includes a plurality of counters **13 – 16,** defining the time clock **6,** one counter for each of the time units employed. The clock counters **13 – 16** are interconnected through the time point module **5** to loop controller **1** to effect the desired control of the associated load means **7** in accordance with a preprogrammed programmer at the loop controller transferring the clock output to the load means over loop **2.**

In the illustrated embodiment of the invention the time clock is shown including a day counter **13,** an hour counter **14,** a minute counter **15** and a second counter **16.** The clock is driven from a special pulse-generating unit **17** which is connected to the second counter **16,** with counters **13 – 16** interconnected in the usual decimal divider chain which transfers pulses automatically to establish the minutes, hour and day as a continuous real time record.

The individual counters are shown as directly presettable units having parallel preset inputs **18** which permit the selective updating of the clock time with the input signals directly appearing on the outputs **34** as a result of the direct preset construction. Both the input and the output are preferably coded in binary-coded-decimal form, hereinafter abbreviated "BCD," and are in bit parallel form to permit the direct interfacing and readout.

The day counter **13** maintains the day based on recycling for each week. Thus, the day counter must record decimal digits of from zero through six for the week. This requires a three-bit wide input **18** and a corresponding three-bit wide output **19** in order to indicate a given day in binary coded decimals. The hour counter **14,** which counts through **24** hours, correspondingly must have a minimum of six-bit wide inputs and outputs, two bits of which are necessary to record the most significant position or number of zero through two. The minute and the second counters **15** and **16** similarly require seven binary bit wide inputs and outputs, four of which indicate the least significant position number of zero through nine and three of which are required for the most significant position of zero through six in decimal form.

The binary data information is read into and from a message frame **4** through the fourth data byte of the message frame which includes eight data bits. As presently described, three frames **4** are required for each setting or complete reading of the time clock **6.**

To set the clock, three message frames **4** are received in a selected sequence to preset the day, hour and minutes, counters **13 – 15** and to reset the seconds counter **16** to zero.

The directly resettable counters **13 – 16** are selectively updated by such message frames **4** carrying the corresponding data in the final data byte. The transfer of the data from the message frame **4** to the appropriate counter **13 – 15** is controlled by a logic circuit **20** which is driven from the command decoder **12.**

The command decoder **12** establishes five outputs, and includes an initiate line **21** and a write line **22** employed to control setting of the clock counters, via the logic circuit **20.** Logic circuit **20** includes a set enable logic gate **23** having inputs connected to the bus **9,** decoder enable line **11** and the initiate line **21,** and a logic power on/off sense circuit **23***a*. If the coded information is, therefore, available and properly processed and if the logic power on/off sense circuit **23***a*, which functions to inhibit the possibility of presetting or resetting the clock **6** during periods of power turn-on/turn-off of circuit **20,** has determined that logic power is completely applied to circuit **20,** then the gate **23** produces an output at line **24** which is connected to enable a select logic unit **25** which has a set day counter output line **26,** a set hour counter output line **27,** and a set minute counter output line **28.** The logic unit **25** is a sequencing or counting unit which responds to the signal at the initiate line **21** to set line **26** and step the unit to next activate line **28.** The logic unit **25** is also connected to line **22** which is operable to activate line **28** and step the unit to next activate line **27.** The three message frames **4** must, therefore, be received in proper sequence from loop controller **1** to properly set the clock unit **6.**

A program format for the three message frames **4** in the assumed four byte message frame would be as follows:

1. Station address, module address, initiate code (**1111**), data byte $D2^2$ $D2^1$ $D2^0$ X X X X S day.
2. Station address, module address, write code (**0010**), data byte X $2_{10}{}^2$ $2_{10}{}^1$ $2_{10}{}^0$ $2_1{}^3$ $2_1{}^2$ $2_1{}^1$ $2_1{}^0$ minutes.
3. Station address, module address, write code (**0010**), data byte X X $2_{10}{}^1$ $2_{10}{}^0$ $2_1{}^3$ $2_1{}^2$ $2_1{}^0$ hours in 24 hours form.

Where numeric data is in BCD, X denotes unused bit, and S = **1** selects the seconds interrupt.

The first message frame **4,** as all message frames for the clock unit **6,** must include the proper remote station address and the point module address. The first setting message frame **4** would also include an initiate command code which, for example, might be all logic ones applied to a command decoder **12** and establish an appropriate output at the initiate line **21** which with the point enable signal line would permit insertion of data information into the clock counter **13.** The data byte of frame **4** will then, in the first three bit positions, include the day in binary-coded-decimal form. Thus, if it is the first day of the week, the three bit would be set in logic **000.** The four next bits of the byte in this first frame are not employed, whereas the final bit in the binary unit is employed to preselect the minute or the seconds interrupt.

The latter bit is interconnected to an interrupt logic control **29** to control the read periods as hereinafter described.

The next message frame which will be transmitted by the loop controller upon return of the above frame and analyzed by the loop controller similarly includes the remote station and point module addresses followed by a write code command in the next byte. The data byte now includes the minute data information for introduction into the minute counter. As previously described, a seven bit side input is required for the hours and likewise for the minutes. The first bit may, therefore, be a data blank, whereas the next seven bits are employed to encode the appropriate hour or minute, as the case may be. All initiate and write frames reset the seconds counter to zero. Thus, the initial active three bits after bit zero are encoded with the most significant number in binary-coded-decimal form and the last four data bits are encoded with respect to the information with respect to the least significant position to read up to **59** and at **60** changes to the hour. This frame message sets the hour and minute counters and is retransmitted in acknowledged form to the loop controller **1**, verified and a third frame is then transmitted.

The third frame which is received includes the hours in **24** hour form, with the information carried by the last six data bits.

The input order is followed completely through for each clock setting, to maintain days, minutes and hours in proper sequence. The same write command is employed and requires that the above order be established and completely followed through. After the third setting frame has been received and processed at the point module, the frame is returned as an acknowledged frame.

The outputs of the several counters **13 – 16** are periodically read, and in the illustrated embodiments at either minute or second intervals.

The clock **6** is provided in the illustrated construction with means to selectively cause controller **1** to read the time at intervals of either minutes or seconds. The clock module **5** has an interrupt or message frame request unit **30** which is coupled to the inputs of the counters **15** and **16** via the interrupt select logic gate **29.** Thus, a minutes interrupt signal line **31** is connected between the minutes and seconds counters **15** and **16** and a seconds interrupt line **32** is similarly connected to the input of the seconds counter **16.** The minute interrupt signal at either line **31** is coupled to the frame handling logic means **8** via the interrupt unit **30** to request an available frame, unless a previous setting message frame has specifically included a "seconds" interrupt command in the final byte as noted above. The interrupt signal is thus continuously and periodically generated to maintain information transfer to controller **1.** When an available frame is received, it is processed by the clock modules **5,** properly filled and transmitted to the loop controller **1** to indicate the pending request for transfer of information to the controller **1.** An output reader multiplex unit **33** has input lines **34** connected to the output of the counters **13** for coupling of the data to the bus **9** and thus for selective connection into a message frame **4,** under the control of the output and command decoder **12.**

The decoder **12** is operable to selectively activate three read lines **35, 36** and **37** which provide for sequentially filling of three frames **4** and particularly transferring of the clock output for processing by controller **1.**

In order to read the output of all four counters **13 – 16** with only three message frames **4,** the day bits are divided and carried by two sequential frames **4.** A satisfactory format for the assumed **36** multiple bit message frame is:

1. Station address, module address, Read X code (**0001**), data byte $D2^0\ 2_{10}{}^2\ 2_{10}{}^1\ 2_{10}{}^0\ 2_1{}^3\ 2_1{}^2\ 2_1{}^1\ 2_1{}^0$ day bits and minutes data.
2. Station address, module address, Read Y code (**1001**), data byte $D2^2\ D2^1\ 2_{10}{}^1\ 2_{10}{}^0\ 2_1{}^3\ 2_1{}^2\ 2_1{}^1\ 2_1{}^0$ day bits and hour data.
3. Station address, module address, Read Z (**1011**), data byte $X\ 2_{10}{}^2\ 2_{10}{}^1\ 2_{10}{}^0\ 2_1{}^3\ 2_1{}^2\ 2_1{}^1\ 2_1{}^0$ seconds.

In accordance with a preferred format, the first message frame **4** includes a read command which enables the first read line **35.** This line activates the day and minute counter section of readout **33** to transfer day and hour data which includes the least significant binary bit for the day in the zero or first data byte and the total minute data in the subsequent seven data bits. The subsequent frame includes an hour read code such as **1001** which activates line **36** and the readout **33** couples the output of counters **13** and **14,** with the data byte received in the first two bit positions the next two binary bit logic signals for completing the day information and the final six bits including the total hour data. Finally, the third frame **4** which is similarly addressed is provided with a seconds read code such as **1011** which enables the third read line **37.** The first or zero bit of the fourth message frame byte is not employed, and only the final seven bits are employed to receive and encode the total data setting of the seconds counter **16.**

In response to a reading either at second or the minute interval, the interrupt signal is operative to fill the available frame **4** with the point module address, the code for activating the first read line **35** and the minute data of the minute counter **15.** The information is continuously inserted into sequential available frames **4** until the loop controller **1** generates a read command which activates read line **35.** The read line **35** is thus also connected to clear the interrupt unit **30.**

Thus, the digital clock provides a continuous timed control of the load means **7.** The second and minute interrupt signals are derived for automatic time updating into the system to thereby ensure accurate control of the load. Thus, if the controller **1** detects a need to update the clock, it automatically transmits the necessary preset message frames **4,** as previously discussed.

With the binary-coded-decimal bit parallel transfer, the information is transferred through the counters **13 – 16** directly to their output without the rapid pulse and compare techniques which have been widely employed. This minimizes the down time of the clock operation. The coded system also minimizes the overall circuitry and associated wiring. This is important where a significant number of remote stations **3** are provided with timed loads requiring real time clock actuation with means to ensure the accurate timed actuation of the loads.

In many applications, it is extremely important that the clock operate properly and continuously to supply the necessary timed control information to the loads **7.** Consequently, the clock units are normally provided with a main power system drive and an auxiliary self-powered standby system drive. A particularly novel main drive **38** and auxiliary drive **39** is shown in the

preferred embodiment and constitute a significant and novel feature of this invention.

Generally, a main drive system **38** includes a coupling circuit **40** connected to the incoming alternating current power supply **41** which will either be the conventional **60** or **50** Hz (Hertz) power. The coupling circuit **40** including a coupling transformer **42** interconnecting the AC line power **41** into the circuit. The voltage is reduced down to a suitable level for driving of the clock circuitry, in particular to a **16** volt RMS level. A half-wave rectifying diode **43** in series with a limiting resister **44** and a pull-down resistor **45** are connected across the transformer secondary. A regulating diode **46**, such as a Zener diode, is connected across the pull-down resistor **45** to limit the voltage of the signal at the junction **47** of the resistors **44** and **45**. This generates an input signal which is coupled to a suitable triggered timing circuit **48** shown as a one-shot integrated circuit, identified by the circuit number **74121**. Each cycle of the line voltage generates a corresponding rectified pulse which fires the circuit **48**. The output is a pulse signal, for example, of **2** milliseconds length, although the particular timing period is not critical. It is merely necessary that the circuit provide a suitable pulse signal for each input cycle of the power supply **41**. The one-shot circuit **48** establishes opposite logic level signals at output line **49** and at line **50**. The output pulse signal at line **50** defines a clock synchronizing pulse which is connected through a steering diode or gate network **52** to the proper pulse dividing network **53** to generate a pulse per second at the clock drive line **54** which is connected as the input side of the second counter **16**.

Thus, if the line frequency is **60** Hz, the circuit **53** will divide by **60** and provide the pulse per second. Similarly, if the line power is a **50** Hz signal, the divider circuit **53** will proportionately divide the input pulses by **50** to provide the desired pulse per second output.

The output counting pulses, which proceed through the minutes, the hour and the day counters in accordance with well-known functioning, with the counters **13 – 16** being driven to maintain the desired binary-coded-decimal encoded time information.

Thus, as long as the line voltage is available, the system is driven directly from the line supply **41**. If the line voltage should fail, the clock unit **16** is driven from the self-powered standby drive **39**. The illustrated embodiment of the standby drive includes a standby oscillator **55** of a frequency corresponding to the line frequency and connected as a standby input to the steering gates **52** for selective introduction or replacement of the conventional clock synchronizing signals to the divider **53**. The oscillator **55** is connected to a battery **56** and operates continuously. A battery charge **57** is connected to charge battery **56** from the supply **41** and maintains the battery fully charged until a line failure occurs. The output of oscillator **55** is not transferred and employed unless the line power fails. The oscillator is an C/MOS integrated circuit which requires minimal power consumption during standby operation and permits relative long periods of use in the event of a power failure.

The failure is detected through a pulse detector and timing means **58** which is connected to line **49** of the one-shot circuit **48**. The means **58** is shown as a retriggerable one-shot circuit also but it has a significantly longer time period than that of the first; for example, a **30** msec. period. The retriggerable one-shot detector **58** is shown as a **74123** unit with the output line **59** connected to the steering gate **52** to switch the connection from the conventional clock sync input line **50** to the output of the standby oscillator **55**. Thus, the line **59** stays active for approximately **30** milliseconds after each synchronizing pulse and will be maintained active as long as the retriggering pulses from the first one-shot circuit **48** are received.

The output line **59** is, therefore, normally maintained at a logic **0** level and activates the gate **52** to connect the divider **53** to circuit **48**. If, however, the normal clock synchronizm pulse signals are not received for a period in excess of thirty milliseconds, the resettable one-shot detector **58** will time out and generate a logic **1** signal at the output line **59**. When the output goes to the logic **1**, the gate **52** automatically switches to connect the auxiliary oscillator **58** of standby power supply **39** to the dividing network **53** to replace the original timing pulses with that from the auxiliary supply.

Thus, the detection and necessary switching are such that no more than two timing or clock pulses will ever be missed by the seconds counter **16**.

By the use of integrated circuits for the oscillator and the like, the present invention provides an automatic auxiliary standby supply requiring minimum power consumption and further providing for automatic transfer with essentially minimal loss of timing.

The present invention thus provides a real time clock means which is readily adapted to a communication network providing for proper updating of the setting and monitoring of the clock setting with a minimum wiring complexity and the like. The novel clock system, thus, provides a very reliable and highly satisfactory real time source which can be employed at one remote point in a data communication loop serving several points and particularly in a primary-secondary time system.

Various modes of carrying out the invention are contemplated as being within the scope of the following claims, particularly pointing out and distinctly claiming the subject matter which is regarded as the invention.

We claim:

1. In a time clock apparatus for interconnection into a control system for generating time related output signals comprising a plurality of counter-stages identifying the time units, an alternating current supply means, s source of clock pulses including an A.C. line coupling and synchronizing means connected to said alternating current supply means and having an output establishing a continuous series of time spaced related driving pulse signals at a selected repetition rate for actuating of said counter-stages, an auxiliary standby power-driven oscillator having an output means and establishing a series of auxiliary pulse signals of a repetition rate corresponding to that of the driving pulse signals, a steering logic gate means having a first input connected to the output means of the first line coupling and synchronizing means and a second input connected to the output means of said standby oscillator, said steering gate means being selectively operable to couple one of said two inputs to said counter-stages and thereby actuating of said counter-stages from the corresponding pulse signals, and a power failure detection means connected to the output means of the source of clock pulses and operable to detect the absence of a selected number of said driving pulse signals within a selected time period and automatically actuate said gate means to connect

said standby power-driven oscillator as the input to said counter-stages.

2. The time clock apparatus of claim **1** wherein said auxiliary oscillator is battery driven, and having a rechargeable baattery connected to drive said oscillator, and a battery charging circuit connecting said battry to said line coupling means.

3. The time clock apparatus of claim **1** wherein said line coupling and synchronizing means insludes a triggerable timing means and having an energizing pulse output connected to the gate means, a half-wave rectifying means connected to said power supply means and to the timing means to pulse said timing means, a retriggerable timing means connected to be driven from said triggerable timing means and having a steering output means connected to selectively actuate said steering logic gate means.

4. The time clock apparatus of claim **1** wherein said coupling and synchronizing means includes triggerable one-shot means and having a control output and a clock synchronization pulse output connected to the steering gate means, a half-wave rectifying means connected to pulse said one-shot means, a retriggerable one-shot means connected to be driven from said control output of said triggerable one-shot means and having a steering output means connected to actuate said steering gate means to connect the auxiliary oscillator to said clock means.

5. In the data communication apparatus of claim **1** wherein said oscillator includes a C/MOS integrated circuit which is driven continuously to establish said pulses at said gate means.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 3,902,311
DATED : September 2, 1975

INVENTOR(S) : MANUEL F. CHACON and FREDERICK J. WOLTERS

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column	1,	Line	57,	between "data" and "information" insert --- and ---;
Column	2,	Line	8,	cancel "to" (first occurrence);
Column	3,	Line	10,	after "suitable" cancel "one-type" and insert --- one-shot type ---;
Column	3,	Line	12,	after "power" insert --- supply ---;
Column	3,	Line	63,	cancel "consturction" and insert --- construction ---;
Column	4,	Line	28,	cancel "staions" and insert --- stations ---;
Column	4,	Line	63,	cancel "The," and insert --- Thus, ---;
Column	7,	Line	8,	before "input" cancel "side" and insert --- wide ---;
Column	8,	Line	24,	after "positions" and before "the" insert --- as ---;
Column	9,	Line	7,	after "40" cancel "including" and insert --- includes ---;
Column	9,	Line	32,	cancel "as" and insert --- at ---;
Column	10,	Line	9,	after "logic" cancel "0" and insert --- "0" ---;

UNITED STATES PATENT AND TRADEMARK OFFICE

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PATENT NO. : 3,902,311

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INVENTOR(S) : MANUEL F. CHACON and FREDERICK J. WOLTERS

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column	10,	Line	14,	cancel the numeral 1 and insert --- "1" ---;
Column	10,	Line	15,	after "logic" cancel the numeral 1 and insert --- "1" ---;
Column Claim 1	10,	Line	46,	at the end of the line cancel "s" and insert --- a ---;
Column Claim 1	10,	Line	62,	at the beginning of the line cancel "of" before "said";
Column Claim 2	11,	Line	5,	after "chargeable" cancel "baattery" and insert --- battery ---;
Column Claim 2	11,	Line	6,	after "said" cancel "battry" and insert --- battery ---.
Column Claim 3	11.	Line	9,	after "means" cancel "insludes" and insert --- includes ---;

Signed and Sealed this

seventeenth Day of February 1976

[SEAL]

Attest:

RUTH C. MASON
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents and Trademarks