(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
05 April 2018 (05.04.2018)

WIPO | PCT

(10) International Publication Number
WO 2018/063204 A1

(51) International Patent Classification:
H01L 25/07 (2006.01) *H01L 29/12* (2006.01)
H01L 25/16 (2006.01) *H01L 29/775* (2006.01)
H01L 25/11 (2006.01)

(21) International Application Number:
PCT/US2016/054294

(22) International Filing Date:
29 September 2016 (29.09.2016)

(25) Filing Language: English

(26) Publication Language: English

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

(54) Title: QUANTUM COMPUTING ASSEMBLIES

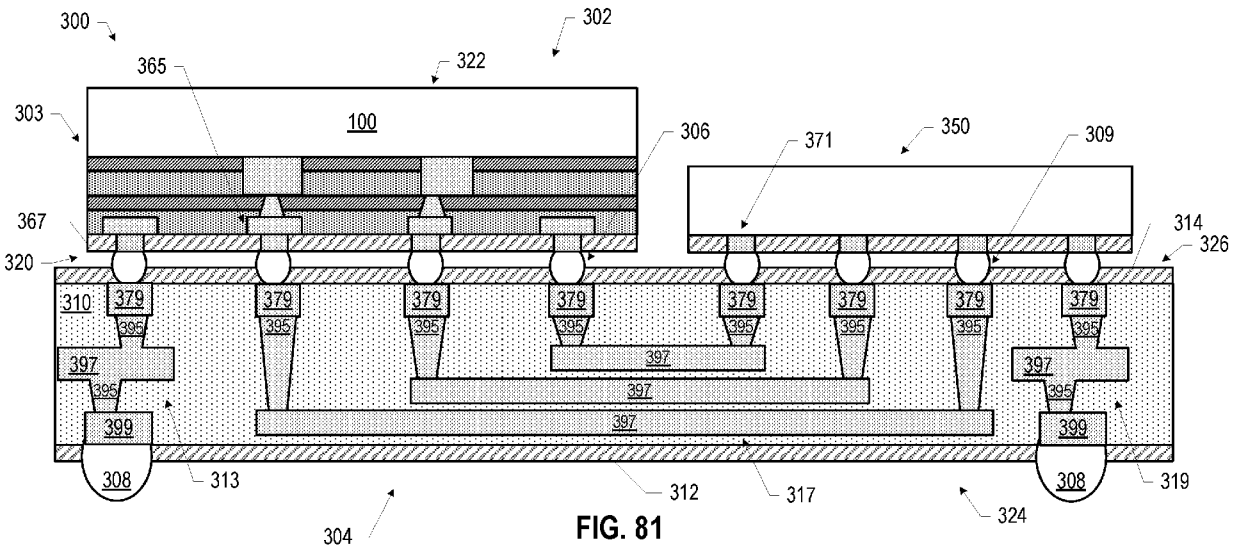


FIG. 81

(57) Abstract: Disclosed herein are quantum computing assemblies, as well as related computing devices and methods. For example, in some embodiments, a quantum computing assembly may include: a quantum device die to generate a plurality of qubits; a control circuitry die to control operation of the quantum device die; and a substrate; wherein the quantum device die and the control circuitry die are disposed on the substrate.

WO 2018/063204 A1

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Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *of inventorship (Rule 4.17(iv))*

Published:

— *with international search report (Art. 21(3))*

QUANTUM COMPUTING ASSEMBLIES

Background

[0001] Quantum computing refers to the field of research related to computation systems that use quantum mechanical phenomena to manipulate data. These quantum mechanical phenomena, such as superposition (in which a quantum variable can simultaneously exist in multiple different states) and entanglement (in which multiple quantum variables have related states irrespective of the distance between them in space or time), do not have analogs in the world of classical computing, and thus cannot be implemented with classical computing devices.

Brief Description of the Drawings

[0002] Embodiments will be readily understood by the following detailed description in conjunction with the accompanying drawings. To facilitate this description, like reference numerals designate like structural elements. Embodiments are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

[0003] FIGS. 1-3 are cross-sectional views of a quantum dot device, in accordance with various embodiments.

[0004] FIGS. 4-33 illustrate various example stages in the manufacture of a quantum dot device, in accordance with various embodiments.

[0005] FIGS. 34-36 are cross-sectional views of another quantum dot device, in accordance with various embodiments.

[0006] FIGS. 37-39 are cross-sectional views of various examples of quantum well stacks that may be used in a quantum dot device, in accordance with various embodiments.

[0007] FIGS. 40-46 illustrate example base/fin arrangements that may be used in a quantum dot device, in accordance with various embodiments.

[0008] FIGS. 47-49 are cross-sectional views of a quantum dot device, in accordance with various embodiments.

[0009] FIGS. 50-71 illustrate various example stages in the manufacture of a quantum dot device, in accordance with various embodiments.

[0010] FIG. 72 is a cross-sectional view of an example quantum dot device, in accordance with various embodiments.

[0011] FIG. 73 is a cross-sectional view of an alternative example stage in the manufacture of the quantum dot device of FIG. 72, in accordance with various embodiments.

[0012] FIG. 74 illustrates an embodiment of a quantum dot device having multiple trenches arranged in a two-dimensional array, in accordance with various embodiments.

[0013] FIG. 75 illustrates an embodiment of a quantum dot device having multiple groups of gates in a single trench on a quantum well stack, in accordance with various embodiments.

[0014] FIGS. 76-79 illustrate various alternative stages in the manufacture of a quantum dot device, in accordance with various embodiments.

[0015] FIG. 80 is a cross-sectional view of a quantum dot device with multiple interconnect layers, in accordance with various embodiments.

[0016] FIG. 81 is a cross-sectional view of a quantum dot device package, in accordance with various embodiments.

[0017] FIGS. 82A and 82B are top views of a wafer and dies that may include any of the quantum dot devices disclosed herein.

[0018] FIG. 83 is a cross-sectional side view of a device assembly that may include any of the quantum dot devices disclosed herein.

[0019] FIG. 84 is a flow diagram of an illustrative method of manufacturing a quantum dot device, in accordance with various embodiments.

[0020] FIGS. 85-86 are flow diagrams of illustrative methods of operating a quantum dot device, in accordance with various embodiments.

[0021] FIG. 87 is a block diagram of an example quantum computing device that may include any of the quantum dot devices disclosed herein, in accordance with various embodiments.

Detailed Description

[0022] Disclosed herein are quantum computing assemblies, as well as related computing devices and methods. For example, in some embodiments, a quantum computing assembly may include: a quantum device die to generate a plurality of qubits; a control circuitry die to control operation of the quantum device die; and a substrate; wherein the quantum device die and the control circuitry die are disposed on the substrate.

[0023] The quantum dot devices disclosed herein may enable the formation of quantum dots to serve as quantum bits ("qubits") in a quantum computing device, as well as the control of these quantum dots to perform quantum logic operations. Unlike previous approaches to quantum dot formation and manipulation, various embodiments of the quantum dot devices disclosed herein provide strong spatial localization of the quantum dots (and therefore good control over quantum dot interactions and manipulation), good scalability in the number of quantum dots included in the device, and/or design flexibility in making electrical connections to the quantum dot devices to integrate the quantum dot devices in larger computing devices.

[0024] In the following detailed description, reference is made to the accompanying drawings that form a part hereof, and in which is shown, by way of illustration, embodiments that may be

practiced. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present disclosure. Therefore, the following detailed description is not to be taken in a limiting sense.

[0025] Various operations may be described as multiple discrete actions or operations in turn in a manner that is most helpful in understanding the claimed subject matter. However, the order of description should not be construed as to imply that these operations are necessarily order dependent. In particular, these operations may not be performed in the order of presentation. Operations described may be performed in a different order from the described embodiment. Various additional operations may be performed, and/or described operations may be omitted in additional embodiments.

[0026] For the purposes of the present disclosure, the phrase "A and/or B" means (A), (B), or (A and B). For the purposes of the present disclosure, the phrase "A, B, and/or C" means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B, and C). The term "between," when used with reference to measurement ranges, is inclusive of the ends of the measurement ranges. As used herein, the notation "A/B/C" means (A), (B), and/or (C).

[0027] The description uses the phrases "in an embodiment" or "in embodiments," which may each refer to one or more of the same or different embodiments. Furthermore, the terms "comprising," "including," "having," and the like, as used with respect to embodiments of the present disclosure, are synonymous. The disclosure may use perspective-based descriptions such as "above," "below," "top," "bottom," and "side"; such descriptions are used to facilitate the discussion and are not intended to restrict the application of disclosed embodiments. The accompanying drawings are not necessarily drawn to scale. As used herein, a "high-k dielectric" refers to a material having a higher dielectric constant than silicon oxide. As used herein, a "magnet line" refers to a magnetic field-generating structure to influence (e.g., change, reset, scramble, or set) the spin states of quantum dots. One example of a magnet line, as discussed herein, is a conductive pathway that is proximate to an area of quantum dot formation and selectively conductive of a current pulse that generates a magnetic field to influence a spin state of a quantum dot in the area.

[0028] FIGS. 1-3 are cross-sectional views of a quantum dot device 100, in accordance with various embodiments. In particular, FIG. 2 illustrates the quantum dot device 100 taken along the section A-A of FIG. 1 (while FIG. 1 illustrates the quantum dot device 100 taken along the section C-C of FIG. 2), and FIG. 3 illustrates the quantum dot device 100 taken along the section B-B of FIG. 1 with a number of components not shown to more readily illustrate how the gates 106/108 and the magnet line 121 may be patterned (while FIG. 1 illustrates a quantum dot device 100 taken along the section D-D of FIG. 3). Although FIG. 1 indicates that the cross-section illustrated in FIG. 2 is taken through

the fin 104-1, an analogous cross section taken through the fin 104-2 may be identical, and thus the discussion of FIG. 2 refers generally to the "fin 104."

[0029] The quantum dot device 100 may include a base 102 and multiple fins 104 extending away from the base 102. The base 102 and the fins 104 may include a substrate and a quantum well stack (not shown in FIGS. 1-3, but discussed below with reference to the substrate 144 and the quantum well stack 146), distributed in any of a number of ways between the base 102 and the fins 104. The base 102 may include at least some of the substrate, and the fins 104 may each include a quantum well layer of the quantum well stack (discussed below with reference to the quantum well layer 152). Examples of base/fin arrangements are discussed below with reference to the base fin arrangements 158 of FIGS. 40-46.

[0030] Although only two fins, 104-1 and 104-2, are shown in FIGS. 1-3, this is simply for ease of illustration, and more than two fins 104 may be included in the quantum dot device 100. In some embodiments, the total number of fins 104 included in the quantum dot device 100 is an even number, with the fins 104 organized into pairs including one active fin 104 and one read fin 104, as discussed in detail below. When the quantum dot device 100 includes more than two fins 104, the fins 104 may be arranged in pairs in a line (e.g., 2N fins total may be arranged in a 1x2N line, or a 2xN line) or in pairs in a larger array (e.g., 2N fins total may be arranged as a 4xN/2 array, a 6xN/3 array, etc.). The discussion herein will largely focus on a single pair of fins 104 for ease of illustration, but all the teachings of the present disclosure apply to quantum dot devices 100 with more fins 104.

[0031] As noted above, each of the fins 104 may include a quantum well layer (not shown in FIGS. 1-3, but discussed below with reference to the quantum well layer 152). The quantum well layer included in the fins 104 may be arranged normal to the z-direction, and may provide a layer in which a two-dimensional electron gas (2DEG) may form to enable the generation of a quantum dot during operation of the quantum dot device 100, as discussed in further detail below. The quantum well layer itself may provide a geometric constraint on the z-location of quantum dots in the fins 104, and the limited extent of the fins 104 (and therefore the quantum well layer) in the y-direction may provide a geometric constraint on the y-location of quantum dots in the fins 104. To control the x-location of quantum dots in the fins 104, voltages may be applied to gates disposed on the fins 104 to adjust the energy profile along the fins 104 in the x-direction and thereby constrain the x-location of quantum dots within quantum wells (discussed in detail below with reference to the gates 106/108). The dimensions of the fins 104 may take any suitable values. For example, in some embodiments, the fins 104 may each have a width 162 between 10 and 30 nanometers. In some embodiments, the fins 104 may each have a height 164 between 200 and 400 nanometers (e.g., between 250 and 350 nanometers, or equal to 300 nanometers).

[0032] The fins 104 may be arranged in parallel, as illustrated in FIGS. 1 and 3, and may be spaced apart by an insulating material 128, which may be disposed on opposite faces of the fins 104. The insulating material 128 may be a dielectric material, such as silicon oxide. For example, in some embodiments, the fins 104 may be spaced apart by a distance 160 between 100 and 250 nanometers.

[0033] Multiple gates may be disposed on each of the fins 104. In the embodiment illustrated in FIG. 2, three gates 106 and two gates 108 are shown as distributed on the top of the fin 104. This particular number of gates is simply illustrative, and any suitable number of gates may be used. Additionally, as discussed below with reference to FIG. 50, multiple groups of gates (like the gates illustrated in FIG. 2) may be disposed on the fin 104.

[0034] As shown in FIG. 2, the gate 108-1 may be disposed between the gates 106-1 and 106-2, and the gate 108-2 may be disposed between the gates 106-2 and 106-3. Each of the gates 106/108 may include a gate dielectric 114; in the embodiment illustrated in FIG. 2, the gate dielectric 114 for all of the gates 106/108 is provided by a common layer of gate dielectric material. In other embodiments, the gate dielectric 114 for each of the gates 106/108 may be provided by separate portions of gate dielectric 114 (e.g., as discussed below with reference to FIGS. 56-59). In some embodiments, the gate dielectric 114 may be a multilayer gate dielectric (e.g., with multiple materials used to improve the interface between the fin 104 and the corresponding gate metal). The gate dielectric 114 may be, for example, silicon oxide, aluminum oxide, or a high-k dielectric, such as hafnium oxide. More generally, the gate dielectric 114 may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of materials that may be used in the gate dielectric 114 may include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, tantalum oxide, tantalum silicon oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate dielectric 114 to improve the quality of the gate dielectric 114.

[0035] Each of the gates 106 may include a gate metal 110 and a hardmask 116. The hardmask 116 may be formed of silicon nitride, silicon carbide, or another suitable material. The gate metal 110 may be disposed between the hardmask 116 and the gate dielectric 114, and the gate dielectric 114 may be disposed between the gate metal 110 and the fin 104. Only one portion of the hardmask 116 is labeled in FIG. 2 for ease of illustration. In some embodiments, the gate metal 110 may be a superconductor, such as aluminum, titanium nitride (e.g., deposited via atomic layer deposition), or

niobium titanium nitride. In some embodiments, the hardmask 116 may not be present in the quantum dot device 100 (e.g., a hardmask like the hardmask 116 may be removed during processing, as discussed below). The sides of the gate metal 110 may be substantially parallel, as shown in FIG. 2, and insulating spacers 134 may be disposed on the sides of the gate metal 110 and the hardmask 116. As illustrated in FIG. 2, the spacers 134 may be thicker closer to the fin 104 and thinner farther away from the fin 104. In some embodiments, the spacers 134 may have a convex shape. The spacers 134 may be formed of any suitable material, such as a carbon-doped oxide, silicon nitride, silicon oxide, or other carbides or nitrides (e.g., silicon carbide, silicon nitride doped with carbon, and silicon oxynitride). The gate metal 110 may be any suitable metal, such as titanium nitride.

[0036] Each of the gates 108 may include a gate metal 112 and a hardmask 118. The hardmask 118 may be formed of silicon nitride, silicon carbide, or another suitable material. The gate metal 112 may be disposed between the hardmask 118 and the gate dielectric 114, and the gate dielectric 114 may be disposed between the gate metal 112 and the fin 104. In the embodiment illustrated in FIG. 2, the hardmask 118 may extend over the hardmask 116 (and over the gate metal 110 of the gates 106), while in other embodiments, the hardmask 118 may not extend over the gate metal 110 (e.g., as discussed below with reference to FIG. 45). In some embodiments, the gate metal 112 may be a different metal from the gate metal 110; in other embodiments, the gate metal 112 and the gate metal 110 may have the same material composition. In some embodiments, the gate metal 112 may be a superconductor, such as aluminum, titanium nitride (e.g., deposited via atomic layer deposition), or niobium titanium nitride. In some embodiments, the hardmask 118 may not be present in the quantum dot device 100 (e.g., a hardmask like the hardmask 118 may be removed during processing, as discussed below).

[0037] The gate 108-1 may extend between the proximate spacers 134 on the sides of the gate 106-1 and the gate 106-2, as shown in FIG. 2. In some embodiments, the gate metal 112 of the gate 108-1 may extend between the spacers 134 on the sides of the gate 106-1 and the gate 106-2. Thus, the gate metal 112 of the gate 108-1 may have a shape that is substantially complementary to the shape of the spacers 134, as shown. Similarly, the gate 108-2 may extend between the proximate spacers 134 on the sides of the gate 106-2 and the gate 106-3. In some embodiments in which the gate dielectric 114 is not a layer shared commonly between the gates 108 and 106, but instead is separately deposited on the fin 104 between the spacers 134 (e.g., as discussed below with reference to FIGS. 56-59), the gate dielectric 114 may extend at least partially up the sides of the spacers 134, and the gate metal 112 may extend between the portions of gate dielectric 114 on the

spacers 134. The gate metal 112, like the gate metal 110, may be any suitable metal, such as titanium nitride.

[0038] The dimensions of the gates 106/108 may take any suitable values. For example, in some embodiments, the z-height 166 of the gate metal 110 may be between 40 and 75 nanometers (e.g., approximately 50 nanometers); the z-height of the gate metal 112 may be in the same range. In embodiments like the ones illustrated in FIG. 2, the z-height of the gate metal 112 may be greater than the z-height of the gate metal 110. In some embodiments, the length 168 of the gate metal 110 (i.e., in the x-direction) may be between 20 and 40 nanometers (e.g., 30 nanometers). In some embodiments, the distance 170 between adjacent ones of the gates 106 (e.g., as measured from the gate metal 110 of one gate 106 to the gate metal 110 of an adjacent gate 106 in the x-direction, as illustrated in FIG. 2) may be between 40 and 60 nanometers (e.g., 50 nanometers). In some embodiments, the thickness 172 of the spacers 134 may be between 1 and 10 nanometers (e.g., between 3 and 5 nanometers, between 4 and 6 nanometers, or between 4 and 7 nanometers). The length of the gate metal 112 (i.e., in the x-direction) may depend on the dimensions of the gates 106 and the spacers 134, as illustrated in FIG. 2. As indicated in FIG. 1, the gates 106/108 on one fin 104 may extend over the insulating material 128 beyond their respective fins 104 and towards the other fin 104, but may be isolated from their counterpart gates by the intervening insulating material 130 and spacers 134.

[0039] Although all of the gates 106 are illustrated in the accompanying drawings as having the same length 168 of the gate metal 110, in some embodiments, the "outermost" gates 106 (e.g., the gates 106-1 and 106-3 of the embodiment illustrated in FIG. 2) may have a greater length 168 than the "inner" gates 106 (e.g., the gate 106-2 in the embodiment illustrated in FIG. 2). Such longer "outside" gates 106 may provide spatial separation between the doped regions 140 and the areas under the gates 108 and the inner gates 106 in which quantum dots 142 may form, and thus may reduce the perturbations to the potential energy landscape under the gates 108 and the inner gates 106 caused by the doped regions 140.

[0040] As shown in FIG. 2, the gates 106 and 108 may be alternatingly arranged along the fin 104 in the x-direction. During operation of the quantum dot device 100, voltages may be applied to the gates 106/108 to adjust the potential energy in the quantum well layer (not shown) in the fin 104 to create quantum wells of varying depths in which quantum dots 142 may form. Only one quantum dot 142 is labeled with a reference numeral in FIGS. 2 and 3 for ease of illustration, but five are indicated as dotted circles in each fin 104. The location of the quantum dots 142 in FIG. 2 is not intended to indicate a particular geometric positioning of the quantum dots 142. The spacers 134 may themselves provide "passive" barriers between quantum wells under the gates 106/108 in the

quantum well layer, and the voltages applied to different ones of the gates 106/108 may adjust the potential energy under the gates 106/108 in the quantum well layer; decreasing the potential energy may form quantum wells, while increasing the potential energy may form quantum barriers.

[0041] The fins 104 may include doped regions 140 that may serve as a reservoir of charge carriers for the quantum dot device 100. For example, an n-type doped region 140 may supply electrons for electron-type quantum dots 142, and a p-type doped region 140 may supply holes for hole-type quantum dots 142. In some embodiments, an interface material 141 may be disposed at a surface of a doped region 140, as shown. The interface material 141 may facilitate electrical coupling between a conductive contact (e.g., a conductive via 136, as discussed below) and the doped region 140. The interface material 141 may be any suitable metal-semiconductor ohmic contact material; for example, in embodiments in which the doped region 140 includes silicon, the interface material 141 may include nickel silicide, aluminum silicide, titanium silicide, molybdenum silicide, cobalt silicide, tungsten silicide, or platinum silicide (e.g., as discussed below with reference to FIGS. 22-23). In some embodiments, the interface material 141 may be a non-silicide compound, such as titanium nitride. In some embodiments, the interface material 141 may be a metal (e.g., aluminum, tungsten, or indium).

[0042] The quantum dot devices 100 disclosed herein may be used to form electron-type or hole-type quantum dots 142. Note that the polarity of the voltages applied to the gates 106/108 to form quantum wells/barriers depend on the charge carriers used in the quantum dot device 100. In embodiments in which the charge carriers are electrons (and thus the quantum dots 142 are electron-type quantum dots), amply negative voltages applied to a gate 106/108 may increase the potential barrier under the gate 106/108, and amply positive voltages applied to a gate 106/108 may decrease the potential barrier under the gate 106/108 (thereby forming a potential well in which an electron-type quantum dot 142 may form). In embodiments in which the charge carriers are holes (and thus the quantum dots 142 are hole-type quantum dots), amply positive voltages applied to a gate 106/108 may increase the potential barrier under the gate 106/108, and amply negative voltages applied to a gate 106 and 108 may decrease the potential barrier under the gate 106/108 (thereby forming a potential well in which a hole-type quantum dot 142 may form). The quantum dot devices 100 disclosed herein may be used to form electron-type or hole-type quantum dots.

[0043] Voltages may be applied to each of the gates 106 and 108 separately to adjust the potential energy in the quantum well layer under the gates 106 and 108, and thereby control the formation of quantum dots 142 under each of the gates 106 and 108. Additionally, the relative potential energy profiles under different ones of the gates 106 and 108 allow the quantum dot device 100 to tune the potential interaction between quantum dots 142 under adjacent gates. For example, if two adjacent

quantum dots 142 (e.g., one quantum dot 142 under a gate 106 and another quantum dot 142 under a gate 108) are separated by only a short potential barrier, the two quantum dots 142 may interact more strongly than if they were separated by a taller potential barrier. Since the depth of the potential wells/height of the potential barriers under each gate 106/108 may be adjusted by adjusting the voltages on the respective gates 106/108, the differences in potential between adjacent gates 106/108 may be adjusted, and thus the interaction tuned.

[0044] In some applications, the gates 108 may be used as plunger gates to enable the formation of quantum dots 142 under the gates 108, while the gates 106 may be used as barrier gates to adjust the potential barrier between quantum dots 142 formed under adjacent gates 108. In other applications, the gates 108 may be used as barrier gates, while the gates 106 are used as plunger gates. In other applications, quantum dots 142 may be formed under all of the gates 106 and 108, or under any desired subset of the gates 106 and 108.

[0045] Conductive vias and lines may make contact with the gates 106/108, and to the doped regions 140, to enable electrical connection to the gates 106/108 and the doped regions 140 to be made in desired locations. As shown in FIGS. 1-3, the gates 106 may extend away from the fins 104, and conductive vias 120 may contact the gates 106 (and are drawn in dashed lines in FIG. 2 to indicate their location behind the plane of the drawing). The conductive vias 120 may extend through the hardmask 116 and the hardmask 118 to contact the gate metal 110 of the gates 106. The gates 108 may extend away from the fins 104, and conductive vias 122 may contact the gates 108 (also drawn in dashed lines in FIG. 2 to indicate their location behind the plane of the drawing). The conductive vias 122 may extend through the hardmask 118 to contact the gate metal 112 of the gates 108. Conductive vias 136 may contact the interface material 141 and may thereby make electrical contact with the doped regions 140. The quantum dot device 100 may include further conductive vias and/or lines (not shown) to make electrical contact to the gates 106/108 and/or the doped regions 140, as desired. The conductive vias and lines included in a quantum dot device 100 may include any suitable materials, such as copper, tungsten (deposited, e.g., by CVD), or a superconductor (e.g., aluminum, tin, titanium nitride, niobium titanium nitride, tantalum, niobium, or other niobium compounds such as niobium tin and niobium germanium).

[0046] During operation, a bias voltage may be applied to the doped regions 140 (e.g., via the conductive vias 136 and the interface material 141) to cause current to flow through the doped regions 140. When the doped regions 140 are doped with an n-type material, this voltage may be positive; when the doped regions 140 are doped with a p-type material, this voltage may be negative. The magnitude of this bias voltage may take any suitable value (e.g., between 0.25 volts and 2 volts).

[0047] The quantum dot device 100 may include one or more magnet lines 121. For example, a single magnet line 121 is illustrated in FIGS. 1-3 proximate to the fin 104-1. The magnet line 121 may be formed of a conductive material, and may be used to conduct current pulses that generate magnetic fields to influence the spin states of one or more of the quantum dots 142 that may form in the fins 104. In some embodiments, the magnet line 121 may conduct a pulse to reset (or "scramble") nuclear and/or quantum dot spins. In some embodiments, the magnet line 121 may conduct a pulse to initialize an electron in a quantum dot in a particular spin state. In some embodiments, the magnet line 121 may conduct current to provide a continuous, oscillating magnet field to which the spin of a qubit may couple. The magnet line 121 may provide any suitable combination of these embodiments, or any other appropriate functionality.

[0048] In some embodiments, the magnet line 121 may be formed of copper. In some embodiments, the magnet line 121 may be formed of a superconductor, such as aluminum. The magnet line 121 illustrated in FIGS. 1-3 is non-coplanar with the fins 104, and is also non-coplanar with the gates 106/108. In some embodiments, the magnet line 121 may be spaced apart from the gates 106/108 by a distance 167. The distance 167 may take any suitable value (e.g., based on the desired strength of magnetic field interaction with the quantum dots 142); in some embodiments, the distance 167 may be between 25 nanometers and 1 micron (e.g., between 50 nanometers and 200 nanometers).

[0049] In some embodiments, the magnet line 121 may be formed of a magnetic material. For example, a magnetic material (such as cobalt) may be deposited in a trench in the insulating material 130 to provide a permanent magnetic field in the quantum dot device 100.

[0050] The magnet line 121 may have any suitable dimensions. For example, the magnet line 121 may have a thickness 169 between 25 and 100 nanometers. The magnet line 121 may have a width 171 between 25 and 100 nanometers. In some embodiments, the width 171 and thickness 169 of a magnet line 121 may be equal to the width and thickness, respectively, of other conductive lines in the quantum dot device 100 (not shown) used to provide electrical interconnects, as known in the art. The magnet line 121 may have a length 173 that may depend on the number and dimensions of the gates 106/108 that are to form quantum dots 142 with which the magnet line 121 is to interact. The magnet line 121 illustrated in FIGS. 1-3 (and the magnet lines 121 illustrated in FIGS. 34-36 below) are substantially linear, but this need not be the case; the magnet lines 121 disclosed herein may take any suitable shape. Conductive vias 123 may contact the magnet line 121.

[0051] The conductive vias 120, 122, 136, and 123 may be electrically isolated from each other by an insulating material 130. The insulating material 130 may be any suitable material, such as an interlayer dielectric (ILD). Examples of the insulating material 130 may include silicon oxide, silicon

nitride, aluminum oxide, carbon-doped oxide, and/or silicon oxynitride. As known in the art of integrated circuit manufacturing, conductive vias and lines may be formed in an iterative process in which layers of structures are formed on top of each other. In some embodiments, the conductive vias 120/122/136/123 may have a width that is 20 nanometers or greater at their widest point (e.g., 30 nanometers), and a pitch of 80 nanometers or greater (e.g., 100 nanometers). In some embodiments, conductive lines (not shown) included in the quantum dot device 100 may have a width that is 100 nanometers or greater, and a pitch of 100 nanometers or greater. The particular arrangement of conductive vias shown in FIGS. 1-3 is simply illustrative, and any electrical routing arrangement may be implemented.

[0052] As discussed above, the structure of the fin 104-1 may be the same as the structure of the fin 104-2; similarly, the construction of gates 106/108 on the fin 104-1 may be the same as the construction of gates 106/108 on the fin 104-2. The gates 106/108 on the fin 104-1 may be mirrored by corresponding gates 106/108 on the parallel fin 104-2, and the insulating material 130 may separate the gates 106/108 on the different fins 104-1 and 104-2. In particular, quantum dots 142 formed in the fin 104-1 (under the gates 106/108) may have counterpart quantum dots 142 in the fin 104-2 (under the corresponding gates 106/108). In some embodiments, the quantum dots 142 in the fin 104-1 may be used as "active" quantum dots in the sense that these quantum dots 142 act as qubits and are controlled (e.g., by voltages applied to the gates 106/108 of the fin 104-1) to perform quantum computations. The quantum dots 142 in the fin 104-2 may be used as "read" quantum dots in the sense that these quantum dots 142 may sense the quantum state of the quantum dots 142 in the fin 104-1 by detecting the electric field generated by the charge in the quantum dots 142 in the fin 104-1, and may convert the quantum state of the quantum dots 142 in the fin 104-1 into electrical signals that may be detected by the gates 106/108 on the fin 104-2. Each quantum dot 142 in the fin 104-1 may be read by its corresponding quantum dot 142 in the fin 104-2. Thus, the quantum dot device 100 enables both quantum computation and the ability to read the results of a quantum computation.

[0053] The quantum dot devices 100 disclosed herein may be manufactured using any suitable techniques. FIGS. 4-33 illustrate various example stages in the manufacture of the quantum dot device 100 of FIGS. 1-3, in accordance with various embodiments. Although the particular manufacturing operations discussed below with reference to FIGS. 4-33 are illustrated as manufacturing a particular embodiment of the quantum dot device 100, these operations may be applied to manufacture many different embodiments of the quantum dot device 100, as discussed herein. Any of the elements discussed below with reference to FIGS. 4-33 may take the form of any of the embodiments of those elements discussed above (or otherwise disclosed herein).

[0054] FIG. 4 illustrates a cross-sectional view of an assembly 200 including a substrate 144. The substrate 144 may include any suitable semiconductor material or materials. In some embodiments, the substrate 144 may include a semiconductor material. For example, the substrate 144 may include silicon (e.g., may be formed from a silicon wafer).

[0055] FIG. 5 illustrates a cross-sectional view of an assembly 202 subsequent to providing a quantum well stack 146 on the substrate 144 of the assembly 200 (FIG. 4). The quantum well stack 146 may include a quantum well layer (not shown) in which a 2DEG may form during operation of the quantum dot device 100. Various embodiments of the quantum well stack 146 are discussed below with reference to FIGS. 37-39.

[0056] FIG. 6 illustrates a cross-sectional view of an assembly 204 subsequent to forming fins 104 in the assembly 202 (FIG. 5). The fins 104 may extend from a base 102, and may be formed in the assembly 202 by patterning and then etching the assembly 202, as known in the art. For example, a combination of dry and wet etch chemistry may be used to form the fins 104, and the appropriate chemistry may depend on the materials included in the assembly 202, as known in the art. At least some of the substrate 144 may be included in the base 102, and at least some of the quantum well stack 146 may be included in the fins 104. In particular, the quantum well layer (not shown) of the quantum well stack 146 may be included in the fins 104. Example arrangements in which the quantum well stack 146 and the substrate 144 are differently included in the base 102 and the fins 104 are discussed below with reference to FIGS. 40-46.

[0057] FIG. 7 illustrates a cross-sectional view of an assembly 206 subsequent to providing an insulating material 128 to the assembly 204 (FIG. 6). Any suitable material may be used as the insulating material 128 to electrically insulate the fins 104 from each other. As noted above, in some embodiments, the insulating material 128 may be a dielectric material, such as silicon oxide.

[0058] FIG. 8 illustrates a cross-sectional view of an assembly 208 subsequent to planarizing the assembly 206 (FIG. 7) to remove the insulating material 128 above the fins 104. In some embodiments, the assembly 206 may be planarized using a chemical mechanical polishing (CMP) technique.

[0059] FIG. 9 is a perspective view of at least a portion of the assembly 208, showing the fins 104 extending from the base 102 and separated by the insulating material 128. The cross-sectional views of FIGS. 4-8 are taken parallel to the plane of the page of the perspective view of FIG. 9. FIG. 10 is another cross-sectional view of the assembly 208, taken along the dashed line along the fin 104-1 in FIG. 9. The cross-sectional views illustrated in FIGS. 11-24, 26, 28, 30, and 32 are taken along the same cross-section as FIG. 10. The cross-sectional views illustrated in FIGS. 25, 27, 29, 31, and 33 are taken along the same cross-section as FIG. 8.

[0060] FIG. 11 is a cross-sectional view of an assembly 210 subsequent to forming a gate stack 174 on the fins 104 of the assembly 208 (FIGS. 8-10). The gate stack 174 may include the gate dielectric 114, the gate metal 110, and a hardmask 116. The hardmask 116 may be formed of an electrically insulating material, such as silicon nitride or carbon-doped nitride.

[0061] FIG. 12 is a cross-sectional view of an assembly 212 subsequent to patterning the hardmask 116 of the assembly 210 (FIG. 11). The pattern applied to the hardmask 116 may correspond to the locations for the gates 106, as discussed below. The hardmask 116 may be patterned by applying a resist, patterning the resist using lithography, and then etching the hardmask (using dry etching or any appropriate technique).

[0062] FIG. 13 is a cross-sectional view of an assembly 214 subsequent to etching the assembly 212 (FIG. 12) to remove the gate metal 110 that is not protected by the patterned hardmask 116 to form the gates 106. In some embodiments, as illustrated in FIG. 13, the gate dielectric 114 may remain after the etched gate metal 110 is etched away; in other embodiments, the gate dielectric 114 may also be etched during the etching of the gate metal 110. Examples of such embodiments are discussed below with reference to FIGS. 56-59.

[0063] FIG. 14 is a cross-sectional view of an assembly 216 subsequent to providing spacer material 132 on the assembly 214 (FIG. 13). The spacer material 132 may include any of the materials discussed above with reference to the spacers 134, for example, and may be deposited using any suitable technique. For example, the spacer material 132 may be a nitride material (e.g., silicon nitride) deposited by sputtering.

[0064] FIG. 15 is a cross-sectional view of an assembly 218 subsequent to etching the spacer material 132 of the assembly 216 (FIG. 14), leaving spacers 134 formed of the spacer material 132 on the sides of the gates 106 (e.g., on the sides of the hardmask 116 and the gate metal 110). The etching of the spacer material 132 may be an anisotropic etch, etching the spacer material 132 "downward" to remove the spacer material 132 on top of the gates 106 and in some of the area between the gates 106, while leaving the spacers 134 on the sides of the gates 106. In some embodiments, the anisotropic etch may be a dry etch.

[0065] FIG. 16 is a cross-sectional view of an assembly 220 subsequent to providing the gate metal 112 on the assembly 218 (FIG. 15). The gate metal 112 may fill the areas between adjacent ones of the gates 106, and may extend over the tops of the gates 106.

[0066] FIG. 17 is a cross-sectional view of an assembly 222 subsequent to planarizing the assembly 220 (FIG. 16) to remove the gate metal 112 above the gates 106. In some embodiments, the assembly 220 may be planarized using a CMP technique. Some of the remaining gate metal 112 may

fill the areas between adjacent ones of the gates 106, while other portions 150 of the remaining gate metal 112 may be located "outside" of the gates 106.

[0067] FIG. 18 is a cross-sectional view of an assembly 224 subsequent to providing a hardmask 118 on the planarized surface of the assembly 222 (FIG. 17). The hardmask 118 may be formed of any of the materials discussed above with reference to the hardmask 116, for example.

[0068] FIG. 19 is a cross-sectional view of an assembly 226 subsequent to patterning the hardmask 118 of the assembly 224 (FIG. 18). The pattern applied to the hardmask 118 may extend over the hardmask 116 (and over the gate metal 110 of the gates 106, as well as over the locations for the gates 108 (as illustrated in FIG. 2). The hardmask 118 may be non-coplanar with the hardmask 116, as illustrated in FIG. 19. The hardmask 118 illustrated in FIG. 19 may thus be a common, continuous portion of hardmask 118 that extends over all of the hardmask 116. The hardmask 118 may be patterned using any of the techniques discussed above with reference to the patterning of the hardmask 116, for example.

[0069] FIG. 20 is a cross-sectional view of an assembly 228 subsequent to etching the assembly 226 (FIG. 19) to remove the portions 150 that are not protected by the patterned hardmask 118 to form the gates 108. Portions of the hardmask 118 may remain on top of the hardmask 116, as shown. The operations performed on the assembly 226 may include removing any gate dielectric 114 that is "exposed" on the fin 104, as shown. The excess gate dielectric 114 may be removed using any suitable technique, such as chemical etching or silicon bombardment.

[0070] FIG. 21 is a cross-sectional view of an assembly 230 subsequent to doping the fins 104 of the assembly 228 (FIG. 20) to form doped regions 140 in the portions of the fins 104 "outside" of the gates 106/108. The type of dopant used to form the doped regions 140 may depend on the type of quantum dot desired, as discussed above. In some embodiments, the doping may be performed by ion implantation. For example, when the quantum dot 142 is to be an electron-type quantum dot 142, the doped regions 140 may be formed by ion implantation of phosphorous, arsenic, or another n-type material. When the quantum dot 142 is to be a hole-type quantum dot 142, the doped regions 140 may be formed by ion implantation of boron or another p-type material. An annealing process that activates the dopants and causes them to diffuse farther into the fins 104 may follow the ion implantation process. The depth of the doped regions 140 may take any suitable value; for example, in some embodiments, the doped regions 140 may extend into the fin 104 to a depth 115 between 500 and 1000 Angstroms.

[0071] The outer spacers 134 on the outer gates 106 may provide a doping boundary, limiting diffusion of the dopant from the doped regions 140 into the area under the gates 106/108. As shown, the doped regions 140 may extend under the adjacent outer spacers 134. In some

embodiments, the doped regions 140 may extend past the outer spacers 134 and under the gate metal 110 of the outer gates 106, may extend only to the boundary between the outer spacers 134 and the adjacent gate metal 110, or may terminate under the outer spacers 134 and not reach the boundary between the outer spacers 134 and the adjacent gate metal 110. The doping concentration of the doped regions 140 may, in some embodiments, be between $10^{17}/cm^3$ and $10^{20}/cm^3$.

[0072] FIG. 22 is a cross-sectional side view of an assembly 232 subsequent to providing a layer of nickel or other material 143 over the assembly 230 (FIG. 21). The nickel or other material 143 may be deposited on the assembly 230 using any suitable technique (e.g., a plating technique, chemical vapor deposition, or atomic layer deposition).

[0073] FIG. 23 is a cross-sectional side view of an assembly 234 subsequent to annealing the assembly 232 (FIG. 22) to cause the material 143 to interact with the doped regions 140 to form the interface material 141, then removing the unreacted material 143. When the doped regions 140 include silicon and the material 143 includes nickel, for example, the interface material 141 may be nickel silicide. Materials other than nickel may be deposited in the operations discussed above with reference to FIG. 22 in order to form other interface materials 141, including titanium, aluminum, molybdenum, cobalt, tungsten, or platinum, for example. More generally, the interface material 141 of the assembly 234 may include any of the materials discussed herein with reference to the interface material 141.

[0074] FIG. 24 is a cross-sectional view of an assembly 236 subsequent to providing an insulating material 130 on the assembly 234 (FIG. 23). The insulating material 130 may take any of the forms discussed above. For example, the insulating material 130 may be a dielectric material, such as silicon oxide. The insulating material 130 may be provided on the assembly 234 using any suitable technique, such as spin coating, chemical vapor deposition (CVD), or plasma-enhanced CVD (PECVD). In some embodiments, the insulating material 130 may be polished back after deposition, and before further processing. In some embodiments, the thickness 131 of the insulating material 130 provided on the assembly 236 (as measured from the hardmask 118, as indicated in FIG. 24) may be between 50 nanometers and 1.2 microns (e.g., between 50 nanometers and 300 nanometers). FIG. 25 is another cross-sectional view of the assembly 236, taken along the section C-C of FIG. 24.

[0075] FIG. 26 is a cross-sectional view of an assembly 238 subsequent to forming a trench 125 in the insulating material 130 of the assembly 236 (FIGS. 24 and 25). The trench 125 may be formed using any desired techniques (e.g., resist patterning followed by etching), and may have a depth 127 and a width 129 that may take the form of any of the embodiments of the thickness 169 and the width 171, respectively, discussed above with reference to the magnet line 121. FIG. 27 is another

cross-sectional view of the assembly 238, taken along the section C-C of FIG. 26. In some embodiments, the assembly 236 may be planarized to remove the hardmasks 116 and 118, then additional insulating material 130 may be provided on the planarized surface before forming the trench 125; in such an embodiment, the hardmasks 116 and 118 would not be present in the quantum dot device 100.

[0076] FIG. 28 is a cross-sectional view of an assembly 240 subsequent to filling the trench 125 of the assembly 238 (FIGS. 26 and 27) with a conductive material to form the magnet line 121. The magnet line 121 may be formed using any desired techniques (e.g., plating followed by planarization, or a semi-additive process), and may take the form of any of the embodiments disclosed herein. FIG. 29 is another cross-sectional view of the assembly 240, taken along the section C-C of FIG. 28.

[0077] FIG. 30 is a cross-sectional view of an assembly 242 subsequent to providing additional insulating material 130 on the assembly 240 (FIGS. 28 and 29). The insulating material 130 provided on the assembly 240 may take any of the forms of the insulating material 130 discussed above. FIG. 31 is another cross-sectional view of the assembly 242, taken along the section C-C of FIG. 30.

[0078] FIG. 32 is a cross-sectional view of an assembly 244 subsequent to forming, in the assembly 242 (FIGS. 30 and 31), conductive vias 120 through the insulating material 130 (and the hardmasks 116 and 118) to contact the gate metal 110 of the gates 106, conductive vias 122 through the insulating material 130 (and the hardmask 118) to contact the gate metal 112 of the gates 108, conductive vias 136 through the insulating material 130 to contact the interface material 141 of the doped regions 140, and conductive vias 123 through the insulating material 130 to contact the magnet line 121. FIG. 33 is another cross-sectional view of the assembly 244, taken along the section C-C of FIG. 32. Further conductive vias and/or lines may be formed in the assembly 244 using conventional interconnect techniques, if desired. The resulting assembly 244 may take the form of the quantum dot device 100 discussed above with reference to FIGS. 1-3.

[0079] In the embodiment of the quantum dot device 100 illustrated in FIGS. 1-3, the magnet line 121 is oriented parallel to the longitudinal axes of the fins 104. In other embodiments, the magnet line 121 may not be oriented parallel to the longitudinal axes of the fins 104. For example, FIGS. 34-36 are various cross-sectional views of an embodiment of a quantum dot device 100 having multiple magnet lines 121, each proximate to the fins 104 and oriented perpendicular to the longitudinal axes of the fins 104. Other than orientation, the magnet lines 121 of the embodiment of FIGS. 34-36 may take the form of any of the embodiments of the magnet line 121 discussed above. The other elements of the quantum dot devices 100 of FIGS. 34-36 may take the form of any of those elements discussed herein. The manufacturing operations discussed above with reference to FIGS. 4-33 may be used to manufacture the quantum dot device 100 of FIGS. 34-36.

[0080] Although a single magnet line 121 is illustrated in FIGS. 1-3, multiple magnet lines 121 may be included in that embodiment of the quantum dot device 100 (e.g., multiple magnet lines 121 parallel to the longitudinal axes of the fins 104). For example, the quantum dot device 100 of FIGS. 1-3 may include a second magnet line 121 proximate to the fin 104-2 in a symmetric manner to the magnet line 121 illustrated proximate to the fin 104-1. In some embodiments, multiple magnet lines 121 may be included in a quantum dot device 100, and these magnet lines 121 may or may not be parallel to one another. For example, in some embodiments, a quantum dot device 100 may include two (or more) magnet lines 121 that are oriented perpendicular to each other (e.g., one or more magnet lines 121 oriented like those illustrated in FIGS. 1-3, and one or more magnet lines 121 oriented like those illustrated in FIGS. 34-36).

[0081] As discussed above, the base 102 and the fin 104 of a quantum dot device 100 may be formed from a substrate 144 and a quantum well stack 146 disposed on the substrate 144. The quantum well stack 146 may include a quantum well layer in which a 2DEG may form during operation of the quantum dot device 100. The quantum well stack 146 may take any of a number of forms, several of which are illustrated in FIGS. 37-39. The various layers in the quantum well stacks 146 discussed below may be grown on the substrate 144 (e.g., using epitaxial processes).

[0082] FIG. 37 is a cross-sectional view of a quantum well stack 146 including only a quantum well layer 152. The quantum well layer 152 may be disposed on the substrate 144 (e.g., as discussed above with reference to FIG. 5), and may be formed of a material such that, during operation of the quantum dot device 100, a 2DEG may form in the quantum well layer 152 proximate to the upper surface of the quantum well layer 152. The gate dielectric 114 of the gates 106/108 may be disposed on the upper surface of the quantum well layer 152 (e.g., as discussed above with reference to FIG. 11). In some embodiments, the quantum well layer 152 of FIG. 37 may be formed of intrinsic silicon, and the gate dielectric 114 may be formed of silicon oxide; in such an arrangement, during use of the quantum dot device 100, a 2DEG may form in the intrinsic silicon at the interface between the intrinsic silicon and the silicon oxide. Embodiments in which the quantum well layer 152 of FIG. 37 is formed of intrinsic silicon may be particularly advantageous for electron-type quantum dot devices 100. In some embodiments, the quantum well layer 152 of FIG. 37 may be formed of intrinsic germanium, and the gate dielectric 114 may be formed of germanium oxide; in such an arrangement, during use of the quantum dot device 100, a 2DEG may form in the intrinsic germanium at the interface between the intrinsic germanium and the germanium oxide. Such embodiments may be particularly advantageous for hole-type quantum dot devices 100. In some embodiments, the quantum well layer 152 may be strained, while in other embodiments, the quantum well layer 152 may not be strained. The thicknesses (i.e., z-heights) of the layers in the

quantum well stack 146 of FIG. 37 may take any suitable values. For example, in some embodiments, the thickness of the quantum well layer 152 (e.g., intrinsic silicon or germanium) may be between 0.8 and 1.2 microns.

[0083] FIG. 38 is a cross-sectional view of a quantum well stack 146 including a quantum well layer 152 and a barrier layer 154. The quantum well stack 146 may be disposed on a substrate 144 (e.g., as discussed above with reference to FIG. 5) such that the barrier layer 154 is disposed between the quantum well layer 152 and the substrate 144. The barrier layer 154 may provide a potential barrier between the quantum well layer 152 and the substrate 144. As discussed above with reference to FIG. 26, the quantum well layer 152 of FIG. 38 may be formed of a material such that, during operation of the quantum dot device 100, a 2DEG may form in the quantum well layer 152 proximate to the upper surface of the quantum well layer 152. For example, in some embodiments in which the substrate 144 is formed of silicon, the quantum well layer 152 of FIG. 38 may be formed of silicon, and the barrier layer 154 may be formed of silicon germanium. The germanium content of this silicon germanium may be 20-80% (e.g., 30%). In some embodiments in which the quantum well layer 152 is formed of germanium, the barrier layer 154 may be formed of silicon germanium (with a germanium content of 20-80% (e.g., 70%)). The thicknesses (i.e., z-heights) of the layers in the quantum well stack 146 of FIG. 38 may take any suitable values. For example, in some embodiments, the thickness of the barrier layer 154 (e.g., silicon germanium) may be between 0 and 400 nanometers. In some embodiments, the thickness of the quantum well layer 152 (e.g., silicon or germanium) may be between 5 and 30 nanometers.

[0084] FIG. 39 is a cross-sectional view of a quantum well stack 146 including a quantum well layer 152 and a barrier layer 154-1, as well as a buffer layer 176 and an additional barrier layer 154-2. The quantum well stack 146 may be disposed on the substrate 144 (e.g., as discussed above with reference to FIG. 5) such that the buffer layer 176 is disposed between the barrier layer 154-1 and the substrate 144. The buffer layer 176 may be formed of the same material as the barrier layer 154, and may be present to trap defects that form in this material as it is grown on the substrate 144. In some embodiments, the buffer layer 176 may be grown under different conditions (e.g., deposition temperature or growth rate) from the barrier layer 154-1. In particular, the barrier layer 154-1 may be grown under conditions that achieve fewer defects than the buffer layer 176. In some embodiments in which the buffer layer 176 includes silicon germanium, the silicon germanium of the buffer layer 176 may have a germanium content that varies from the substrate 144 to the barrier layer 154-1; for example, the silicon germanium of the buffer layer 176 may have a germanium content that varies from zero percent at the silicon substrate 144 to a nonzero percent (e.g., 30%) at the barrier layer 154-1. The thicknesses (i.e., z-heights) of the layers in the quantum well stack 146

of FIG. 39 may take any suitable values. For example, in some embodiments, the thickness of the buffer layer 176 (e.g., silicon germanium) may be between 0.3 and 4 microns (e.g., 0.3-2 microns, or 0.5 microns). In some embodiments, the thickness of the barrier layer 154-1 (e.g., silicon germanium) may be between 0 and 400 nanometers. In some embodiments, the thickness of the quantum well layer 152 (e.g., silicon or germanium) may be between 5 and 30 nanometers (e.g., 10 nanometers). The barrier layer 154-2, like the barrier layer 154-1, may provide a potential energy barrier around the quantum well layer 152, and may take the form of any of the embodiments of the barrier layer 154-1. In some embodiments, the thickness of the barrier layer 154-2 (e.g., silicon germanium) may be between 25 and 75 nanometers (e.g., 32 nanometers).

[0085] As discussed above with reference to FIG. 38, the quantum well layer 152 of FIG. 39 may be formed of a material such that, during operation of the quantum dot device 100, a 2DEG may form in the quantum well layer 152 proximate to the upper surface of the quantum well layer 152. For example, in some embodiments in which the substrate 144 is formed of silicon, the quantum well layer 152 of FIG. 39 may be formed of silicon, and the barrier layer 154-1 and the buffer layer 176 may be formed of silicon germanium. In some such embodiments, the silicon germanium of the buffer layer 176 may have a germanium content that varies from the substrate 144 to the barrier layer 154-1; for example, the silicon germanium of the buffer layer 176 may have a germanium content that varies from zero percent at the silicon substrate 144 to a nonzero percent (e.g., 30%) at the barrier layer 154-1. In other embodiments, the buffer layer 176 may have a germanium content equal to the germanium content of the barrier layer 154-1 but may be thicker than the barrier layer 154-1 so as to absorb the defects that arise during growth.

[0086] In some embodiments, the quantum well layer 152 of FIG. 39 may be formed of germanium, and the buffer layer 176 and the barrier layer 154-1 may be formed of silicon germanium. In some such embodiments, the silicon germanium of the buffer layer 176 may have a germanium content that varies from the substrate 144 to the barrier layer 154-1; for example, the silicon germanium of the buffer layer 176 may have a germanium content that varies from zero percent at the substrate 144 to a nonzero percent (e.g., 70%) at the barrier layer 154-1. The barrier layer 154-1 may in turn have a germanium content equal to the nonzero percent. In other embodiments, the buffer layer 176 may have a germanium content equal to the germanium content of the barrier layer 154-1 but may be thicker than the barrier layer 154-1 so as to absorb the defects that arise during growth. In some embodiments of the quantum well stack 146 of FIG. 39, the buffer layer 176 and/or the barrier layer 154-2 may be omitted.

[0087] The substrate 144 and the quantum well stack 146 may be distributed between the base 102 and the fins 104 of the quantum dot device 100, as discussed above. This distribution may occur in

any of a number of ways. For example, FIGS. 40-46 illustrate example base/fin arrangements 158 that may be used in a quantum dot device 100, in accordance with various embodiments.

[0088] In the base/fin arrangement 158 of FIG. 40, the quantum well stack 146 may be included in the fins 104, but not in the base 102. The substrate 144 may be included in the base 102, but not in the fins 104. When the base/fin arrangement 158 of FIG. 40 is used in the manufacturing operations discussed with reference to FIGS. 5-6, the fin etching may etch through the quantum well stack 146, and stop when the substrate 144 is reached.

[0089] In the base/fin arrangement 158 of FIG. 41, the quantum well stack 146 may be included in the fins 104, as well as in a portion of the base 102. A substrate 144 may be included in the base 102 as well, but not in the fins 104. When the base/fin arrangement 158 of FIG. 41 is used in the manufacturing operations discussed with reference to FIGS. 5-6, the fin etching may etch partially through the quantum well stack 146, and stop before the substrate 144 is reached. FIG. 42 illustrates a particular embodiment of the base/fin arrangement 158 of FIG. 41. In the embodiment of FIG. 42, the quantum well stack 146 of FIG. 39 is used; the fins 104 include the barrier layer 154-1, the quantum well layer 152, and the barrier layer 154-2, while the base 102 includes the buffer layer 176 and the substrate 144.

[0090] In the base/fin arrangement 158 of FIG. 43, the quantum well stack 146 may be included in the fins 104, but not the base 102. The substrate 144 may be partially included in the fins 104, as well as in the base 102. When the base/fin arrangement 158 of FIG. 43 is used in the manufacturing operations discussed with reference to FIGS. 5-6, the fin etching may etch through the quantum well stack 146 and into the substrate 144 before stopping. FIG. 44 illustrates a particular embodiment of the base/fin arrangement 158 of FIG. 43. In the embodiment of FIG. 44, the quantum well stack 146 of FIG. 39 is used; the fins 104 include the quantum well stack 146 and a portion of the substrate 144, while the base 102 includes the remainder of the substrate 144.

[0091] Although the fins 104 have been illustrated in many of the preceding figures as substantially rectangular with parallel sidewalls, this is simply for ease of illustration, and the fins 104 may have any suitable shape (e.g., shape appropriate to the manufacturing processes used to form the fins 104). For example, as illustrated in the base/fin arrangement 158 of FIG. 45, in some embodiments, the fins 104 may be tapered. In some embodiments, the fins 104 may taper by 3-10 nanometers in x-width for every 100 nanometers in z-height (e.g., 5 nanometers in x-width for every 100 nanometers in z-height). When the fins 104 are tapered, the wider end of the fins 104 may be the end closest to the base 102, as illustrated in FIG. 45. FIG. 46 illustrates a particular embodiment of the base/fin arrangement 158 of FIG. 34. In FIG. 46, the quantum well stack 146 is included in the

tapered fins 104 while a portion of the substrate 144 is included in the tapered fins and a portion of the substrate 144 provides the base 102.

[0092] FIGS. 47-49 are cross-sectional views of another embodiment of a quantum dot device 100, in accordance with various embodiments. In particular, FIG. 48 illustrates the quantum dot device 100 taken along the section A-A of FIG. 47 (while FIG. 47 illustrates the quantum dot device 100 taken along the section C-C of FIG. 48), and FIG. 49 illustrates the quantum dot device 100 taken along the section D-D of FIG. 48 (while FIG. 48 illustrates the quantum dot device 100 taken along the section A-A of FIG. 49). The quantum dot device 100 of FIGS. 47-49, taken along the section B-B of FIG. 47, may be the same as illustrated in FIG. 3. Although FIG. 47 indicates that the cross section illustrated in FIG. 48 is taken through the trench 107-1, an analogous cross section taken through the trench 107-2 may be identical, and thus the discussion of FIG. 48 refers generally to the "trench 107."

[0093] The quantum dot device 100 may include a quantum well stack 146 disposed on a base 102. An insulating material 128 may be disposed above the quantum well stack 146, and multiple trenches 107 in the insulating material 128 may extend toward the quantum well stack 146. In the embodiment illustrated in FIGS. 47-49, a gate dielectric 114 may be disposed between the quantum well stack 146 and the insulating material 128 so as to provide the "bottom" of the trenches 107. The quantum well stack 146 of the quantum dot device 100 of FIGS. 47-49 may take the form of any of the quantum well stacks disclosed herein (e.g., as discussed above with reference to FIGS. 37-39). The various layers in the quantum well stack 146 of FIGS. 47-49 may be grown on the base 102 (e.g., using epitaxial processes).

[0094] Although only two trenches, 107-1 and 107-2, are shown in FIGS. 47-49, this is simply for ease of illustration, and more than two trenches 107 may be included in the quantum dot device 100. In some embodiments, the total number of trenches 107 included in the quantum dot device 100 is an even number, with the trenches 107 organized into pairs including one active trench 107 and one read trench 107, as discussed in detail below. When the quantum dot device 100 includes more than two trenches 107, the trenches 107 may be arranged in pairs in a line (e.g., 2N trenches total may be arranged in a 1x2N line, or a 2xN line) or in pairs in a larger array (e.g., 2N trenches total may be arranged as a 4xN/2 array, a 6xN/3 array, etc.). For example, FIG. 74 illustrates a quantum dot device 100 including an example two-dimensional array of trenches 107. As illustrated in FIGS. 47 and 49, in some embodiments, multiple trenches 107 may be oriented in parallel. The discussion herein will largely focus on a single pair of trenches 107 for ease of illustration, but all the teachings of the present disclosure apply to quantum dot devices 100 with more trenches 107.

[0095] As discussed above with reference to FIGS. 1-3, in the quantum dot device 100 of FIGS. 47-49, a quantum well layer itself may provide a geometric constraint on the z-location of quantum dots in the quantum well stack 146. To control the x- and y-location of quantum dots in the quantum well stack 146, voltages may be applied to gates disposed at least partially in the trenches 107 above the quantum well stack 146 to adjust the energy profile along the trenches 107 in the x- and y-direction and thereby constrain the x- and y-location of quantum dots within quantum wells (discussed in detail below with reference to the gates 106/108). The dimensions of the trenches 107 may take any suitable values. For example, in some embodiments, the trenches 107 may each have a width 162 between 10 and 30 nanometers. In some embodiments, the trenches 107 may each have a depth 164 between 200 and 400 nanometers (e.g., between 250 and 350 nanometers, or equal to 300 nanometers). The insulating material 128 may be a dielectric material (e.g., an interlayer dielectric), such as silicon oxide. In some embodiments, the insulating material 128 may be a chemical vapor deposition (CVD) or flowable CVD oxide. In some embodiments, the trenches 107 may be spaced apart by a distance 160 between 50 and 500 nanometers.

[0096] Multiple gates may be disposed at least partially in each of the trenches 107. In the embodiment illustrated in FIG. 48, three gates 106 and two gates 108 are shown as distributed at least partially in a single trench 107. This particular number of gates is simply illustrative, and any suitable number of gates may be used. Additionally, as discussed below with reference to FIG. 75, multiple groups of gates (like the gates illustrated in FIG. 48) may be disposed at least partially in the trench 107.

[0097] As shown in FIG. 48, the gate 108-1 may be disposed between the gates 106-1 and 106-2, and the gate 108-2 may be disposed between the gates 106-2 and 106-3. Each of the gates 106/108 may include a gate dielectric 114; in the embodiment illustrated in FIG. 48, the gate dielectric 114 for all of the gates 106/108 is provided by a common layer of gate dielectric material disposed between the quantum well stack 146 and the insulating material 128. In other embodiments, the gate dielectric 114 for each of the gates 106/108 may be provided by separate portions of gate dielectric 114 (e.g., as discussed below with reference to FIGS. 76-79). In some embodiments, the gate dielectric 114 may be a multilayer gate dielectric (e.g., with multiple materials used to improve the interface between the trench 107 and the corresponding gate metal). The gate dielectric 114 may be, for example, silicon oxide, aluminum oxide, or a high-k dielectric, such as hafnium oxide. More generally, the gate dielectric 114 may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of materials that may be used in the gate dielectric 114 may include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide,

zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, tantalum oxide, tantalum silicon oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate dielectric 114 to improve the quality of the gate dielectric 114.

[0098] Each of the gates 106 may include a gate metal 110 and a hardmask 116. The hardmask 116 may be formed of silicon nitride, silicon carbide, or another suitable material. The gate metal 110 may be disposed between the hardmask 116 and the gate dielectric 114, and the gate dielectric 114 may be disposed between the gate metal 110 and the quantum well stack 146. As shown in FIG. 47, in some embodiments, the gate metal 110 of a gate 106 may extend over the insulating material 128 and into a trench 107 in the insulating material 128. Only one portion of the hardmask 116 is labeled in FIG. 48 for ease of illustration. In some embodiments, the gate metal 110 may be a superconductor, such as aluminum, titanium nitride (e.g., deposited via atomic layer deposition), or niobium titanium nitride. In some embodiments, the hardmask 116 may not be present in the quantum dot device 100 (e.g., a hardmask like the hardmask 116 may be removed during processing, as discussed below). The sides of the gate metal 110 may be substantially parallel, as shown in FIG. 48, and insulating spacers 134 may be disposed on the sides of the gate metal 110 and the hardmask 116 along the longitudinal axis of the trench 107. As illustrated in FIG. 48, the spacers 134 may be thicker closer to the quantum well stack 146 and thinner farther away from the quantum well stack 146. In some embodiments, the spacers 134 may have a convex shape. The spacers 134 may be formed of any suitable material, such as a carbon-doped oxide, silicon nitride, silicon oxide, or other carbides or nitrides (e.g., silicon carbide, silicon nitride doped with carbon, and silicon oxynitride). The gate metal 110 may be any suitable metal, such as titanium nitride. As illustrated in FIG. 48, no spacer material may be disposed between the gate metal 110 and the sidewalls of the trench 107 in the y-direction.

[0099] Each of the gates 108 may include a gate metal 112 and a hardmask 118. The hardmask 118 may be formed of silicon nitride, silicon carbide, or another suitable material. The gate metal 112 may be disposed between the hardmask 118 and the gate dielectric 114, and the gate dielectric 114 may be disposed between the gate metal 112 and the quantum well stack 146. As shown in FIG. 49, in some embodiments, the gate metal 112 of a gate 108 may extend over the insulating material 128 and into a trench 107 in the insulating material 128. In the embodiment illustrated in FIG. 48, the hardmask 118 may extend over the hardmask 116 (and over the gate metal 110 of the gates 106), while in other embodiments, the hardmask 118 may not extend over the gate metal 110. In some embodiments, the gate metal 112 may be a different metal from the gate metal 110; in other

embodiments, the gate metal 112 and the gate metal 110 may have the same material composition. In some embodiments, the gate metal 112 may be a superconductor, such as aluminum, titanium nitride (e.g., deposited via atomic layer deposition), or niobium titanium nitride. In some embodiments, the hardmask 118 may not be present in the quantum dot device 100 (e.g., a hardmask like the hardmask 118 may be removed during processing, as discussed below).

[0100] The gate 108-1 may extend between the proximate spacers 134 on the sides of the gate 106-1 and the gate 106-2 along the longitudinal axis of the trench 107, as shown in FIG. 48. In some embodiments, the gate metal 112 of the gate 108-1 may extend between the spacers 134 on the sides of the gate 106-1 and the gate 106-2 along the longitudinal axis of the trench 107. Thus, the gate metal 112 of the gate 108-1 may have a shape that is substantially complementary to the shape of the spacers 134, as shown. Similarly, the gate 108-2 may extend between the proximate spacers 134 on the sides of the gate 106-2 and the gate 106-3 along the longitudinal axis of the trench 107. In some embodiments in which the gate dielectric 114 is not a layer shared commonly between the gates 108 and 106, but instead is separately deposited in the trench 107 between the spacers 134 (e.g., as discussed below with reference to FIGS. 76-79), the gate dielectric 114 may extend at least partially up the sides of the spacers 134 (and up the proximate sidewalls of the trench 107), and the gate metal 112 may extend between the portions of gate dielectric 114 on the spacers 134 (and the proximate sidewalls of the trench 107). The gate metal 112, like the gate metal 110, may be any suitable metal, such as titanium nitride. As illustrated in FIG. 49, in some embodiments, no spacer material may be disposed between the gate metal 112 and the sidewalls of the trench 107 in the y-direction; in other embodiments (e.g., as discussed below with reference to FIGS. 72 and 73), spacers 134 may also be disposed between the gate metal 112 and the sidewalls of the trench 107 in the y-direction.

[0101] The dimensions of the gates 106/108 may take any suitable values. For example, in some embodiments, the z-height 166 of the gate metal 110 in the trench 107 may be between 225 and 375 nanometers (e.g., approximately 300 nanometers); the z-height 175 of the gate metal 112 may be in the same range. This z-height 166 of the gate metal 110 in the trench 107 may represent the sum of the z-height of the insulating material 128 (e.g., between 200 and 300 nanometers) and the thickness of the gate metal 110 on top of the insulating material 128 (e.g., between 25 and 75 nanometers, or approximately 50 nanometers). In embodiments like the ones illustrated in FIGS. 47-49, the z-height 175 of the gate metal 112 may be greater than the z-height 166 of the gate metal 110. In some embodiments, the length 168 of the gate metal 110 (i.e., in the x-direction) may be between 20 and 40 nanometers (e.g., 30 nanometers). Although all of the gates 106 are illustrated in the accompanying drawings as having the same length 168 of the gate metal 110, in some

embodiments, the "outermost" gates 106 (e.g., the gates 106-1 and 106-3 of the embodiment illustrated in FIG. 48) may have a greater length 168 than the "inner" gates 106 (e.g., the gate 106-2 in the embodiment illustrated in FIG. 48). Such longer "outside" gates 106 may provide spatial separation between the doped regions 140 and the areas under the gates 108 and the inner gates 106 in which quantum dots 142 may form, and thus may reduce the perturbations to the potential energy landscape under the gates 108 and the inner gates 106 caused by the doped regions 140.

[0102] In some embodiments, the distance 170 between adjacent ones of the gates 106 (e.g., as measured from the gate metal 110 of one gate 106 to the gate metal 110 of an adjacent gate 106 in the x-direction, as illustrated in FIG. 48) may be between 40 and 100 nanometers (e.g., 50 nanometers). In some embodiments, the thickness 172 of the spacers 134 may be between 1 and 10 nanometers (e.g., between 3 and 5 nanometers, between 4 and 6 nanometers, or between 4 and 7 nanometers). The length of the gate metal 112 (i.e., in the x-direction) may depend on the dimensions of the gates 106 and the spacers 134, as illustrated in FIG. 48. As indicated in FIGS. 47 and 49, the gates 106/108 in one trench 107 may extend over the insulating material 128 between that trench 107 and an adjacent trench 107, but may be isolated from their counterpart gates by the intervening insulating material 130 and spacers 134.

[0103] As shown in FIG. 48, the gates 106 and 108 may be alternatingly arranged in the x-direction. During operation of the quantum dot device 100, voltages may be applied to the gates 106/108 to adjust the potential energy in the quantum well stack 146 to create quantum wells of varying depths in which quantum dots 142 may form, as discussed above with reference to the quantum dot device 100 of FIGS. 1-3. Only one quantum dot 142 is labeled with a reference numeral in FIG. 48 for ease of illustration, but five are indicated as dotted circles below each trench 107.

[0104] The quantum well stack 146 of the quantum dot device 100 of FIGS. 47-49 may include doped regions 140 that may serve as a reservoir of charge carriers for the quantum dot device 100, in accordance with any of the embodiments discussed above. The quantum dot devices 100 discussed with reference to FIGS. 47-49 may be used to form electron-type or hole-type quantum dots 142, as discussed above with reference to FIGS. 1-3.

[0105] Conductive vias and lines may make contact with the gates 106/108 of the quantum dot device 100 of FIGS. 47-49, and to the doped regions 140, to enable electrical connection to the gates 106/108 and the doped regions 140 to be made in desired locations. As shown in FIGS. 47-49, the gates 106 may extend both "vertically" and "horizontally" away from the quantum well stack 146, and conductive vias 120 may contact the gates 106 (and are drawn in dashed lines in FIG. 48 to indicate their location behind the plane of the drawing). The conductive vias 120 may extend through the hardmask 116 and the hardmask 118 to contact the gate metal 110 of the gates 106.

The gates 108 may similarly extend away from the quantum well stack 146, and conductive vias 122 may contact the gates 108 (also drawn in dashed lines in FIG. 48 to indicate their location behind the plane of the drawing). The conductive vias 122 may extend through the hardmask 118 to contact the gate metal 112 of the gates 108. Conductive vias 136 may contact the interface material 141 and may thereby make electrical contact with the doped regions 140. The quantum dot device 100 of FIGS. 47-49 may include further conductive vias and/or lines (not shown) to make electrical contact to the gates 106/108 and/or the doped regions 140, as desired. The conductive vias and lines included in a quantum dot device 100 may include any suitable materials, such as copper, tungsten (deposited, e.g., by CVD), or a superconductor (e.g., aluminum, tin, titanium nitride, niobium titanium nitride, tantalum, niobium, or other niobium compounds such as niobium tin and niobium germanium).

[0106] In some embodiments, the quantum dot device 100 of FIGS. 47-49 may include one or more magnet lines 121. For example, a single magnet line 121 is illustrated in FIGS. 47-49, proximate to the trench 107-1. The magnet line(s) 121 of the quantum dot device of FIGS. 47-49 may take the form of any of the embodiments of the magnet lines 121 discussed herein. For example, the magnet line 121 may be formed of a conductive material, and may be used to conduct current pulses that generate magnetic fields to influence the spin states of one or more of the quantum dots 142 that may form in the quantum well stack 146. In some embodiments, the magnet line 121 may conduct a pulse to reset (or "scramble") nuclear and/or quantum dot spins. In some embodiments, the magnet line 121 may conduct a pulse to initialize an electron in a quantum dot in a particular spin state. In some embodiments, the magnet line 121 may conduct current to provide a continuous, oscillating magnetic field to which the spin of a qubit may couple. The magnet line 121 may provide any suitable combination of these embodiments, or any other appropriate functionality.

[0107] In some embodiments, the magnet line 121 of FIGS. 47-49 may be formed of copper. In some embodiments, the magnet line 121 may be formed of a superconductor, such as aluminum. The magnet line 121 illustrated in FIGS. 47-49 is non-coplanar with the trenches 107, and is also non-coplanar with the gates 106/108. In some embodiments, the magnet line 121 may be spaced apart from the gates 106/108 by a distance 167. The distance 167 may take any suitable value (e.g., based on the desired strength of magnetic field interaction with particular quantum dots 142); in some embodiments, the distance 167 may be between 25 nanometers and 1 micron (e.g., between 50 nanometers and 200 nanometers).

[0108] In some embodiments, the magnet line 121 of FIGS. 47-49 may be formed of a magnetic material. For example, a magnetic material (such as cobalt) may be deposited in a trench in the insulating material 130 to provide a permanent magnetic field in the quantum dot device 100.

[0109] The magnet line 121 of FIGS. 47-49 may have any suitable dimensions. For example, the magnet line 121 may have a thickness 169 between 25 and 100 nanometers. The magnet line 121 may have a width 171 between 25 and 100 nanometers. In some embodiments, the width 171 and thickness 169 of a magnet line 121 may be equal to the width and thickness, respectively, of other conductive lines in the quantum dot device 100 (not shown) used to provide electrical interconnects, as known in the art. The magnet line 121 may have a length 173 that may depend on the number and dimensions of the gates 106/108 that are to form quantum dots 142 with which the magnet line 121 is to interact. The magnet line 121 illustrated in FIGS. 47-49 are substantially linear, but this need not be the case; the magnet lines 121 disclosed herein may take any suitable shape. Conductive vias 123 may contact the magnet line 121.

[0110] The conductive vias 120, 122, 136, and 123 may be electrically isolated from each other by an insulating material 130, all of which may take any of the forms discussed above with reference to FIGS. 1-3. The particular arrangement of conductive vias shown in FIGS. 47-49 is simply illustrative, and any electrical routing arrangement may be implemented.

[0111] As discussed above, the structure of the trench 107-1 may be the same as the structure of the trench 107-2; similarly, the construction of gates 106/108 in and around the trench 107-1 may be the same as the construction of gates 106/108 in and around the trench 107-2. The gates 106/108 associated with the trench 107-1 may be mirrored by corresponding gates 106/108 associated with the parallel trench 107-2, and the insulating material 130 may separate the gates 106/108 associated with the different trenches 107-1 and 107-2. In particular, quantum dots 142 formed in the quantum well stack 146 under the trench 107-1 (under the gates 106/108) may have counterpart quantum dots 142 in the quantum well stack 146 under the trench 107-2 (under the corresponding gates 106/108). In some embodiments, the quantum dots 142 under the trench 107-1 may be used as "active" quantum dots in the sense that these quantum dots 142 act as qubits and are controlled (e.g., by voltages applied to the gates 106/108 associated with the trench 107-1) to perform quantum computations. The quantum dots 142 associated with the trench 107-2 may be used as "read" quantum dots in the sense that these quantum dots 142 may sense the quantum state of the quantum dots 142 under the trench 107-1 by detecting the electric field generated by the charge in the quantum dots 142 under the trench 107-1, and may convert the quantum state of the quantum dots 142 under the trench 107-1 into electrical signals that may be detected by the gates 106/108 associated with the trench 107-2. Each quantum dot 142 under the trench 107-1 may be read by its corresponding quantum dot 142 under the trench 107-2. Thus, the quantum dot device 100 enables both quantum computation and the ability to read the results of a quantum computation.

[0112] The quantum dot devices 100 disclosed herein may be manufactured using any suitable techniques. In some embodiments, the manufacture of the quantum dot device 100 of FIGS. 47-49 may begin as described above with reference to FIGS. 4-5; however, instead of forming fins 104 in the quantum well stack 146 of the assembly 202, manufacturing may proceed as illustrated in FIGS. 50-71 (and described below). Although the particular manufacturing operations discussed below with reference to FIGS. 50-71 are illustrated as manufacturing a particular embodiment of the quantum dot device 100, these operations may be applied to manufacture many different embodiments of the quantum dot device 100, as discussed herein. Any of the elements discussed below with reference to FIGS. 50-71 may take the form of any of the embodiments of those elements discussed above (or otherwise disclosed herein).

[0113] FIG. 50 is a cross-sectional view of an assembly 1204 subsequent to providing a layer of gate dielectric 114 on the quantum well stack 146 of the assembly 202 (FIG. 5). In some embodiments, the gate dielectric 114 may be provided by atomic layer deposition (ALD), or any other suitable technique.

[0114] FIG. 51 is a cross-sectional view of an assembly 1206 subsequent to providing an insulating material 128 on the assembly 1204 (FIG. 50). Any suitable material may be used as the insulating material 128 to electrically insulate the trenches 107 from each other, as discussed above. As noted above, in some embodiments, the insulating material 128 may be a dielectric material, such as silicon oxide. In some embodiments, the gate dielectric 114 may not be provided on the quantum well stack 146 before the deposition of the insulating material 128; instead, the insulating material 128 may be provided directly on the quantum well stack 146, and the gate dielectric 114 may be provided in trenches 107 of the insulating material 128 after the trenches 107 are formed (as discussed below with reference to FIG. 52 and FIGS. 60-65).

[0115] FIG. 52 is a cross-sectional view of an assembly 1208 subsequent to forming trenches 107 in the insulating material 128 of the assembly 1206 (FIG. 51). The trenches 107 may extend down to the gate dielectric 114, and may be formed in the assembly 1206 by patterning and then etching the assembly 1206 using any suitable conventional lithographic process known in the art. For example, a hardmask may be provided on the insulating material 128, and a photoresist may be provided on the hardmask; the photoresist may be patterned to identify the areas in which the trenches 107 are to be formed, the hardmask may be etched in accordance with the patterned photoresist, and the insulating material 128 may be etched in accordance with the etched hardmask (after which the remaining hardmask and photoresist may be removed). In some embodiments, a combination of dry and wet etch chemistry may be used to form the trenches 107 in the insulating material 128, and the appropriate chemistry may depend on the materials included in the assembly 1208, as known in

the art. Although the trenches 107 illustrated in FIG. 52 (and other accompanying drawings) are shown as having substantially parallel sidewalls, in some embodiments, the trenches 107 may be tapered, narrowing towards the quantum well stack 146. FIG. 53 is a view of the assembly 1208 taken along the section A-A of FIG. 52, through a trench 107 (while FIG. 52 illustrates the assembly 1208 taken along the section D-D of FIG. 53). FIGS. 54-57 maintain the perspective of FIG. 53.

[0116] As noted above, in some embodiments, the gate dielectric 114 may be provided in the trenches 107 (instead of before the insulating material 128 is initially deposited, as discussed above with reference to FIG. 50). For example, the gate dielectric 114 may be provided in the trenches 107 in the manner discussed below with reference to FIG. 78 (e.g., using ALD). In such embodiments, the gate dielectric 114 may be disposed at the bottom of the trenches 107, and extend up onto the sidewalls of the trenches 107.

[0117] FIG. 54 is a cross-sectional view of an assembly 1210 subsequent to providing a gate metal 110 and a hardmask 116 on the assembly 1208 (FIGS. 52-53). The hardmask 116 may be formed of an electrically insulating material, such as silicon nitride or carbon-doped nitride. The gate metal 110 of the assembly 1210 may fill the trenches 107 and extend over the insulating material 128.

[0118] FIG. 55 is a cross-sectional view of an assembly 1212 subsequent to patterning the hardmask 116 of the assembly 1210 (FIG. 54). The pattern applied to the hardmask 116 may correspond to the locations for the gates 106, as discussed below. The hardmask 116 may be patterned by applying a resist, patterning the resist using lithography, and then etching the hardmask (using dry etching or any appropriate technique).

[0119] FIG. 56 is a cross-sectional view of an assembly 1214 subsequent to etching the assembly 1212 (FIG. 55) to remove the gate metal 110 that is not protected by the patterned hardmask 116 to form the gates 106. The etching of the gate metal 110 may form multiple gates 106 associated with a particular trench 107, and also separate portions of gate metal 110 corresponding to gates 106 associated with different trenches 107 (e.g., as illustrated in FIG. 47). In some embodiments, as illustrated in FIG. 56, the gate dielectric 114 may remain on the quantum well stack 146 after the etched gate metal 110 is etched away; in other embodiments, the gate dielectric 114 may also be etched during the etching of the gate metal 110. Examples of such embodiments are discussed below with reference to FIGS. 76-79.

[0120] FIG. 57 is a cross-sectional view of an assembly 1216 subsequent to providing spacer material 132 on the assembly 1214 (FIG. 56). FIG. 58 is a view of the assembly 1216 taken along the section D-D of FIG. 57, through the region between adjacent gates 106 (while FIG. 57 illustrates the assembly 1216 taken along the section A-A of FIG. 58, along a trench 107). The spacer material 132 may include any of the materials discussed above with reference to the spacers 134, for example,

and may be deposited using any suitable technique. For example, the spacer material 132 may be a nitride material (e.g., silicon nitride) deposited by chemical vapor deposition (CVD) or atomic layer deposition (ALD). As illustrated in FIGS. 57 and 58, the spacer material 132 may be conformally deposited on the assembly 1214.

[0121] FIG. 59 is a cross-sectional view of an assembly 1218 subsequent to providing capping material 133 on the assembly 1216 (FIGS. 57 and 58). FIG. 60 is a view of the assembly 1218 taken along the section D-D of FIG. 59, through the region between adjacent gates 106 (while FIG. 59 illustrates the assembly 1218 taken along the section A-A of FIG. 60, along a trench 107). The capping material 133 may be any suitable material; for example, the capping material 133 may be silicon oxide deposited by CVD or ALD. As illustrated in FIGS. 59 and 60, the capping material 133 may be conformally deposited on the assembly 1216.

[0122] FIG. 61 is a cross-sectional view of an assembly 1220 subsequent to providing a sacrificial material 135 on the assembly 1218 (FIGS. 59 and 60). FIG. 62 is a view of the assembly 1220 taken along the section D-D of FIG. 61, through the region between adjacent gates 106 (while FIG. 61 illustrates the assembly 1220 taken along the section A-A of FIG. 62, through a trench 107). The sacrificial material 135 may be deposited on the assembly 1218 to completely cover the capping material 133, then the sacrificial material 135 may be recessed to expose portions 137 of the capping material 133. In particular, the portions 137 of capping material 133 disposed near the hardmask 116 on the gate metal 110 may not be covered by the sacrificial material 135. As illustrated in FIG. 62, all of the capping material 133 disposed in the region between adjacent gates 106 may be covered by the sacrificial material 135. The recessing of the sacrificial material 135 may be achieved by any etching technique, such as a dry etch. The sacrificial material 135 may be any suitable material, such as a bottom anti-reflective coating (BARC).

[0123] FIG. 63 is a cross-sectional view of an assembly 1222 subsequent to treating the exposed portions 137 of the capping material 133 of the assembly 1220 (FIGS. 61 and 62) to change the etching characteristics of the exposed portions 137 relative to the rest of the capping material 133. FIG. 64 is a view of the assembly 1222 taken along the section D-D of FIG. 63, through the region between adjacent gates 106 (while FIG. 63 illustrates the assembly 1222 taken along the section A-A of FIG. 64, through a trench 107). In some embodiments, this treatment may include performing a high-dose ion implant in which the implant dose is high enough to cause a compositional change in the portions 137 and achieve a desired change in etching characteristics.

[0124] FIG. 65 is a cross-sectional view of an assembly 1224 subsequent to removing the sacrificial material 135 and the unexposed capping material 133 of the assembly 1222 (FIGS. 63 and 64). FIG. 66 is a view of the assembly 1224 taken along the section D-D of FIG. 65, through the region

between adjacent gates 106 (while FIG. 65 illustrates the assembly 1224 taken along the section A-A of FIG. 66, through a trench 107). The sacrificial material 135 may be removed using any suitable technique (e.g., by ashing, followed by a cleaning step), and the untreated capping material 133 may be removed using any suitable technique (e.g., by etching). In embodiments in which the capping material 133 is treated by ion implantation (e.g., as discussed above with reference to FIGS. 63 and 64), a high temperature anneal may be performed to incorporate the implanted ions in the portions 137 of the capping material 133 before removing the untreated capping material 133. The remaining treated capping material 133 in the assembly 1224 may provide capping structures 145 disposed proximate to the "tops" of the gates 106 and extending over the spacer material 132 disposed on the "sides" of the gates 106.

[0125] FIG. 67 is a cross-sectional view of an assembly 1226 subsequent to directionally etching the spacer material 132 of the assembly 1224 (FIGS. 65 and 66) that isn't protected by a capping structure 145, leaving spacer material 132 on the sides and top of the gates 106 (e.g., on the sides and top of the hardmask 116 and the gate metal 110). FIG. 68 is a view of the assembly 1226 taken along the section D-D of FIG. 67, through the region between adjacent gates 106 (while FIG. 67 illustrates the assembly 1226 taken along the section A-A of FIG. 68, through a trench 107). The etching of the spacer material 132 may be an anisotropic etch, etching the spacer material 132 "downward" to remove the spacer material 132 in some of the area between the gates 106 (as illustrated in FIGS. 67 and 68), while leaving the spacer material 135 on the sides and tops of the gates 106. In some embodiments, the anisotropic etch may be a dry etch. FIGS. 69-71 maintain the cross-sectional perspective of FIG. 67.

[0126] FIG. 69 is a cross-sectional view of an assembly 1228 subsequent to removing the capping structures 145 from the assembly 1226 (FIGS. 67 and 68). The capping structures 145 may be removed using any suitable technique (e.g., a wet etch). The spacer material 132 that remains in the assembly 1228 may include spacers 134 disposed on the sides of the gates 106, and portions 139 disposed on the top of the gates 106.

[0127] FIG. 70 is a cross-sectional view of an assembly 1230 subsequent to providing the gate metal 112 on the assembly 1228 (FIG. 69). The gate metal 112 may fill the areas between adjacent ones of the gates 106, and may extend over the tops of the gates 106 and over the spacer material portions 139. The gate metal 112 of the assembly 1230 may fill the trenches 107 (between the gates 106) and extend over the insulating material 128.

[0128] FIG. 71 is a cross-sectional view of an assembly 1232 subsequent to planarizing the assembly 1230 (FIG. 70) to remove the gate metal 112 above the gates 106, as well as to remove the spacer material portions 139 above the hardmask 116. In some embodiments, the assembly 1230 may be

planarized using a chemical mechanical polishing (CMP) technique. The planarizing of the assembly 1230 may also remove some of the hardmask 116, in some embodiments. Some of the remaining gate metal 112 may fill the areas between adjacent ones of the gates 106, while other portions 150 of the remaining gate metal 112 may be located "outside" of the gates 106. The assembly 1232 may be further processed substantially as discussed above with reference to FIGS. 18-33 to form the quantum dot device 100 of FIGS. 47-49.

[0129] In the embodiment of the quantum dot device 100 illustrated in FIGS. 47-49, the magnet line 121 is oriented parallel to the longitudinal axes of the trenches 107. In other embodiments, the magnet line 121 of the quantum dot device 100 of FIGS. 47-49 may not be oriented parallel to the longitudinal axes of the trenches 107; for example, any of the magnet line arrangements discussed above with reference to FIGS. 34-36 may be used.

[0130] Although a single magnet line 121 is illustrated in FIGS. 47-49, multiple magnet lines 121 may be included in that embodiment of the quantum dot device 100 (e.g., multiple magnet lines 121 parallel to the longitudinal axes of the trenches 107). For example, the quantum dot device 100 of FIGS. 47-49 may include a second magnet line 121 proximate to the trench 107-2 in a symmetric manner to the magnet line 121 illustrated proximate to the trench 107-1. In some embodiments, multiple magnet lines 121 may be included in a quantum dot device 100, and these magnet lines 121 may or may not be parallel to one another. For example, in some embodiments, a quantum dot device 100 may include two (or more) magnet lines 121 that are oriented perpendicular to each other.

[0131] As discussed above, in the embodiment illustrated in FIGS. 47-49 (and FIGS. 50-71), there may not be any substantial spacer material between the gate metal 112 and the proximate sidewalls of the trench 107 in the y-direction. In other embodiments, spacers 134 may also be disposed between the gate metal 112 and the sidewalls of the trench 107 in the y-direction. A cross-sectional view of such an embodiment is shown in FIG. 72 (analogous to the cross-sectional view of FIG. 49). To manufacture such a quantum dot device 100, the operations discussed above with reference to FIGS. 59-68 may not be performed; instead, the spacer material 132 of the assembly 1216 of FIGS. 57 and 58 may be anisotropically etched (as discussed with reference to FIGS. 67 and 68) to form the spacers 134 on the sides of the gates 106 and on the sidewalls of the trench 107. FIG. 73 is a cross-sectional view of an assembly 1256 that may be formed by such a process (taking the place of the assembly 1226 of FIG. 68); the view along the section A-A of the assembly 1256 may be similar to FIG. 69, but may not include the spacer material portions 139. The assembly 1256 may be further processed as discussed above with reference to FIGS. 70-71 (or other embodiments discussed herein) to form a quantum dot device 100.

[0132] As noted above, a quantum dot device 100 may include multiple trenches 107 arranged in an array of any desired size. For example, FIG. 74 is a top cross-sectional view, like the view of FIG. 3, of a quantum dot device 100 having multiple trenches 107 arranged in a two-dimensional array. Magnet lines 121 are not depicted in FIG. 74, although they may be included in any desired arrangements. In the particular example illustrated in FIG. 74, the trenches 107 may be arranged in pairs, each pair including an "active" trench 107 and a "read" trench 107, as discussed above. The particular number and arrangement of trenches 107 in FIG. 74 is simply illustrative, and any desired arrangement may be used. Similarly, a quantum dot device 100 may include multiple sets of fins 104 (and accompanying gates, as discussed above with reference to FIGS. 1-3) arranged in a two-dimensional array.

[0133] As noted above, a single trench 107 may include multiple groups of gates 106/108, spaced apart along the trench by a doped region 140. FIG. 75 is a cross-sectional view of an example of such a quantum dot device 100 having multiple groups of gates 180 at least partially disposed in a single trench 107 above a quantum well stack 146, in accordance with various embodiments. Each of the groups 180 may include gates 106/108 (not labeled in FIG. 75 for ease of illustration) that may take the form of any of the embodiments of the gates 106/108 discussed herein. A doped region 140 (and its interface material 141) may be disposed between two adjacent groups 180 (labeled in FIG. 75 as groups 180-1 and 180-2), and may provide a common reservoir for both groups 180. In some embodiments, this "common" doped region 140 may be electrically contacted by a single conductive via 136. The particular number of gates 106/108 illustrated in FIG. 75, and the particular number of groups 180, is simply illustrative, and a trench 107 may include any suitable number of gates 106/108 arranged in any suitable number of groups 180. The quantum dot device 100 of FIG. 75 may also include one or more magnet lines 121, arranged as desired. Similarly, in embodiments of the quantum dot device 100 that include fins, a single fin 104 may include multiple groups of gates 106/108, spaced apart along the fin.

[0134] As discussed above with reference to FIGS. 47-49, in some embodiments in which the gate dielectric 114 is not a layer shared commonly between the gates 108 and 106, but instead is separately deposited on the trench 107 between the spacers 134, the gate dielectric 114 may extend at least partially up the sides of the spacers 134, and the gate metal 112 may extend between the portions of gate dielectric 114 on the spacers 134. FIGS. 76-79 illustrate various alternative stages in the manufacture of such an embodiment of a quantum dot device 100, in accordance with various embodiments. In particular, the operations illustrated in FIGS. 76-79 (as discussed below) may take the place of the operations illustrated in FIGS. 56-70.

[0135] FIG. 76 is a cross-sectional view of an assembly 1258 subsequent to etching the assembly 1212 (FIG. 55) to remove the gate metal 110, and the gate dielectric 114 that is not protected by the patterned hardmask 116, to form the gates 106.

[0136] FIG. 77 is a cross-sectional view of an assembly 1260 subsequent to providing spacers 134 on the sides of the gates 106 (e.g., on the sides of the hardmask 116, the gate metal 110, and the gate dielectric 114) and spacer material portions 139 above the gates 106 (e.g., on the hardmask 116) of the assembly 1258 (FIG. 76). The provision of the spacer material portions 139/spacers 134 may take any of the forms discussed above with reference to FIGS. 57-69 or 72, for example.

[0137] FIG. 78 is a cross-sectional view of an assembly 1262 subsequent to providing a gate dielectric 114 in the trench 107 between the gates 106 of the assembly 1260 (FIG. 77). In some embodiments, the gate dielectric 114 provided between the gates 106 of the assembly 1260 may be formed by atomic layer deposition (ALD) and, as illustrated in FIG. 78, may cover the exposed quantum well stack 146 between the gates 106, and may extend onto the adjacent spacers 134.

[0138] FIG. 79 is a cross-sectional view of an assembly 1264 subsequent to providing the gate metal 112 on the assembly 1262 (FIG. 78). The gate metal 112 may fill the areas in the trench 107 between adjacent ones of the gates 106, and may extend over the tops of the gates 106, as shown. The provision of the gate metal 112 may take any of the forms discussed above with reference to FIG. 70, for example. The assembly 1264 may be further processed as discussed above with reference to FIG. 71, for example.

[0139] In some embodiments, techniques for depositing the gate dielectric 114 and the gate metal 112 for the gates 108 like those illustrated in FIGS. 78-79 may be used to form the gates 108 using alternative manufacturing steps to those illustrated in FIGS. 70-71. For example, the insulating material 130 may be deposited on the assembly 1228 (FIG. 69), the insulating material 130 may be "opened" to expose the areas in which the gates 108 are to be disposed, a layer of gate dielectric 114 and gate metal 112 may be deposited on this structure to fill the openings (e.g., as discussed with reference to FIGS. 78-79), the resulting structure may be polished back to remove the excess gate dielectric 114 and gate metal 112 (e.g., as discussed above with reference to FIG. 71), the insulating material 130 at the sides of the outermost gates 106 may be opened to expose the quantum well stack 147, the exposed quantum well stack 147 may be doped and provided with an interface material 141 (e.g., as discussed above with reference to FIGS. 22-23), and the openings may be filled back in with insulating material 130 to form an assembly like the assembly 236 of FIGS. 24 and 25. Further processing may be performed as described herein.

[0140] In some embodiments, the quantum dot device 100 may be included in a die and coupled to a package substrate to form a quantum dot device package. For example, FIG. 80 is a side cross-

sectional view of a die 302 including the quantum dot device 100 of FIG. 48 and conductive pathway layers 303 disposed thereon, while FIG. 81 is a side cross-sectional view of a quantum dot device package 300 in which the die 302 and another die 350 are coupled to a package substrate 304 (e.g., in a system-on-a-chip (SoC) arrangement). Details of the quantum dot device 100 are omitted from FIG. 81 for economy of illustration. As noted above, the particular quantum dot device 100 illustrated in FIGS. 80 and 81 may take a form similar to the embodiments illustrated in FIGS. 2 and 48, but any of the quantum dot devices 100 disclosed herein may be included in a die (e.g., the die 302) and coupled to a package substrate (e.g., the package substrate 304). In particular, any number of fins 104 or trenches 107, gates 106/108, doped regions 140, magnet lines 121, and other components discussed herein with reference to various embodiments of the quantum dot device 100 may be included in the die 302.

[0141] The die 302 may include a first face 320 and an opposing second face 322. The base 102 may be proximate to the second face 322, and conductive pathways 315 from various components of the quantum dot device 100 may extend to conductive contacts 365 disposed at the first face 320. The conductive pathways 315 may include conductive vias, conductive lines, and/or any combination of conductive vias and lines. For example, FIG. 80 illustrates an embodiment in which one conductive pathway 315 (extending between a magnet line 121 and associated conductive contact 365) includes a conductive via 123, a conductive line 393, a conductive via 398, and a conductive line 396. More or fewer structures may be included in the conductive pathways 315, and analogous conductive pathways 315 may be provided between ones of the conductive contacts 365 and the gates 106/108, doped regions 140, or other components of the quantum dot device 100. In some embodiments, conductive lines of the die 302 (and the package substrate 304, discussed below) may extend into and out of the plane of the drawing, providing conductive pathways to route electrical signals to and/or from various elements in the die 302.

[0142] The conductive vias and/or lines that provide the conductive pathways 315 in the die 302 may be formed using any suitable techniques. Examples of such techniques may include subtractive fabrication techniques, additive or semi-additive fabrication techniques, single Damascene fabrication techniques, dual Damascene fabrication techniques, or any other suitable technique. In some embodiments, layers of oxide material 390 and layers of nitride material 391 may insulate various structures in the conductive pathways 315 from proximate structures, and/or may serve as etch stops during fabrication. In some embodiments, an adhesion layer (not shown) may be disposed between conductive material and proximate insulating material of the die 302 to improve mechanical adhesion between the conductive material and the insulating material.

[0143] The gates 106/108, the doped regions 140, and the quantum well stack 146 (as well as the proximate conductive vias/lines) may be referred to as part of the "device layer" of the quantum dot device 100. The conductive lines 393 may be referred to as a Metal 1 or "M1" interconnect layer, and may couple the structures in the device layer to other interconnect structures. The conductive vias 398 and the conductive lines 396 may be referred to as a Metal 2 or "M2" interconnect layer, and may be formed directly on the M1 interconnect layer.

[0144] A solder resist material 367 may be disposed around the conductive contacts 365, and in some embodiments may extend onto the conductive contacts 365. The solder resist material 367 may be a polyimide or similar material, or may be any appropriate type of packaging solder resist material. In some embodiments, the solder resist material 367 may be a liquid or dry film material including photoimageable polymers. In some embodiments, the solder resist material 367 may be non-photoimageable (and openings therein may be formed using laser drilling or masked etch techniques). The conductive contacts 365 may provide the contacts to couple other components (e.g., a package substrate 304, as discussed below, or another component) to the conductive pathways 315 in the quantum dot device 100, and may be formed of any suitable conductive material (e.g., a superconducting material). For example, solder bonds may be formed on the one or more conductive contacts 365 to mechanically and/or electrically couple the die 302 with another component (e.g., a circuit board), as discussed below. The conductive contacts 365 illustrated in FIG. 80 take the form of bond pads, but other first level interconnect structures may be used (e.g., posts) to route electrical signals to/from the die 302, as discussed below.

[0145] The combination of the conductive pathways and the proximate insulating material (e.g., the insulating material 130, the oxide material 390, and the nitride material 391) in the die 302 may provide an interlayer dielectric (ILD) stack of the die 302. As noted above, interconnect structures may be arranged within the quantum dot device 100 to route electrical signals according to a wide variety of designs (in particular, the arrangement is not limited to the particular configuration of interconnect structures depicted in FIG. 80 or any of the other accompanying figures, and may include more or fewer interconnect structures). During operation of the quantum dot device 100, electrical signals (such as power and/or input/output (I/O) signals) may be routed to and/or from the gates 106/108, the magnet line(s) 121, and/or the doped regions 140 (and/or other components) of the quantum dot device 100 through the interconnects provided by conductive vias and/or lines, and through the conductive pathways of the package substrate 304 (discussed below).

[0146] Example superconducting materials that may be used for the structures in the conductive pathways 313, 317, 319 (discussed below), and 315, and/or conductive contacts of the die 302 and/or the package substrate 304, may include aluminum, niobium, tin, titanium, osmium, zinc,

molybdenum, tantalum, vanadium, or composites of such materials (e.g., niobium-titanium, niobium-aluminum, or niobium-tin). In some embodiments, the conductive contacts 365, 379, and/or 399 may include aluminum, and the first level interconnects 306 and/or the second level interconnects 308 may include an indium-based solder.

[0147] As noted above, the quantum dot device package 300 of FIG. 81 may include a die 302 (including one or more quantum dot devices 100) and a die 350. As discussed in detail below, the quantum dot device package 300 may include electrical pathways between the die 302 and the die 350 so that the dies 302 and 350 may communicate during operation. In some embodiments, the die 350 may be a non-quantum logic device that may provide support or control functionality for the quantum dot device(s) 100 of the die 320. For example, as discussed further below, in some embodiments, the die 350 may include a switching matrix to control the writing and reading of data from the die 320 (e.g., using any known word line/bit line or other addressing architecture). In some embodiments, the die 350 may control the voltages (e.g., microwave pulses) applied to the gates 106/108, and/or the doped regions 140, of the quantum dot device(s) 100 included in the die 302. In some embodiments, the die 350 may include magnet line control logic to provide microwave pulses to the magnet line(s) 121 of the quantum dot device(s) 100 in the die 302. The die 350 may include any desired control circuitry to support operation of the die 302. By including this control circuitry in a separate die, the manufacture of the die 302 may be simplified and focused on the needs of the quantum computations performed by the quantum dot device(s) 100, and conventional manufacturing and design processes for control logic (e.g., switching array logic) may be used to form the die 350.

[0148] Although a singular "die 350" is illustrated in FIG. 81 and discussed herein, the functionality provided by the die 350 may, in some embodiments, be distributed across multiple dies 350 (e.g., multiple dies coupled to the package substrate 304, or otherwise sharing a common support with the die 302). Similarly, one or more dies providing the functionality of the die 350 may support one or more dies providing the functionality of the die 302; for example, the quantum dot device package 300 may include multiple dies having one or more quantum dot devices 100, and a die 350 may communicate with one or more such "quantum dot device dies."

[0149] The die 350 may take any of the forms discussed below with reference to the non-quantum processing device 2028 of FIG. 87. Mechanisms by which the control logic of the die 350 may control operation of the die 302 may be take the form of an entirely hardware embodiment or an embodiment combining software and hardware aspects. For example, the die 350 may implement an algorithm executed by one or more processing units, e.g. one or more microprocessors. In various embodiments, aspects of the present disclosure may take the form of a computer program

product embodied in one or more computer readable medium(s), preferably non-transitory, having computer readable program code embodied (e.g., stored) in or coupled to the die 350. In various embodiments, such a computer program may, for example, be downloaded (updated) to the die 350 (or attendant memory) or be stored upon manufacturing of the die 350. In some embodiments, the die 350 may include at least one processor and at least one memory element, along with any other suitable hardware and/or software to enable its intended functionality of controlling operation of the die 302 as described herein. A processor of the die 350 may execute software or an algorithm to perform the activities discussed herein. A processor of the die 350 may be communicatively coupled to other system elements via one or more interconnects or buses (e.g., through one or more conductive pathways 319). Such a processor may include any combination of hardware, software, or firmware providing programmable logic, including by way of non-limiting example, a microprocessor, a digital signal processor (DSP), a field-programmable gate array (FPGA), a programmable logic array (PLA), an application specific integrated circuit (ASIC), or a virtual machine processor. The processor of the die 350 may be communicatively coupled to the memory element of the die 350, for example, in a direct-memory access (DMA) configuration. A memory element of the die 350 may include any suitable volatile or non-volatile memory technology, including double data rate (DDR) random access memory (RAM), synchronous RAM (SRAM), dynamic RAM (DRAM), flash, read-only memory (ROM), optical media, virtual memory regions, magnetic or tape memory, or any other suitable technology. In some embodiments, the memory element and the processor of the "die 350" may themselves be provided by separate physical dies that are in electrical communication. The information being tracked or sent to the die 350 could be provided in any database, register, control list, cache, or storage structure, all of which can be referenced at any suitable timeframe. The die 350 can further include suitable interfaces for receiving, transmitting, and/or otherwise communicating data or information in a network environment (e.g., via the conductive pathways 319).

[0150] In some embodiments, the die 350 may be configured to apply appropriate voltages to any one of the gates 106/108 (acting as, e.g., plunger, barrier gates, and/or accumulation gates) in order to initialize and manipulate the quantum dots 142, as discussed above. For example, by controlling the voltage applied to a gate 106/108 acting as a plunger gate, the die 350 may modulate the electric field underneath that gate to create an energy valley between the tunnel barriers created by adjacent barrier gates. In another example, by controlling the voltage applied to a gate 106/108 acting as a barrier gate, the die 350 may change the height of the tunnel barrier. When a barrier gate is used to set a tunnel barrier between two plunger gates, the barrier gate may be used to transfer charge carriers between quantum dots 142 that may be formed under these plunger gates. When a barrier gate is used to set a tunnel barrier between a plunger gate and an accumulation

gate, the barrier gate may be used to transfer charge carriers in and out of the quantum dot array via the accumulation gate. The term "accumulation gate" may refer to a gate used to form a 2DEG in an area that is between the area where the quantum dots 142 may be formed and a charge carrier reservoir (e.g., the doped regions 140). Changing the voltage applied to the accumulation gate may allow the die 350 to control the number of charge carriers in the area under the accumulation gate. For example, changing the voltage applied to the accumulation gate may reduce the number of charge carriers in the area under the gate so that single charge carriers can be transferred from the reservoir into the quantum well layer 152, and vice versa.

[0151] As noted above, the die 350 may provide electrical signals to control spins of charge carriers in quantum dots 142 of the quantum dot device(s) 100 of the die 302 by controlling a magnetic field generated by one or more magnet line(s) 121. In this manner, the die 350 may initialize and manipulate spins of the charge carriers in the quantum dots 142 to implement qubit operations. If the magnetic field for a die 302 is generated by a microwave transmission line, then the die 350 may set/manipulate the spins of the charge carriers by applying appropriate pulse sequences to manipulate spin precession. Alternatively, the magnetic field for a quantum dot device 100 of the die 302 may be generated by a magnet with one or more pulsed gates; the die 350 may apply the pulses to these gates.

[0152] In some embodiments, the die 350 may be configured to determine the values of the control signals applied to the elements of the die 302 (e.g. determine the voltages to be applied to the various gates 106/108) to achieve desired quantum operations (communicated to the die 350 through the package substrate 304 via the conductive pathways 319). In other embodiments, the die 350 may be preprogrammed with at least some of the control parameters (e.g. with the values for the voltages to be applied to the various gates 106/108) during the initialization of the die 350.

[0153] In the quantum dot device package 300 (FIG. 81), first level interconnects 306 may be disposed between the first face 320 of the die 302 and the second face 326 of a package substrate 304. Having first level interconnects 306 disposed between the first face 320 of the die 302 and the second face 326 of the package substrate 304 (e.g., using solder bumps as part of flip chip packaging techniques) may enable the quantum dot device package 300 to achieve a smaller footprint and higher die-to-package-substrate connection density than could be achieved using conventional wirebond techniques (in which conductive contacts between the die 302 and the package substrate 304 are constrained to be located on the periphery of the die 302). For example, a die 302 having a square first face 320 with side length N may be able to form only 4N wirebond interconnects to the package substrate 304, versus N^2 flip chip interconnects (utilizing the entire "full field" surface area of the first face 320). Additionally, in some applications, wirebond interconnects may generate

unacceptable amounts of heat that may damage or otherwise interfere with the performance of the quantum dot device 100. Using solder bumps as the first level interconnects 306 may enable the quantum dot device package 300 to have much lower parasitic inductance relative to using wirebonds to couple the die 302 and the package substrate 304, which may result in an improvement in signal integrity for high-speed signals communicated between the die 302 and the package substrate 304. Similarly, first level interconnects 309 may be disposed between conductive contacts 371 of the die 350 and conductive contacts 379 at the second face 326 of the package substrate 304, as shown, to couple electronic components (not shown) in the die 350 to conductive pathways in the package substrate 304.

[0154] The package substrate 304 may include a first face 324 and an opposing second face 326. Conductive contacts 399 may be disposed at the first face 324, and conductive contacts 379 may be disposed at the second face 326. Solder resist material 314 may be disposed around the conductive contacts 379, and solder resist material 312 may be disposed around the conductive contacts 399; the solder resist materials 314 and 312 may take any of the forms discussed above with reference to the solder resist material 367. In some embodiments, the solder resist material 312 and/or the solder resist material 314 may be omitted. Conductive pathways may extend through the insulating material 310 between the first face 324 and the second face 326 of the package substrate 304, electrically coupling various ones of the conductive contacts 399 to various ones of the conductive contacts 379, in any desired manner. The insulating material 310 may be a dielectric material (e.g., an ILD), and may take the form of any of the embodiments of the insulating material 130 disclosed herein, for example. The conductive pathways may include one or more conductive vias 395 and/or one or more conductive lines 397, for example.

[0155] For example, the package substrate 304 may include one or more conductive pathways 313 to electrically couple the die 302 to conductive contacts 399 on the first face 324 of the package substrate 304; these conductive pathways 313 may be used to allow the die 302 to electrically communicate with a circuit component to which the quantum dot device package 300 is coupled (e.g., a circuit board or interposer, as discussed below). The package substrate 304 may include one or more conductive pathways 319 to electrically couple the die 350 to conductive contacts 399 on the first face 324 of the package substrate 304; these conductive pathways 319 may be used to allow the die 350 to electrically communicate with a circuit component to which the quantum dot device package 300 is coupled (e.g., a circuit board or interposer, as discussed below).

[0156] The package substrate 304 may include one or more conductive pathways 317 to electrically couple the die 302 to the die 350 through the package substrate 304. In particular, the package substrate 304 may include conductive pathways 317 that couple different ones of the conductive

contacts 379 on the second face 326 of the package substrate 304 so that, when the die 302 and the die 350 are coupled to these different conductive contacts 379, the die 302 and the die 350 may communicate through the package substrate 304. Although the die 302 and the die 350 are illustrated in FIG. 81 as being disposed on the same second face 326 of the package substrate 304, in some embodiments, the die 302 and the die 350 may be disposed on different faces of the package substrate 304 (e.g., one on the first face 324 and one on the second face 326), and may communicate via one or more conductive pathways 317.

[0157] In some embodiments, the conductive pathways 317 may be microwave transmission lines. Microwave transmission lines may be structured for the effective transmission of microwave signals, and may take the form of any microwave transmission lines known in the art. For example, a conductive pathway 317 may be a coplanar waveguide, a stripline, a microstrip line, or an inverted microstrip line. The die 350 may provide microwave pulses along the conductive pathways 317 to the die 302 to provide electron spin resonance (ESR) pulses to the quantum dot device(s) 100 to manipulate the spin states of the quantum dots 142 that form therein. In some embodiments, the die 350 may generate a microwave pulse that is transmitted over a conductive pathway 317 and induces a magnetic field in the magnet line(s) 121 of a quantum dot device 100 and causes a transition between the spin-up and spin-down states of a quantum dot 142. In some embodiments, the die 350 may generate a microwave pulse that is transmitted over a conductive pathway 317 and induces a magnetic field in a gate 106/108 to cause a transition between the spin-up and spin-down states of a quantum dot 142. The die 350 may enable any such embodiments, or any combination of such embodiments.

[0158] The die 350 may provide any suitable control signals to the die 302 to enable operation of the quantum dot device(s) 100 included in the die 302. For example, the die 350 may provide voltages (through the conductive pathways 317) to the gates 106/108, and thereby tune the energy profile in the quantum well stack 146.

[0159] In some embodiments, the quantum dot device package 300 may be a cored package, one in which the package substrate 304 is built on a carrier material (not shown) that remains in the package substrate 304. In such embodiments, the carrier material may be a dielectric material that is part of the insulating material 310; laser vias or other through-holes may be made through the carrier material to allow conductive pathways 313 and/or 319 to extend between the first face 324 and the second face 326.

[0160] In some embodiments, the package substrate 304 may be or may otherwise include a silicon interposer, and the conductive pathways 313 and/or 319 may be through-silicon vias. Silicon may have a desirably low coefficient of thermal expansion compared with other dielectric materials that

may be used for the insulating material 310, and thus may limit the degree to which the package substrate 304 expands and contracts during temperature changes relative to such other materials (e.g., polymers having higher coefficients of thermal expansion). A silicon interposer may also help the package substrate 304 achieve a desirably small line width and maintain high connection density to the die 302 and/or the die 350.

[0161] Limiting differential expansion and contraction may help preserve the mechanical and electrical integrity of the quantum dot device package 300 as the quantum dot device package 300 is fabricated (and exposed to higher temperatures) and used in a cooled environment (and exposed to lower temperatures). In some embodiments, thermal expansion and contraction in the package substrate 304 may be managed by maintaining an approximately uniform density of the conductive material in the package substrate 304 (so that different portions of the package substrate 304 expand and contract uniformly), using reinforced dielectric materials as the insulating material 310 (e.g., dielectric materials with silicon dioxide fillers), or utilizing stiffer materials as the insulating material 310 (e.g., a prepreg material including glass cloth fibers). In some embodiments, the die 350 may be formed of semiconductor materials or compound semiconductor materials (e.g., III-V materials) to enable higher efficiency amplification and signal generation to minimize the heat generated during operation and reduce the impact on the quantum operations of the die 302. In some embodiments, the metallization in the die 350 may use superconducting materials (e.g., titanium nitride, niobium, niobium nitride, and niobium titanium nitride) to minimize heating.

[0162] The conductive contacts 365 of the die 302 may be electrically coupled to the conductive contacts 379 of the package substrate 304 via the first level interconnects 306, and the conductive contacts 371 of the die 350 may be electrically coupled to the conductive contacts 379 of the package substrate 304 via the first level interconnects 309. In some embodiments, the first level interconnects 306/309 may include solder bumps or balls (as illustrated in FIG. 81); for example, the first level interconnects 306/309 may be flip chip (or controlled collapse chip connection, "C4") bumps disposed initially on the die 302/die 350 or on the package substrate 304. Second level interconnects 308 (e.g., solder balls or other types of interconnects) may couple the conductive contacts 399 on the first face 324 of the package substrate 304 to another component, such as a circuit board (not shown). Examples of arrangements of electronics packages that may include an embodiment of the quantum dot device package 300 are discussed below with reference to FIG. 83. The die 302 and/or the die 350 may be brought in contact with the package substrate 304 using a pick-and-place apparatus, for example, and a reflow or thermal compression bonding operation may be used to couple the die 302 and/or the die 350 to the package substrate 304 via the first level interconnects 306 and/or the first level interconnects 309, respectively.

[0163] The conductive contacts 365, 371, 379, and/or 399 may include multiple layers of material that may be selected to serve different purposes. In some embodiments, the conductive contacts 365, 371, 379, and/or 399 may be formed of aluminum, and may include a layer of gold (e.g., with a thickness of less than 1 micron) between the aluminum and the adjacent interconnect to limit the oxidation of the surface of the contacts and improve the adhesion with adjacent solder. In some embodiments, the conductive contacts 365, 371, 379, and/or 399 may be formed of aluminum, and may include a layer of a barrier metal such as nickel, as well as a layer of gold, wherein the layer of barrier metal is disposed between the aluminum and the layer of gold, and the layer of gold is disposed between the barrier metal and the adjacent interconnect. In such embodiments, the gold may protect the barrier metal surface from oxidation before assembly, and the barrier metal may limit the diffusion of solder from the adjacent interconnects into the aluminum.

[0164] In some embodiments, the structures and materials in the quantum dot device 100 may be damaged if the quantum dot device 100 is exposed to the high temperatures that are common in conventional integrated circuit processing (e.g., greater than 100 degrees Celsius, or greater than 200 degrees Celsius). In particular, in embodiments in which the first level interconnects 306/309 include solder, the solder may be a low-temperature solder (e.g., a solder having a melting point below 100 degrees Celsius) so that it can be melted to couple the conductive contacts 365/371 and the conductive contacts 379 without having to expose the die 302 to higher temperatures and risk damaging the quantum dot device 100. Examples of solders that may be suitable include indium-based solders (e.g., solders including indium alloys). When low-temperature solders are used, however, these solders may not be fully solid during handling of the quantum dot device package 300 (e.g., at room temperature or temperatures between room temperature and 100 degrees Celsius), and thus the solder of the first level interconnects 306/309 alone may not reliably mechanically couple the die 302/die 350 and the package substrate 304 (and thus may not reliably electrically couple the die 302/die 350 and the package substrate 304). In some such embodiments, the quantum dot device package 300 may further include a mechanical stabilizer to maintain mechanical coupling between the die 302/die 350 and the package substrate 304, even when solder of the first level interconnects 306/309 is not solid. Examples of mechanical stabilizers may include an underfill material disposed between the die 302/die 350 and the package substrate 304, a corner glue disposed between the die 302/die 350 and the package substrate 304, an overmold material disposed around the die 302/die 350 on the package substrate 304, and/or a mechanical frame to secure the die 302/die 350 and the package substrate 304.

[0165] In some embodiments of the quantum dot device package 300, the die 350 may not be included in the package 300; instead, the die 350 may be electrically coupled to the die 302 through

another type of common physical support. For example, the die 350 may be separately packaged from the die 302 (e.g., the die 350 may be mounted to its own package substrate), and the two packages may be coupled together through an interposer, a printed circuit board, a bridge, a package-on-package arrangement, or in any other manner. Examples of device assemblies that may include the die 302 and the die 350 in various arrangements are discussed below with reference to FIG. 83.

[0166] FIGS. 82A-B are top views of a wafer 450 and dies 452 that may be formed from the wafer 450; the dies 452 may be included in any of the quantum dot device packages (e.g., the quantum dot device package 300) disclosed herein. The wafer 450 may include semiconductor material and may include one or more dies 452 having conventional and quantum dot device elements formed on a surface of the wafer 450. Each of the dies 452 may be a repeating unit of a semiconductor product that includes any suitable conventional and/or quantum dot device. After the fabrication of the semiconductor product is complete, the wafer 450 may undergo a singulation process in which each of the dies 452 is separated from one another to provide discrete "chips" of the semiconductor product. A die 452 may include one or more quantum dot devices 100 and/or supporting circuitry to route electrical signals to the quantum dot devices 100 (e.g., interconnects including conductive vias and lines), as well as any other IC components. In some embodiments, the wafer 450 or the die 452 may include a memory device (e.g., a static random access memory (SRAM) device), a logic device (e.g., AND, OR, NAND, or NOR gate), or any other suitable circuit element. Multiple ones of these devices may be combined on a single die 452. For example, a memory array formed by multiple memory devices may be formed on a same die 452 as a processing device (e.g., the processing device 2002 of FIG. 74) or other logic that is configured to store information in the memory devices or execute instructions stored in the memory array.

[0167] FIG. 83 is a cross-sectional side view of a device assembly 400 that may include any of the embodiments of the quantum dot device packages 300 disclosed herein. The device assembly 400 includes a number of components disposed on a circuit board 402. The device assembly 400 may include components disposed on a first face 440 of the circuit board 402 and an opposing second face 442 of the circuit board 402; generally, components may be disposed on one or both faces 440 and 442.

[0168] In some embodiments, the circuit board 402 may be a printed circuit board (PCB) including multiple metal layers separated from one another by layers of dielectric material and interconnected by electrically conductive vias. Any one or more of the metal layers may be formed in a desired circuit pattern to route electrical signals (optionally in conjunction with other metal layers) between the components coupled to the circuit board 402. In other embodiments, the circuit board 402 may

be a package substrate or flexible board. In some embodiments, the die 302 and the die 350 (FIG. 81) may be separately packaged and coupled together via the circuit board 402 (e.g., the conductive pathways 317 may run through the circuit board 402).

[0169] The device assembly 400 illustrated in FIG. 83 includes a package-on-interposer structure 436 coupled to the first face 440 of the circuit board 402 by coupling components 416. The coupling components 416 may electrically and mechanically couple the package-on-interposer structure 436 to the circuit board 402, and may include solder balls (as shown in FIG. 81), male and female portions of a socket, an adhesive, an underfill material, and/or any other suitable electrical and/or mechanical coupling structure.

[0170] The package-on-interposer structure 436 may include a package 420 coupled to an interposer 404 by coupling components 418. The coupling components 418 may take any suitable form for the application, such as the forms discussed above with reference to the coupling components 416. For example, the coupling components 418 may be the second level interconnects 308. Although a single package 420 is shown in FIG. 83, multiple packages may be coupled to the interposer 404; indeed, additional interposers may be coupled to the interposer 404. The interposer 404 may provide an intervening substrate used to bridge the circuit board 402 and the package 420. The package 420 may be a quantum dot device package 300 or may be a conventional IC package, for example. In some embodiments, the package 420 may take the form of any of the embodiments of the quantum dot device package 300 disclosed herein, and may include a quantum dot device die 302 coupled to a package substrate 304 (e.g., by flip chip connections). Generally, the interposer 404 may spread a connection to a wider pitch or reroute a connection to a different connection. For example, the interposer 404 may couple the package 420 (e.g., a die) to a ball grid array (BGA) of the coupling components 416 for coupling to the circuit board 402. In the embodiment illustrated in FIG. 83, the package 420 and the circuit board 402 are attached to opposing sides of the interposer 404; in other embodiments, the package 420 and the circuit board 402 may be attached to a same side of the interposer 404. In some embodiments, three or more components may be interconnected by way of the interposer 404. In some embodiments, a quantum dot device package 300 including the die 302 and the die 350 (FIG. 81) may be one of the packages disposed on an interposer like the interposer 404. In some embodiments, the die 302 and the die 350 (FIG. 81) may be separately packaged and coupled together via the interposer 404 (e.g., the conductive pathways 317 may run through the interposer 404).

[0171] The interposer 404 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In some embodiments, the interposer 404 may be formed of alternate rigid or flexible materials that may include the same materials

described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials. The interposer 404 may include metal interconnects 408 and vias 410, including but not limited to through-silicon vias (TSVs) 406. The interposer 404 may further include embedded devices 414, including both passive and active devices. Such devices may include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, electrostatic discharge (ESD) devices, and memory devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and microelectromechanical systems (MEMS) devices may also be formed on the interposer 404. The package-on-interposer structure 436 may take the form of any of the package-on-interposer structures known in the art.

[0172] The device assembly 400 may include a package 424 coupled to the first face 440 of the circuit board 402 by coupling components 422. The coupling components 422 may take the form of any of the embodiments discussed above with reference to the coupling components 416, and the package 424 may take the form of any of the embodiments discussed above with reference to the package 420. The package 424 may be a quantum dot device package 300 (e.g., including the die 302 and the die 350, or just the die 302) or may be a conventional IC package, for example. In some embodiments, the package 424 may take the form of any of the embodiments of the quantum dot device package 300 disclosed herein, and may include a quantum dot device die 302 coupled to a package substrate 304 (e.g., by flip chip connections).

[0173] The device assembly 400 illustrated in FIG. 83 includes a package-on-package structure 434 coupled to the second face 442 of the circuit board 402 by coupling components 428. The package-on-package structure 434 may include a package 426 and a package 432 coupled together by coupling components 430 such that the package 426 is disposed between the circuit board 402 and the package 432. The coupling components 428 and 430 may take the form of any of the embodiments of the coupling components 416 discussed above, and the packages 426 and 432 may take the form of any of the embodiments of the package 420 discussed above. Each of the packages 426 and 432 may be a quantum dot device package 300 or may be a conventional IC package, for example. In some embodiments, one or both of the packages 426 and 432 may take the form of any of the embodiments of the quantum dot device package 300 disclosed herein, and may include a die 302 coupled to a package substrate 304 (e.g., by flip chip connections). In some embodiments, a quantum dot device package 300 including the die 302 and the die 350 (FIG. 81) may be one of the packages in a package-on-package structure like the package-on-package structure 434. In some embodiments, the die 302 and the die 350 (FIG. 81) may be separately packaged and coupled together using a package-on-package structure like the package-on-package structure 434 (e.g., the

conductive pathways 317 may run through a package substrate of one or both of the packages of the dies 302 and 350).

[0174] As noted above, any suitable techniques may be used to manufacture the quantum dot devices 100 disclosed herein. FIG. 84 is a flow diagram of an illustrative method 1000 of manufacturing a quantum dot device, in accordance with various embodiments. Although the operations discussed below with reference to the method 1000 are illustrated in a particular order and depicted once each, these operations may be repeated or performed in a different order (e.g., in parallel), as suitable. Additionally, various operations may be omitted, as suitable. Various operations of the method 1000 may be illustrated with reference to one or more of the embodiments discussed above, but the method 1000 may be used to manufacture any suitable quantum dot device (including any suitable ones of the embodiments disclosed herein).

[0175] At 1002, a substrate may be provided. The substrate may include one or more conductive pathways between a first set of contacts and a second set of contacts. For example, a package substrate 304 (or an interposer 404, or a circuit board 402, etc.) may include one or more conductive pathways 317 between conductive contacts 379 that are to couple to a die 302 and one or more conductive contacts 379 that are to couple to a die 350 (e.g., as discussed above with reference to FIG. 81).

[0176] At 1004, a quantum device die may be coupled to the first set of contacts such that the quantum device die is disposed on the substrate. For example, a die 302 may be coupled to some of the conductive contacts 379 of a package substrate 304 (or an interposer 404, or a circuit board 402, etc.) by first level interconnects 306.

[0177] At 1006, one or more control dies may be coupled to the second set of contacts such that the one or more control dies are disposed on the substrate. The control dies may be configured to provide voltages to one or more components of the quantum device die through the one or more conductive pathways. For example, a die 350 may be coupled to some of the conductive contacts 379 of a package substrate 304 (or an interposer 404, or a circuit board 402, etc.) by first level interconnects 309; the die 350 and the die 302 may be in electrical communication through the conductive pathways 317.

[0178] A number of techniques are disclosed herein for operating a quantum dot device 100. FIGS. 85-86 are flow diagrams of particular illustrative methods 1020 and 1040, respectively, of operating a quantum dot device, in accordance with various embodiments. Although the operations discussed below with reference to the methods 1020 and 1040 are illustrated in a particular order and depicted once each, these operations may be repeated or performed in a different order (e.g., in parallel), as suitable. Additionally, various operations may be omitted, as suitable. Various

operations of the methods 1020 and 1040 may be illustrated with reference to one or more of the embodiments discussed above, but the methods 1020 and 1040 may be used to operate any suitable quantum dot device (including any suitable ones of the embodiments disclosed herein).

[0179] Turning to the method 1020 of FIG. 85, at 1022, a control circuitry die may provide one or more voltages to a quantum device die through a substrate on which the quantum device die and the control circuitry die are disposed. For example, a die 350 may provide one or more voltages to a gate 106/108, magnet line 121, and/or doped region 140 of a quantum dot device 100 included in a die 302; the die 350 and the die 302 may be coupled to a common package substrate 304, interposer 404, circuit board 402, or other substrate.

[0180] At 1024, the state of qubits in the quantum device die may change at least partially in response to the one or more voltages applied at 1022. For example, the spin state of one or more quantum-dot-based qubits (e.g., the spin state of one or more quantum dots 142) may change in response to changes in the voltages applied to the gates 106/108, magnet line 121, and/or doped regions 140 (e.g., because the states are directly changed, or changed as the result of quantum interaction with other quantum dots 142).

[0181] Turning to the method 1040 of FIG. 86, at 1042, an electrical signal may be provided, by a control die, to a first gate of a quantum dot device as part of causing a first quantum dot to form in a quantum well stack under the first gate. For example, a voltage may be applied, by a die 350, to a gate 108-1 of a quantum dot device 100 included in a die 302 as part of causing a first quantum dot 142 to form in the quantum well stack 146 below the gate 108-1.

[0182] At 1044, an electrical signal may be provided, by the control die, to a second gate disposed of the quantum dot device as part of causing a second quantum dot to form in the quantum well stack under the second gate. For example, a voltage may be applied, by the die 350, to the gate 108-2 of the quantum dot device 100 included in the die 302 as part of causing a second quantum dot 142 to form in the quantum well stack 146 below the gate 108-2.

[0183] At 1046, an electrical signal may be provided, by the control die, to a third gate of the quantum dot device as part of (1) causing a third quantum dot to form in the quantum well stack under the third gate or (2) providing a potential barrier between the first quantum dot and the second quantum dot. For example, a voltage may be applied, by the die 350, to the gate 106-2 of the quantum dot device 100 included in the die 302 as part of (1) causing a third quantum dot 142 to form in the quantum well stack 146 below the gate 106-2 (e.g., when the gate 106-2 acts as a "plunger" gate) or (2) providing a potential barrier between the first quantum dot (under the gate 108-1) and the second quantum dot (under the gate 108-2) (e.g., when the gate 106-2 acts as a "barrier" gate).

[0184] FIG. 87 is a block diagram of an example quantum computing device 2000 that may include any of the quantum dot devices disclosed herein. A number of components are illustrated in FIG. 87 as included in the quantum computing device 2000, but any one or more of these components may be omitted or duplicated, as suitable for the application. In some embodiments, some or all of the components included in the quantum computing device 2000 may be attached to one or more printed circuit boards (e.g., a motherboard). In some embodiments, various ones of these components may be fabricated onto a single system-on-a-chip (SoC) die. Additionally, in various embodiments, the quantum computing device 2000 may not include one or more of the components illustrated in FIG. 87, but the quantum computing device 2000 may include interface circuitry for coupling to the one or more components. For example, the quantum computing device 2000 may not include a display device 2006, but may include display device interface circuitry (e.g., a connector and driver circuitry) to which a display device 2006 may be coupled. In another set of examples, the quantum computing device 2000 may not include an audio input device 2024 or an audio output device 2008, but may include audio input or output device interface circuitry (e.g., connectors and supporting circuitry) to which an audio input device 2024 or audio output device 2008 may be coupled.

[0185] The quantum computing device 2000 may include a processing device 2002 (e.g., one or more processing devices). As used herein, the term "processing device" or "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory. The processing device 2002 may include a quantum processing device 2026 (e.g., one or more quantum processing devices), and a non-quantum processing device 2028 (e.g., one or more non-quantum processing devices). The quantum processing device 2026 may include one or more of the quantum dot devices 100 disclosed herein, and may perform data processing by performing operations on the quantum dots that may be generated in the quantum dot devices 100, and monitoring the result of those operations. For example, as discussed above, different quantum dots may be allowed to interact, the quantum states of different quantum dots may be set or transformed, and the quantum states of quantum dots may be read (e.g., by another quantum dot). The quantum processing device 2026 may be a universal quantum processor, or specialized quantum processor configured to run one or more particular quantum algorithms. In some embodiments, the quantum processing device 2026 may execute algorithms that are particularly suitable for quantum computers, such as cryptographic algorithms that utilize prime factorization, encryption/decryption, algorithms to optimize chemical reactions, algorithms to model protein folding, etc. The quantum processing device 2026 may also include support circuitry to support the processing capability of the

quantum processing device 2026, such as input/output channels, multiplexers, signal mixers, quantum amplifiers, and analog-to-digital converters. For example, the quantum processing device 2026 may include circuitry (e.g., a current source) to provide current pulses to one or more magnet lines 121 included in the quantum dot device 100.

[0186] As noted above, the processing device 2002 may include a non-quantum processing device 2028. In some embodiments, the non-quantum processing device 2028 may provide peripheral logic to support the operation of the quantum processing device 2026. For example, the non-quantum processing device 2028 may control the performance of a read operation, control the performance of a write operation, control the clearing of quantum bits, etc. The non-quantum processing device 2028 may also perform conventional computing functions to supplement the computing functions provided by the quantum processing device 2026. For example, the non-quantum processing device 2028 may interface with one or more of the other components of the quantum computing device 2000 (e.g., the communication chip 2012 discussed below, the display device 2006 discussed below, etc.) in a conventional manner, and may serve as an interface between the quantum processing device 2026 and conventional components. The non-quantum processing device 2028 may include one or more digital signal processors (DSPs), application-specific integrated circuits (ASICs), central processing units (CPUs), graphics processing units (GPUs), cryptoprocessors (specialized processors that execute cryptographic algorithms within hardware), server processors, or any other suitable processing devices.

[0187] The quantum computing device 2000 may include a memory 2004, which may itself include one or more memory devices such as volatile memory (e.g., dynamic random access memory (DRAM)), nonvolatile memory (e.g., read-only memory (ROM)), flash memory, solid state memory, and/or a hard drive. In some embodiments, the states of qubits in the quantum processing device 2026 may be read and stored in the memory 2004. In some embodiments, the memory 2004 may include memory that shares a die with the non-quantum processing device 2028. This memory may be used as cache memory and may include embedded dynamic random access memory (eDRAM) or spin transfer torque magnetic random-access memory (STT-MRAM).

[0188] The quantum computing device 2000 may include a cooling apparatus 2030. The cooling apparatus 2030 may maintain the quantum processing device 2026 at a predetermined low temperature during operation to reduce the effects of scattering in the quantum processing device 2026. This predetermined low temperature may vary depending on the setting; in some embodiments, the temperature may be 5 degrees Kelvin or less. In some embodiments, the non-quantum processing device 2028 (and various other components of the quantum computing device 2000) may not be cooled by the cooling apparatus 2030, and may instead operate at room

temperature. The cooling apparatus 2030 may be, for example, a dilution refrigerator, a helium-3 refrigerator, or a liquid helium refrigerator.

[0189] In some embodiments, the quantum computing device 2000 may include a communication chip 2012 (e.g., one or more communication chips). For example, the communication chip 2012 may be configured for managing wireless communications for the transfer of data to and from the quantum computing device 2000. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a nonsolid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not.

[0190] The communication chip 2012 may implement any of a number of wireless standards or protocols, including but not limited to Institute for Electrical and Electronic Engineers (IEEE) standards including Wi-Fi (IEEE 1402.11 family), IEEE 1402.16 standards (e.g., IEEE 1402.16-2005 Amendment), Long-Term Evolution (LTE) project along with any amendments, updates, and/or revisions (e.g., advanced LTE project, ultramobile broadband (UMB) project (also referred to as "3GPP2"), etc.). IEEE 1402.16 compatible Broadband Wireless Access (BWA) networks are generally referred to as WiMAX networks, an acronym that stands for Worldwide Interoperability for Microwave Access, which is a certification mark for products that pass conformity and interoperability tests for the IEEE 1402.16 standards. The communication chip 2012 may operate in accordance with a Global System for Mobile Communication (GSM), General Packet Radio Service (GPRS), Universal Mobile Telecommunications System (UMTS), High Speed Packet Access (HSPA), Evolved HSPA (E-HSPA), or LTE network. The communication chip 2012 may operate in accordance with Enhanced Data for GSM Evolution (EDGE), GSM EDGE Radio Access Network (GERAN), Universal Terrestrial Radio Access Network (UTRAN), or Evolved UTRAN (E-UTRAN). The communication chip 2012 may operate in accordance with Code Division Multiple Access (CDMA), Time Division Multiple Access (TDMA), Digital Enhanced Cordless Telecommunications (DECT), Evolution-Data Optimized (EV-DO), and derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The communication chip 2012 may operate in accordance with other wireless protocols in other embodiments. The quantum computing device 2000 may include an antenna 2022 to facilitate wireless communications and/or to receive other wireless communications (such as AM or FM radio transmissions).

[0191] In some embodiments, the communication chip 2012 may manage wired communications, such as electrical, optical, or any other suitable communication protocols (e.g., the Ethernet). As noted above, the communication chip 2012 may include multiple communication chips. For

instance, a first communication chip 2012 may be dedicated to shorter-range wireless communications such as Wi-Fi or Bluetooth, and a second communication chip 2012 may be dedicated to longer-range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, EV-DO, or others. In some embodiments, a first communication chip 2012 may be dedicated to wireless communications, and a second communication chip 2012 may be dedicated to wired communications.

[0192] The quantum computing device 2000 may include battery/power circuitry 2014. The battery/power circuitry 2014 may include one or more energy storage devices (e.g., batteries or capacitors) and/or circuitry for coupling components of the quantum computing device 2000 to an energy source separate from the quantum computing device 2000 (e.g., AC line power).

[0193] The quantum computing device 2000 may include a display device 2006 (or corresponding interface circuitry, as discussed above). The display device 2006 may include any visual indicators, such as a heads-up display, a computer monitor, a projector, a touchscreen display, a liquid crystal display (LCD), a light-emitting diode display, or a flat panel display, for example.

[0194] The quantum computing device 2000 may include an audio output device 2008 (or corresponding interface circuitry, as discussed above). The audio output device 2008 may include any device that generates an audible indicator, such as speakers, headsets, or earbuds, for example.

[0195] The quantum computing device 2000 may include an audio input device 2024 (or corresponding interface circuitry, as discussed above). The audio input device 2024 may include any device that generates a signal representative of a sound, such as microphones, microphone arrays, or digital instruments (e.g., instruments having a musical instrument digital interface (MIDI) output).

[0196] The quantum computing device 2000 may include a global positioning system (GPS) device 2018 (or corresponding interface circuitry, as discussed above). The GPS device 2018 may be in communication with a satellite-based system and may receive a location of the quantum computing device 2000, as known in the art.

[0197] The quantum computing device 2000 may include an other output device 2010 (or corresponding interface circuitry, as discussed above). Examples of the other output device 2010 may include an audio codec, a video codec, a printer, a wired or wireless transmitter for providing information to other devices, or an additional storage device.

[0198] The quantum computing device 2000 may include an other input device 2020 (or corresponding interface circuitry, as discussed above). Examples of the other input device 2020 may include an accelerometer, a gyroscope, a compass, an image capture device, a keyboard, a cursor control device such as a mouse, a stylus, a touchpad, a bar code reader, a Quick Response (QR) code reader, any sensor, or a radio frequency identification (RFID) reader.

[0199] The quantum computing device 2000, or a subset of its components, may have any appropriate form factor, such as a hand-held or mobile computing device (e.g., a cell phone, a smart phone, a mobile internet device, a music player, a tablet computer, a laptop computer, a netbook computer, an ultrabook computer, a personal digital assistant (PDA), an ultramobile personal computer, etc.), a desktop computing device, a server or other networked computing component, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a vehicle control unit, a digital camera, a digital video recorder, or a wearable computing device.

[0200] The following paragraphs provide various examples of the embodiments disclosed herein.

[0201] Example 1 is a quantum computing assembly, including: a quantum device die to generate a plurality of qubits; a control circuitry die to control operation of the quantum device die; and a substrate; wherein the quantum device die and the control circuitry die are disposed on the substrate.

[0202] Example 2 may include the subject matter of Example 1, and may further specify that the substrate is a package substrate, and the quantum device die and the control circuitry die are included in a common package.

[0203] Example 3 may include the subject matter of Example 1, and may further specify that the substrate is an interposer.

[0204] Example 4 may include the subject matter of Example 1, and may further specify that the substrate is a printed circuit board.

[0205] Example 5 may include the subject matter of Example 1, and may further specify that the quantum device die and the control circuitry die are included in a package-on-package structure.

[0206] Example 6 may include the subject matter of any of Examples 1-5, and may further specify that the substrate includes at least one microwave transmission line between the quantum device die and the control circuitry die.

[0207] Example 7 may include the subject matter of any of Examples 1-6, and may further specify that the substrate includes at least one conductive pathway between a face of the substrate to which the control circuitry die is coupled, and an opposing face of the substrate.

[0208] Example 8 may include the subject matter of any of Examples 1-7, and may further specify that the control circuitry die includes a processing device or a memory element.

[0209] Example 9 may include the subject matter of any of Examples 1-8, and may further specify that the quantum device die and the control circuitry die are each coupled to the substrate with solder connections.

[0210] Example 10 may include the subject matter of any of Examples 1-9, and may further specify that the quantum device die includes a plurality of gates, and the control circuitry die is to provide voltages to the plurality of gates through the substrate.

[0211] Example 11 may include the subject matter of any of Examples 1-10, and may further specify that the quantum device die includes one or more magnet lines, and the control circuitry die is to provide electrical pulses to the one or more magnet lines through the substrate.

[0212] Example 12 may include the subject matter of any of Examples 1-11, and may further specify that the control circuitry die includes a switching matrix for selecting one or more of the qubits to read or write.

[0213] Example 13 may include the subject matter of any of Examples 1-12, and may further specify that the qubits are quantum-dot-based qubits.

[0214] Example 14 may include the subject matter of any of Examples 1-13, and may further specify that the substrate includes electrical pathways between the quantum device die and the control circuitry die, and the electrical pathways include superconducting material.

[0215] Example 15 may include the subject matter of any of Examples 1-14, and may further include a memory device to store data generated by the control circuitry die during operation of the quantum device die.

[0216] Example 16 may include the subject matter of any of Examples 1-15, and may further include a cooling apparatus to maintain a temperature of the quantum device die and the control circuitry die in a desired range.

[0217] Example 17 may include the subject matter of any of Examples 1-16, and may further include a wired or wireless network controller to receive and transmit data from the control circuitry die.

[0218] Example 18 is a method of manufacturing a quantum computing assembly, including: providing a substrate, wherein the substrate includes one or more electrical pathways between a first set of contacts and a second set of contacts; coupling a quantum device die to the first set of contacts such that the quantum device die is disposed on the substrate; and coupling one or more control dies to the second set of contacts such that the one or more control dies are disposed on the substrate, wherein the control dies are to provide voltages to one or more components of the quantum device die through the one or more electrical pathways.

[0219] Example 19 may include the subject matter of Example 18, and may further specify that the one or more electrical pathways includes a coplanar waveguide, a strip line or a microstrip line.

[0220] Example 20 may include the subject matter of any of Examples 18-19-, and may further include providing an overmold material on the quantum device die and the one or more control dies, or providing an underfill material under the quantum device die and the one or more control dies.

[0221] Example 21 may include the subject matter of any of Examples 18-20, and may further specify that the quantum device die is disposed on an intermediate structure, and coupling the quantum device die to the first set of contacts includes physically securing the intermediate structure on the first set of contacts.

[0222] Example 22 may include the subject matter of any of Examples 18-21, and may further specify that one or more control dies are disposed on an intermediate structure, and coupling the one or more control dies to the second set of contacts includes physically securing the intermediate structure on the second set of contacts.

[0223] Example 23 is a method of operating a quantum computing assembly, including: providing, by a control circuitry die, one or more voltages to a quantum device die through a substrate on which the quantum device die and the control circuitry die are disposed; and changing the state of qubits, in the quantum device die, at least in part in response to the one or more voltages.

[0224] Example 24 may include the subject matter of Example 23, and may further specify that providing the one or more voltages to the quantum device die includes providing electron spin resonance (ESR) pulses to a magnet line or one or more gates of the quantum device die.

[0225] Example 25 may include the subject matter of any of Examples 23-24, and may further specify that changing the state of the qubits includes changing the spin state of quantum-dot-based qubits.

[0226] Example 26 may include the subject matter of any of Examples 23-25, and may further include detecting, by the control circuitry die, the state of the qubits in the quantum device die.

[0227] Example 27 may include the subject matter of Example 26, and may further include communicating, by the control circuitry die, the state of the qubits through the substrate.

[0228] Example 28 may include the subject matter of any of Examples 23-27, and may further specify that the control circuitry die includes a silicon-based processing device.

[0229] Example 29 may include the subject matter of any of Examples 23-28, and may further specify that the substrate includes an interposer.

Claims:

1. A quantum computing assembly, comprising:

a quantum device die to generate a plurality of qubits;

a control circuitry die to control operation of the quantum device die; and

a substrate;

wherein the quantum device die and the control circuitry die are disposed on the substrate.

2. The quantum computing assembly of claim 1, wherein the substrate is a package substrate, and the quantum device die and the control circuitry die are included in a common package.

3. The quantum computing assembly of claim 1, wherein the substrate is an interposer.

4. The quantum computing assembly of claim 1, wherein the substrate is a printed circuit board.

5. The quantum computing assembly of claim 1, wherein the quantum device die and the control circuitry die are included in a package-on-package structure.

6. The quantum computing assembly of claim 1, wherein the substrate includes at least one microwave transmission line between the quantum device die and the control circuitry die.

7. The quantum computing assembly of claim 1, wherein the substrate includes at least one conductive pathway between a face of the substrate to which the control circuitry die is coupled, and an opposing face of the substrate.

8. The quantum computing assembly of claim 1, wherein the control circuitry die includes a processing device or a memory element.

9. The quantum computing assembly of claim 1, wherein the quantum device die and the control circuitry die are each coupled to the substrate with solder connections.

10. The quantum computing assembly of any of claims 1-9, wherein the quantum device die includes a plurality of gates, and the control circuitry die is to provide voltages to the plurality of gates through the substrate.

11. The quantum computing assembly of any of claims 1-9, wherein the quantum device die includes one or more magnet lines, and the control circuitry die is to provide electrical pulses to the one or more magnet lines through the substrate.

12. The quantum computing assembly of any of claims 1-9, wherein the control circuitry die includes a switching matrix for selecting one or more of the qubits to read or write.

13. The quantum computing assembly of any of claims 1-9, wherein the qubits are quantum-dot-based qubits.

14. The quantum computing assembly of any of claims 1-9, wherein the substrate includes electrical pathways between the quantum device die and the control circuitry die, and the electrical pathways include superconducting material.

15. The quantum computing assembly of any of claims 1-9, further comprising:
a memory device to store data generated by the control circuitry die during operation of the quantum device die.
16. The quantum computing assembly of any of claims 1-9, further comprising:
a wired or wireless network controller to receive and transmit data from the control circuitry die.
17. A method of manufacturing a quantum computing assembly, including:
providing a substrate, wherein the substrate includes one or more electrical pathways between a first set of contacts and a second set of contacts;
coupling a quantum device die to the first set of contacts such that the quantum device die is disposed on the substrate; and
coupling one or more control dies to the second set of contacts such that the one or more control dies are disposed on the substrate, wherein the control dies are to provide voltages to one or more components of the quantum device die through the one or more electrical pathways.
18. The method of claim 17, wherein the one or more electrical pathways includes a coplanar waveguide, a strip line or a microstrip line.
19. The method of claim 17, wherein the quantum device die is disposed on an intermediate structure, and coupling the quantum device die to the first set of contacts includes physically securing the intermediate structure on the first set of contacts.
20. The method of any of claims 17-19, wherein one or more control dies are disposed on an intermediate structure, and coupling the one or more control dies to the second set of contacts includes physically securing the intermediate structure on the second set of contacts.
21. A method of operating a quantum computing assembly, comprising:
providing, by a control circuitry die, one or more voltages to a quantum device die through a substrate on which the quantum device die and the control circuitry die are disposed; and
changing the state of qubits, in the quantum device die, at least in part in response to the one or more voltages.
22. The method of claim 21, wherein providing the one or more voltages to the quantum device die includes providing electron spin resonance (ESR) pulses to a magnet line or one or more gates of the quantum device die.
23. The method of claim 21, wherein changing the state of the qubits includes changing the spin state of quantum-dot-based qubits.
24. The method of any of claims 21-23, further comprising:
detecting, by the control circuitry die, the state of the qubits in the quantum device die.

25. The method of claim 24, further comprising:

communicating, by the control circuitry die, the state of the qubits through the substrate.

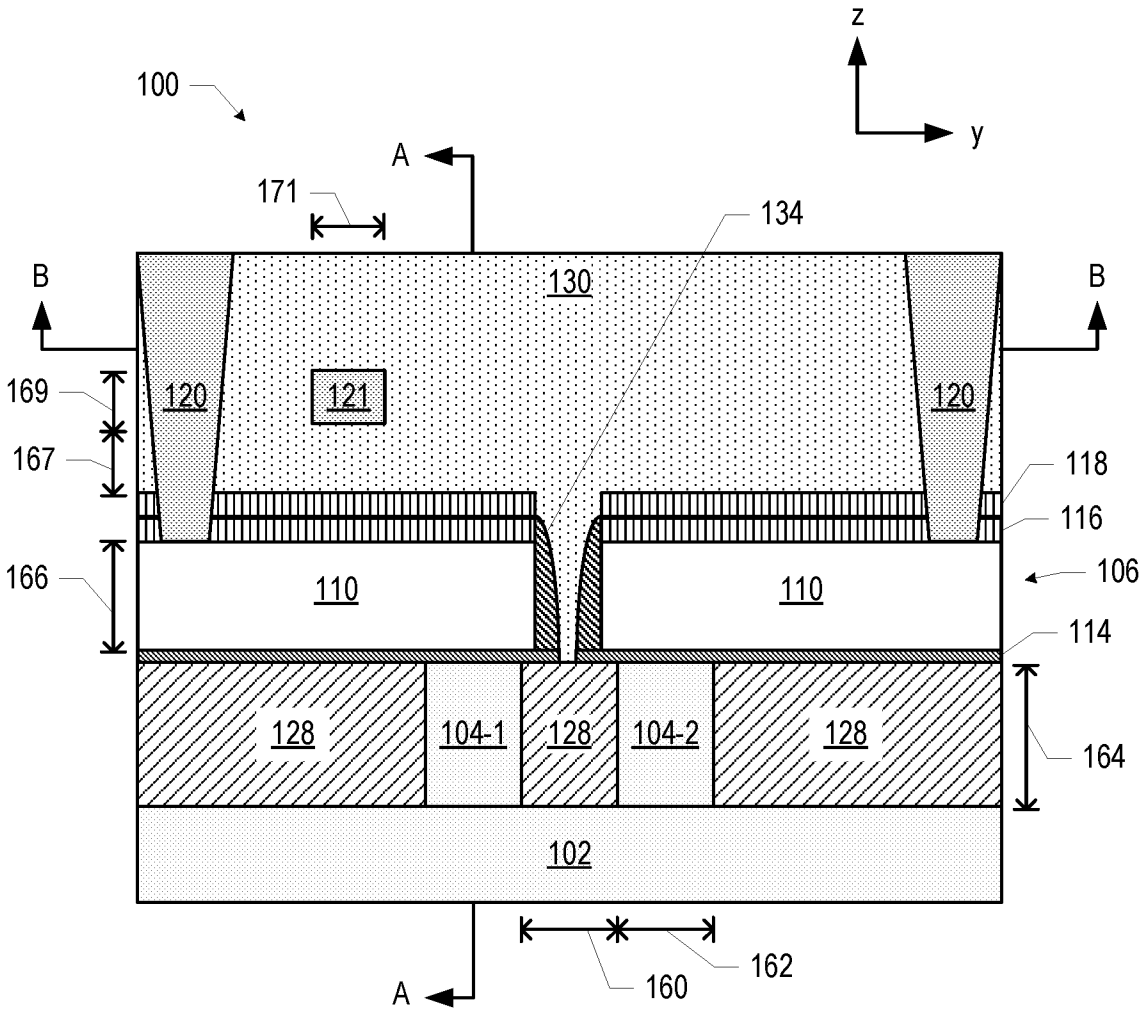

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104-1
128
104-2
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160
A

FIG. 1

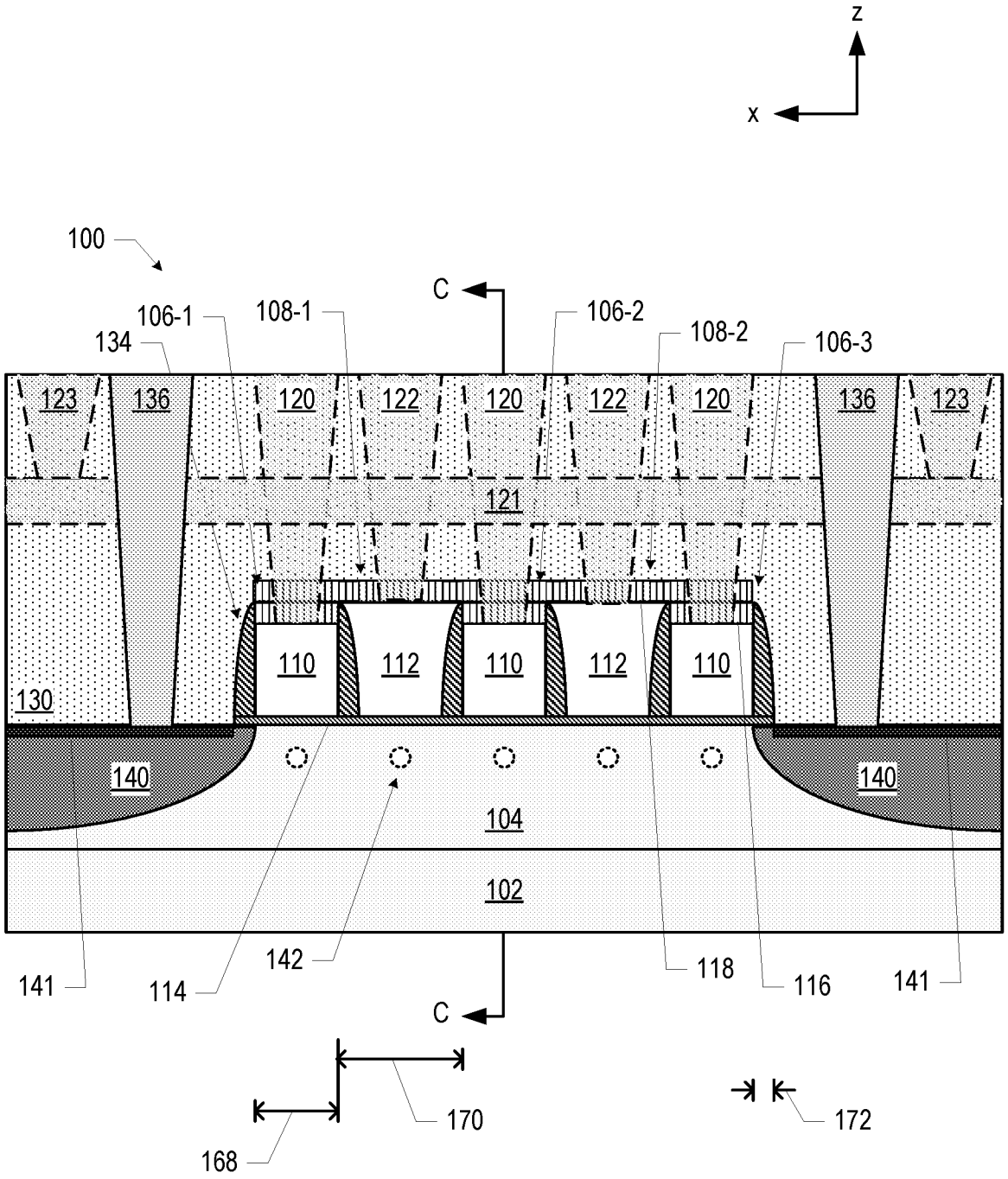

z
x
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C
106-1
108-1
106-2
108-2
106-3
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172

FIG. 2

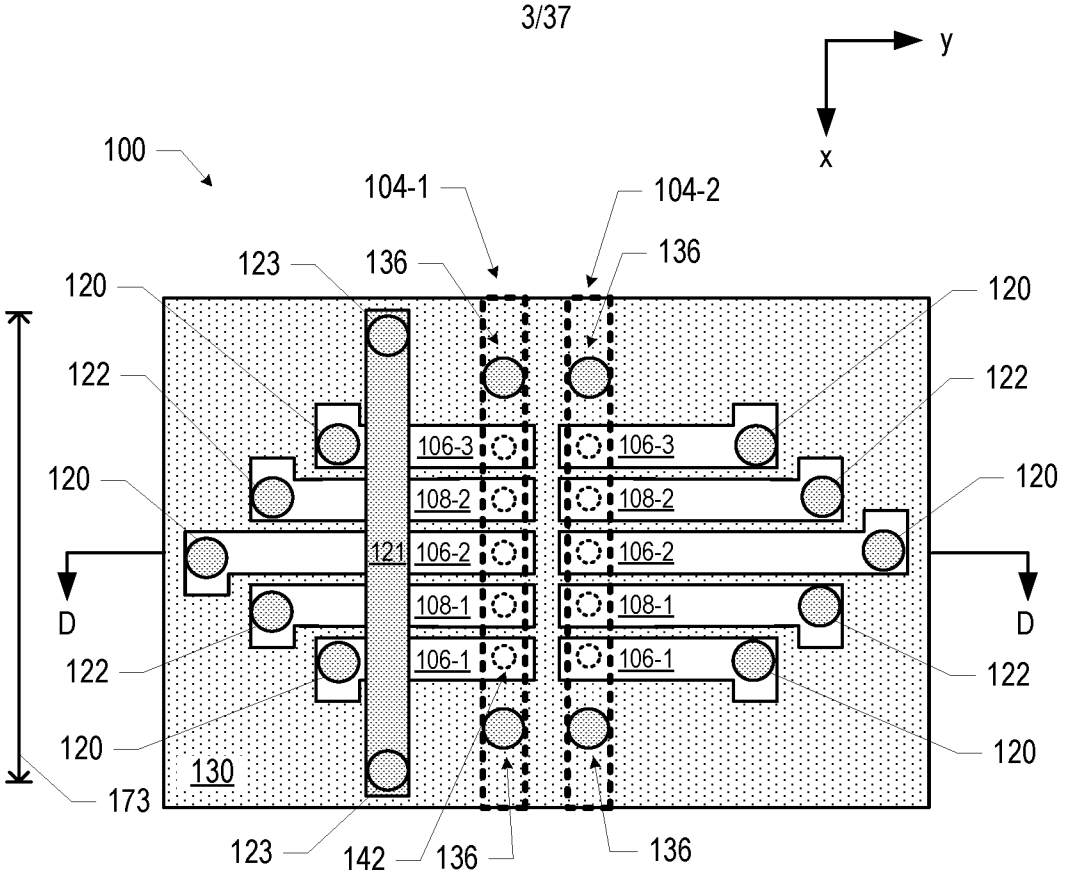


FIG. 3

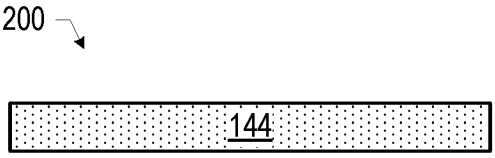


FIG. 4

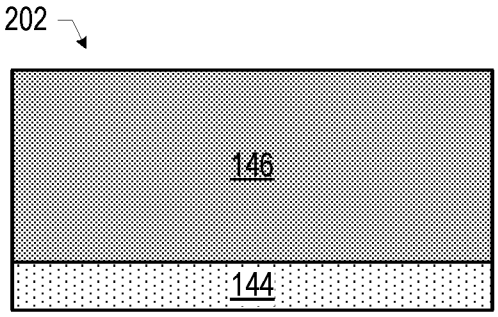


FIG. 5

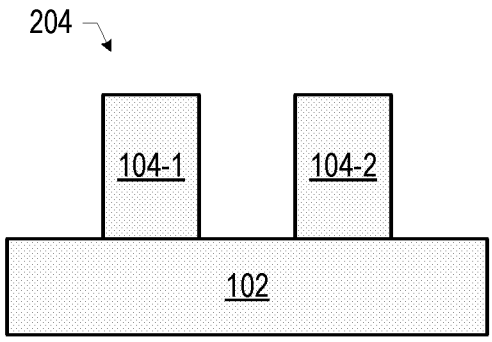


FIG. 6

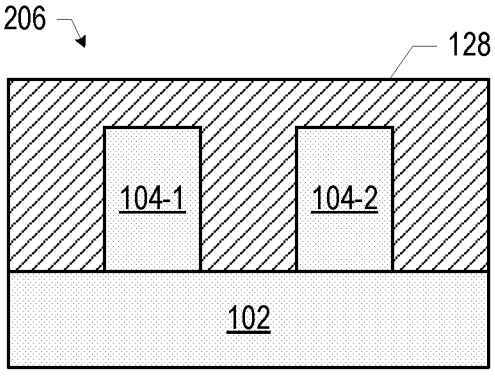


FIG. 7

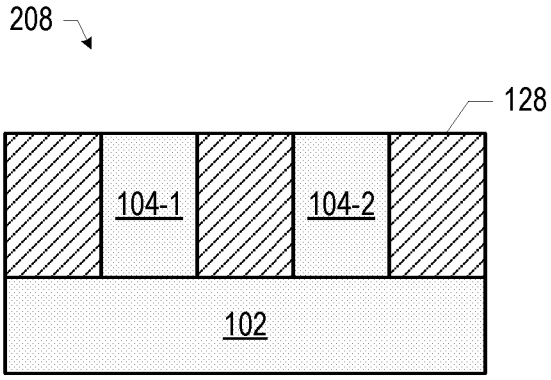


FIG. 8

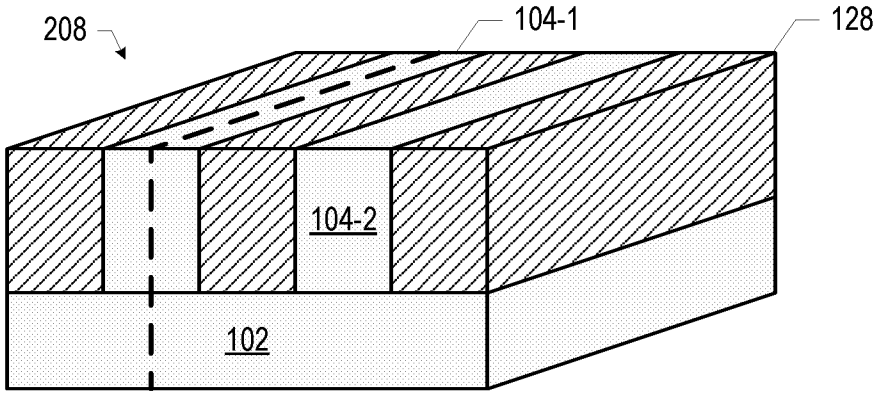


FIG. 9

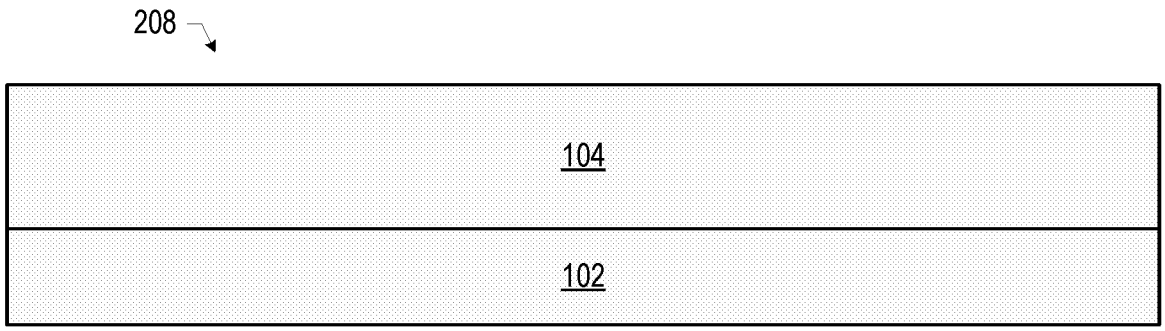


FIG. 10

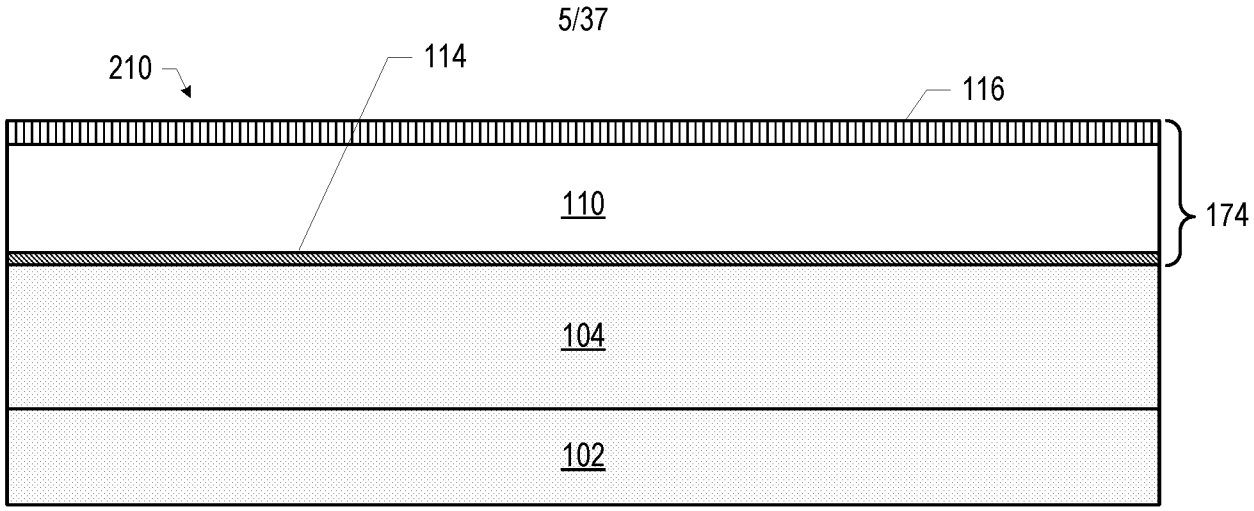


FIG. 11

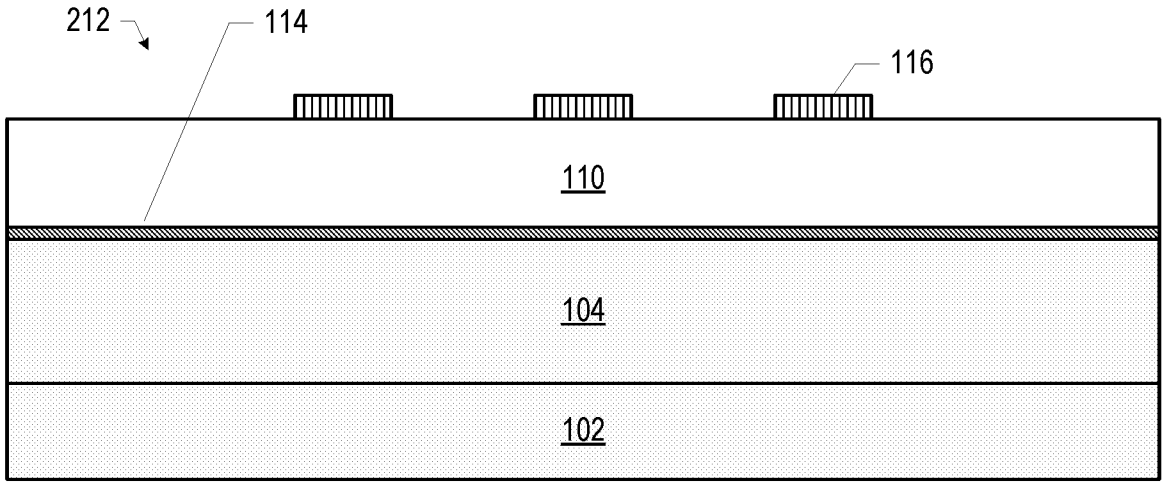


FIG. 12

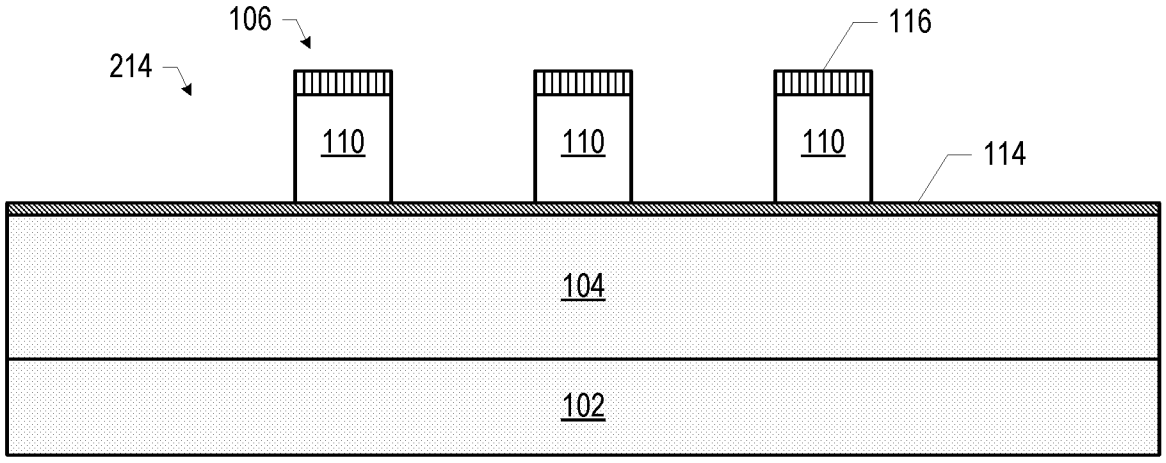


FIG. 13

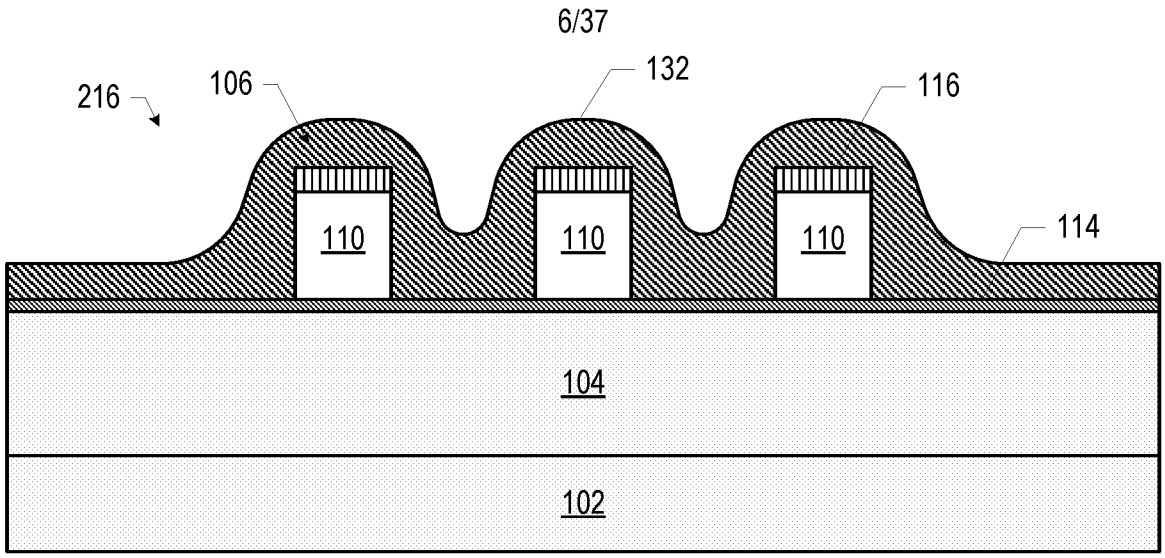


FIG. 14

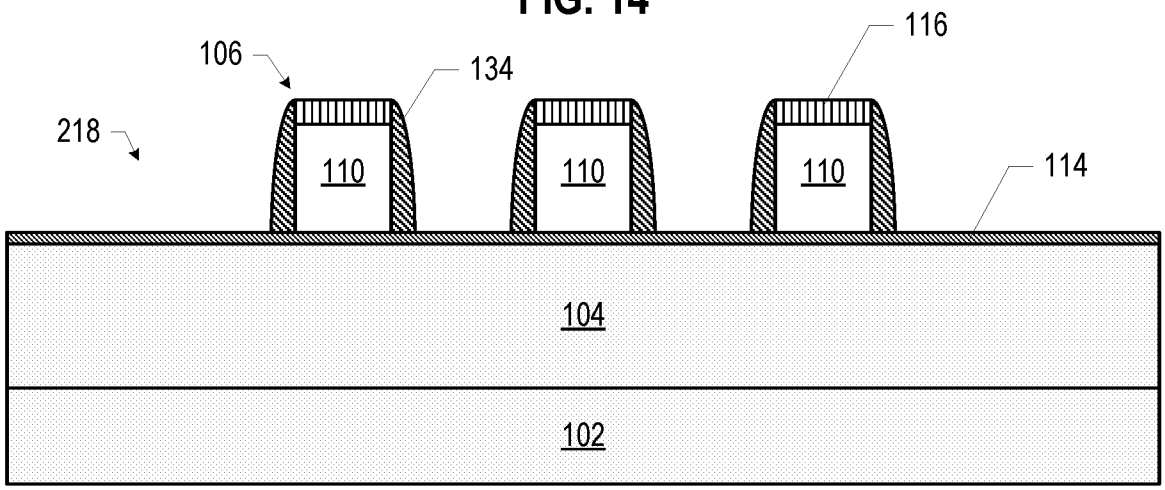


FIG. 15

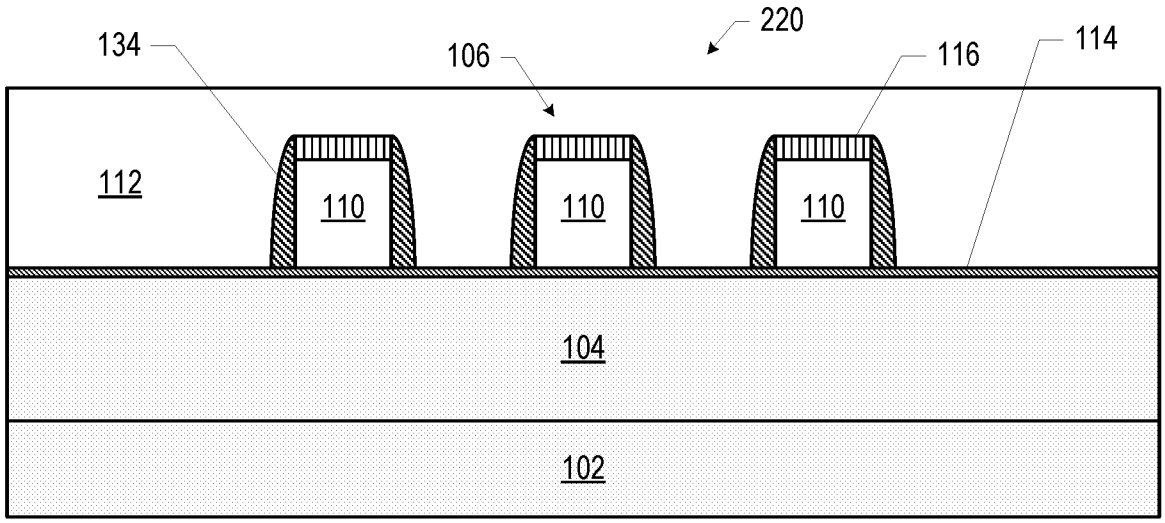


FIG. 16

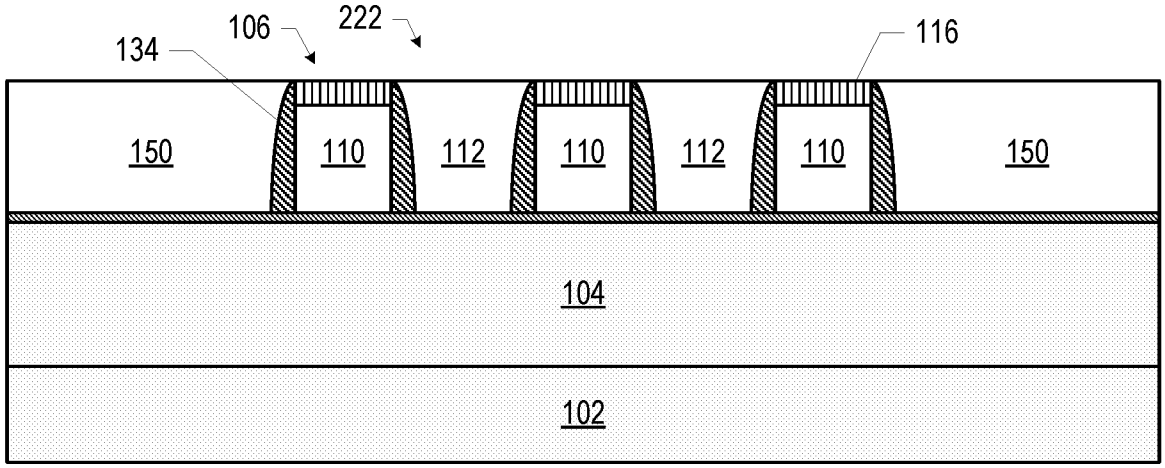


FIG. 17

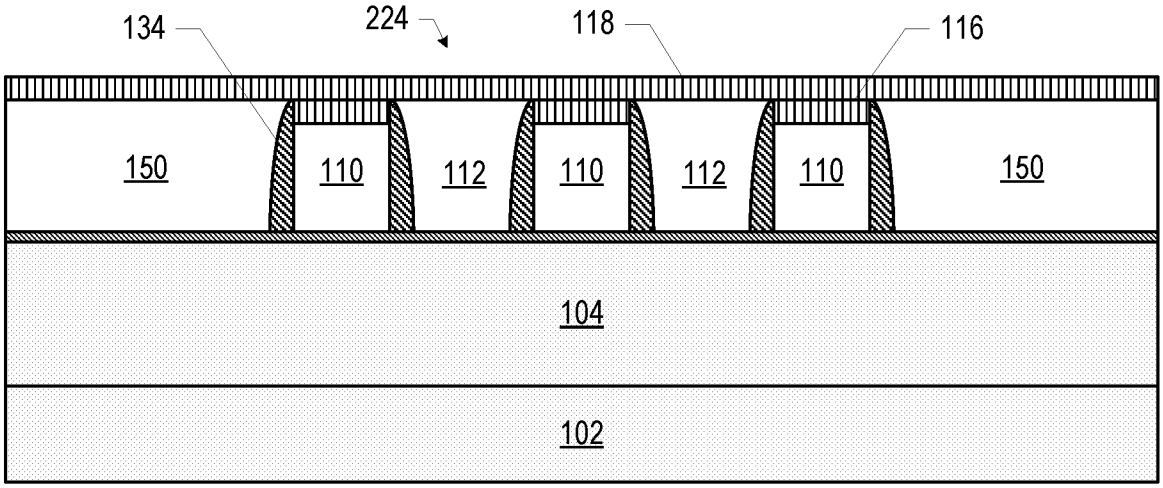


FIG. 18

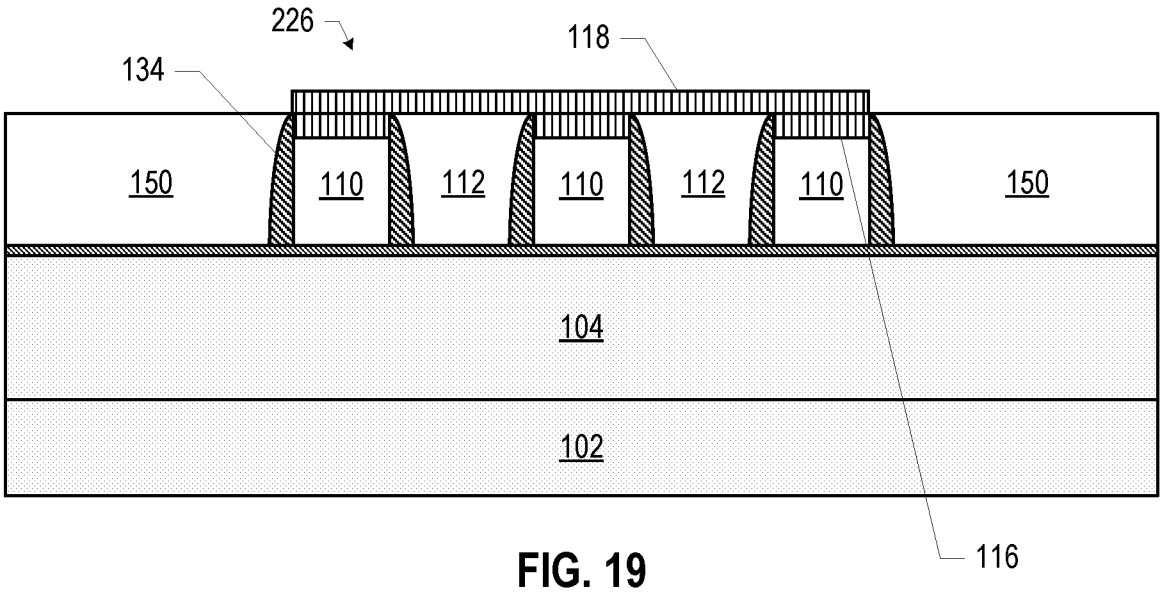


FIG. 19

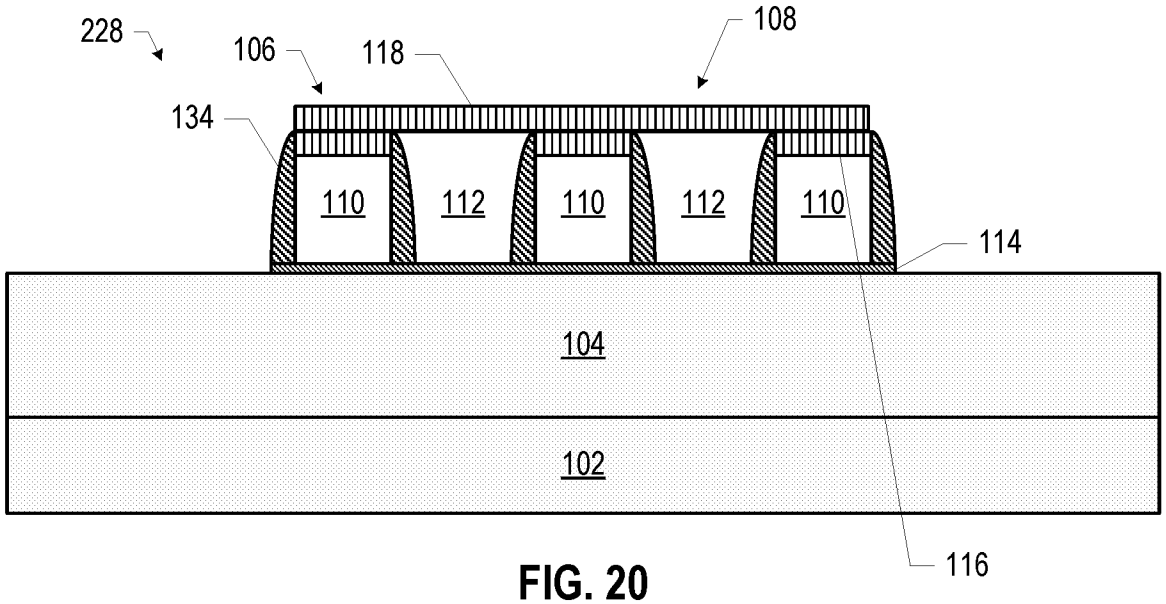

228
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FIG. 20

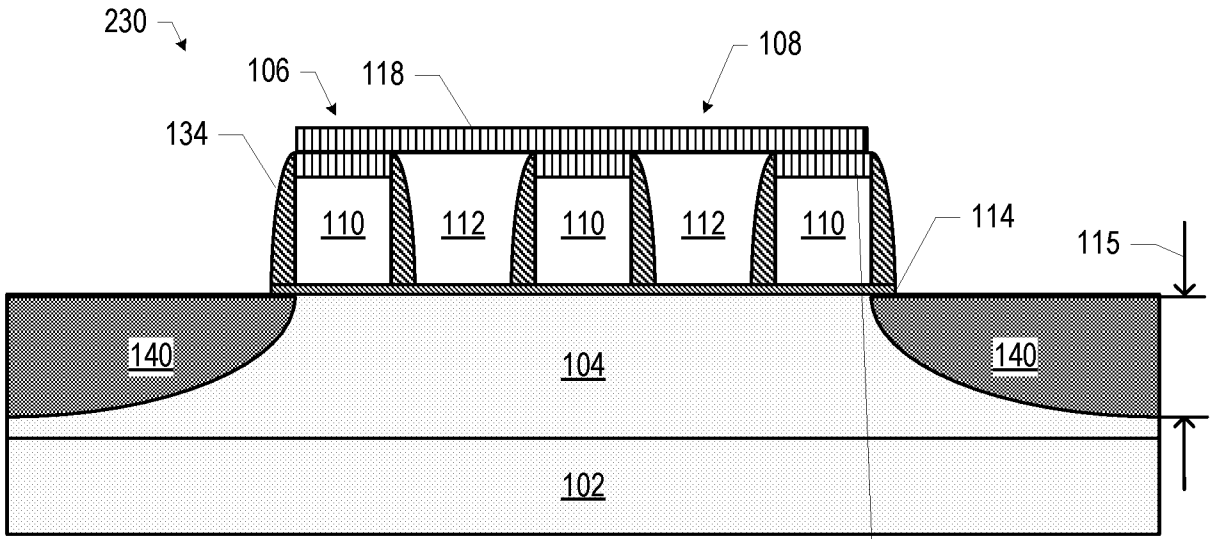

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FIG. 21

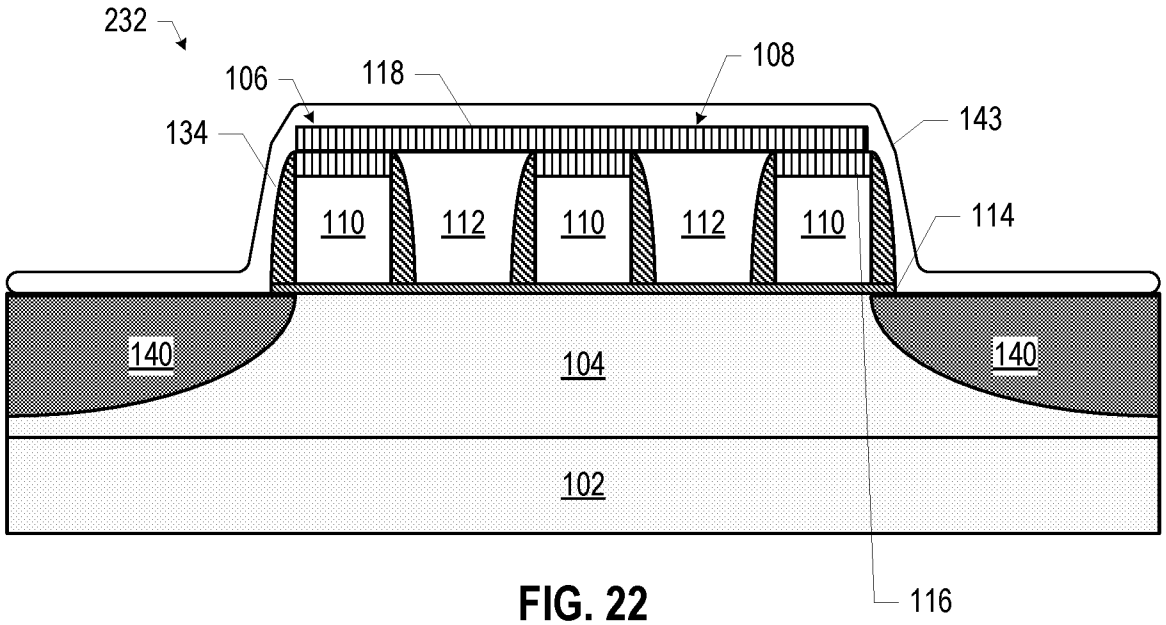

232
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FIG. 22

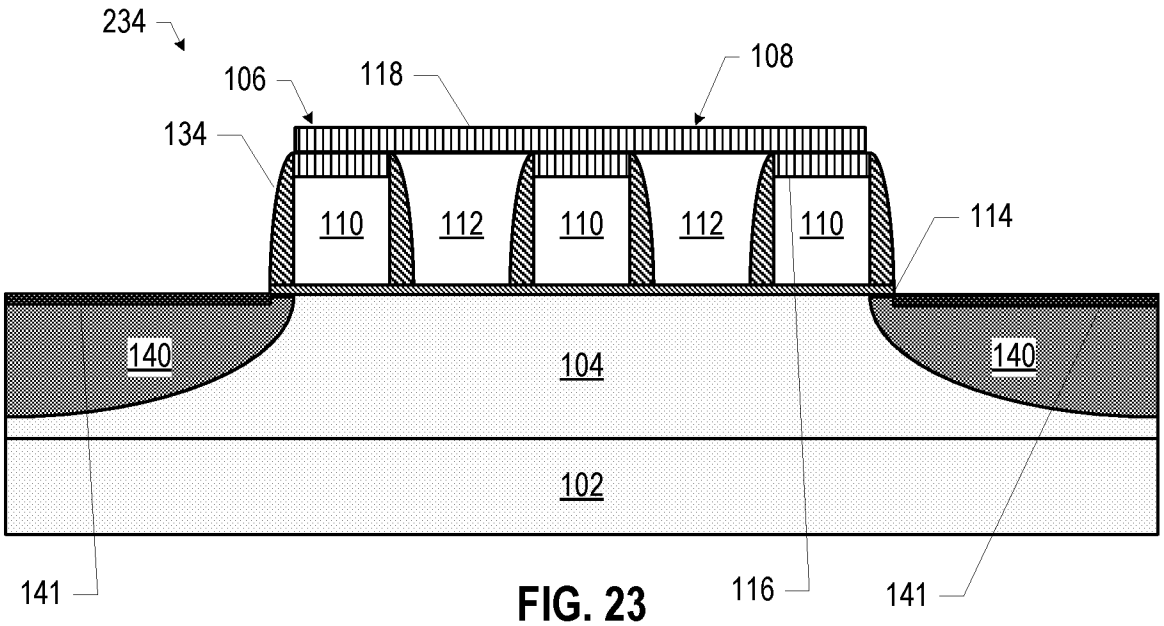

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FIG. 23

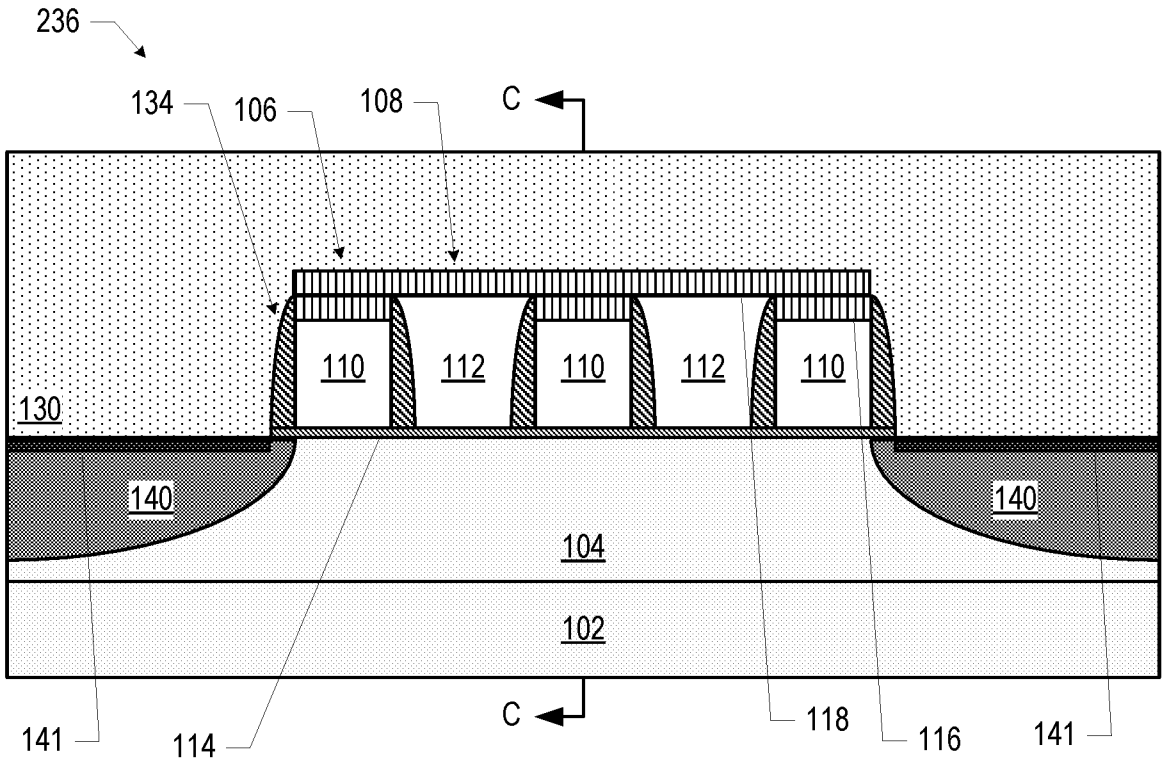

236
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102
C
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141

FIG. 24

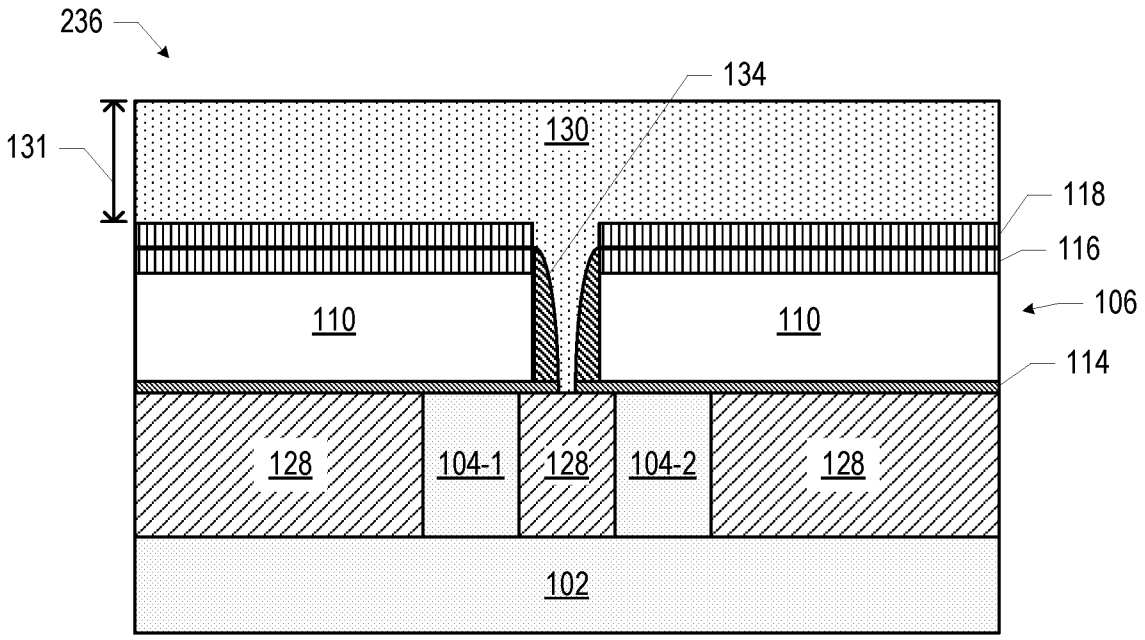

236
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106
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FIG. 25

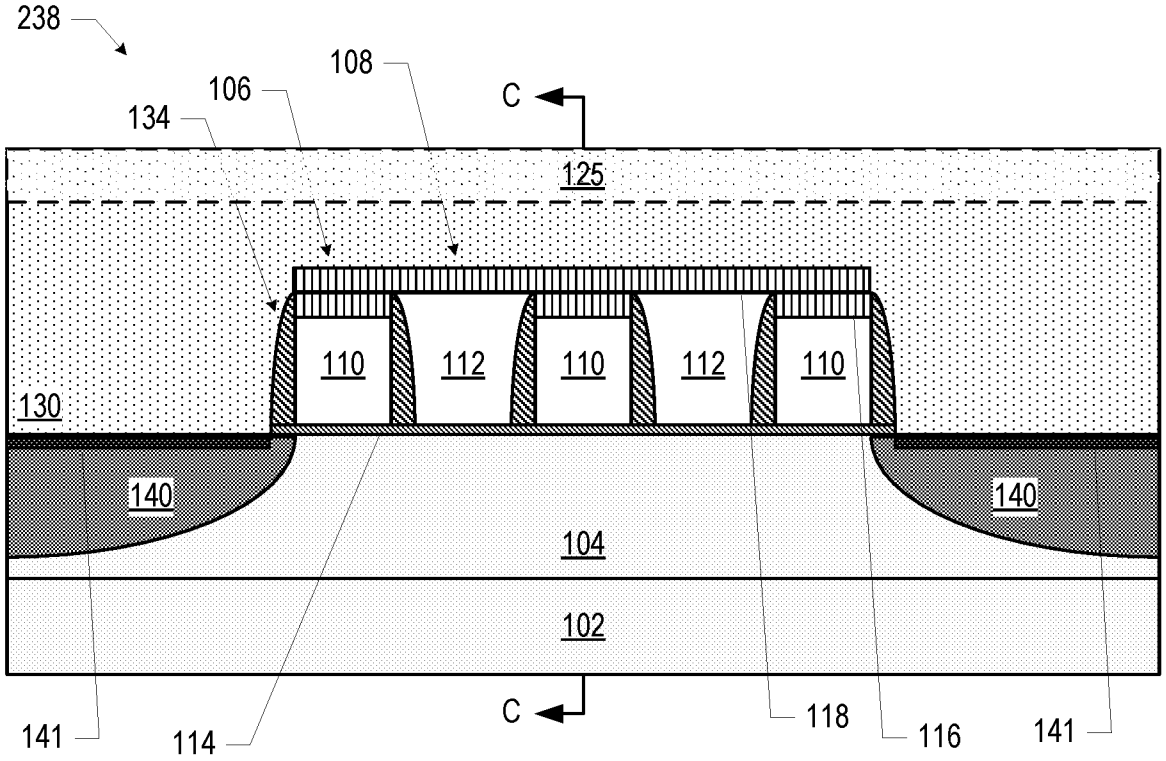

238
108
106
134
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104
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C
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116
141

FIG. 26

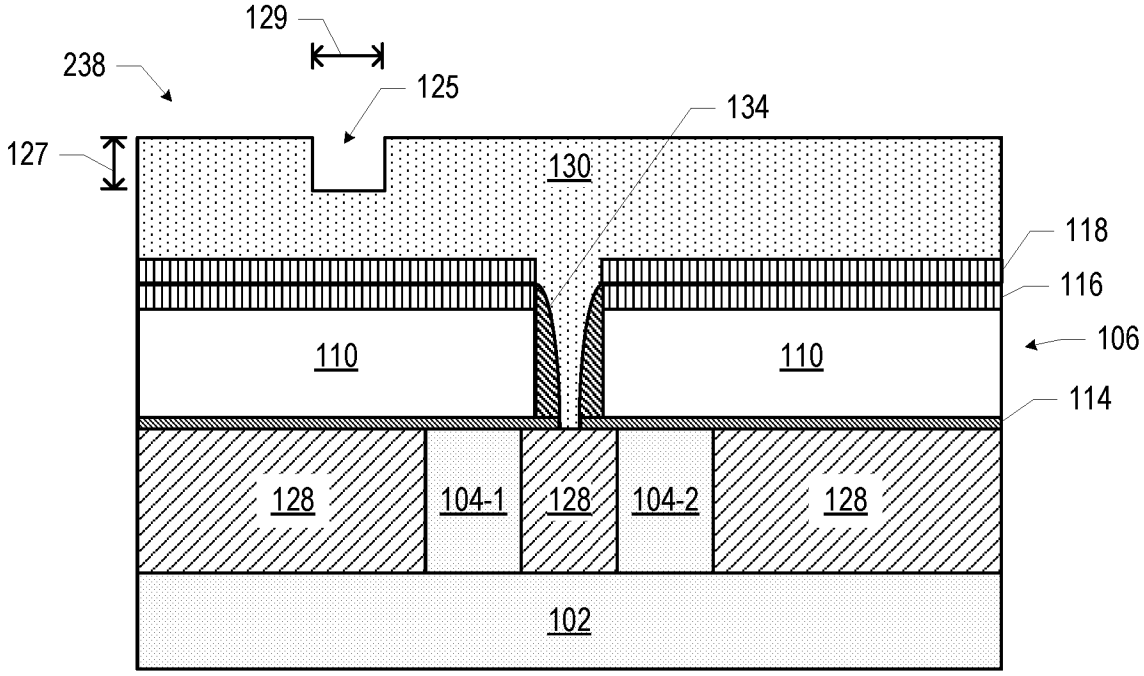

129
238
125
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127
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118
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106
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104-1
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FIG. 27

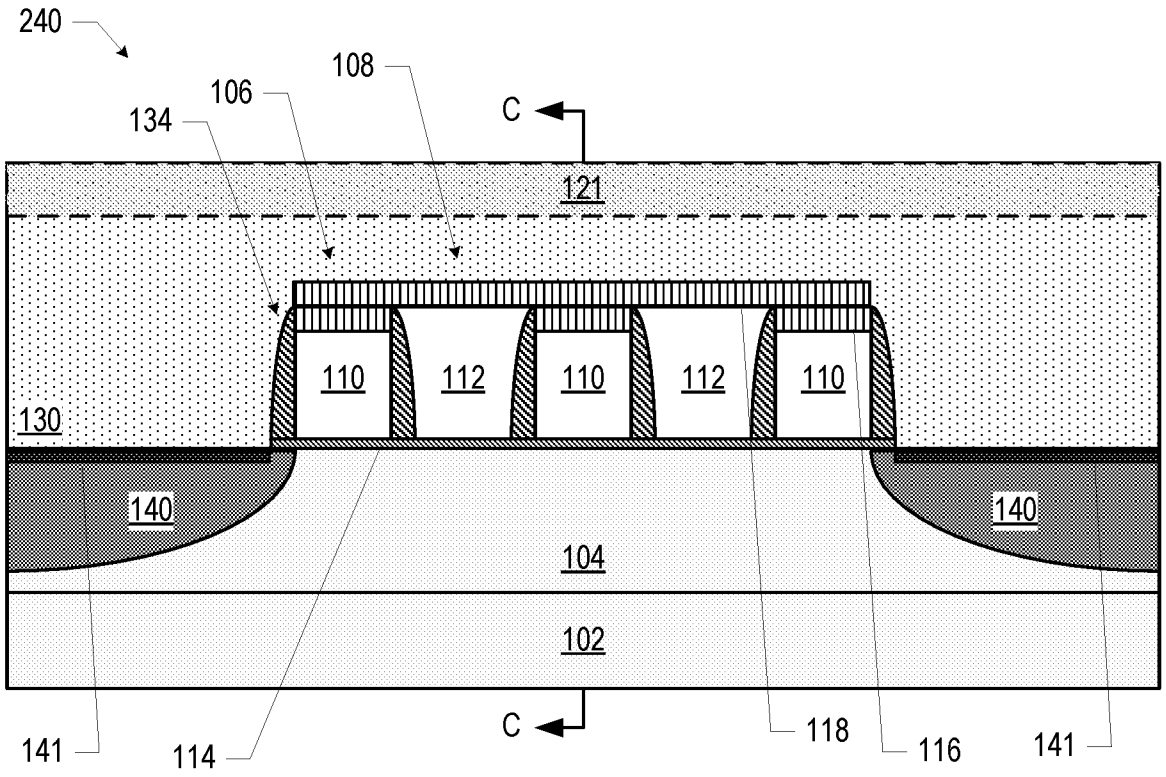

240
108
106
134
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121
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112
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112
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130
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104
102
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FIG. 28

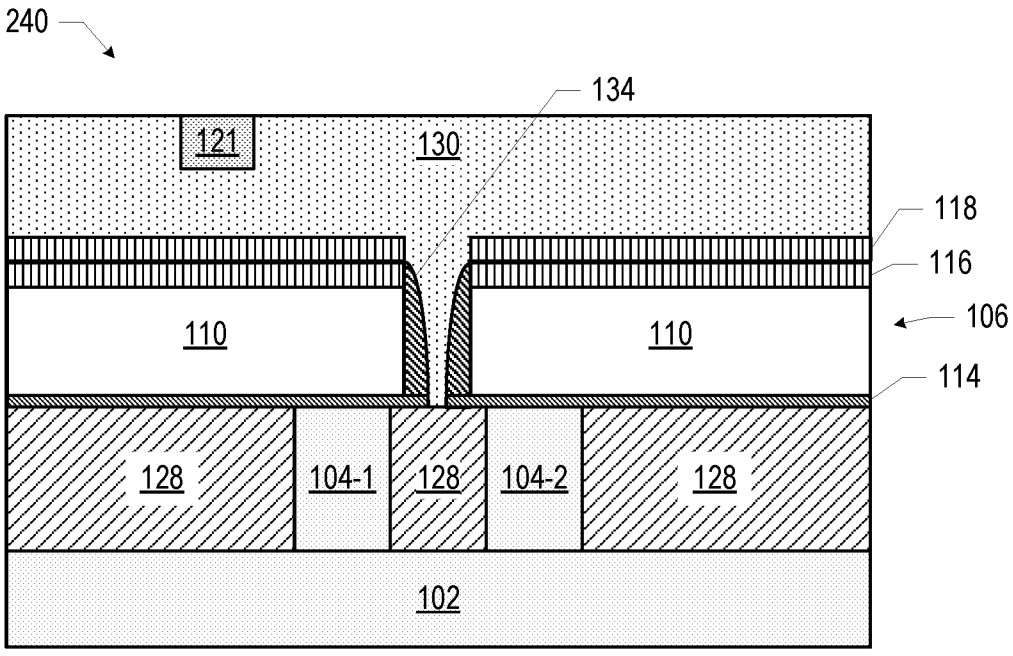

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104-1
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104-2
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102

FIG. 29

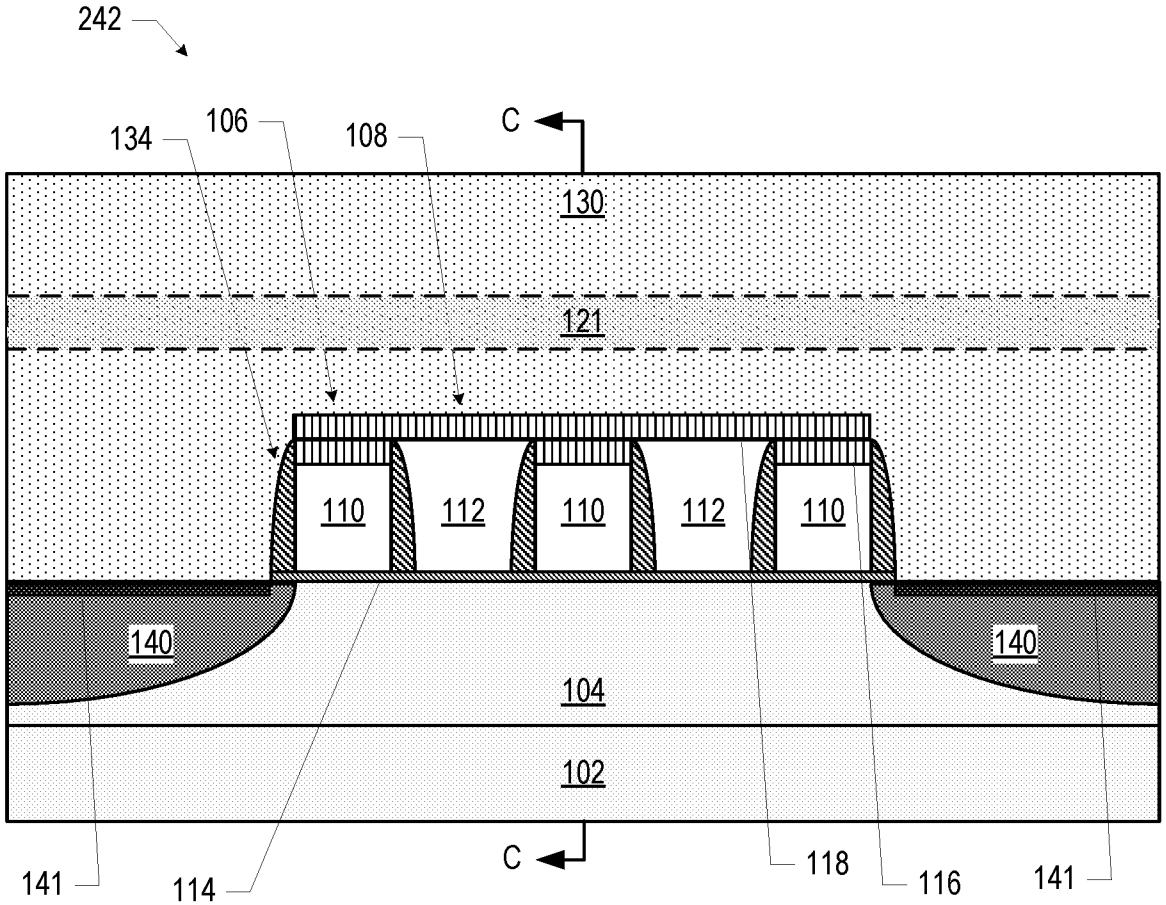

242
134
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FIG. 30

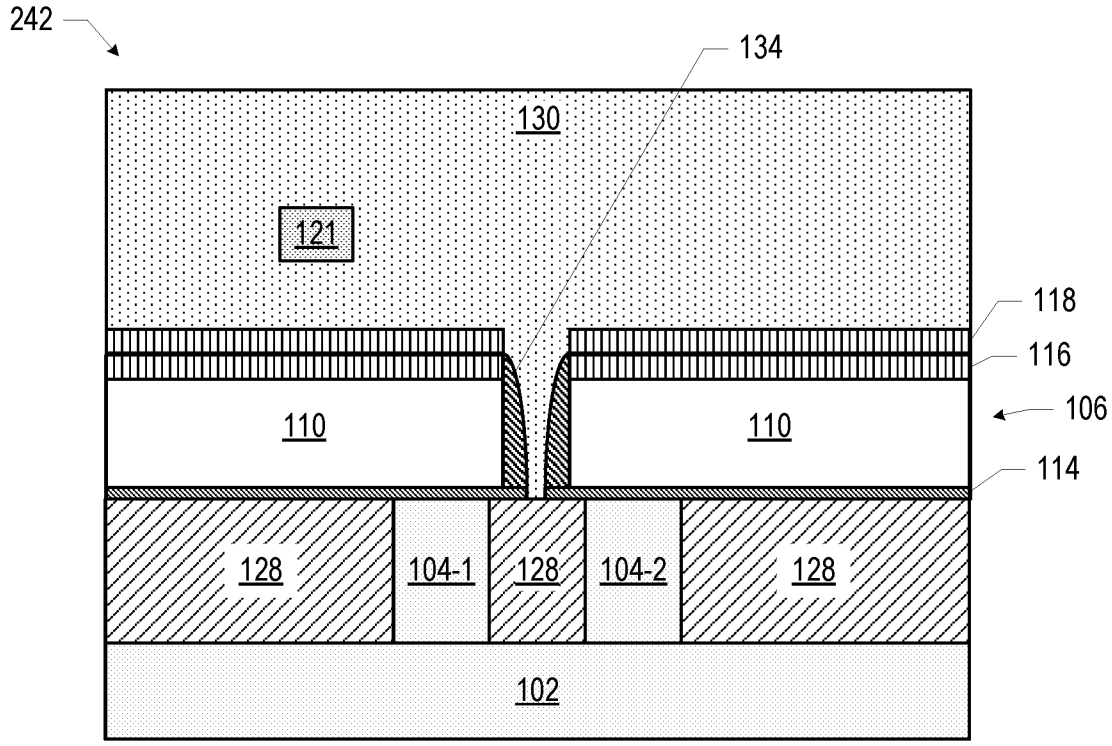

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104-1
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104-2
128
102

FIG. 31

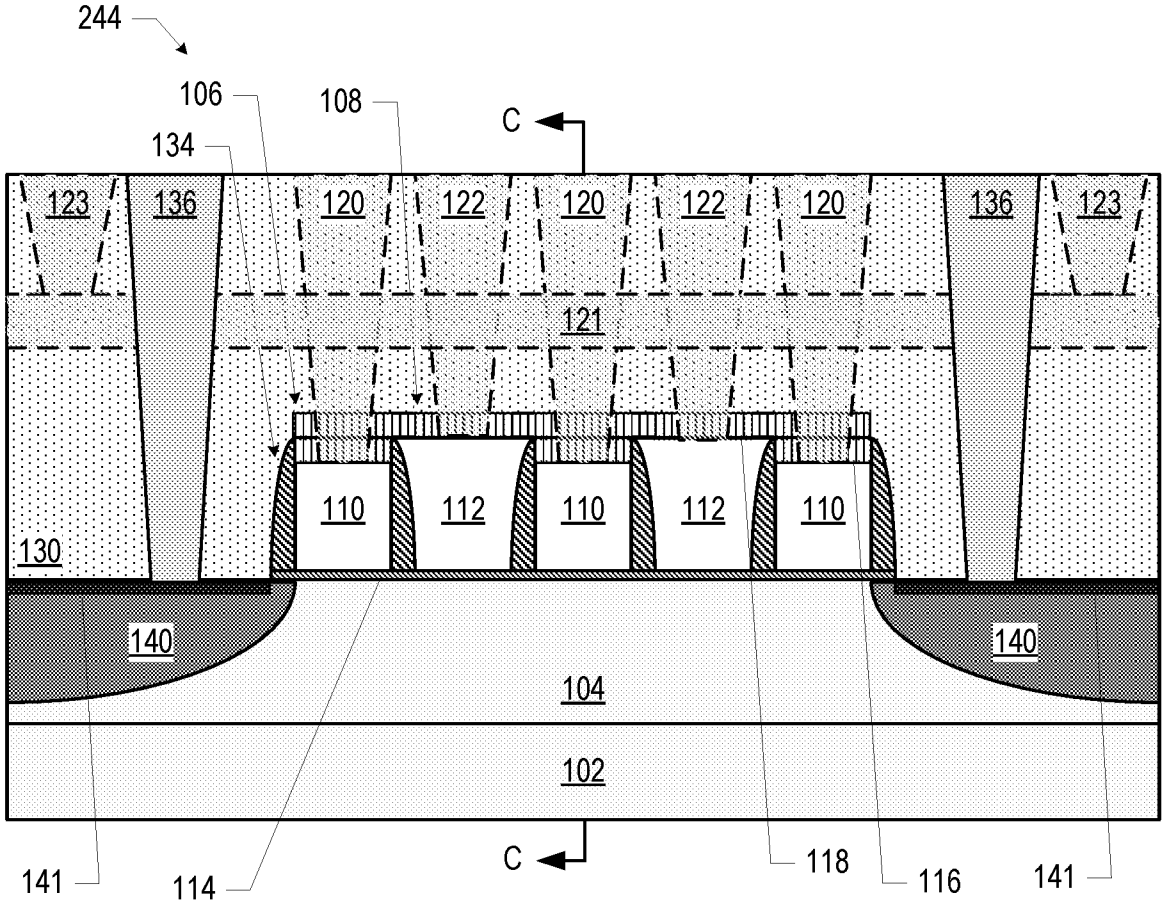

244
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108
C
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136
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116
141

FIG. 32

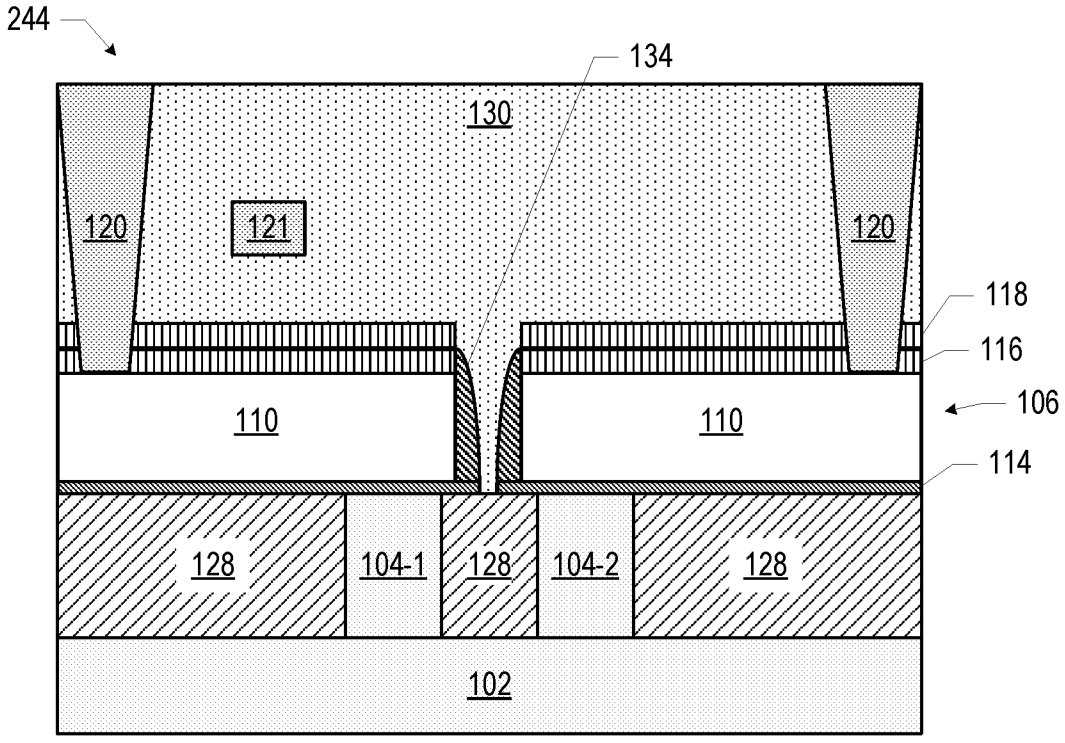

244
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104-1
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104-2
128
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FIG. 33

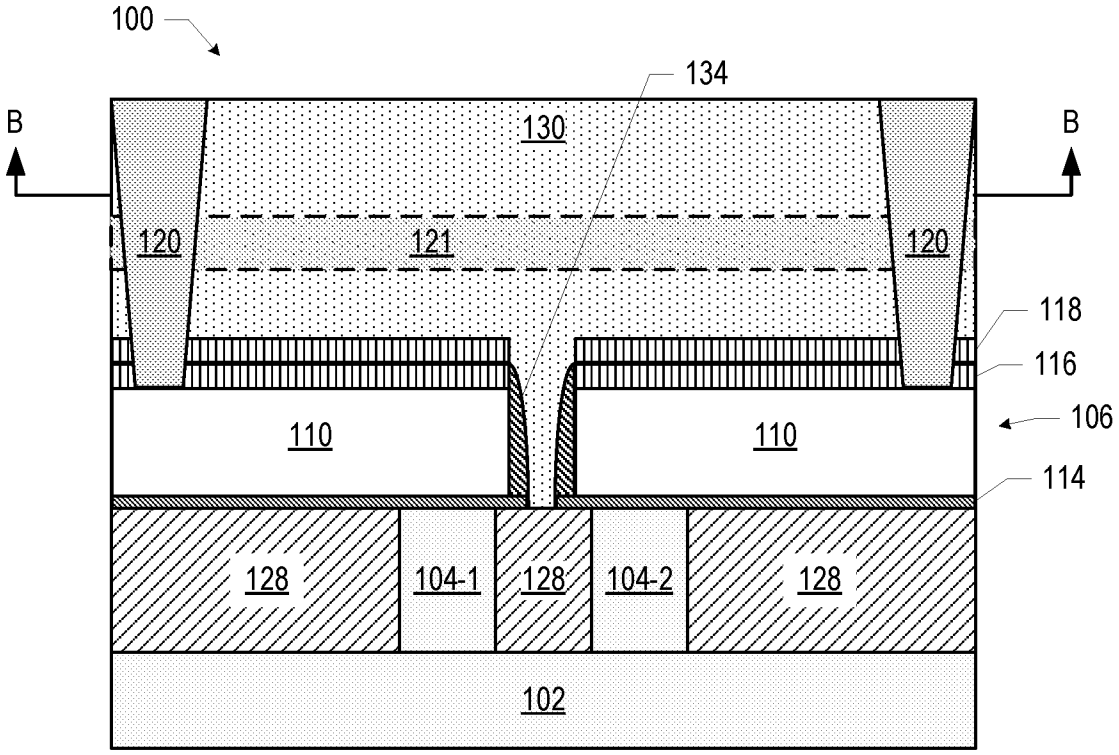

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104-1
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104-2
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102

FIG. 34

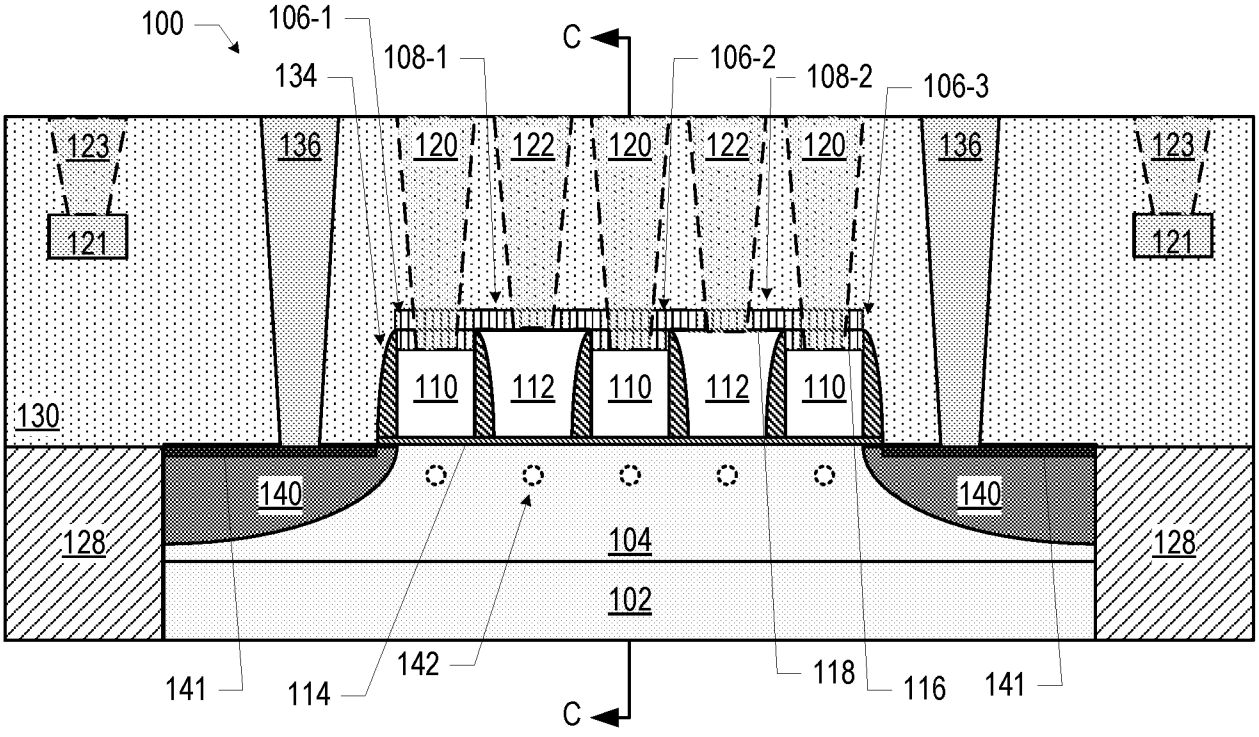

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106-1
108-1
C
106-2
108-2
106-3
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123
136
120
122
120
122
120
136
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121
121
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141
C

FIG. 35

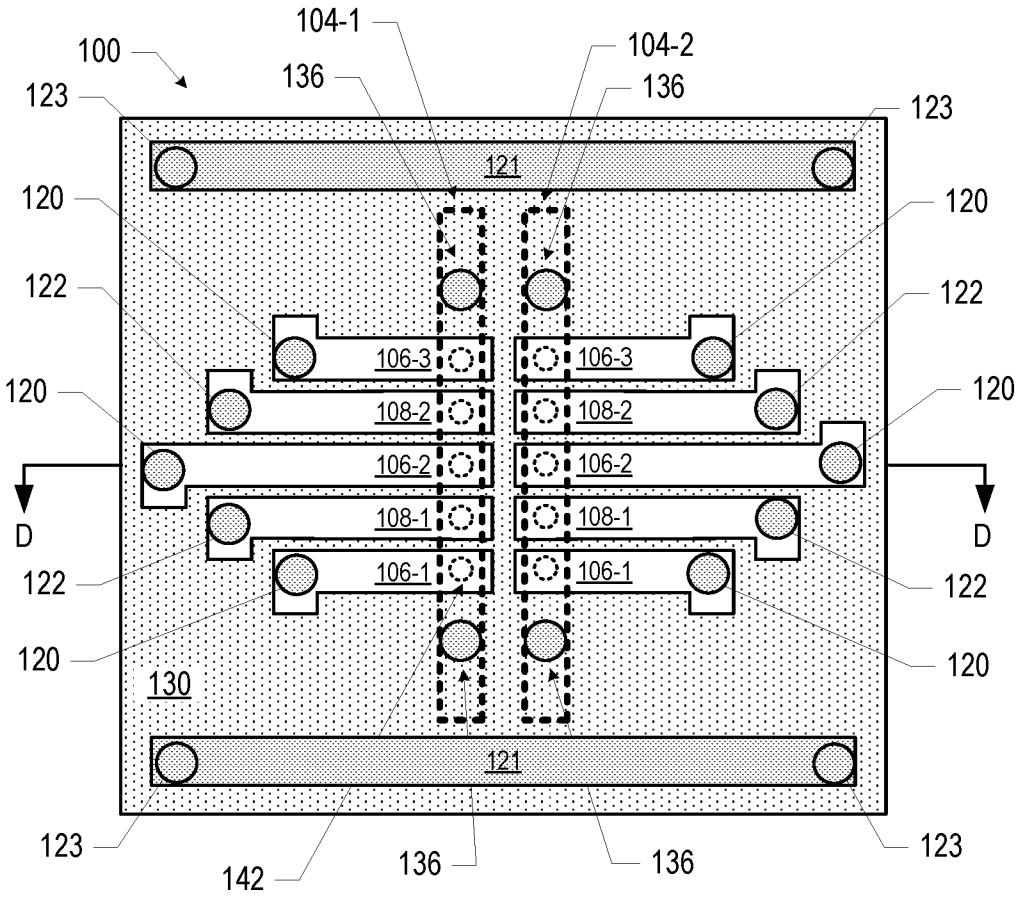

100
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104-2
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136
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123
121
120
120
122
122
106-3
106-3
120
120
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108-2
106-2
106-2
D
D
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122
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106-1
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130
121
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123
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136
136

FIG. 36

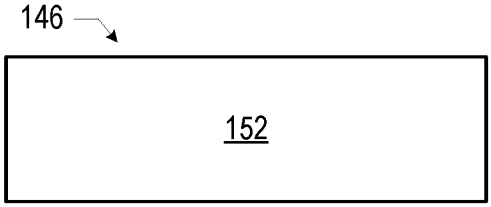


FIG. 37

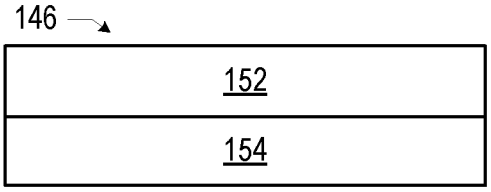


FIG. 38

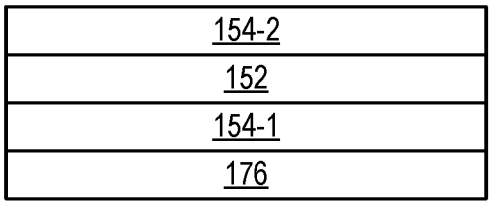


FIG. 39

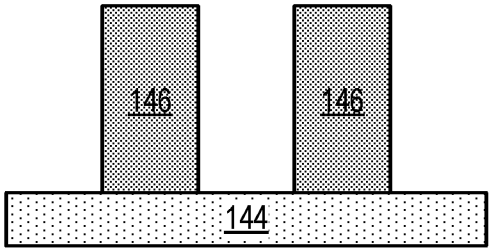


FIG. 40

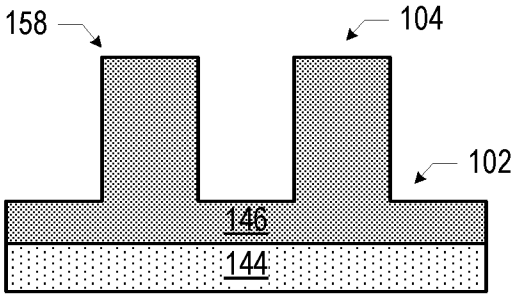


FIG. 41

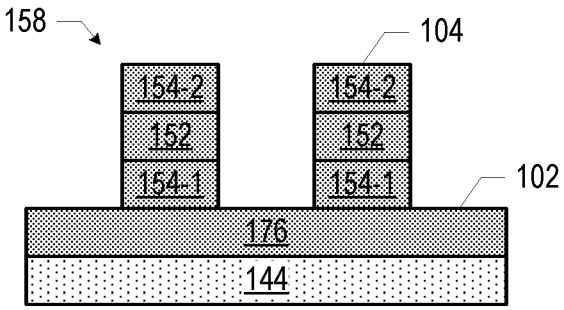


FIG. 42

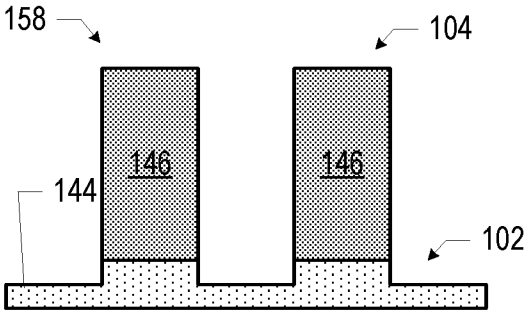


FIG. 43

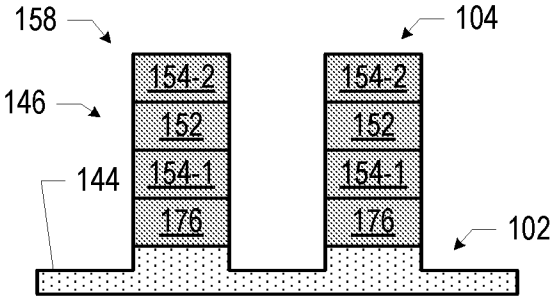


FIG. 44

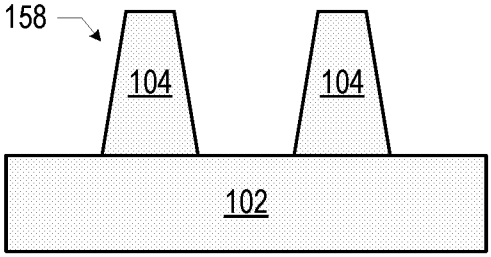


FIG. 45

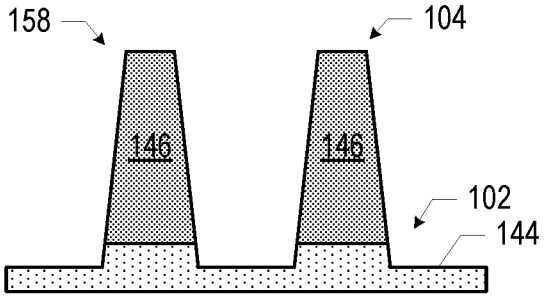


FIG. 46

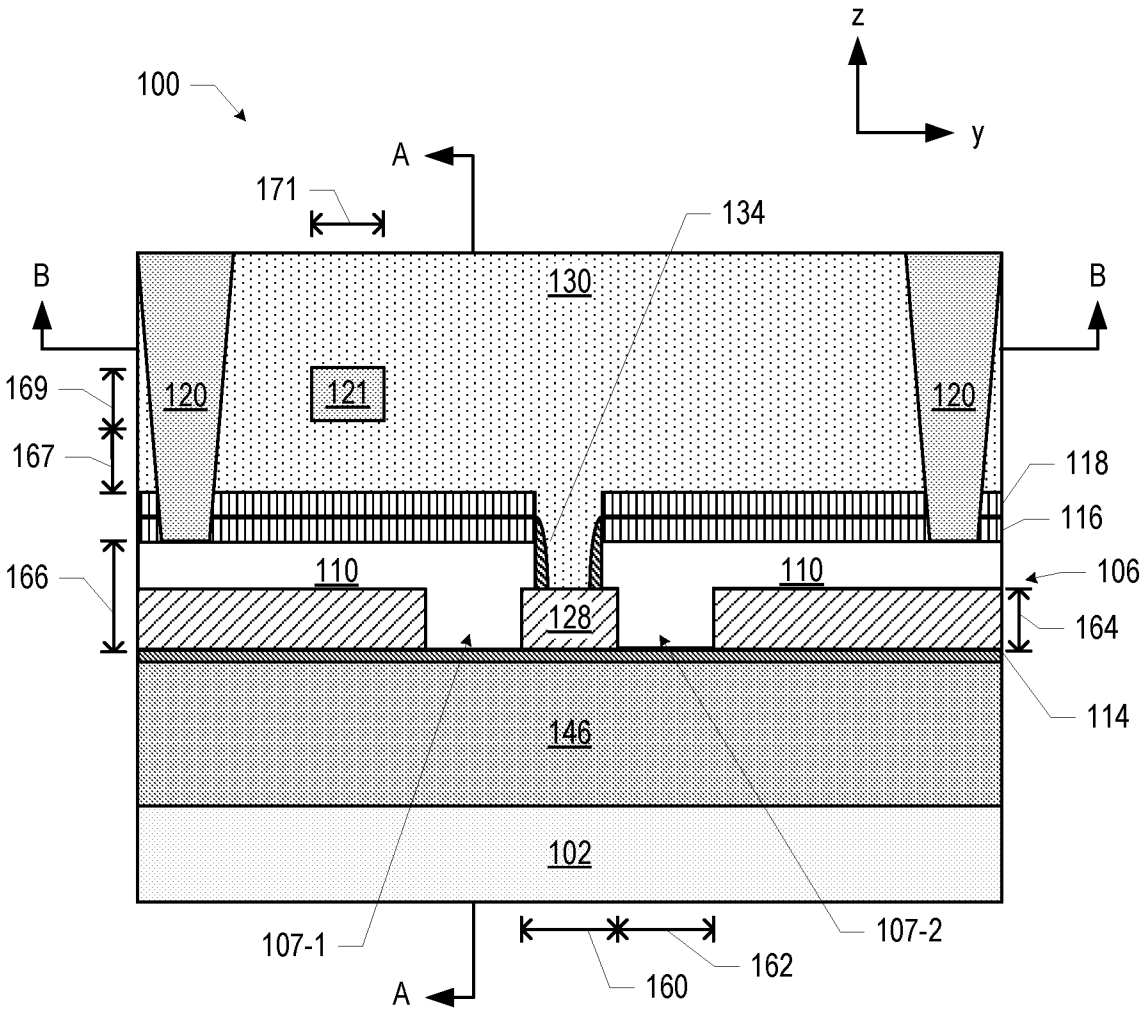

z
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100
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B
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164
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107-1
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162
160
A

FIG. 47

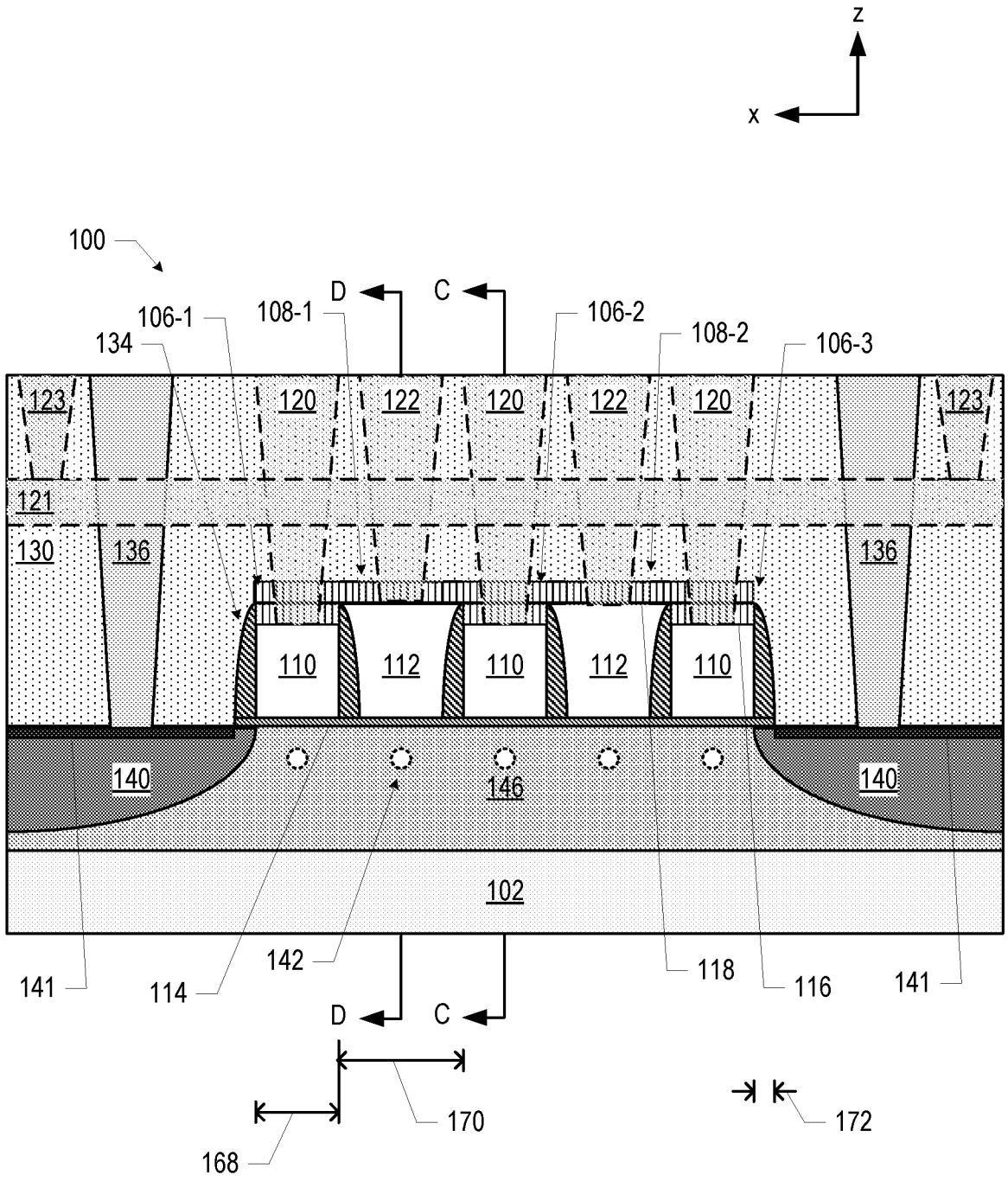

z
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FIG. 48

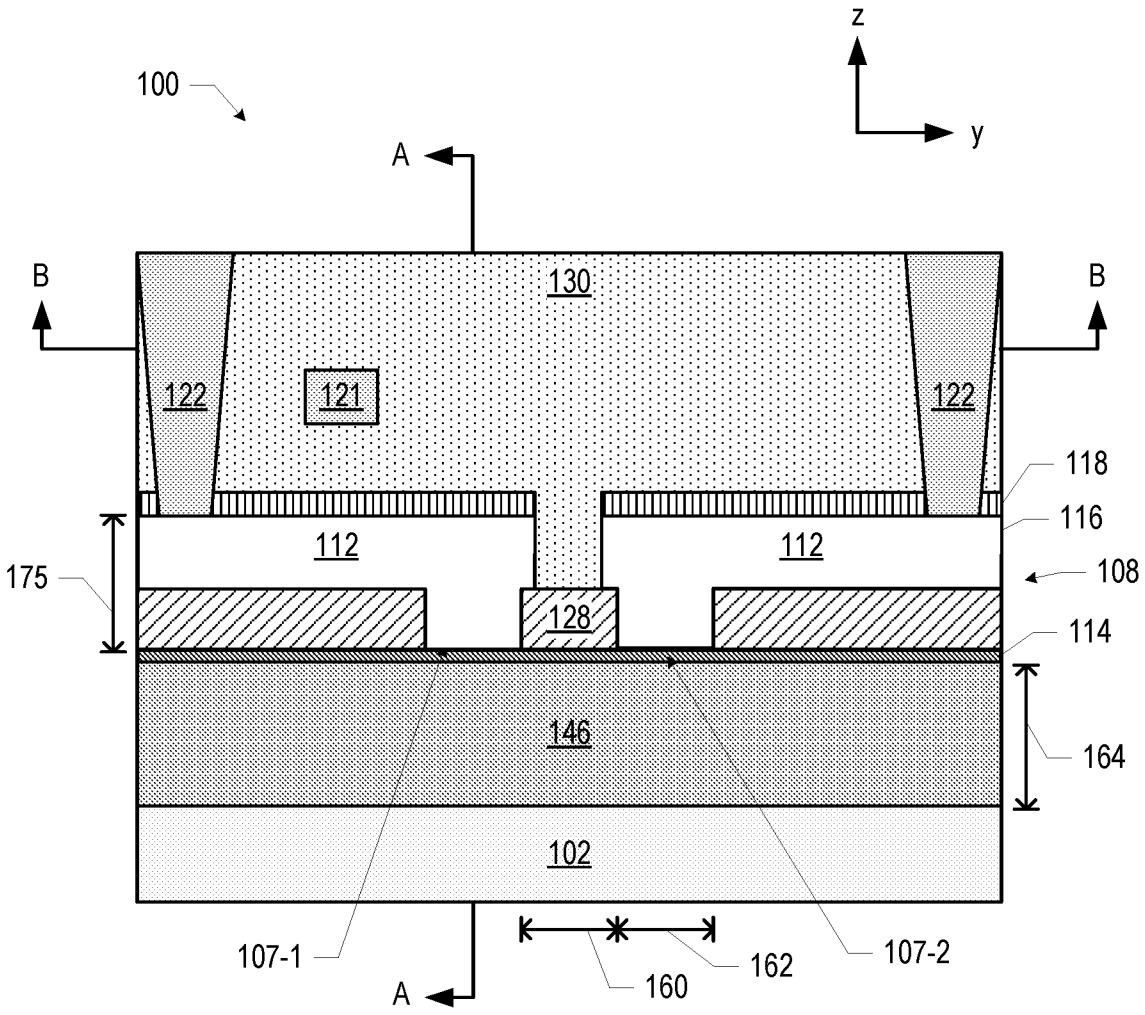

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175
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A

FIG. 49

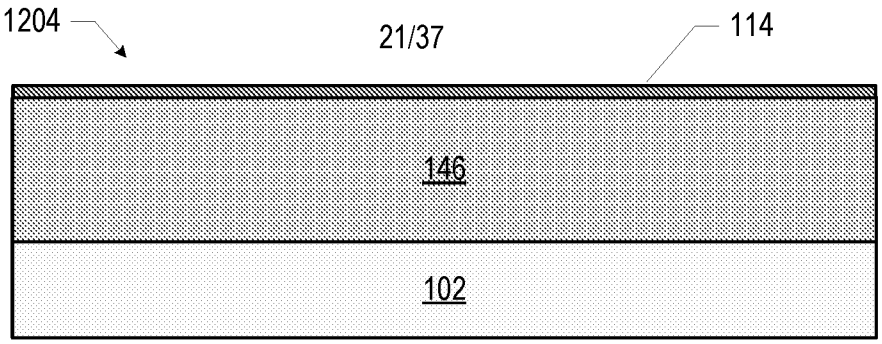


FIG. 50

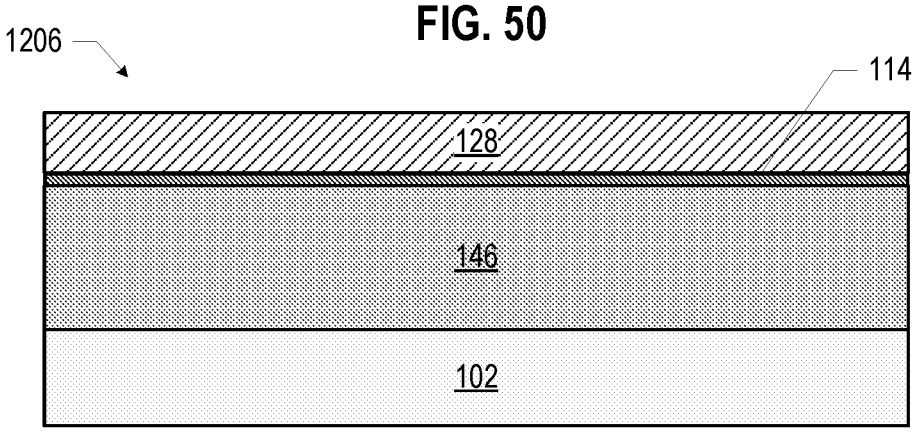


FIG. 51

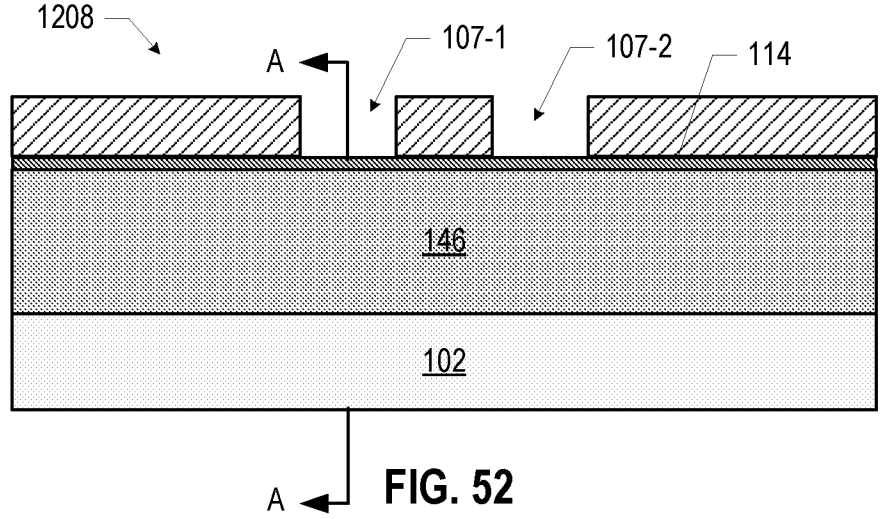


FIG. 52

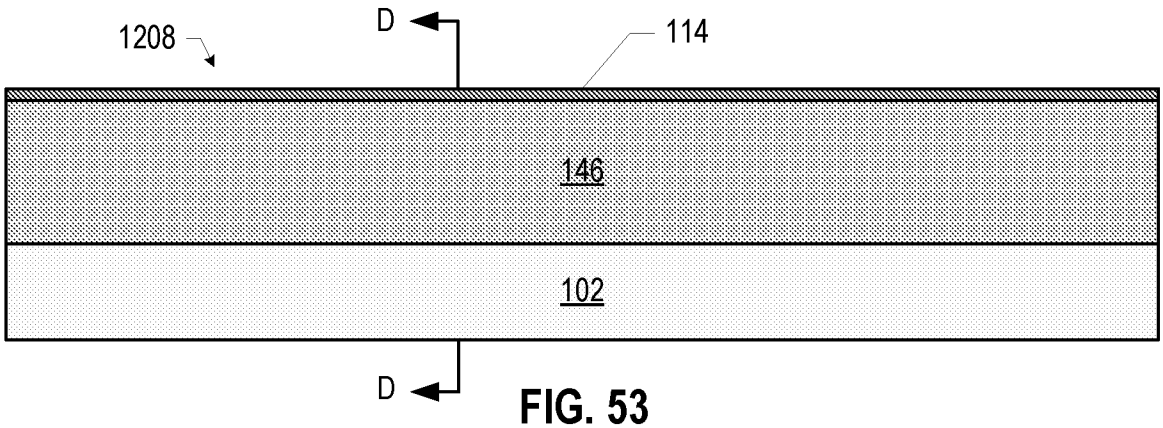


FIG. 53

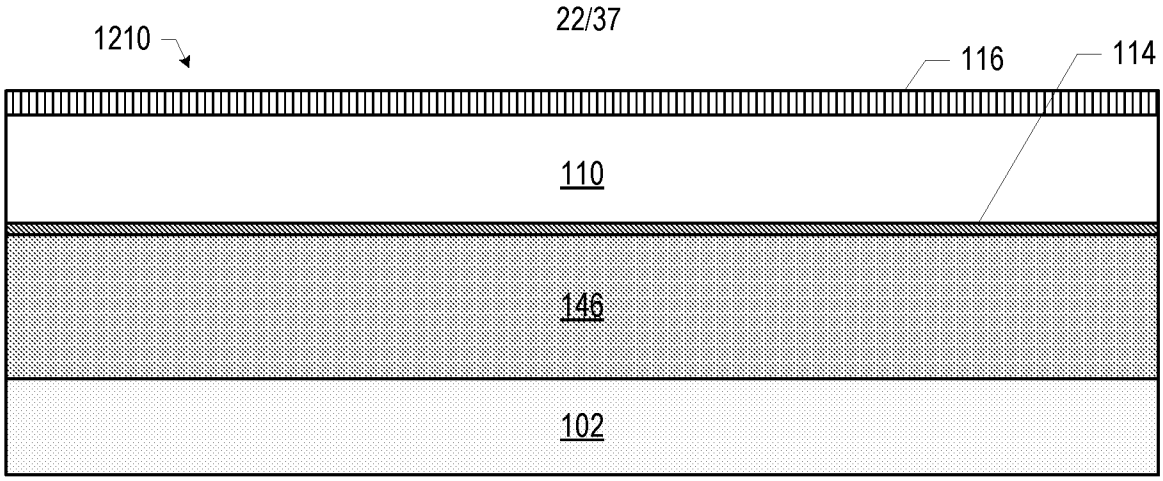


FIG. 54

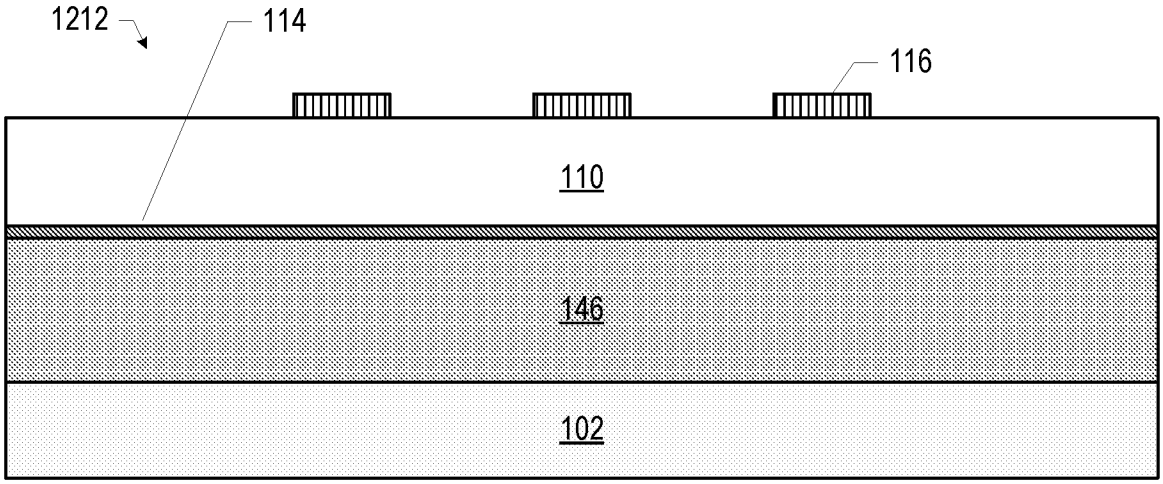


FIG. 55

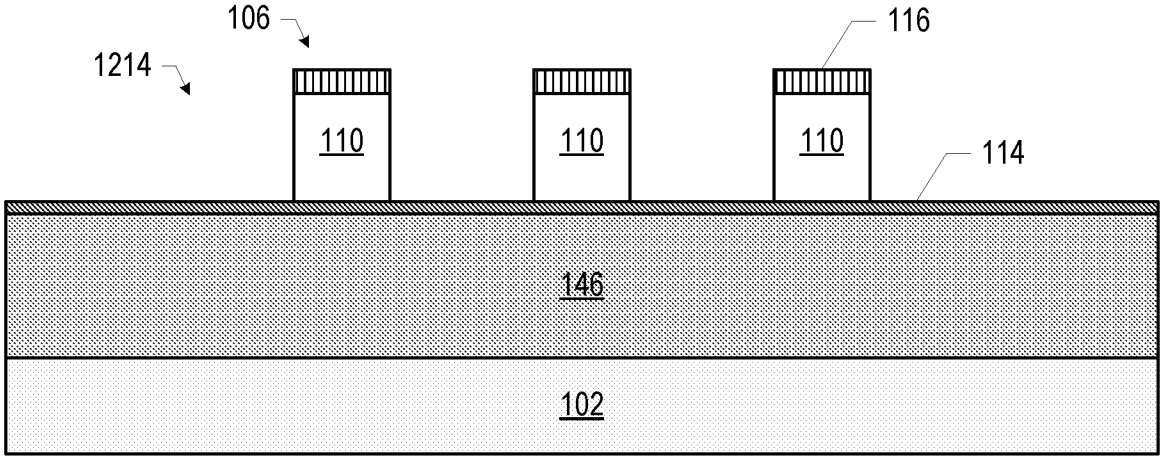


FIG. 56

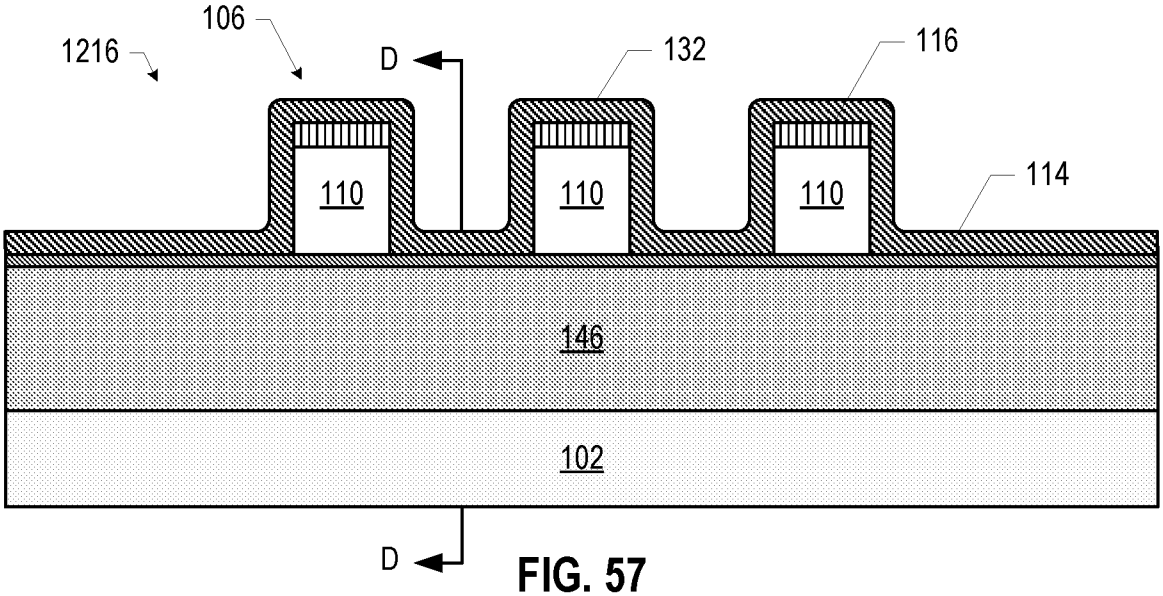

106
1216
D
132
116
110
110
110
114
146
102
D

FIG. 57

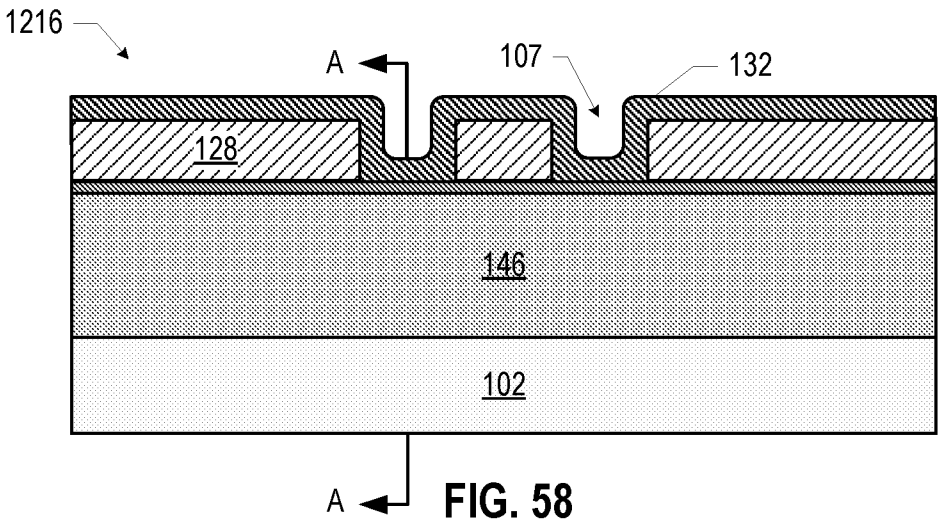

1216
A
107
132
128
146
102
A

FIG. 58

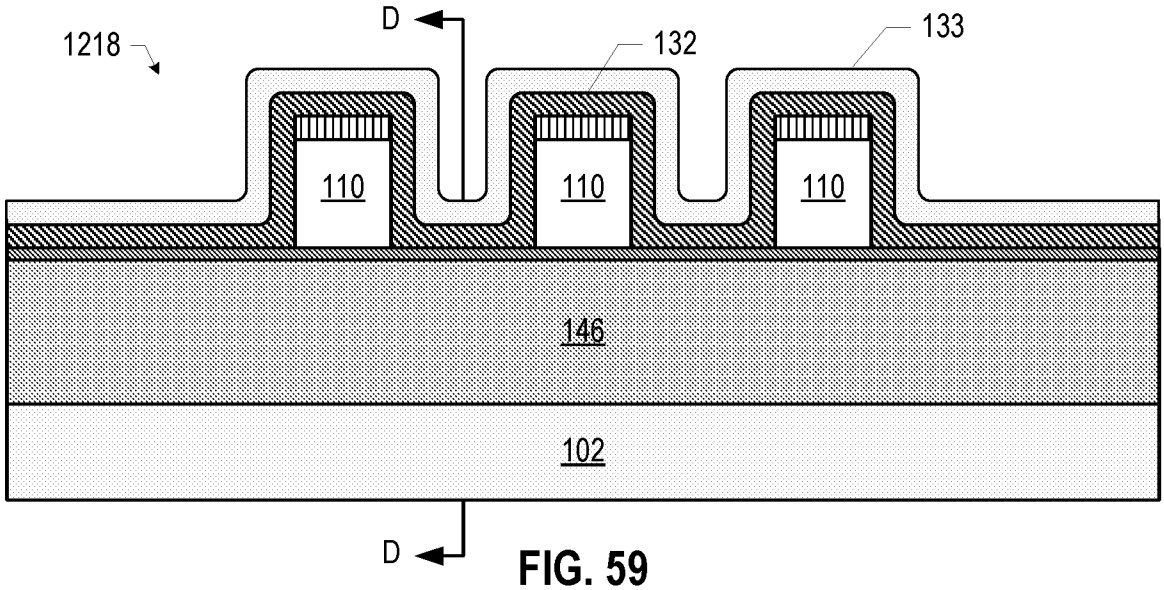

1218
D
132
133
110
110
110
146
102
D

FIG. 59

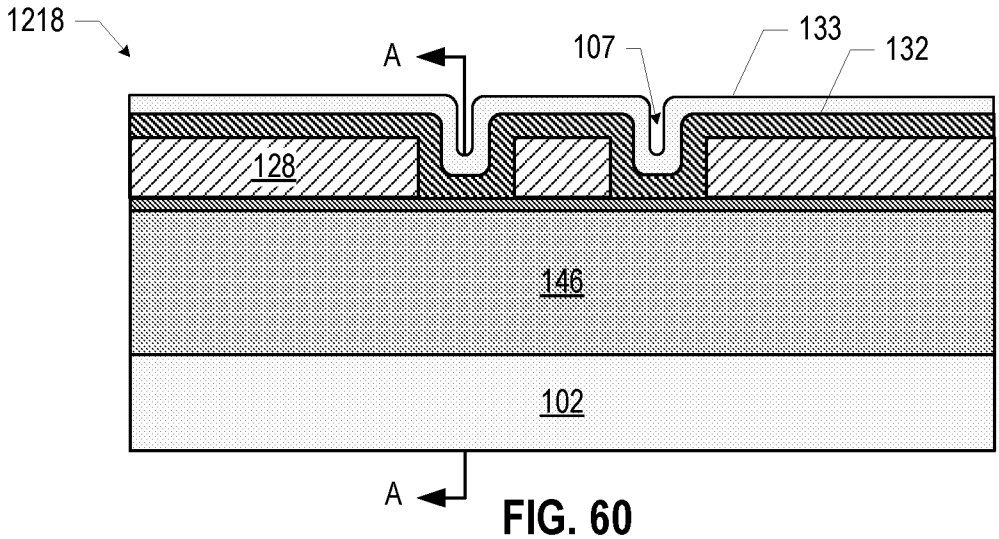

1218
A
107
133
132
128
146
102
A

FIG. 60

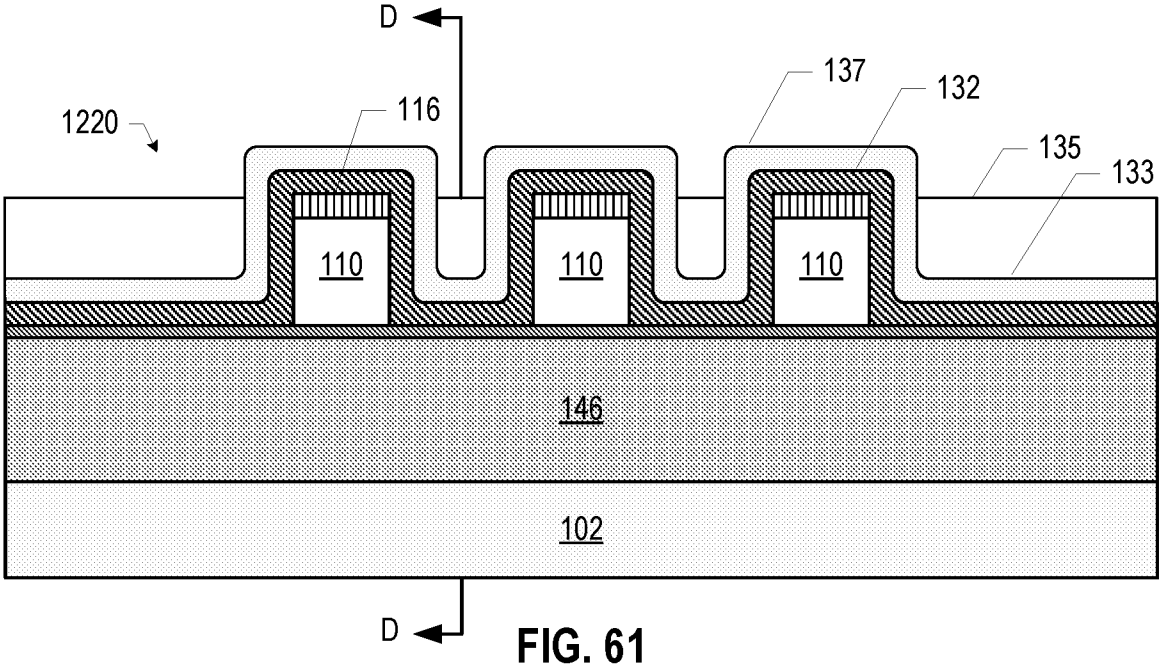

D
1220
116
137
132
135
133
110
110
110
146
102
D

FIG. 61

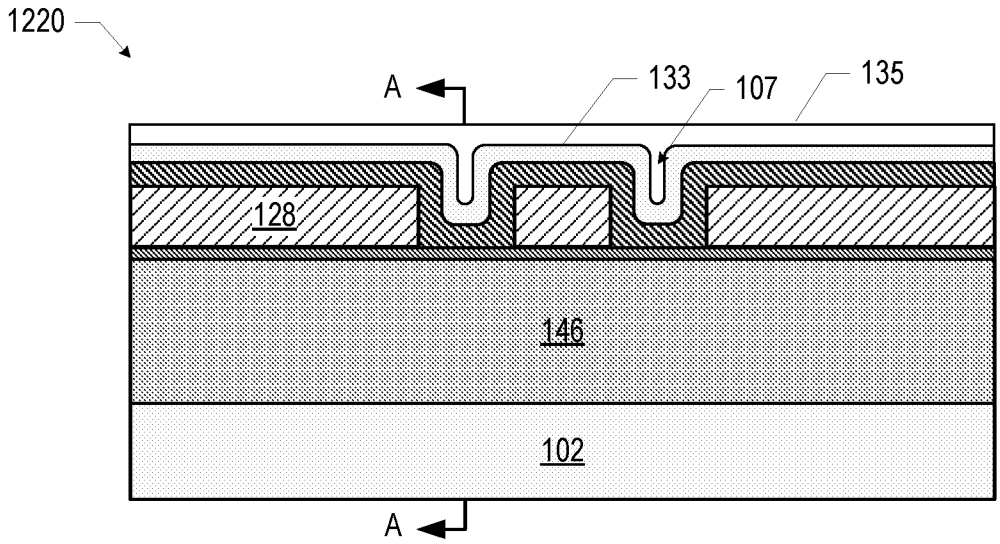

1220
A
133
107
135
128
146
102
A

FIG. 62

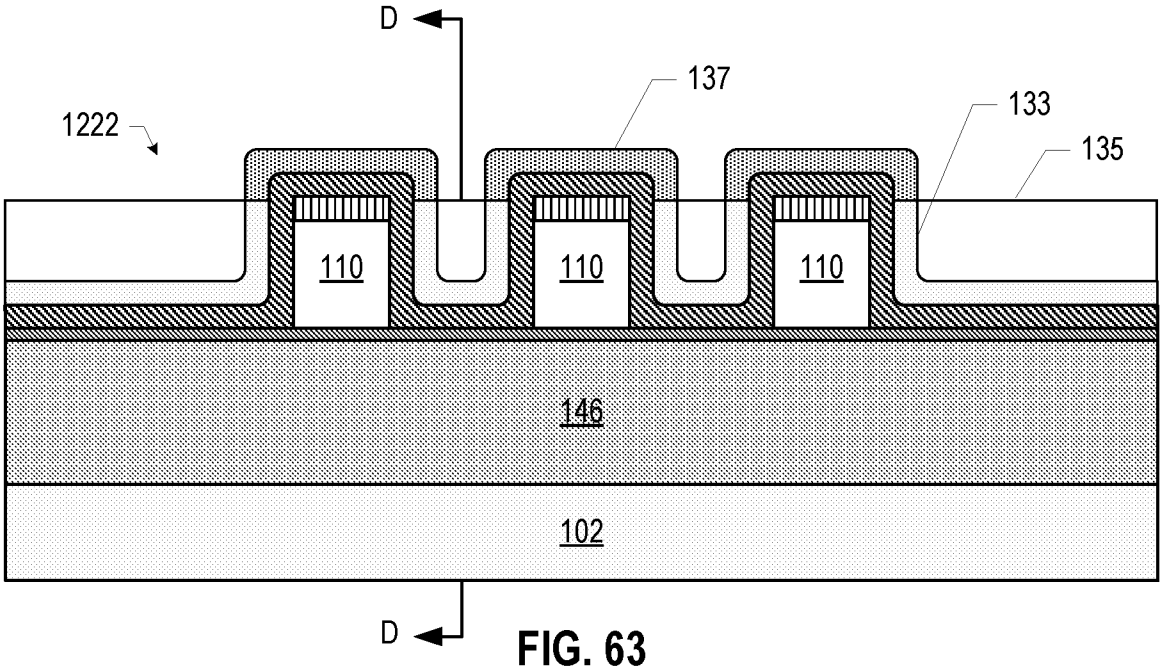

D
137
133
135
1222
110
110
110
146
102
D

FIG. 63

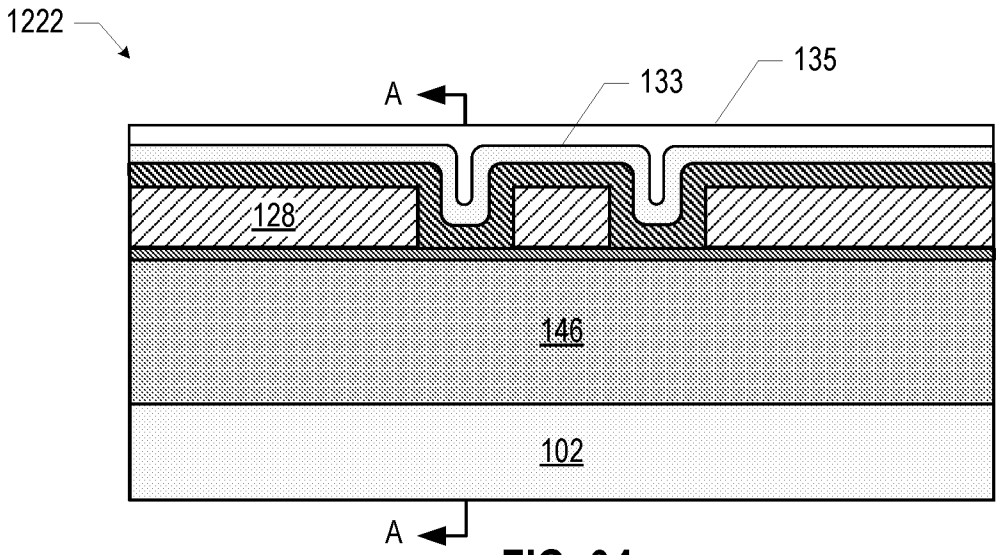

1222
A
133
135
128
146
102
A

FIG. 64

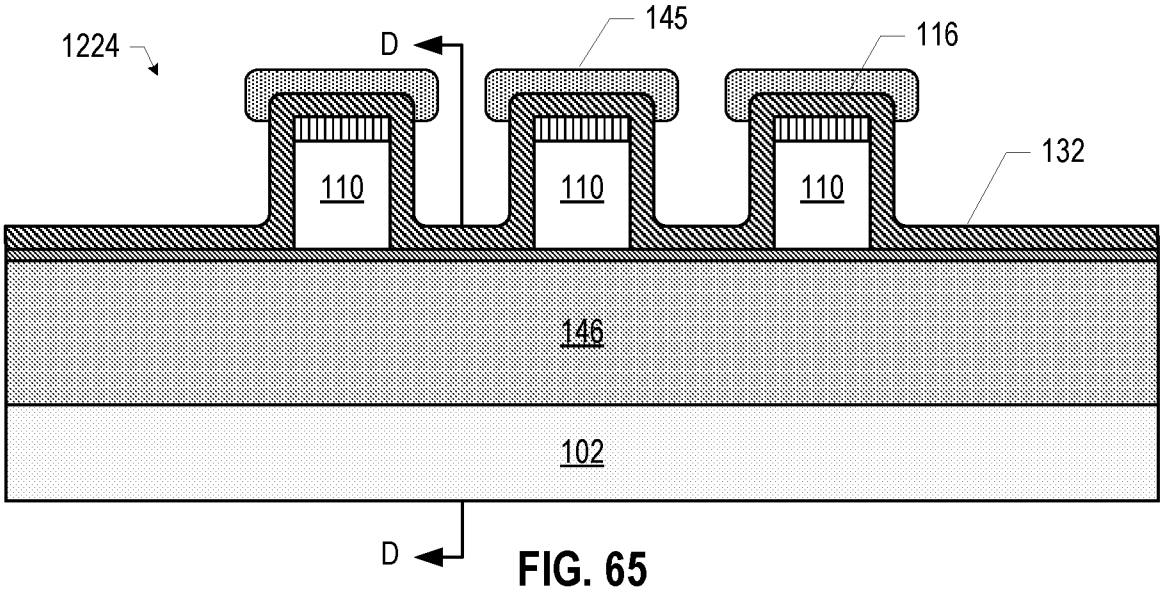

1224
D
145
116
132
110
110
110
146
102
D

FIG. 65

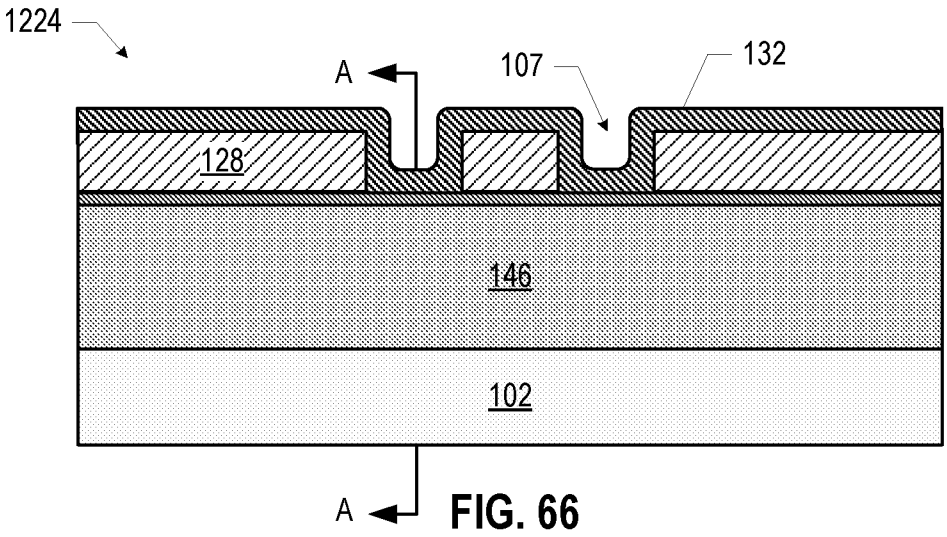

1224
A
107
132
128
146
102
A

FIG. 66

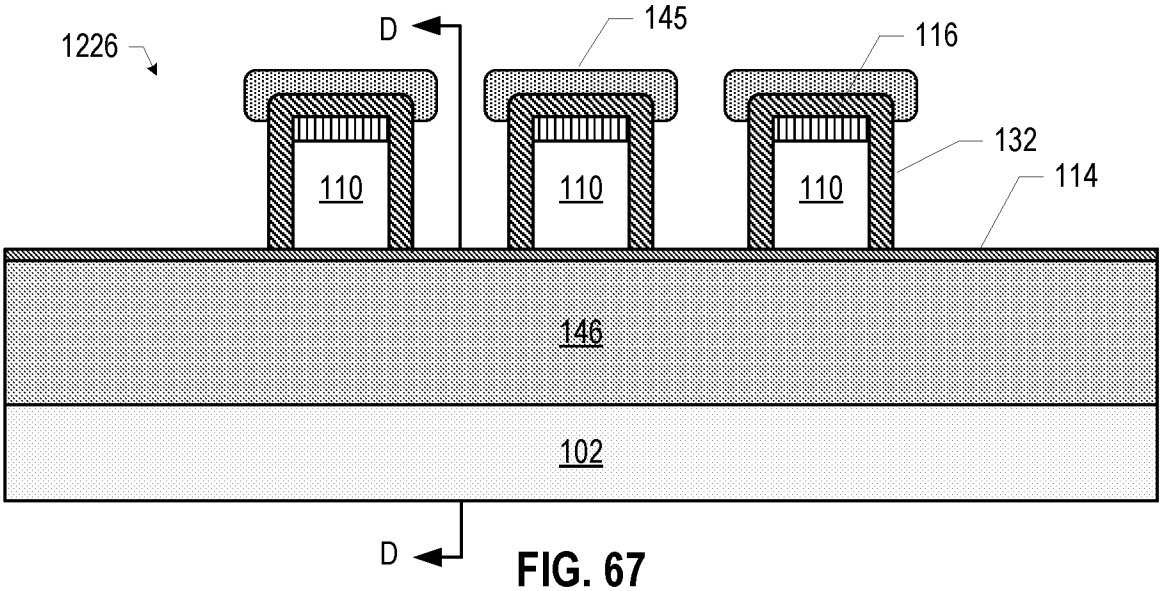

1226
D
145
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114
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146
102
D

FIG. 67

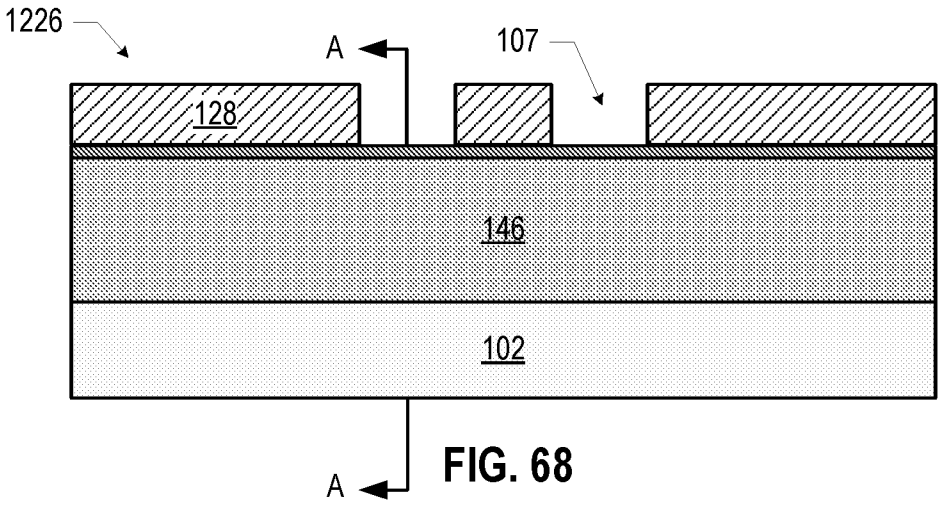

1226
A
107
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A

FIG. 68

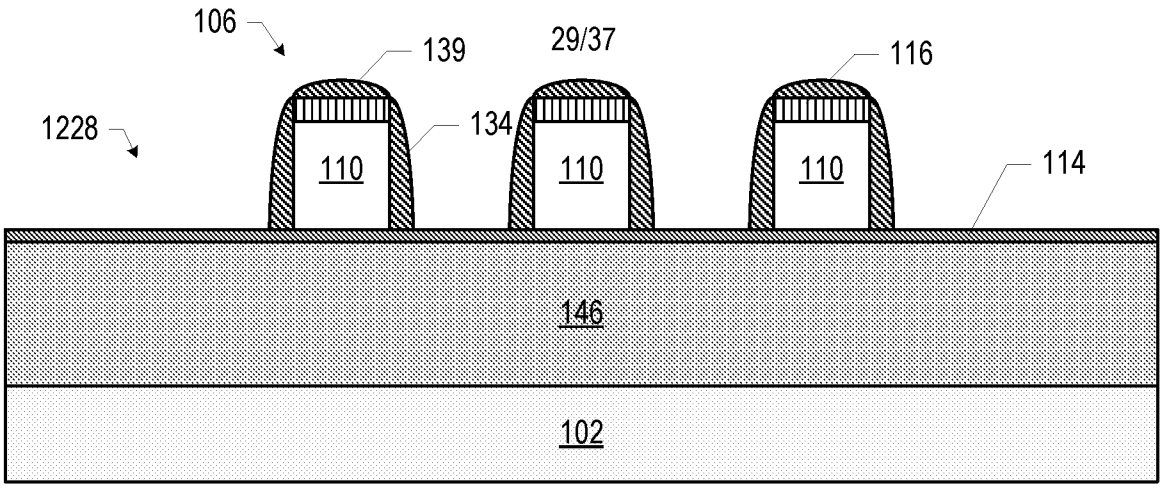


FIG. 69

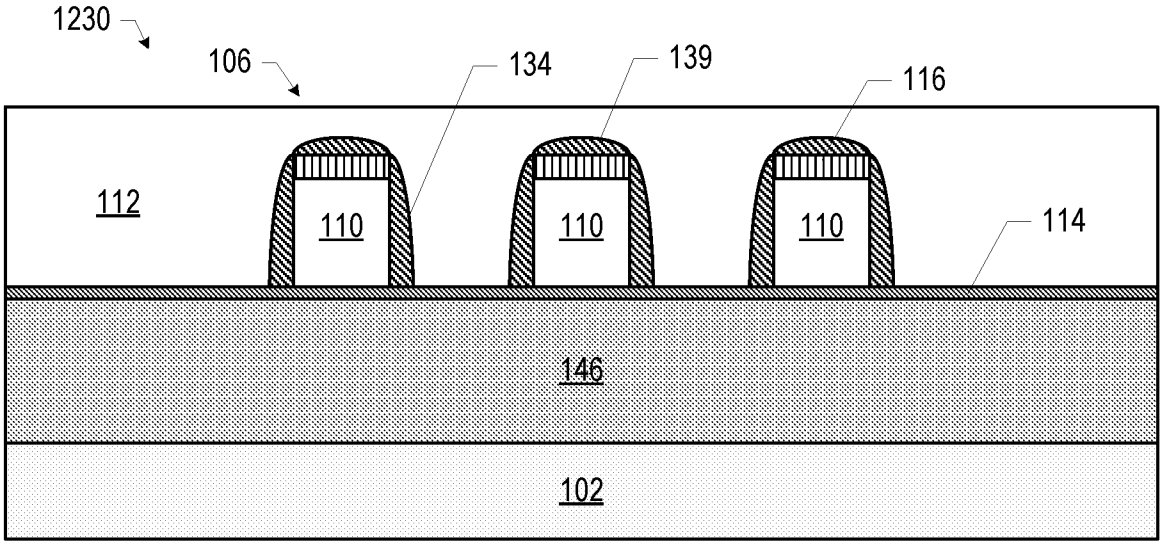


FIG. 70

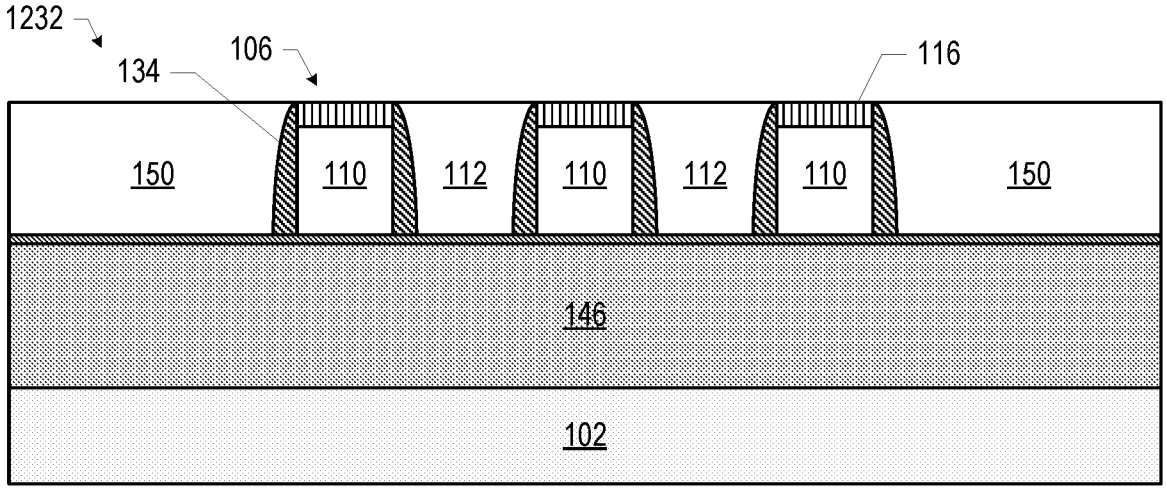


FIG. 71

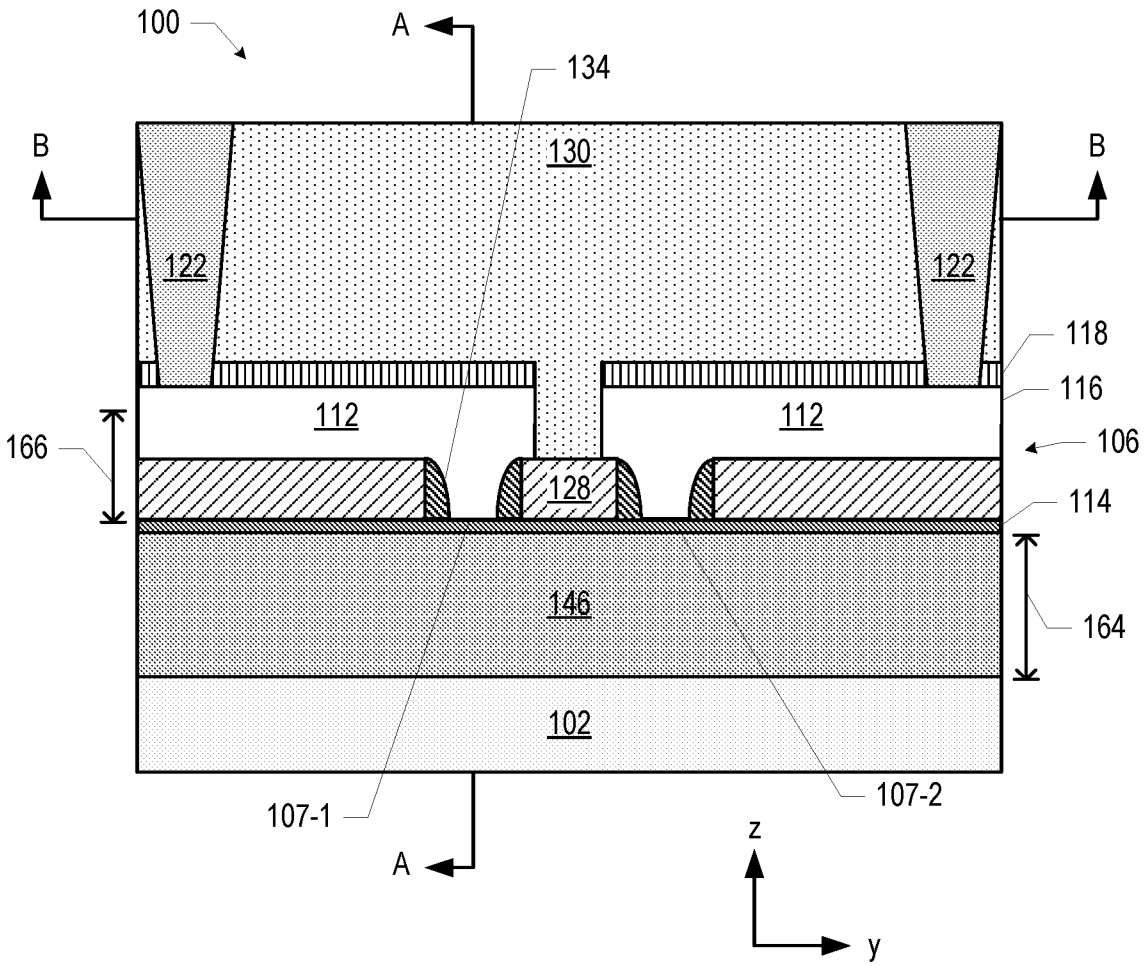

100
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134
B
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B
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122
118
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112
112
166
106
128
114
146
164
102
107-1
107-2
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z
y

FIG. 72

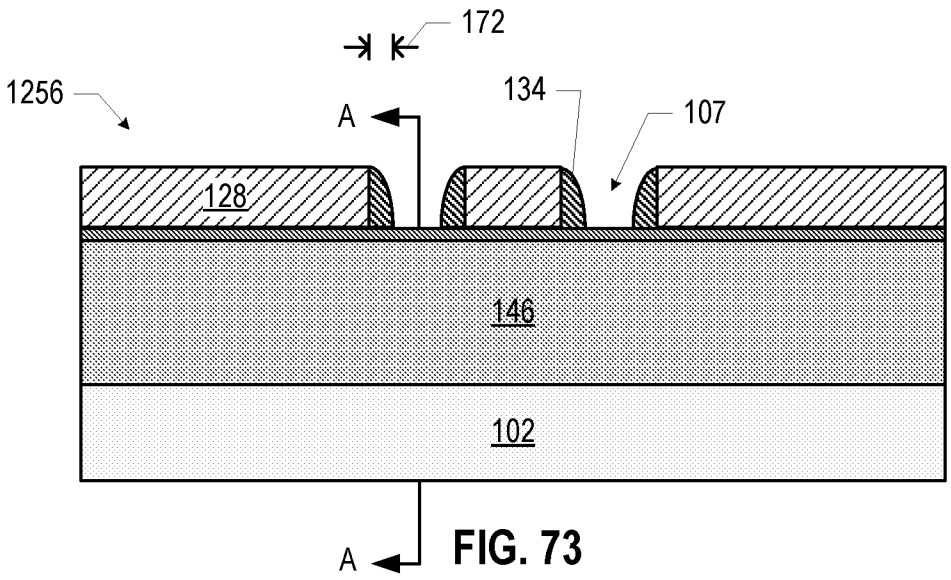
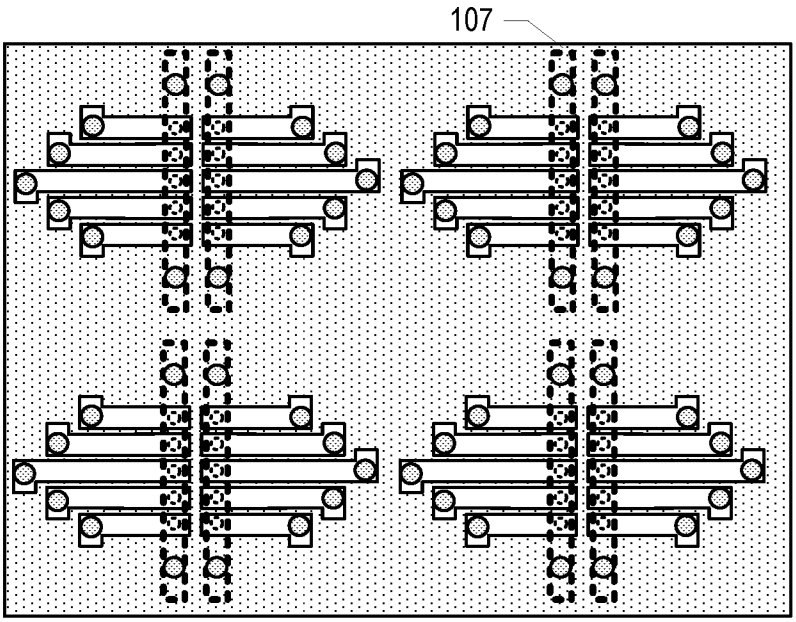

172
1256
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107
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A

FIG. 73

FIG. 74



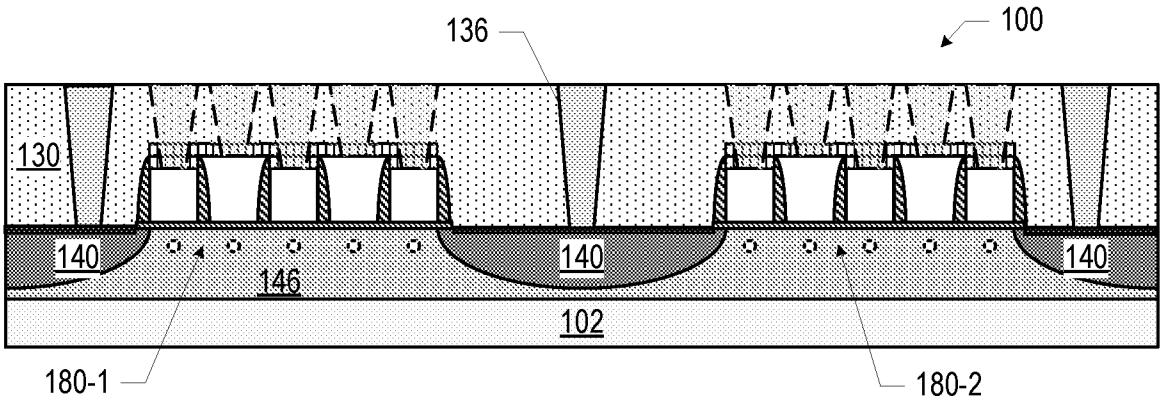


FIG. 75

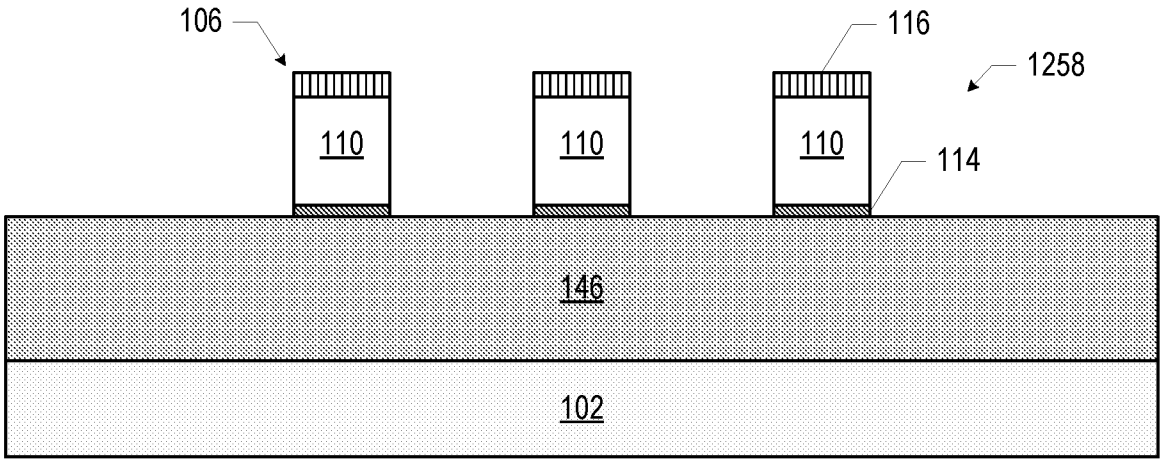


FIG. 76

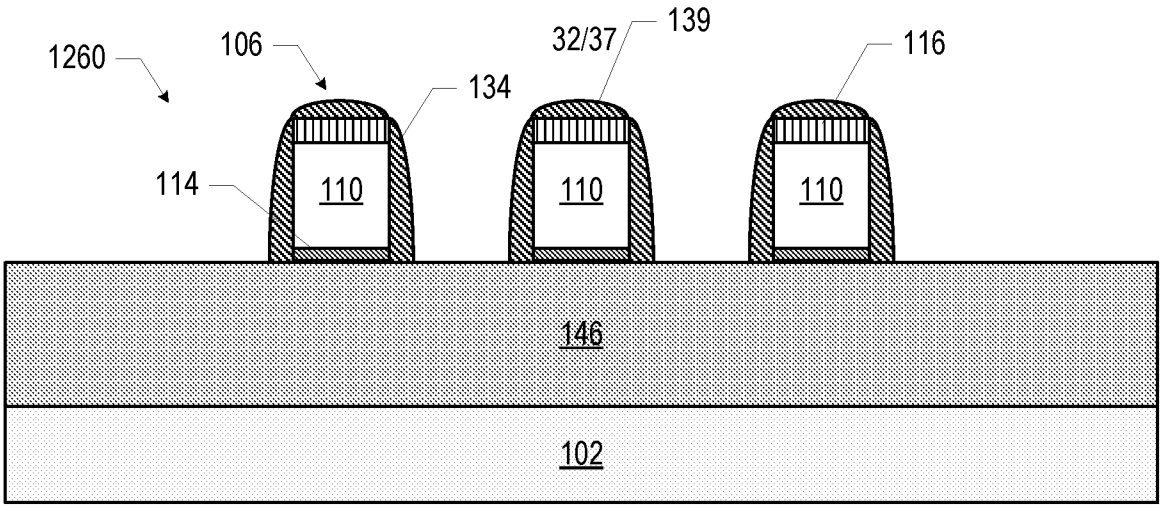


FIG. 77

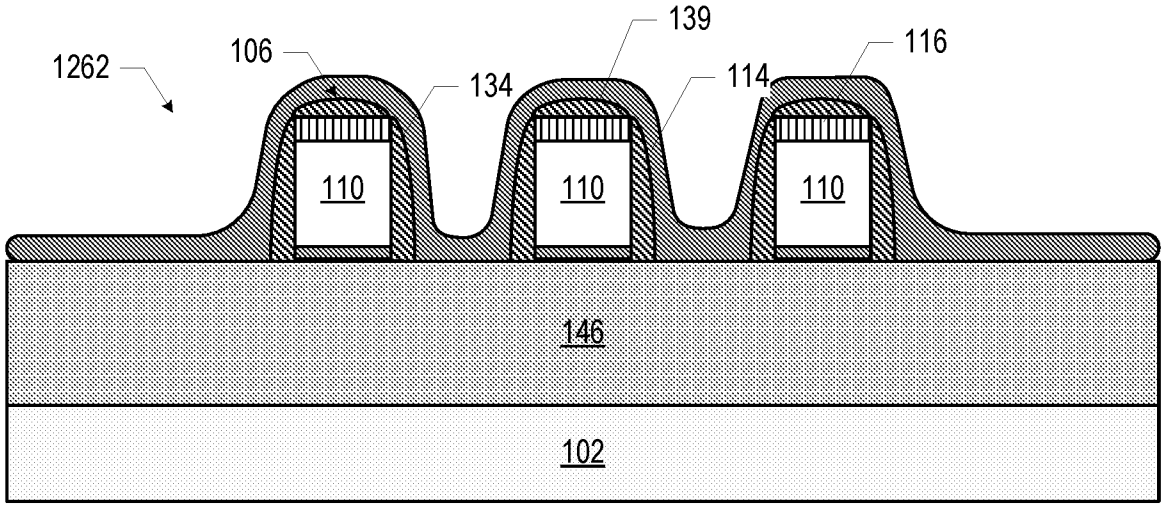


FIG. 78

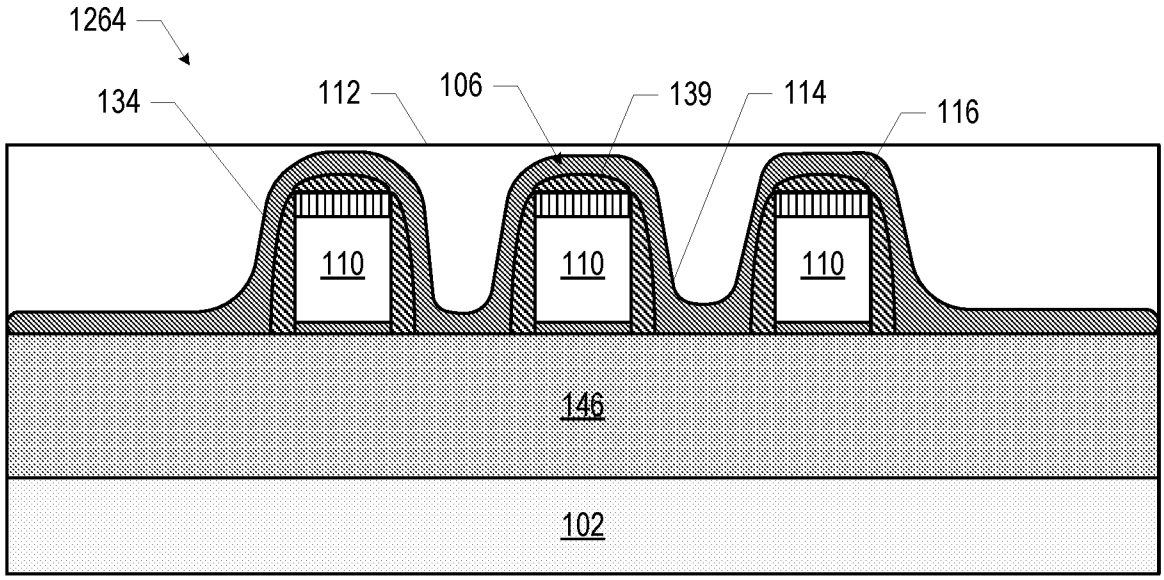


FIG. 79

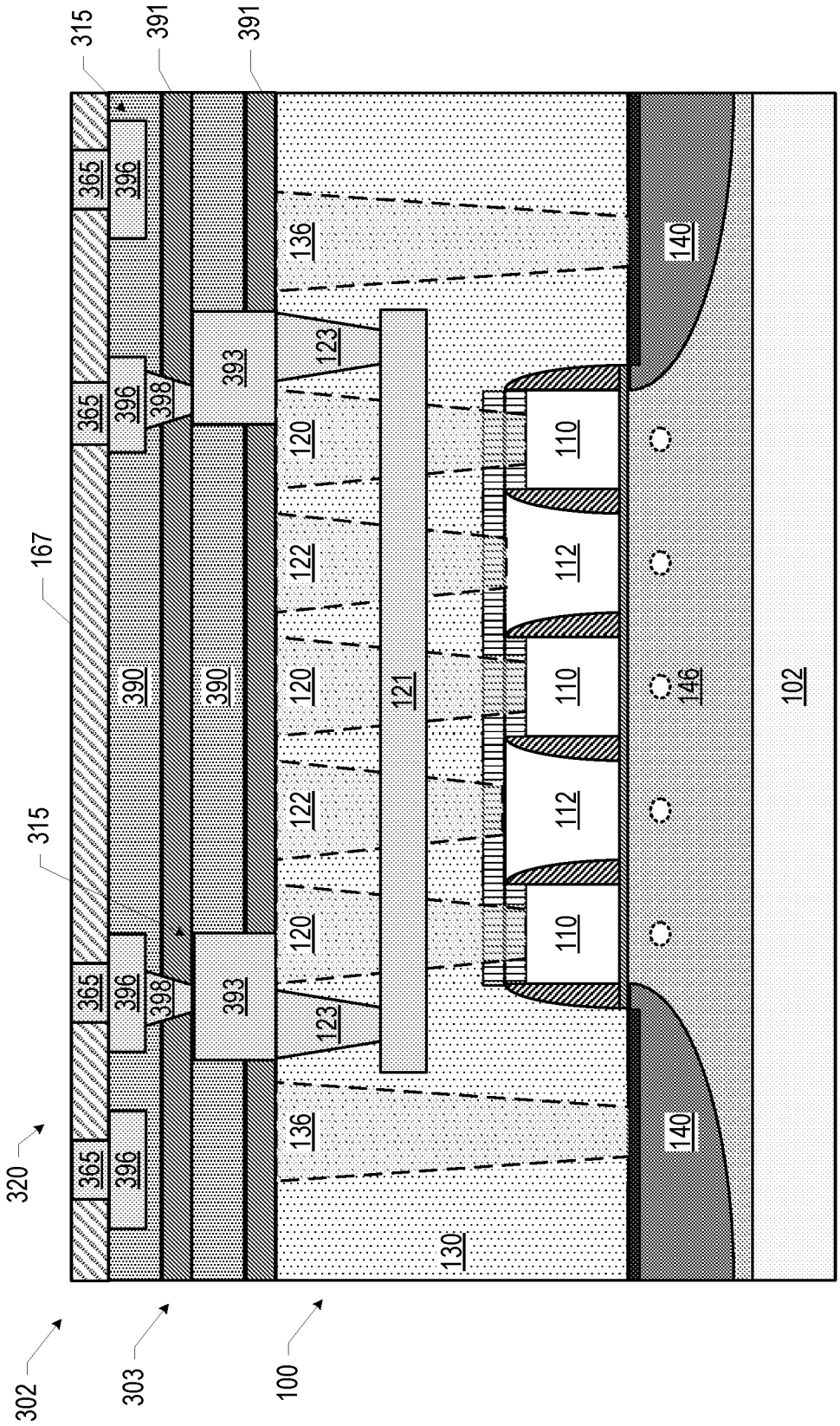

315
391
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365
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140
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123
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167
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110
146
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315
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365
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393
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136
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302
303
100

FIG. 80

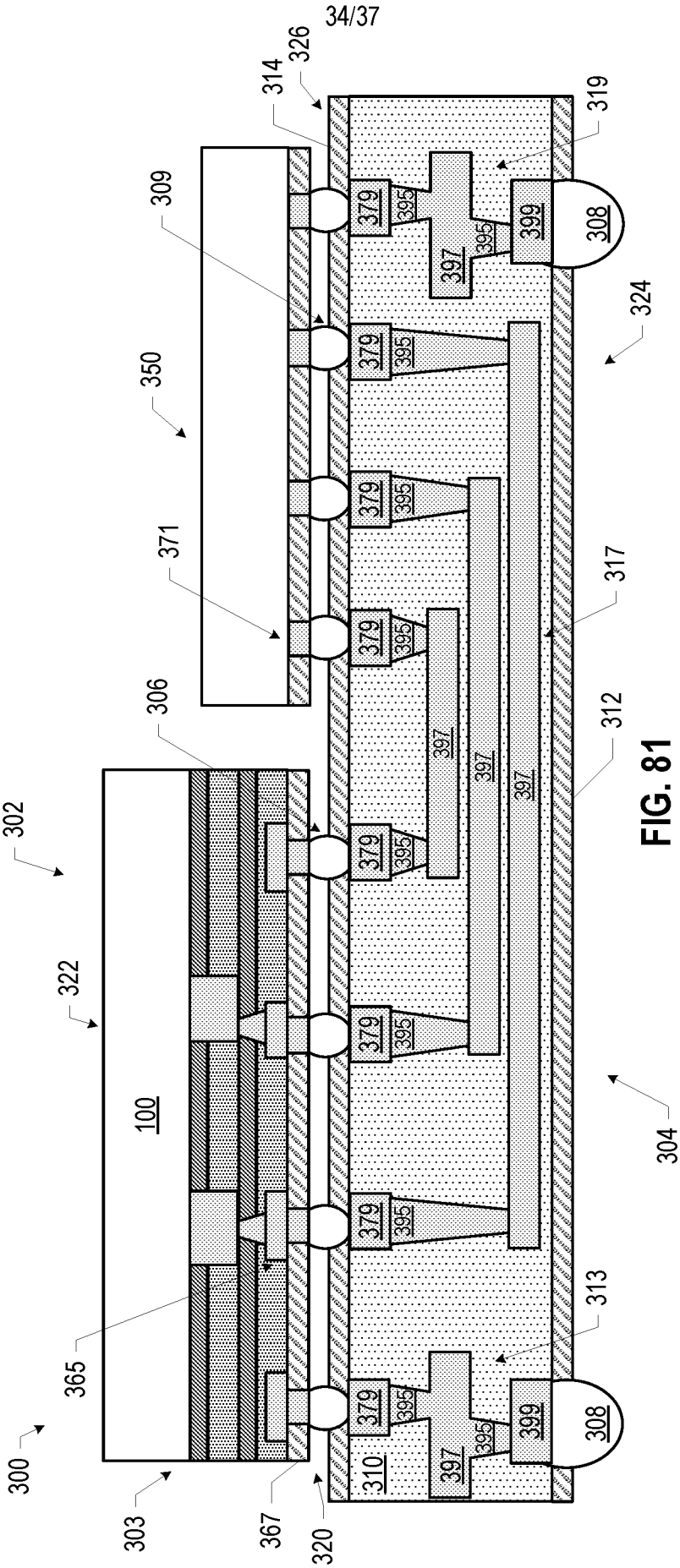

326
314
319
309
379
395
397
399
308
324
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371
317
306
312
302
322
100
304
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303
367
320
310

FIG. 81

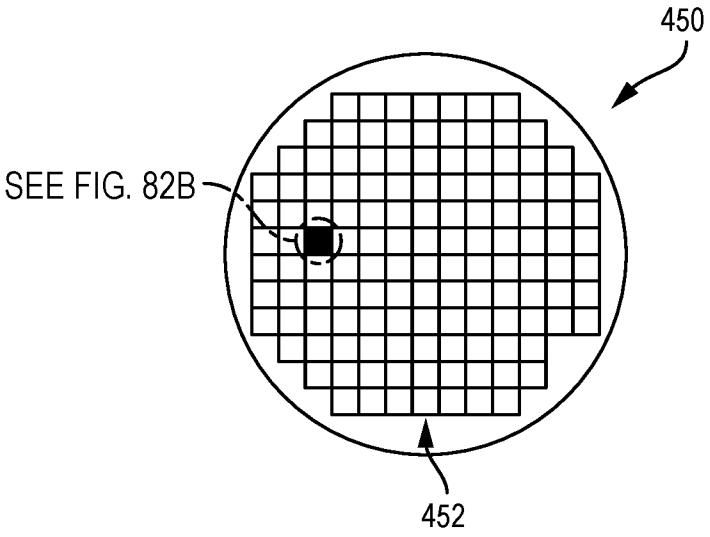


FIG. 82A

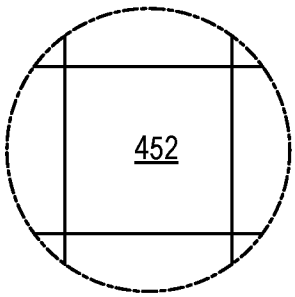


FIG. 82B

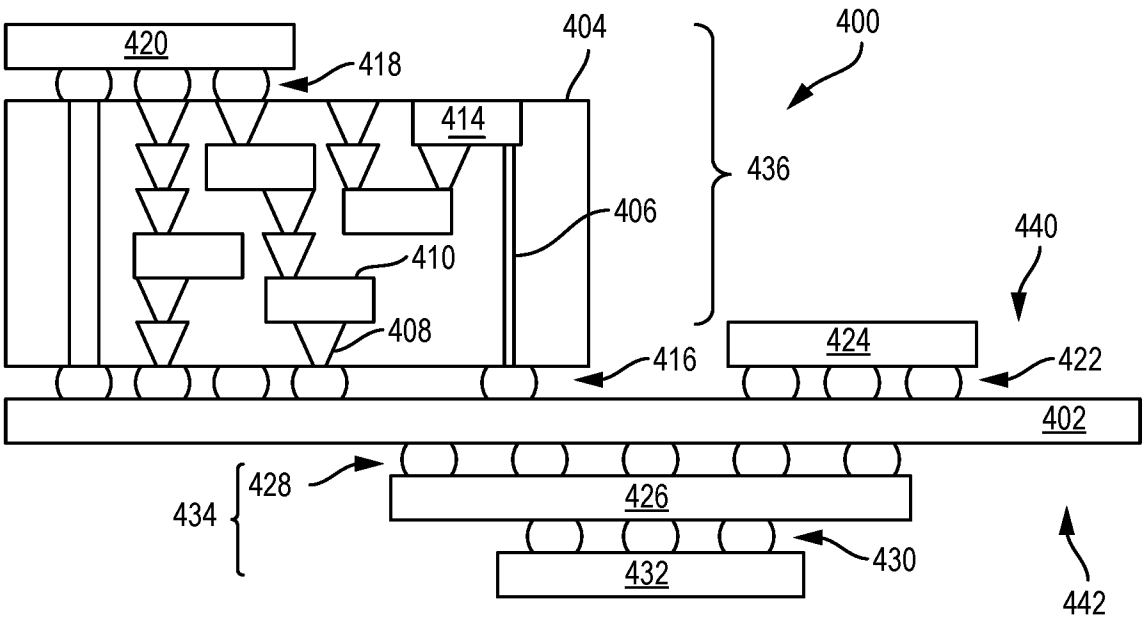


FIG. 83

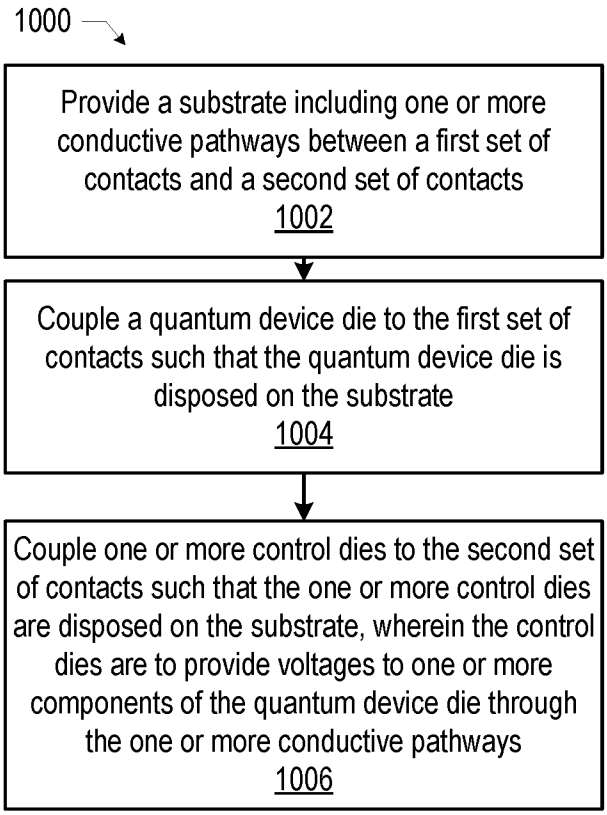


FIG. 84

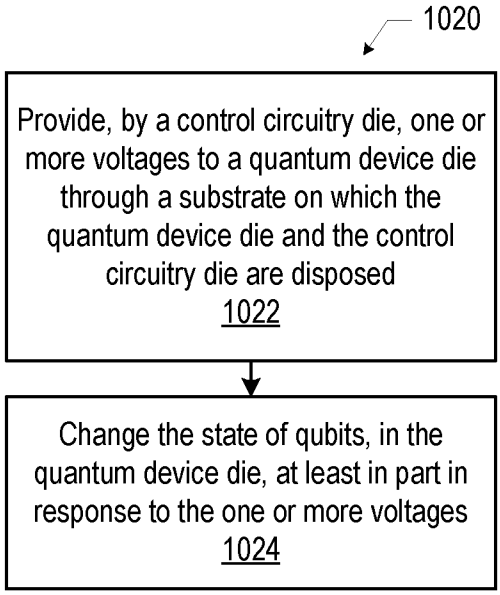


FIG. 85

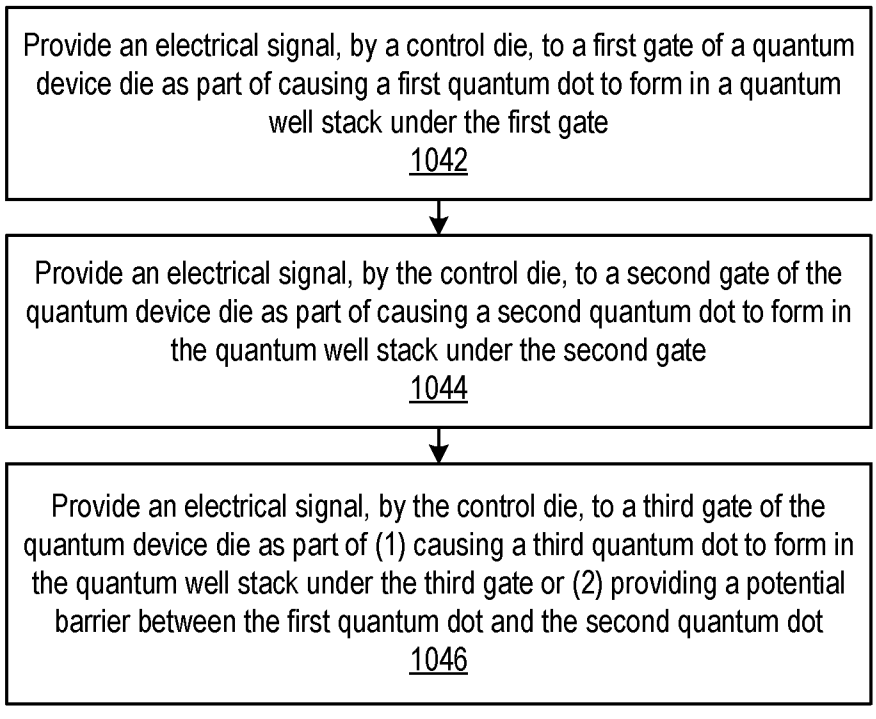


FIG. 86

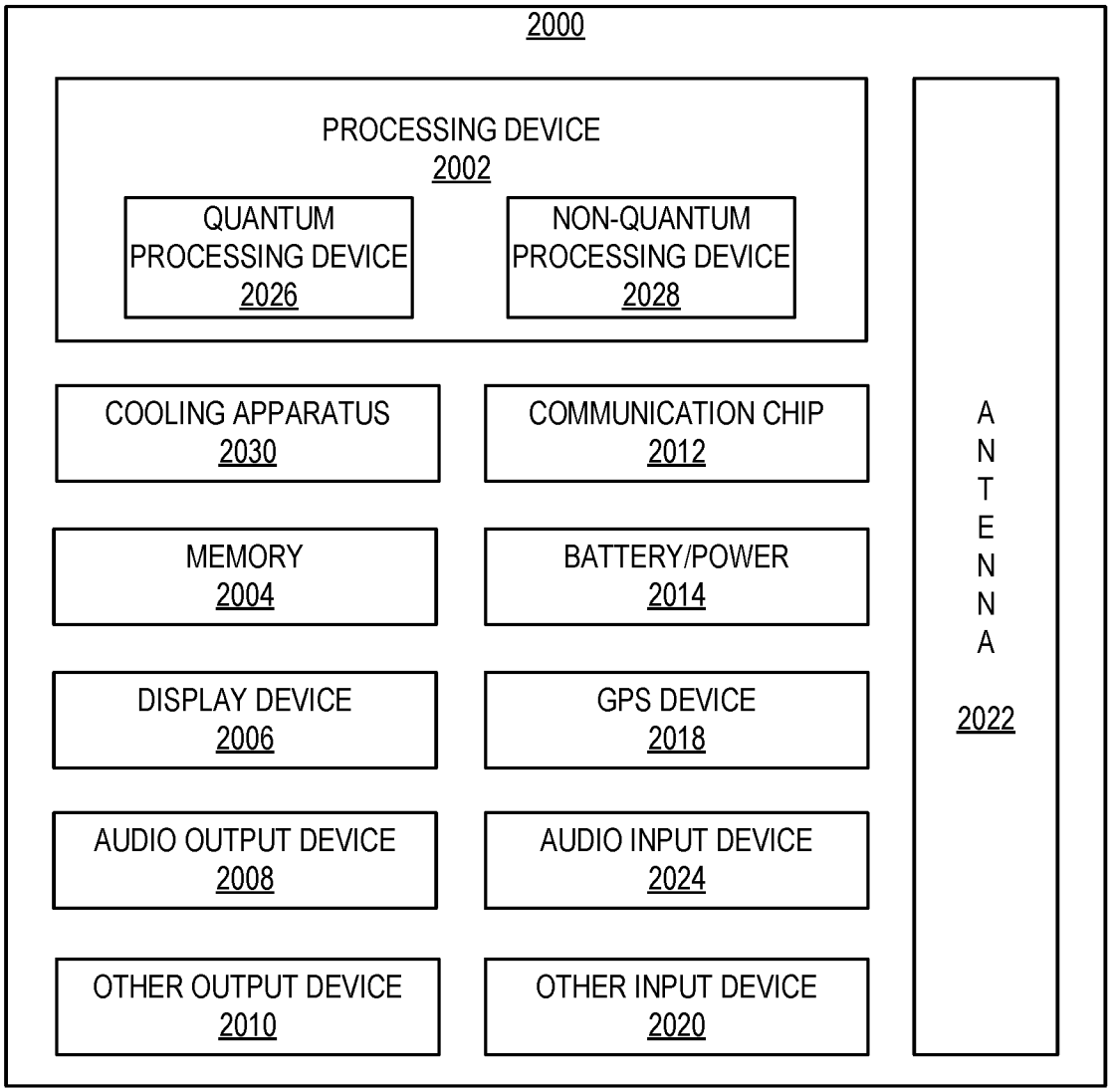

2000
PROCESSING DEVICE
2002
QUANTUM PROCESSING DEVICE
2026
NON-QUANTUM PROCESSING DEVICE
2028
COOLING APPARATUS
2030
COMMUNICATION CHIP
2012
MEMORY
2004
BATTERY/POWER
2014
DISPLAY DEVICE
2006
GPS DEVICE
2018
AUDIO OUTPUT DEVICE
2008
AUDIO INPUT DEVICE
2024
OTHER OUTPUT DEVICE
2010
OTHER INPUT DEVICE
2020
ANTENNA
2022

FIG. 87

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/054294

A. CLASSIFICATION OF SUBJECT MATTER

H01L 25/07(2006.01)i, H01L 25/16(2006.01)i, H01L 25/11(2006.01)i, H01L 29/12(2006.01)i, H01L 29/775(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 25/07; H04L 9/08; G06N 99/00; H03K 19/195; H01L 31/0328; H01L 29/06; G06F 15/76; H01L 39/22; G06F 7/58; H01L 25/16; H01L 25/11; H01L 29/12; H01L 29/775

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: quantum, qubit, control, die, substrate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2015-0046681 A1 (D-WAVE SYSTEMS INC.) 12 February 2015 See paragraphs [0055]-[0056] and figure 1.	1-25
A	US 2015-0200778 A1 (THE REGENTS OF THE UNIVERSITY OF MICHIGAN) 16 July 2015 See paragraphs [0030]-[0049] and figures 1-2A.	1-25
A	WO 2015-143439 A1 (GOOGLE INC.) 24 September 2015 See claim 1 and figure 1.	1-25
A	US 2002-0179897 A1 (MARK A. ERIKSSON et al.) 05 December 2002 See paragraphs [0035]-[0050] and figures 1-2.	1-25
A	US 2006-0225165 A1 (ALEC MAASSEN VAN DEN BRINK et al.) 05 October 2006 See paragraph [0104] and figure 11.	1-25

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 June 2017 (29.06.2017)	**29 June 2017 (29.06.2017)**

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International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
CHOI, Sang Won
Telephone No. +82-42-481-8291

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/054294

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		CA 2853583 C	07/06/2016
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		CN 101019241 B	29/09/2010
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		CN 101238195 A	06/08/2008
		CN 101238195 B	27/04/2016
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		CN 101331578 B	05/12/2012

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/054294

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		EP 1941028 A2	09/07/2008
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