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(54) OSCILLATOR CIRCUIT

(71) We, HEWLETT-PACKARD LIMITED, a British company, of South Queensferry, West Lothian EH30 9TG, Scotland, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to an oscillator for delivering an output sequence of clock pulses locked to the current phase of a synchronizing train of binary input pulses with random logic levels in the return-to-zero format at a substantially stable bit frequency.

The clock pulses recovered by such oscillators may for example be used for the purpose of regenerating the shape of signals in communication channels or as sampling pulses in sampling circuits. Generally, standard clock recovery oscillators with resonant filters should have a high Q-factor, as the train of input pulses may have long runs of signal with zero level so that a decay of the amplitude of the output pulses from the resonant filter should be prevented. However, a high Q-factor of the resonant filter in the oscillator has the disadvantage that the oscillator is not "transparent" to signals with a substantial jitter so that information at the sampler output would be lost.

It is therefore desirable to provide a clock recovery circuitry which on the one hand is resynchronized by each input pulse and on the other hand maintains a clock supply even if an unlimited number of resynchronizing pulses is missing in the input pulse train.

In accordance with the invention, there is provided an oscillator for delivering an output sequence of clock pulses locked to the current phase of a synchronizing train of binary input pulses with random logic levels in the return-to-zero format at a substantially stable bit frequency, the oscillator comprising:

OR gate means having a first input for receiving the binary input pulses, said OR gate means being connected in a loop with

feedback means connecting an output of said OR gate means with a second input thereof, said loop including inverting means and delay means for inverting and delaying by substantially 180° at said bit frequency the pulses received at said first and second inputs of said OR gate means, said feedback means being arranged to deliver the inverted and delayed pulses to said second input, thereby to derive said sequence of clock pulses; and

means connected to said loop for providing said sequence of clock pulses delayed by substantially 90° at said bit frequency with respect to the pulses at said first and second inputs.

As will be described below, the oscillators of the preferred embodiments will be resynchronized by each single input pulse, and are thus adapted for signals with a substantial amount of "jitter". This property makes the circuitry attractive for application in, for example, test equipment, as a sequence of clock signals can be derived in phase locked relationship to the possibly slightly varying phases of the input pulses and thus these clock signals can be used for the regeneration of the shape of the input pulses without suppressing any jittering pulses. Such "jitter transparency" together with infinite clock memory cannot be obtained by the conventional linear filter recovery circuits with a high Q-factor. The RZ input data can be supplied to a sampler clocked with clock pulses derived by the oscillator of the invention in order to obtain regenerated NRZ data.

Another application may be to use the recovered data as the input to a device, such as a phase-locked loop, to measure the jitter present on the data signal.

In a preferred embodiment of the invention, the delay means comprises a first phase shift circuit connected between an input gate and an output gate of the OR gate means, and a second phase shift circuit in the feedback means between the output gate and the input gate. This embodiment is of specific

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interest at frequencies in the range from audio frequencies through 50 M bits/s and delivers the clock pulses with a phase shift of 90° relative to the input signals and accurately matched to the phase and frequency of these input signals so that the clock pulses have just the 'central' phase required for sampling purposes.

For applications involving input signals with high runs of zeros, the stability of the oscillator becomes more important. In these cases provision may be made for compensating for any temperature induced delay.

Preferred embodiments of the invention will now be described by way of example with reference to the accompanying drawings, in which:

Figure 1 is, in schematic form, a simplified circuit diagram of a clock recovery oscillator,

Figures 2.1 to 2.3 are, in schematic form, waveforms of signals occurring at points A to D of the oscillator of Figure 1,

Figure 3 is, in schematic form, a circuit diagram of a modification of the clock recovery oscillator of Figure 1,

Figure 4 shows another embodiment of an oscillator in accordance with the invention, and

Figures 5.1 to 5.3 are, in schematic form, waveforms of signals occurring at points A to D of the oscillator of Figure 4.

Referring to Figure 1, an OR-gate  $G_1$  with a propagation delay time  $\tau_g$  has a signal input A, an inverted feedback output B, a feedback input C and a non-inverted signal output D. A wide bandwidth delay circuit E, for example a coaxial cable with a length of 23 cm and a resistance of 50 ohms, is connected between the inverted output B and the input C of the OR-gate  $G_1$ .

In the practical embodiment, the fixed delay  $\tau$  would be made  $\frac{1}{2fb} - \tau_g$  where fb is the mean frequency of the input signal. However, in the following waveform diagrams, the gate propagation delay  $\tau_g$  is neglected for the sake of simplicity.

Figure 2.1 shows schematically clock waveforms at points B, C and D, of the circuit of figure 1, when a random input pulse appears at the input A actually in phase with the current clock signals provided by the oscillator. As can be seen from figure 2.1, in this case the input pulse has no effect on the operation of the oscillator, and the oscillator has an indefinite clock memory so that the clock pulses continue to be delivered even if a plurality of zero level input signals appear.

Figure 2.2 shows the relationship of the signals at the same circuit points when an input pulse is delayed by  $\Delta t$  relative to the oscillator waveform. It can be concluded

from this likewise self-explanatory diagram that the derived clock pulses are in phase with the trailing edge of the delayed input pulse.

Figure 2.3 shows in similar manner the signal relationship at the same circuit points when an input pulse is early by  $\Delta t$  relative to the oscillator output signals. Again in this case the subsequent clock output signals will be in phase with the trailing edge of the latest input pulse.

Thus in all these cases the oscillator is resynchronized by a single input pulse. The oscillator may receive input signals with a substantial amount of jitter which is desirable for certain applications, such as in samplers where the sampling pulses should be locked to the slightly varying phase of the signals to be sampled.

For sampling applications a delay flipflop S1 for sampling the RZ-data is connected to the signal input A and has a clock input connected to a tolerancing delay circuit F which in turn is connected to the non-inverted output D of the OR-gate  $G_1$ . This delay circuit may consist of an RC-filter with a delay of 0.7 ns. The delay of this delay circuit is added to the propagation delay  $\tau_g$  of about 1.1 ns of the OR-gate  $G_1$ , giving a total delay of substantially 90° in terms of the phase angle, so that the RZ-data pulses are centrally sampled by the delay flipflop S1. It will be noted that the input RZ-data will be converted into sampled NRZ data since the sampling pulse, or in this case the edge of the clock pulse, is available only once per bit period and the sampled value is kept in between sampling pulses. However, the major aspect is the recovering of the clock from the RZ-data.

Figure 3 shows schematically a part of the circuit of figure 1 together with an additional circuit consisting of an OR-gate  $G_2$  connected in series with a DC-amplifier V. The delay circuit E<sup>1</sup> has in addition to a fixed delay section a variable delay section connected to the amplifier V. The OR-gate  $G_2$  is held in one state and is in close thermal contact with OR-gate  $G_1$ , e.g. in the same integrated circuit package. The OR-gate  $G_2$  serves for sensing the temperature induced delay variations of the OR-gate  $G_1$  and cooperates with amplifier V to control the amount of delay in the feedback path of  $G_1$  so that the effect of temperature changes is compensated. For this purpose amplifier V must have an input/output DC-transfer function which compensates for the difference between the propagation delay versus temperature characteristic of the OR-gate  $G_1$  and the output voltage versus temperature characteristic of the OR-gate  $G_2$ .

In practice, the variable delay section may be a varactor diode at the end of the fixed delay line, such as a coaxial cable. Amplifier

V may be an operational amplifier with a diode shaping network, if required, in its feedback loop, as is known to those skilled in the art. Such a temperature compensating circuit is appropriate at signal frequencies where the propagation delay  $\tau_g$  is a significant fraction of  $\tau$  and  $\tau_g$  is a function of temperature.

Figure 4 shows schematically a further improved oscillator for lower bit rates in the range from audio to 50 Mbits/s. An input NOR-gate G3 has its output connected to a damped resonant circuit including an inductance L1, a capacitor C1 and a resistor R1. The resonant frequency  $f_{LC}$  of said resonant circuit corresponds substantially to the input signal frequency  $f_b$ , while the Q-factor of the filter, i.e.  $2\pi f_b R_1 C_1$ , is approximately 1.

Said resonant circuit is further connected to the input of an OR-gate G4 with an inverted output for delivering the recovered clock signals at the frequency  $f_b$ , as well as a non-inverted output for providing feedback signals. Between this non-inverted output and one input of the NOR-gate G3 is connected a feedback resonant circuit with elements L2, C2, R2 with values corresponding to those of the elements of the resonant circuit in the forward path of the oscillator circuit. A delay flipflop  $S_1^1$  with a function corresponding to that of flipflop  $S_1$  in Figure 1 has its data input connected to the signal input A and further has its clock input connected to the inverted output of OR-gate G4.

This oscillator operates in substantially the same manner as the oscillator of Figure 1, except that the clock pulses at outputs B and D have a  $90^\circ$  phase lag relative to the input pulses, as shown in Figures 5.1 to 5.3. This property is desired for sampling circuits, as in these the sampling pulses should appear in central time position with regard to the signal pulses to be sampled. The  $90^\circ$  delay is produced by the resonant circuit L1, C1, R1, and thus the delay circuit F between the output D and the flipflop  $S_1$  of the oscillator of Figure 1 is not required. The resonant circuit L2, C2, R2 provides a further delay of  $90^\circ$ , to produce the required  $180^\circ$  delay of the feedback pulses.

The values of the various circuit parameters in the specific embodiment according to Figure 4 are selected so that this circuit is suitable for 2,048 Mbits/s. The design according to Figure 4 is to be used for fre-

quencies where the expression  $\frac{1}{2\tau_g}$  is large enough to allow practical values of the components L1, L2, C1 and C2.

As will be obvious to the designer of digital circuits, the precedingly described embodiments could be modified in various

manners without departing from the general concept of an oscillator with a relatively low Q-factor and an indefinite clock memory.

WHAT WE CLAIM IS:—

1. An oscillator for delivering an output sequence of clock pulses locked to the current phase of a synchronizing train of binary input pulses with random logic levels in the return-to-zero format at a substantially stable bit frequency, the oscillator comprising:

OR gate means having a first input for receiving the binary input pulses, said OR gate means being connected in a loop with feedback means connecting an output of said OR gate means with a second input thereof, said loop including inverting means and delay means for inverting and delaying by substantially  $180^\circ$  at said bit frequency the pulses received at said first and second inputs of said OR gate means, said feedback means being arranged to deliver the inverted and delayed pulses to said second input, thereby to derive said sequence of clock pulses; and

means connected to said loop for providing said sequence of clock pulses delayed by substantially  $90^\circ$  at said bit frequency with respect to the pulses at said first and second inputs.

2. An oscillator as claimed in claim 1, wherein the OR gate means comprises an input gate and an output gate, and the delay means comprises a first phase shift circuit connected between the output of the input gate and the input of the output gate for causing a delay of substantially  $90^\circ$  at the bit frequency, and a second phase shift circuit in the feedback means between the second output of the OR gate means and the second input of the OR gate means for causing a phase shift of substantially  $90^\circ$  at the bit frequency, both phase shift circuits having a low Q-factor of about unity and wherein said delayed clock pulse providing means comprises a further output of said OR gate means.

3. An oscillator as claimed in claim 2, wherein the input gate is a NOR gate including said inverting means, and the output gate is an OR gate having an inverting output forming said further output of said OR gate means and a non-inverting output forming said first-mentioned output of said OR gate means.

4. An oscillator as claimed in claim 1, wherein said OR gate means includes said inverting means and said output is an inverting output, said delay means comprises a delay circuit connected in said feedback means between said output and said second input, and said delayed clock pulse providing means comprises a further delay circuit connected to a further, non-inverting output of said OR gate means.

5. An oscillator as claimed in any preceding claim, wherein the delay means includes a fixed delay circuit and a variable delay circuit in said feedback means, the oscillator further comprising a temperature sensing circuit connected to a control amplifier for adjusting the delay of the variable delay circuit in order to compensate for any temperature induced changes in the propagation delay of the OR gate means.
6. An oscillator substantially as hereinbefore described with reference to Figure 1, Figure 1 as modified by Figure 3, or Figure 4 of the accompanying drawings.

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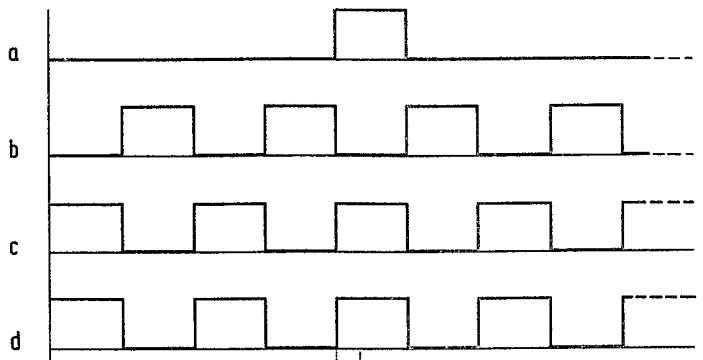


Fig.2.1

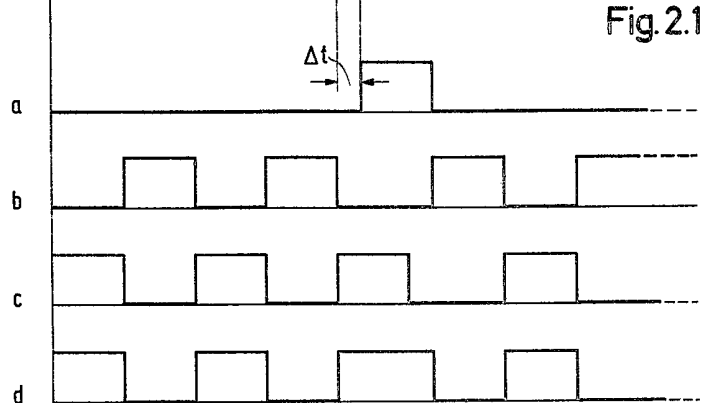


Fig.2.2

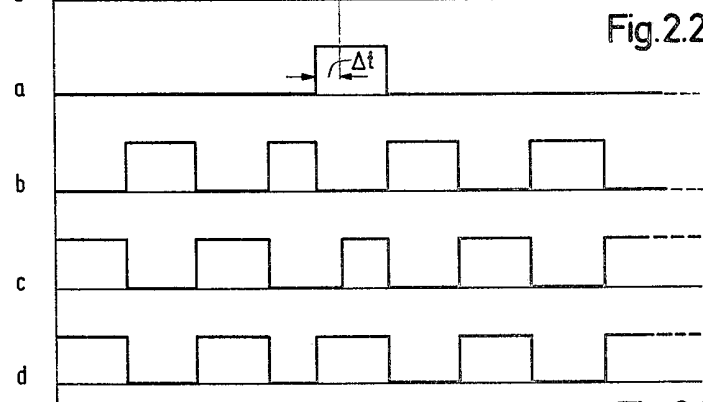


Fig.2.3

TIME →

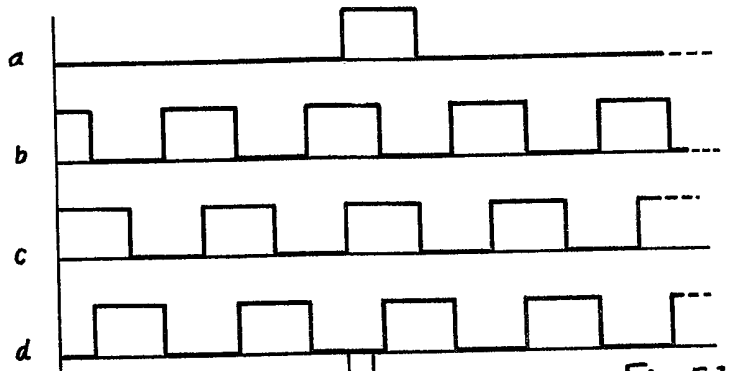


Fig. 5.1

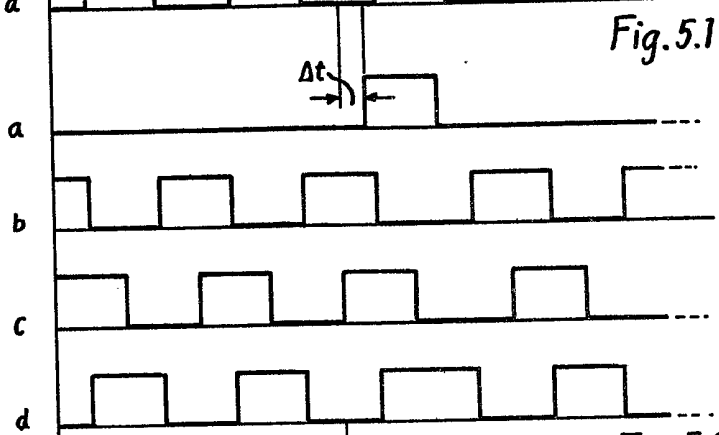
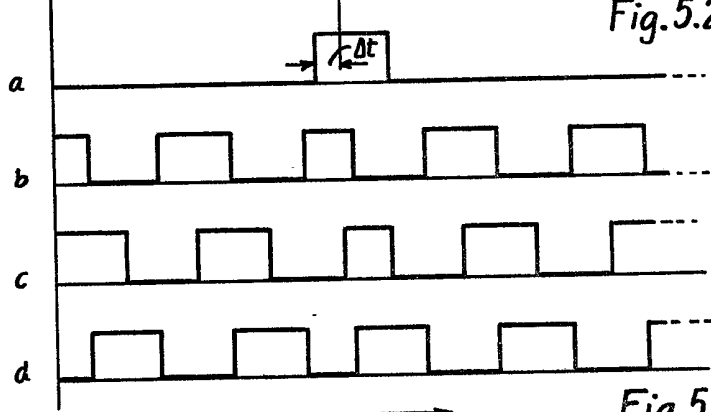


Fig. 5.2



TIME

Fig. 5.3