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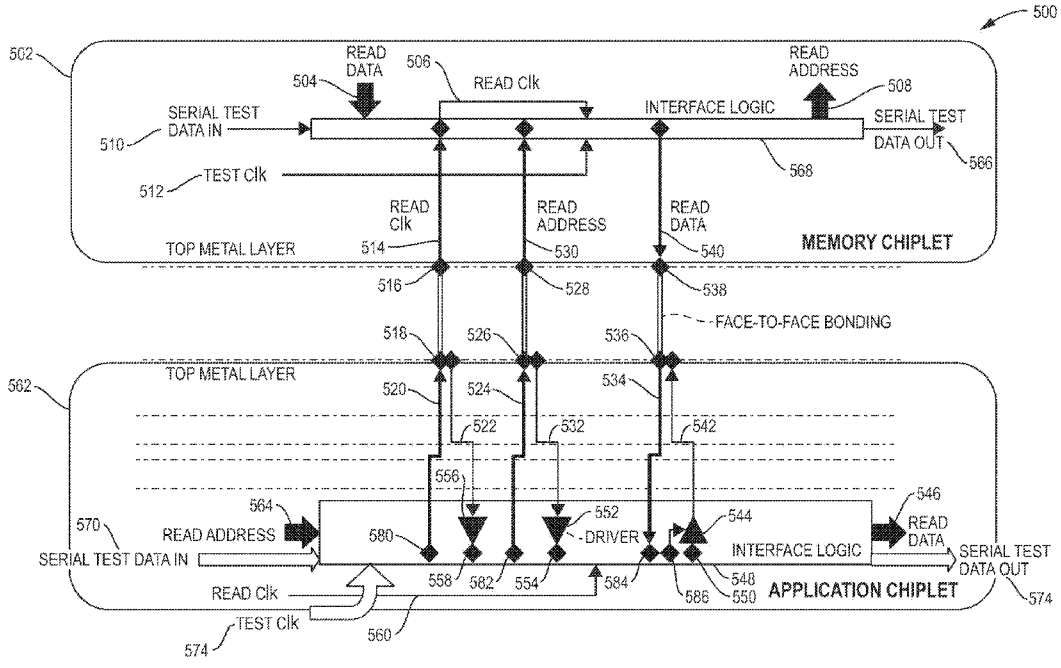


FIG. 5

(57) Abstract: A method, and related systems, of making a known-good stack are disclosed. The method includes forming a first semiconductor device having an interface logic with a plurality of interconnects electrically coupled to a surface of the first semiconductor device. The method also includes activating an interconnect loopback configured to receive a first one of the plurality of interconnects and electrically communicate back to the interface logic through the interconnect loopback. The method electrically couples a test signal to the first one of the plurality of interconnects and tests a return signal returned from the interconnect loopback to thereby test a path from the first one of the plurality of interconnects and through the interconnect loopback back to the interface logic.

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METHOD AND SYSTEM FOR TESTING STACKED FACE-TO FACE BONDED CHIPLETS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application claims the benefit of and priority to U.S. Provisional Patent Application No. 63/518,988, filed on August 11, 2023, entitled "INTEGRATED CIRCUIT HAVING MEMORIES AND A SHARED WRITE PORT", identified by Docket Number P23-133-US-PSP, the entire contents of which is incorporated herein by reference in its entirety.

[0002] The present application claims the benefit of and priority to U.S. Provisional Patent Application No. 63/602,733, filed on November 27, 2023, entitled "METHOD AND SYSTEM FOR KNOWN-GOOD-DIE TESTABILITY OF FACE-TO-FACE BONDED CHIPLETS", the entire contents of which is incorporated herein by reference in its entirety.

[0003] The present application claims the benefit of and priority to U.S. Provisional Patent Application No. 63/602,737, filed on November 27, 2023, entitled "SYSTEM AND METHOD FOR HAVING CORRECT-BY-CONSTRUCTION TIMING CLOSURE", the entire contents of which is incorporated herein by reference in its entirety.

[0004] The present application claims the benefit of and priority to U.S. Provisional Patent Application No. 63/567,649, filed on March 20, 2024, entitled "ASSEMBLY HAVING A FACE-TO-FACE BONDED CHIPLET", identified by Docket Number P24-052-US-PSP, the entire contents of which is incorporated herein by reference in its entirety.

[0005] The present application claims the benefit and priority to U.S. Provisional Patent Application No. 63/637,742, filed on April 23, 2024, entitled "INTEGRATED CIRCUIT HAVING MICROVAULT MEMORIES", identified by Docket Number P24-081-US-PSP, the entire contents of which is incorporated herein by reference in its entirety.

[0006] The present application claims the benefit of and priority to U.S. Provisional Patent Application No. 63/637,764, filed on April 23, 2024, entitled "FEFET STRUCTURES ON INTEGRATED CIRCUITS", identified by Docket Number P24-082-US-PSP, the entire contents of which is incorporated herein by reference in its entirety.

[0007] The present application claims the benefit of and priority to U.S. Provisional Patent Application No. 63/674,471, filed on July 23, 2024, entitled "SYSTEM, METHOD, AND APPARATUS FOR WAFER-SCALE MEMORY", identified by Docket Number P24-135-US-PSP, the entire contents of which is incorporated herein by reference in its entirety.

BACKGROUND

Relevant Field

[0008] The present disclosure relates to integrated circuits. More particularly, the present disclosure relates to integrated circuits that are known-good-die testable when face-to-face bonding of chiplets.

Description of Related Art

[0009] Chiplets refer to miniature chips that are designed to work as a single entity while using advanced packaging technology. These miniaturized chips are created by dividing the larger chip into several smaller chips, each with its own function or capability. The concept originated from the semiconductor industry's need to overcome the physical restrictions of traditional monolithic chip designs and achieve higher levels of integration. The idea behind chiplets is to create a modular system of interconnected and interchangeable chips that can be combined in different configurations to create advanced computing systems with improved performance, power efficiency, and functionality.

[0010] Chiplets can be based on different architectures, such as CPU, GPU, memory, or IO, and can be assembled and stacked in a variety of ways, depending on the specific application requirements. One of the advantages of the chiplet approach is the ability to mix and match different chiplets from different manufacturers to create custom solutions that meet specific computing needs. This approach also allows for faster time to market, reduced development costs, and increased flexibility, as chiplets can be upgraded or replaced without the need for a complete system redesign.

[0011] The use of chiplets may be used in various industries, including consumer electronics, cloud computing, and data centers, where the demand for high-performance computing and energy efficiency is high. Chiplets are expected to play a significant role in the future of computing and are likely to unlock new possibilities for creating more powerful and/or sophisticated electronic devices.

[0012] **SUMMARY**

[0013] A method of creating a known-good stack involves forming a first semiconductor device that has an interface logic with multiple interconnects electrically connected to the device's surface. Then, an interconnect loopback is activated, which is designed to receive one of these interconnects and electrically communicate back to the interface logic through the loopback. A test signal is electrically coupled to the first

interconnect, and a return signal from the interconnect loopback is tested to evaluate the path from the first interconnect through the loopback and back to the interface logic.

[0014] In one embodiment, the method involves activating the interconnect loopback by loading a test signal into a buffer. In the method, the activation of the interconnect loopback may be achieved by activating a tri-state buffer that is coupled to either the interconnect loopback itself or the first one of the plurality of interconnects. This serves as an optional feature for the method.

[0015] The method may involve optionally bonding the first semiconductor device to a second semiconductor device for improved performance and functionality. A boundary scan may be used to test electrical connections between the plurality of interconnects of the first semiconductor device and a complementary plurality of interconnects of the second semiconductor device, as an optional feature.

[0016] In one embodiment, the method may include bonding a complementary interface logic of the second semiconductor device with several complementary interconnects electrically connected to a surface of the second semiconductor device. Additionally, the method can involve coupling the multiple interconnects of the first semiconductor device to the complementary set of interconnects of the second semiconductor device. The method can also include performing a boundary scan to test the connectivity of the complementary interface logic to the interface logic, which is an optional feature that may enhance the overall effectiveness and accuracy of the process.

[0017] In the method, the act of electrically coupling the test signal to the first one of the plurality of interconnects involves applying the test signal directly to the first one of the plurality of interconnects, as an optional feature. In the method, the process of electrically coupling the test signal to the first one of the plurality of interconnects can involve applying the test signal to the interconnect loopback as an optional feature. In one embodiment of the method, at least one conductive bond is disposed on the surface of the first semiconductor device, with the first of the plurality of interconnects serving as a conductive path that is configured to electrically couple the conductive bond with the interface logic. Additionally, the interconnect loopback may comprise another conductive path that is configured to be electrically coupled to the interface logic.

[0018] The method may include an additional step of buffering the test signal in accordance with a clock, which is an optional feature that can be employed in the process. In the method, an optional feature includes buffering the return signal following the guidelines of a clock. In the method, the interface logic comprises an external interface that is connected to

the first one of the multiple interconnects, serving as an optional feature for enhanced functionality. In the method, the interface logic comprises an external interface that is connected to the interconnect loopback, providing an optional feature for better communication and interaction within the system.

[0019] The method may include an interconnect loopback, which features a comparator designed to compare the test signal with the return signal to determine the signal integrity. In the method, the interconnect loopback can also include a delay circuit configured to introduce a controlled delay in the return signal, which enables testing of the timing characteristics of the first one of the plurality of interconnects. In the method described, an additional optional feature includes dynamically adjusting the test signal based on predefined test patterns to enhance its effectiveness. In one embodiment of the method, test data is serially loaded into a boundary scan cell to generate a test signal on the first one of the plurality of interconnects. The return signal is then sampled into a second boundary scan cell, and the return signal is shifted. In the method, there is also an optional feature that includes comparing the sampled return signal with an expected return signal.

[0020] In the method described, an optional feature includes the first one of the plurality of interconnects being a read address interconnect. In this case, the test signal would be a read address, and the return signal would be a return read address that is returned from the first one of the plurality of interconnects through the interconnect loopback. In one embodiment of the method, the return read address is applied to a read data output bus of the interface logic of the first semiconductor device, enhancing the functionality of the overall process. In the method, an additional step can include signaling a register clock signal into the interface logic, and buffering the return read address in a register. In the method mentioned previously, an optional feature includes testing the return read address by examining the output of the register.

[0021] The method, as described earlier, can include an interconnect loopback that features at least one buffer. This buffer is specifically designed to selectively couple the interconnect loopback to the first of the multiple interconnects, providing enhanced functionality and flexibility in the system. In the method, the first interconnect from the plurality of interconnects can be a clock interconnect, with the test signal being a clock signal and the return signal being a return clock signal that is returned from the first interconnect through the interconnect loopback. This configuration serves as an optional feature within the method.

[0022] In the method, an optional feature includes applying the return clock signal to a read data output bus of the interface logic of the first semiconductor device. In one embodiment

of the method, a register clock signal is signaled into the interface logic, and the return clock signal is buffered in a register. In the method, an optional step includes testing the return clock signal in the register to ensure its proper functioning and accuracy. In one embodiment, the method involves an interconnect loopback, which includes at least one tri-state buffer that is configured to selectively couple the interconnect loopback to the first one of the plurality of interconnects. In one embodiment of the method, the first one of the plurality of interconnects functions as a read data interconnect, the test signal represents read test data, and the return signal constitutes return read test data that is sent back from the first interconnect through the interconnect loopback. The method includes the optional feature of applying the returned read test data to a read data output bus of the interface logic of the first semiconductor device. In one embodiment of the method, it may further comprise signaling a register clock signal into the interface logic and buffering the return read test data in a register, providing an optional feature that enhances the efficiency of the method. An optional feature of the method includes testing the return read test data by examining the output of the register.

[0023] In a method, the interconnect loopback comprises at least one tri-state buffer that can selectively couple the interconnect loopback to the first interconnect among the plurality of interconnects. In one embodiment of the method, the first interconnect among the plurality of interconnects serves as a write clock interconnect. In this case, the test signal corresponds to a write clock signal, and the return signal is a returned write clock signal that is sent back from the first interconnect through an interconnect loopback. In the method of coordinating data transfers in a system with at least two semiconductor devices, an optional feature includes applying the write clock signal to a read data output bus of the interface logic of the first semiconductor device. In one embodiment of the method, there is the additional step of signaling a register clock signal into the interface logic and buffering the returned write clock signal in a register.

[0024] In the method, the act of testing the returned write clock signal can be optionally carried out by examining an output of the register. In one embodiment of the method, the first one of the plurality of interconnects serves as a write address interconnect. In this case, the test signal is designed to define a write address, and the return signal constitutes a returned write address that comes back from the first one of the plurality of interconnects through the interconnect loopback. In the method, an optional feature involves applying the returned write address to a read data output bus of the interface logic of the first semiconductor device. In the method, an optional feature includes signaling a register clock signal into the interface logic and buffering the returned write address in a register.

[0025] In one embodiment of the method, the act of testing the returned write address involves examining an output of the register. In the method, the first one of the multiple interconnects can be a write data interconnect, where the test signal defines the write test data and the return signal consists of returned write test data that is returned from the first interconnect through the interconnect loopback. This setup serves as an optional feature for the method. In an embodiment of the method, the returned write test data is applied to a read data output bus of the interface logic of the first semiconductor device. In the method, an optional feature includes signaling a register clock signal into the interface logic and buffering the returned write test data in a register. In the method mentioned, the act of testing the returned write test data can involve examining the output of the register. This is an optional feature that may be employed to ensure the accuracy and functionality of the test data.

[0026] A stack system may include a first semiconductor device that includes an interface logic with multiple interconnects electrically coupled to the device's surface. This device also has an interconnect loopback designed to receive a first interconnect from the multiple interconnects and communicate back to the interface logic through the loopback. Additionally, there is a test signal connection in electrical communication with the first interconnect and a return signal connection for testing the path from the test signal connection, through the first interconnect, the interconnect loopback, back to the interface logic, and ultimately to the return signal connection.

[0027] The system includes a first semiconductor device, and an optional feature of this system is the presence of a second semiconductor device bonded to the first semiconductor device. In one embodiment, the system includes a second semiconductor device that features a complementary plurality of interconnects bonded to the plurality of interconnects of the first semiconductor device. This configuration allows the first and second semiconductor devices to provide a boundary scan chain for testing electrical connections between their respective interconnects, ensuring proper functionality and performance.

[0028] The system, as described previously, may also include a complementary interface logic on the second semiconductor device. This complementary interface logic features a plurality of complementary interconnects electrically coupled to the surface of the second semiconductor device. In this embodiment, the plurality of interconnects from the first semiconductor device are connected to the complementary plurality of interconnects on the second semiconductor device. The system includes interface logic and complementary interface logic, which are designed to provide a boundary scan for testing their connectivity.

This boundary scan is an optional feature that can be utilized in certain embodiments for enhanced functionality.

[0029] In the system, the interface logic and the complementary interface logic may be coupled together to form an integration boundary scan, which implements the boundary scan as an optional feature. The system includes a first semiconductor device, which further comprises a buffer coupled to the test signal from the interconnect loopback. In the system, the first semiconductor device can optionally include a tri-state buffer that is designed to drive the test signal onto the interconnect loopback. In one embodiment of the system, the test signal connection is electrically coupled to the first interconnect, providing a means for efficient communication between different components of the system. The system may include a test signal connection that is electrically coupled to the interconnect loopback, which serves as an optional feature. In one embodiment of the system, the first interconnect serves as a conductive path that electrically connects a conductive bond on the surface of the first semiconductor device with the interface logic. Additionally, the interconnect loopback, which is also a conductive path, is electrically connected to the interface logic and the conductive bond.

[0030] In an embodiment of the system, the interface logic comprises an external interface that is connected to the first interconnect. In one embodiment of the system, the interface logic comprises an external interface that is connected to the interconnect loopback, providing additional functionality and flexibility for the users. In one embodiment of the system, an interconnect loopback feature is present that includes a comparator. This comparator is configured to compare the test signal with the return signal in order to determine signal integrity. In the system mentioned, the interconnect loopback may comprise a delay circuit specifically designed to add a controlled delay in the return signal. This feature serves to test the timing characteristics of the first interconnect.

[0031] The system may consists of a test signal connector that is designed to dynamically adjust a test signal according to a predefined test pattern. This allows for flexibility and adaptability in testing processes, providing an optional feature for enhanced system performance. In one embodiment, the system includes a boundary scan cell that generates the test signal on the first interconnect and a second boundary scan cell that is configured to sample the return signal. The system also includes a comparator that is designed to compare the sampled return signal with an expected return signal, offering an optional feature for improved performance. In one embodiment, the system includes a first interconnect which is a read address interconnect. This interconnect enables the test signal connection to receive a read address from the system components. Moreover, the return signal is designed to be a returned

read address that is sent back to the first interconnect through the interconnect loopback, ensuring proper functionality and communication within the system. The system includes an additional feature, which is a read data output bus that is designed to receive the returned read address.

[0032] The system can also include a register that is configured to buffer the returned read address on a register clock signal, as an additional optional feature. The system further comprises a comparator that is configured to test the returned read address being outputted by the register, providing an optional feature for increased functionality. In one embodiment of the system, the first interconnect functions as a clock interconnect, where the test signal is a clock signal and the return signal is a returned clock signal from the first interconnect through the interconnect loopback. The system includes a read data output bus, which is designed to receive the returned clock signal from the interface logic. The system further includes a register that is designed to buffer a returned clock signal when it receives a register clock signal. This additional feature provides an optional enhancement for better performance and efficiency. The system includes a comparator that is designed to compare the returned clock signal stored in the register with a predetermined value, providing an additional optional feature for enhanced functionality. The system consists of a first interconnect, which is a read data interconnect, and a test signal connection that is configured to receive read test data.

[0033] Additionally, the return signal in the system may be a returned read test data from the first interconnect through the interconnect loopback, serving as an optional feature. The system features an optional component, which includes a read data output bus designed to receive the returned read test data. The system may feature an additional register clock signal connection to the interface logic, and a register designed to buffer the returned read test data based on a clock signal received through the register clock signal connection. This optional enhancement can improve the data handling capabilities of the system for more efficient operations. The system includes an additional feature, which is a comparator that is designed to test the returned read test data against a predetermined value.

[0034] The system, as described earlier, may optionally include at least one tri-state buffer. This tri-state buffer is designed to selectively couple the interconnect loopback to the first interconnect among the plurality of interconnects that are present in the system. In one embodiment of the system, the first interconnect is a write clock interconnect, the test signal is a write clock signal, and the return signal is a returned write clock signal from the first interconnect through the interconnect loopback. The system can include a read data output bus designed to receive the returned write clock signal from the interface logic. The system includes

an optional feature where it further comprises a register clock signal connector and a register. This register is configured to buffer the returned write clock signal in response to a register clock signal from the register clock signal connector. The system includes a comparator, which is an optional feature, designed to compare the returned write clock signal to a predetermined value. This allows the system to analyze the performance and potential discrepancies within the clock signal as it is being utilized. In one embodiment of the system, the first interconnect operates as a write address interconnect, where the test signal is a write address, and the return signal corresponds to a returned write address received from the first interconnect through the interconnect loopback.

[0035] The system includes an additional feature of a read data output bus, which is designed to receive the returned write address from the interface logic. This read data output bus complements the functionalities of the system and enhances its performance. The system may optionally include a register clock signal connection and a register designed to buffer the returned write address upon receiving a register clock signal from the register clock signal connection. The system, in accordance with some embodiments, further includes a comparator that is designed to compare the output generated by the register to a predetermined value. In one embodiment, the system includes a first interconnect which functions as a write data interconnect, a test signal comprising write test data, and a return signal in the form of returned write test data from the first interconnect through the interconnect loopback. The system includes a read data output bus, which is designed to receive the returned write test data from the interface logic, adding an optional feature to enhance its functionality. The system includes a register clock signal interface and a register. The register is designed to buffer the returned write test data when it receives a register clock signal through the register clock signal interface. This feature is optional and can be present in some embodiments of the system. The system mentioned may further comprise a comparator, which is configured to compare the output of the register to a predetermined value, providing an optional feature for users.

[0036] One method of manufacturing involves the formation of a first semiconductor device according to various possible embodiments, providing different options and approaches to semiconductor production. The method of forming a stack of semiconductor devices entails stacking a first semiconductor device, which is designed according to one of several possible embodiments, on top of another semiconductor device. In the method of forming a stack of semiconductor devices, a first semiconductor device is provided according to one of the numerous possible embodiments. Then, another semiconductor device is bonded to the first semiconductor device, resulting in a stacked configuration. A method of using semiconductor

devices can involve providing a first semiconductor device based on specific embodiments, and testing one of the multiple interconnects of the device as a part of this process. A possible method of designing a semiconductor device involves creating a digital representation of the interface logic in a first semiconductor device, utilizing one of the various previously described embodiments to achieve this formation. The method may also include the optional step of forming a photomask from the digital representation to enhance the overall process. The system comprises a first semiconductor device that is designed with features from one of the various embodiments, which provides the means for testing an interconnect of the plurality of interconnects.

[0037] BRIEF DESCRIPTION OF THE DRAWINGS

[0038] These and other aspects will become more apparent from the following detailed description of the various embodiments of the present disclosure with reference to the drawings wherein:

[0039] Fig. 1 is a block diagram of an integrated circuit that may be part of a semiconductor device such as a chiplet in accordance with an embodiment of the present disclosure;

[0040] Fig. 2 shows a perspective view of an assembly having the integrated circuit of Fig. 1 implemented on a semiconductor device that is electrically connected to another device to form the assembly in accordance with an embodiment of the present disclosure;

[0041] Fig. 3 shows a block diagram illustrating the memory address space of the integrated circuit of Fig. 1 in accordance with an embodiment of the present disclosure;

[0042] Fig. 4 shows a block diagram illustrating the memory address space with the signal interfaces of the integrated circuit of Fig. 1 in accordance with an embodiment of the present disclosure;

[0043] Fig. 5 shows a diagram of two semiconductor devices, such as two chiplets, that automatically test the connectivity of read interconnects within a semiconductor device and the integrated connectivity in accordance with an embodiment of the present disclosure; and

[0044] Fig. 6 shows a diagram of two semiconductor devices, such as two chiplets, that automatically test the connectivity of write interconnects within a semiconductor device and the integrated connectivity in accordance with an embodiment of the present disclosure; and

[0045] Fig. 7 shows a flow chart diagram of a method for testing a semiconductor device and bonding together two semiconductor devices and performing an integration test after bonding in accordance with an embodiment of the present disclosure.

[0046] DETAILED DESCRIPTION

[0047] Fig. 1 shows a block diagram of an integrated circuit 100 that may be packaged as a bondable chiplet (e.g., face-to-face chiplet bondable) in accordance with an embodiment of the present disclosure. The integrated circuit (IC) 100 includes a modules group 106 consisting of modules 108, 110, 112, and 114. The IC 100 also features a shared write port 102, configured to write to the modules group 106 using a write peripheral 104. Additionally, it includes read peripherals 116, 118, 120, and 122 and read ports 124, 126, 128, and 130, configured to read from the modules 108, 110, 112, 114.

[0048] The write port 102 may be configured to provide a single write address space for all of the modules group 106 where each of the modules 108, 110, 112, 114 has a dedicated read port 124, 126, 128, 130 respectively. The integrated circuit 100 may be packaged as part of a chiplet configured to be electrically connected to another integrated circuit device (e.g., another chiplet, or IC package, with or without electrical contacts, electrical bumps, etc.). The chiplet may be electrically connected to another device including, for example, by bonding, soldering, wafer-to-wafer bonding, face-to-face chiplet bonding, chiplet-to-wafer bonding, chiplet-to-interposer bonding, and/or may be connected together with an interposer or other interfacing technology. None, one, or more of interposers may be used or other interfacing technologies that are common to heterogeneous 3D system-in-package solutions may be utilized in electrically connecting a chiplet to another device.

[0049] Each read port (124, 126, 128, 130) in the chiplet may feature electrical contacts on a side of the chiplet or on multiple sides of the chiplet. The read ports 124, 126, 128, 130 may use multi-cycle pipelined circuitry. Upon bonding to another device (e.g., wafer, chiplet, chip, SOC, package, FPGA, etc.), the electrical contacts may line up in a manner that provides dedicated access to specific modules of the modules 108, 110, 112, 114. For instance, a processing/computing element may have exclusive access to module 108 via the read port 124, which may contain the neural network weights in a register file. Similarly, a different processing/computing element may have exclusive read access to module 110 via the read port 126, which includes a different register file. In this specific embodiment, this arrangement of the electrical contacts ensures that each computing/processing element has the dedicated access it needs to carry out its specific computation efficiently thereby providing a compact, modular, and scalable system that allows different processing elements to maintain dedicated access to specific modules 108, 110, 112, 114. Without dedicated access, different processing elements might have to queue up to use the same resource which would slow down overall processing speed. By providing dedicated access, the proposed chiplet ensures that each processing

element can operate at its maximum capability without interference from other computing elements in this specific embodiment.

[0050] The write peripheral 104 is a peripheral circuitry responsible for processing and writing data into the memory cells found within the modules 108, 110, 112, 114. The write peripheral 104 may include dedicated contacts so that a chip electrically connected (e.g., bonded) to a chiplet of the integrated circuit, such that the write port 102 is accessible via a shared write logic system that involves utilizing a shift register-based, different voltage design, preferably high voltage design, that has a shared write address and data components. This shared write logic system is designed to be accessed via a bonded chip, another bonded chiplet, and/or via other circuitry in the same package as the integrated circuit 100. A shift register could allow the system to move data through a series of stages, with each subsequent stage receiving the data from the previous stage. By utilizing a shift register, the system can increase the data throughput while maintaining a low rate of data transfers. The shared write address space refers to the location where data is written in the chiplet.

[0051] In another embodiment, an interlock 132 may disable the read ports 124, 126, 128, 130 while data is being written to the modules group 106 via the write port 102. Likewise, the interlock 132 may disable the write port 102 when read operations are being carried out on the read ports 124, 126, 128, 130. The written data can later be accessed concurrently by all processing elements that need to read the data via a respective one of the read ports 124, 126, 128, 130. This ensures that all processing elements have the most commonly used data available to them without regard to other reads being concurrently carried out by other processing elements.

[0052] The write peripheral 104 circuit includes a write driver. This unit receives the data to be written and converts it into suitable signals that can change the state of the memory cells. Depending on the type of memory technology used, these signals could involve voltage levels, current pulses, or other types of energy. The shared write logic system may be high voltage due to the specific voltage requirements of the chiplet. The write driver must provide enough power to reliably change the state of the memory cells, but it must also operate within suitable parameters to avoid causing damage or unnecessary wear.

[0053] The write peripheral 104 circuit may also feature a data buffer or write buffer. This component temporarily stores the data to be written, allowing the write operation to be performed at a predetermined pace. By balancing the speed of incoming data with the speed at which the memory cells can be written, the write buffer helps prevent data loss and optimizes system performance.

[0054] The write peripheral 104 may also include, in some embodiments, a write control unit that orchestrates the sequence of operations in the write process. It generates control signals to activate the write driver at the appropriate times, controls the flow of data from the write buffer, and coordinates the timing of the write operations. By synchronizing these various activities, the write control unit ensures efficient and reliable write operations.

[0055] The write peripheral 104 may also include data encoding mechanisms to improve reliability and data integrity. For example, before the data is written to the memory cells, these mechanisms encode it in a way that allows potential errors to be detected, and in some cases, corrected when the data is later read. This can be helpful in systems where data integrity has a higher priority, such as in servers or scientific research devices.

[0056] The write peripheral 104 may also include a timing unit that serves as the system's heartbeat, supplying clock signals that synchronize the operation of the system's various components. In some systems, it may include components like oscillators, clock generators, or phase-locked loops. The timing unit may ensure that all operations occur at the suitable time relative to each other.

[0057] The IC 100 may be implemented as a face-to-face bonded chiplet, with modules 108, 110, 112, and 114 formed from a non-volatile memory. In some specific embodiments, the IC 100 may also feature a dynamic allocation circuitry to allocate memory blocks to the modules group 106 based on the usage of the modules group 106 (e.g., each module 108 may include dynamic allocation circuitry for dynamically allocating a range of read locations for a respective processing element).

[0058] The IC 100 features a plurality of clocks, with each clock of the plurality of clocks feeding a respective module of the plurality of modules, providing each respective module with decoupled timing relative to the other modules of the plurality of modules. The modules group 106 may be arranged in any topology known to one of ordinary skill in the relevant art. Bit-cell density can be up to 10 times more dense than embedded SRAM cells in the modules group 106.

[0059] The IC 100 may be formed on a chiplet that includes a first side and a second side, with the second side configured for bonding to a second semiconductor device. The IC 100 may include a high voltage write logic adjacent to the first side of the chiplet. A decoder circuitry, a driver circuitry, and a register circuitry may be formed on the silicon substrate portion of the chiplet, while the modules group 106 is formed on a second layer portion of the chiplet. The second semiconductor device may comprise a plurality of processing elements. Each processing element includes a respective interface to communicate with a respective

module of the plurality of modules on the modules group 106 when the second semiconductor device is bonded to the chiplet.

[0060] The silicon substrate traditionally serves as the initial stage of IC fabrication, focusing on the creation of active components, particularly transistors. Techniques like diffusion, ion implantation, oxidation, and material deposition are employed to fashion the intricate structures of transistors. These processes operate at small scales. The application of photolithography, etching, and implantation techniques enables the definition of transistor structures with precision. The silicon substrate's significance lies in its ability to establish the fundamental building blocks necessary for signal processing, amplification, and control within the IC. This layer is sometimes called Front-End-Of-The-Line ("FEOL").

[0061] Next in the manufacturing process, a second layer may be added that traditionally takes on the role of interconnect fabrication, facilitating the electrical connections between various IC components. The interconnects may be, but are not limited to, wires, conductive paths, waveguides, signal paths, logical paths, digital paths, buses, ports, etc. This phase traditionally focused on the creation of passive components, including interconnects, vias, and metal-insulator-metal (MIM) capacitors. The second layer processes typically differ from the processes used on the silicon substrate in terms of precision and scale. The interconnects are formed by depositing and patterning metal layers, typically aluminum or copper, to construct the wiring network. Dielectric layers, such as silicon dioxide or low-k dielectrics, are introduced to insulate the interconnects and prevent signal interference between different wiring layers. The second layer's traditional function is to establish the necessary interconnections that enable the routing and distribution of electrical signals throughout the IC. However, as described herein, circuity may be utilized within this second layer (sometimes referred to as Back-End-Of-The-Line ("BEOL")).

[0062] Alternate embodiments of the IC 100 may be implemented as a stacked die, a monolithic design, TSVs, or silicon through vias. In a stacked die design, several dies may be stacked on top of each other, with each die performing different functions, such as memory and processing. The stacked die may communicate through wire bonds, microbumps, or bump-less bonds. In a monolithic design, the various functions and modules of the IC 100 may be integrated onto a single die, forming a more compact and power-efficient design.

[0063] Additionally, the IC 100 may include one or more interlocks 132 to prevent conflicts in reading and writing data. The modules group 106 may be formed from a variety of non-volatile or semi-volatile (e.g., very long refresh periods) memory technologies, such as Static Random-Access Memory (SRAM), Ferroelectric Field Effect Transistor (FeFET),

Ferroelectric Random Access Memory (FeRAM), Resistive Random Access Memory (ReRAM), Spin-Orbit Torque (SOT) Memory, Spin Transfer Torque (STT) Memory, charge trap, floating gate memories, and/or Schottky diodes.

[0064] The modules group 106 may utilize a Static Random-Access Memory (SRAM) Topology. The SRAM topology may employ a cross-coupled flip-flop structure (e.g., latching flip-flops), ensuring the stored data remains intact as long as power is supplied. Thus, in some specific embodiments, the modules group 106 may utilize heterogeneous types of memory including volatile and non-volatile memory types.

[0065] The modules group 106 may utilize a Flash Memory Topology. The Flash memory is a non-volatile memory technology used in applications where data persistence is needed, such as solid-state drives (SSDs) and USB flash drives. The flash memory topology disclosed herein according to one specific embodiment features a matrix of memory cells, each consisting of a floating-gate transistor or charge trap device. The modules group 106 may also use wear-leveling techniques to prolong the lifespan of the memory cells.

[0066] The modules group 106 may utilize a Ferroelectric Random-Access Memory (FeRAM) Topology. The FeRAM topology utilizes a ferroelectric material capable of retaining polarization states. One such memory topology may, in specific embodiments, utilize a FeFET to retain state information and program the ferroelectric material. These ferroelectric materials may be used to retain state information and act as a memory bit cell.

[0067] The modules group 106 may utilize a Phase Change Memory (PCM) Topology, which is a non-volatile memory technology that utilizes reversible phase changes in materials to store data. The PCM topology may include any phase change material, for example a chalcogenide alloy or a chalcogenide glass housed within a memory cell.

[0068] The modules group 106 may utilize a Resistive Random-Access Memory (ReRAM) Topology, which is a non-volatile memory technology based on resistive switching phenomena. The ReRAM topology may utilize a thin-film material that exhibits reversible changes in resistance upon the application of electrical stimuli.

[0069] The modules group 106 may utilize a Spin-Orbit Torque (SOT) Magnetic Random-Access Memory Topology. SOT-MRAM is a type of non-volatile memory that utilizes spin-orbit torque to switch the magnetic state of a storage element. The SOT-MRAM topology may incorporate a magnetic tunnel junction (MTJ) structure and leverages the spin-orbit coupling effect to write and read data. The magnetic tunnel junction may have a dielectric layer between a magnetic fixed layer and a magnetic free layer. Writing may be done by switching magnetization of the free magnetic layer by injecting an in-plane current in an

adjacent SOT layer. Reading may be done by putting current into the magnetic tunnel junction. The SOT-MRAM can optimize the spin-orbit materials by using current-driven switching schemes while minimizing write energy consumption, in some specific embodiments.

[0070] The modules group 106 may utilize a Spin Transfer Torque (STT) Magnetic Random-Access Memory Topology. The STT-MRAM is another type of non-volatile memory that relies on spin transfer torque to manipulate the magnetic state of a storage element. The STT-MRAM topology can use a magnetic tunnel junction (MTJ) structure, where the magnetization orientation determines the stored data. Additionally, the orientation of a magnetic layer in a magnetic tunnel junction or spin valve can be changed using a spin-polarized current, for example.

[0071] The IC 100 may include a single write peripheral 104 with a dedicated clock, or each module 108, 110, 112, 114 may have its own dedicated write peripheral utilizing a shared clock (not shown in Fig. 1). Additionally, the modules group 106 may be organized into separate partitions, each with a dedicated read peripheral 116, 118, 120, 122 having an independent clock.

[0072] Another possible embodiment of the IC 100 includes an interface (e.g., the same, different, higher or lower voltage) to enable data transfer external to the packaging of the IC 100. The IC 100 may also include an integrated microcontroller unit (MCU) or a digital signal processor (DSP) for processing data within the IC in yet additional specific embodiments.

[0073] Fig. 2 shows a perspective view of an assembly 200 of the integrated circuit 212 of Fig. 1 implemented on a chiplet 230 that is bonded to a second device 226 in accordance with an embodiment of the present disclosure. The integrated circuit 212 is the circuitry within the chiplet 230. The second device 226 may be a chiplet, semiconductor wafer, semiconductor package, encased circuitry, etc. For example, the second device 226 may be an AI accelerator such that each processing unit has read access to one module (or a predetermined set) of the modules group 236. In yet another embodiment, the second device 226 may be a network controller where there is an offload circuit to read the data from each of the modules to processing incoming/outgoing packets, etc. The assembly 200 includes a modules group 236 having a plurality of modules, including a first module 232 and a second module 234. Fig. 2 shows several modules, however, for clarity, only modules 232, 234 have reference numbers. The integrated circuit 212 further comprises a shared write port 222. The shared write port 222 interfaces into the write peripheral 202.

[0074] Although the second device 226 may use the shared write port 222 via an address & data bus with a clock and an enable signal to write data to any modules within the modules group 236, other ways of writing data may be considered. For example, serial connections, parallel connections, various buses, or ports, may be used, such as a DDR (Double Data Rate) Interface, a SRAM (Static Random-Access Memory) Interface, a NAND Flash Memory Interface, a NOR Flash Memory Interface, a HBM (High Bandwidth Memory) Interface, a GDDR (Graphics Double Data Rate) Interface, a NVMe (Non-Volatile Memory Express) Interface, SPI, IC2, etc. Each of the modules has a read port with a read address 218 (to send an address to a module 234) and read data 220 (which is the data read from the module 232.

[0075] The modules group 236 is formed on a chiplet 230 having two sides including a surface 228 that can be bonded to and complement a second device 226. The chiplet 230 may be formed by forming circuitry on a silicon substrate 204 and then by adding a second layer 206. In other embodiments, these layers may be reversed and/or other layers may be added, removed, etc. The read address 218 and read data 220 are used for reading the module 232.

[0076] Although the second device 226 may use an address & data bus with a clock and an enable signal to read data from the module 232, other ways of reading data may be considered. For example, serial connections, parallel connections, various buses, or ports, may be used, such as a DDR (Double Data Rate) Interface, a SRAM (Static Random-Access Memory) Interface, a NAND Flash Memory Interface, a NOR Flash Memory Interface, a HBM (High Bandwidth Memory) Interface, a GDDR (Graphics Double Data Rate) Interface, a NVMe (Non-Volatile Memory Express) Interface, SPI, IC2, etc.

[0077] All of the read ports 220 are configured to be inactive when a write operation is applied to the shared write port 222. The read ports 220 may also be configured to process reads concurrently with each other. The shared write port 222 is configured to write to an address space, where the shared write port 222 is configured to write to the first module 232 via a first portion of the address space and write to the second module 234 via a second portion of the address space. Each module of the plurality of modules 236 includes an independent read port for concurrent reading via a respective independent read port of any of the plurality of modules.

[0078] Each read port for a respective module may include contacts for circuitry found within the second device 226 to interface via metallic contacts. Thus, there may be metallic contacts on the top layer 208 that are configured to interface with metallic contacts on the

surface 228 of the chiplet 230 such that the metallic contacts allow for a read space that is coextensive with a read space of a module of the modules 236. The read spaces of the modules group 236 may all be coextensive with each other (as is described with reference to Figs. 3 and 4).

[0079] In one embodiment, the read peripheral for the first module 232 is implemented on a silicon substrate 204 (sometimes referred to as a Front-end-of-the-line). The second layer 206 (sometimes call the Back-end-of-the-line) may be built next in the manufacturing process on top of the silicon substrate 204 (and any circuitry) and may contain the respective memory bit cells. In an alternative embodiment, the read peripheral for the first module 232 is implemented in the second layer 206 and is disposed between the modules group 236 and the surface 228 of the chiplet 230.

[0080] The modules group 236 may be configured to process write commands only during reset. The write commands may be "slow write" commands. That is, the modules group 236 may have very low write speeds relative to its read speed. The write logic may be frozen (or disabled) when the modules group 236 are used for reading data. In some specific embodiments, the integrated circuit 212 provides functionality to allocate memory blocks to the modules group 236 based on the usage of the modules group 236. In other embodiments, the memory addresses are fixed along with the allocation. The integrated circuit 212 may be implemented as a face-to-face bonded chiplet 230. The face-to face bonding may be bump-less wafer bonding.

[0081] The modules group 236 can have a single write peripheral 202. In other embodiments, each module of the modules group 236 may have a dedicated write peripheral that utilizes a shared clock. In yet other embodiments, the modules group 236 may also be organized into separate partitions with each partition having a dedicated read peripheral, where each dedicated read peripheral has an independent clock. The partitions may be one, two, or more modules of the modules group 236.

[0082] The write peripheral 202 circuitry's overall architecture may include a series of different components, including write drivers, address decoders, sense amplifiers, data input latches, data bus, etc. and/or some combination thereof. Write drivers or write buffers, may be tasked with transferring data onto the memory cell. They may enhance the input signal to achieve a level appropriate for the memory cell. Address decoders may be used to interpret the memory address that is fed as an input where the data needs to be written. By activating the specific row and column of the memory array linked to that address, they may be used to select the target memory cell. Sense amplifiers may be used to identify and boost the signal from the

memory cells during reading operations, also participate in refreshing the memory cell post data write in write operations. The write operation is instigated by a write enable signal. When a write command is initiated, this signal propels the write drivers and decoders into the writing process. Data input latches may be used as temporary storage units, retaining the data set to be written into the memory until the write operation is implemented. A data bus with a transmission route, can be used to facilitate the movement of data from the data input latches to the memory cells.

[0083] A write operation to the modules group may be performed through a priority arbitration circuit that facilitates the modules to be accessed in a predetermined order, and the shared write port 222 may be configured to write to a virtual address space that is mapped onto a physical memory space. The integrated circuit 212 may include a high voltage write logic used within the write peripheral 202, and the second semiconductor device 226 may comprise a plurality of processing elements, whereby each processing element includes a respective interface to communicate with a respective module of the modules group 236. Furthermore, the chiplet 230 may include an interface to the shared write port 222 on the second side to thereby interface with a complementary interface on the second semiconductor device 226.

[0084] The integrated circuit 212 may also include a power gating circuitry that selectively powers down a module of the modules 236 when not in use. Additionally, the integrated circuit 212 may have a write peripheral 202 of the modules group 236 connected to a dedicated I/O pad to enable data transfer external to the package of the integrated circuit.

[0085] The integrated circuit 212 may utilize multiple modules of the modules group 234 grouped together. These modules may be synchronized with one another in specific embodiments. In some cases, all the modules are synchronized, while in other instances, only specific modules are to be synchronized. For instance, the circuit on a second device 226 may need to synchronize with a specific module when reading data from one of the modules in the module grousp 236.

[0086] To synchronize the modules, the integrated circuit 212 may use various timing technologies. In some cases, a plurality of clocks may feed each respective module of the modules group 236, thereby allowing each module to have decoupled timing relative to the other modules in the group. This decoupling ensures that any delay in one module will not affect the functioning of other modules. It is worth noting that the clocks used may or may not need to be synchronized. In some cases, a common clock can be used to synchronize the modules. In yet other embodiments, the clock signal or signals may be provided by the second device 226.

[0087] In alternative embodiments, other synchronization techniques can be used, such as phase comparison of the clock signals or a phase-locked loop (PLL) synchronization method. Another embodiment for synchronizing the modules in the IC could use delay-locked loop (DLL) synchronization. In this method, a delay element is added to the clock signal path, and the output is compared to the input clock signal. The feedback loop adjusts the delay element until the output of the DLL matches the input, resulting in synchronization of the clock signals.

[0088] In another embodiment, the integrated circuit 212 could use a combination of different synchronization techniques to achieve synchronization between the modules. For example, some modules may use PLL synchronization while others use clock delay lines or DLL synchronization, depending on their specific requirements. Additionally, the integrated circuit 212 can also use redundant synchronization techniques to ensure reliability and redundancy in case one method fails. For example, the integrated circuit 212 could use both PLL synchronization and DLL synchronization simultaneously, so that if one method fails, the other can still maintain synchronization.

[0089] Fig. 3 shows a block diagram 300 illustrating the memory address space of the integrated circuit of Fig. 1 in accordance with an embodiment of the present disclosure. The memory address space includes a write address space 316 and read data address spaces 310, 312, 314.

[0090] The write address space 316 consists of various units where data, e.g., weights, and/or instructions can be stored. These units are referred to as memory addresses. The module groups 302 includes multiple memory modules 304, 306, 308. The write address space 316 may be distributed among the memory modules 304, 306, 308 such that the write address space 316 spans from 0 to N*M-1. As shown in Fig. 3, the modules group 302 has N memory modules 304, 306, 308, where N is a positive integer, and each module has a memory size of M. The total number of specific write memory addresses in the write address space will be N*M, which can be referenced by an integer from 0 to N*M-1.

[0091] Starting at 0, memory addresses of the write address space 316 are ordered sequentially up to N*M-1. In other words, the first address is 0 and the final address is N*M-1, encompassing a total of N*M addresses. This ordering can be linear (each address increases by one) or some other specified pattern depending.

[0092] The write memory addressing can be implemented in a variety of ways based on the system architecture. One method used in a specific embodiment is to use the base and limit registers. In one specific embodiment, the base register holds the smallest legal physical

write memory address, and the limit register specifies the size of the range. Therefore, to generate a logical address, you would add the base to the relative address. In other embodiments, a memory addressing scheme may be used where the base used is set to be 0. Yet additional write addressing techniques will be appreciated by one or ordinary skill in the relevant art.

[0093] For any device that writes to the modules group 302, each memory module can possess a specific set of write memory addresses such all memory addresses within the modules group 302 is specific with respect to writing data. e.g., the first module starting at 0 and the last one ending at N*M-1. This allocation, in some embodiments, may be dependent on the memory management system of the device writing data to the modules 304, 306, 308, which could range from simple fixed partitioning schemes to more complex dynamic partitioning models.

[0094] For instance, in a straightforward linear model where each module (304, 306, or 308) has an equal size of M addresses, the first module 304 would possess write addresses 0 to M-1, the second module would have write addresses M to 2M-1, the third module would have write addresses 2M to 3*M-1, and so forth. The Nth module 308, therefore, would possess write addresses from (N-1)*M to N*M-1.

[0095] It is contemplated that one of ordinary skill in the relevant art may use other implementations of write memory addresses from 0 to N*M-1 that depends on various factors such as the hardware architecture, operating system, memory management schemes, and the nature of the programs being run on the system, etc.

[0096] The modules group 302 has different read data address spaces 310, 312, 314. These read address spaces 310, 312, 314 may have overlapping addresses spaces, may have contiguous address spaces, or may have coextensive address spaces. The read address spaces 310, 312, 314 may be independent relative to each other. The system includes three independent read address spaces, labeled as read address spaces 310, 312, and 314. Each of these read address spaces is distinct from the others, meaning that reads can be performed in each space without affecting the others.

[0097] The read address spaces 310, 312, 314 may be defined as contiguous blocks of memory addresses, each with its own starting address and ending address. In modules group 302, each read address space 310, 312, 314 may have a range of addresses that corresponds to values from 0 to M-1, where M is a maximum value determined by the size of the modules 304, 306, 308 being used.

[0098] In one embodiment, allowing one processing unit to interface with each read address space 310, 312, 314, the concurrent reads may be implemented as described herein.

The independence of the read address spaces 310, 312, 314 ensures that each processing unit can access its desired data without causing any interference or conflict with other processing units.

[0099] Fig. 4 shows a block diagram illustrating the memory address space with the signal interfaces of the integrated circuit of Fig. 1 in accordance with an embodiment of the present disclosure. The signals used in Fig. 4 may be used with any embodiment described herein. However, one of ordinary skill in the relevant art will appreciate that different signaling schemes may be used.

[00100] The modules group 402 includes modules 404, 406, 408 that share a common write peripheral 411. The write peripheral 411 includes a write address bus that includes the address of the data being written, a write data bus that includes the data, a write clock cause the writes to occur (e.g., either on a leading or trailing edge of the clock signal, etc.). The writes only occur if the write enable signal indicates a write should occur. Any logic may be used, e.g., high voltage may correspond to 1 and a low voltage may correspond to 0, or vice versa. In some embodiments, the write peripheral 411 may be on the chiplet 230 and in other embodiments, the write peripheral 411 is on the second device 226.

[00101] The modules group 402 has modules 404, 406, 408 where each has a respective read peripheral 410, 412, 414. Each of the read peripheral 410, 412, 414 has a read address bus to send an address for reading, a read data bus to receive the data, a read clock which is the clock used to control the timing of the output of the digital data, and an output enable that is a precondition to outputting data. Any logic may be used, e.g., high voltage may correspond to 1 and a low voltage may correspond to 0, or vice versa. In yet additional embodiments, multi-bit or analog data storage may be used. In some embodiments, one or more of the read peripherals 410, 412, 414 may be on the chiplet 230 and in other embodiments, one or more of the read peripherals 410, 412, 414 are on the second device 226.

[00102] FIG. 5 illustrates a stack 500 consisting of two semiconductor devices 562, 502 that can be bonded together. The first semiconductor device 562 may be an application chiplet, while the second semiconductor device 502 may be a memory chiplet. The application chiplet 562 includes circuitry to facilitate interconnect testing prior to bonding by using interconnect loopbacks 522, 532, 542. The first semiconductor device 562 has several test signal connections 580, 582, 550 which can be used to test a path by examining how the signal is returned via a respective one of a return signal connections 558, 554, 584. These connections may be coupled to boundary scan cells and/or external circuitry that is external to the interface

logic 548. A tri-state buffer 544 may have an enable connection 586 that can control whether or not the tri-state buffer 544 is in an active state or an inactive state.

[00103] The stack 500 can facilitate the design and integration of a second semiconductor device 502 (e.g., system-on-chip (SoC) or application chiplet) with a first semiconductor device 562 (e.g., a co-chiplet) and more particularly, to a known-good-die application design method to facilitate independent testing.

[00104] In some embodiments, the first and second semiconductor devices 562, 502 are bonded together at the final stages. Thus, to achieve independently verified chiplets, the disclosed method provides a thin interface module (e.g., the interface logic 548) on the first semiconductor device 562 (e.g., an application SoC base-die) wherein the inputs and outputs may be registered on a clock edge. By doing this, the application designer can focus on ensuring independent validity of each semiconductor device.

[00105] With the thin interface logic 548 in place, the application designer's responsibility is primarily to interface with the thin interface logic 548 according to specifications. By following this approach, the design complexities associated with co-chiplet integration can be effectively managed, leading to improved efficiency and reliability.

[00106] Independent testing of the semiconductor devices 562, 502 can be used to minimize yield loss during post-integration stages. For example, in a 3D Memory Fab, each memory chiplet may be fabricated and individually tested to identify known-good dies, which are then inventoried. The testing process utilizes a serial scan-based built-in self-test (BIST) technique to ensure thorough testing and verification of the memory chiplets. During the place and route stage, the interface logic 548 is placed by the placement tool, while custom scripts can facilitate vertical routing of the loopbacks 522, 532, 542 and bonds 518, 524, 536 etc. The rest of the design may then be fully routed to establish complete connectivity. Subsequently, the application wafer for the first semiconductor device 562 may be fabricated with top metal bonds 518, 524, 536.

[00107] The first semiconductor device 562 (e.g., as a fully fabricated application wafer) may be subjected to testing using pass-thru interface logic, allowing comprehensive evaluation of the application device's functionality and performance. Optionally, testing at the wafer level may also be carried out to further ensure the quality and reliability of the first semiconductor device 562 (e.g., an application chiplet). Throughout this testing phase, the aim is to identify any defects or issues that may affect the device's functionality or integration.

[00108] In the hybrid package integration phase, the known good second semiconductor device 502 (e.g., a memory chiplet), obtained from previous testing, may be face-to-face

bonded with the known good first semiconductor device 562 (e.g., the application chiplet). This bonding process can facilitate a secure and reliable connection between the semiconductor devices 502, 562 (e.g., a memory chiplet and an application chiplet). Moreover, by optionally performing the semiconductor device bonding at the wafer level, post-packaging yield can be enhanced, thereby reducing potential yield losses and improving overall production efficiency.

[00109] The first semiconductor device 562 includes an interface logic 548 that facilitates communication to external circuitry and external semiconductor devices. The interface logic 548 also includes interconnect loopbacks 522, 532, 542 to test the connectivity between the interface logic 548 and conductive pads (or bonds) 518, 526, 536 found on the surface of the first semiconductor device 562. These connections may be tested prior to bonding with another device (or in some embodiments, after bonding). The conductive pad 518 of the first semiconductor device 562 may be electrically coupled to the conductive pad 516 of the second semiconductor device 502. Additionally, the conductive pads 526 of the first semiconductor device 562 may be electrically coupled to the conductive pads 528 of the second semiconductor device 502. And, the conductive pads 526 of the first semiconductor device 562 may be electrically coupled to the conductive pads 538 of the second semiconductor device 502.

[00110] The interface logic 548 comprises several input or output interfaces to other circuitry (not shown) within the first semiconductor device 562, including a read address input 564, a read clock input 560, and a read data output 546 (each of which may have boundary scan cells to facilitate boundary scan testing). The read clock input 560 is connected to a read clock interconnect 520, which extends to the surface of the first semiconductor device 562 and terminates at a conductive pad 518. Additionally, the conductive pad 518 is connected to an interconnect loopback 522 that is coupled to a buffer 556. The buffer 556 is further connected to the read clock output 558, which should have the same value as the read clock input 560 of the interface logic 548 if the integrity of the circuit is sound. Thus, the buffer 556 can couple and/or amply a signal from the interconnect loopback 522 such that when external circuitry applies a clock signal to the read clock input 560 the value of the output to the read clock output 558 can be checked to test the integrity of the path from the interface logic 548 to the conductive pad 518 and finally back to the read clock output 558.

[00111] Similarly, the interface logic 548 comprises a read address interconnect 524 connected to the read address input 564. The read address interconnect 524 extends to the surface of the first semiconductor device 562 and connects to conductive pads 526. An interconnect loopback 532 is coupled to the conductive pads 526 and linked to a buffer 522,

allowing for testing of the read address output 554 by external test circuitry. Although only one connection is shown, one of ordinary skill in the art would know how to extend this to parallel data lines (e.g., 8 interconnects, with 8 conductive pads, 8 interconnect loopbacks, 8 buffers, etc.) to form an 8-bit address space. Any other number of bits or address size may be used.

[00112] And for the read address interconnect 524, consider that the test signal is a read address, and the return signal is a return read address obtained from the interconnect loopback 522. The return read address 532 may be applied to a read data output bus 546 of the interface logic 548, amplified or coupled by a buffer 552, tested, etc.

[00113] The interconnect loopbacks 522, 532, 542 in the interface logic 548 may include additional components such as comparators and delay circuits to ensure signal integrity and test timing characteristics. A test may include dynamically adjusting the test signal based on predefined test patterns, allowing comprehensive testing and validation of the interconnects.

[00114] For the clock interconnect 520, the test signal is a clock signal, and the return signal is a return clock signal received from the interconnect loopback 532. Similarly, the return clock signal can be applied to a read data output bus of the interface logic 548, buffered in a register, tested, etc.

[00115] For the read data interconnect 534, the test signal represents test data that is applied via a read data input connection 550 which can be amplified by a tri-state buffer 544, and the return signal is a return test data received via the read data output connection 584 from test data applied to the interconnect loopback 542. The test data may be received and/or outputted to a bus of the interface logic 548, buffered in a register, tested, etc.

[00116] When the first semiconductor device 562 and second semiconductor device 502 are bonded together, their respective conductive pads (518, 516), (526, 528), and (536, 538) are electrically coupled together. This enables the transfer of electrical signals between the first and second semiconductor devices 562, 502.

[00117] The second semiconductor device 502 includes an interface logic 568 consisting of various interconnects (each of which may include a boundary scan cell for testing). This interface logic 568 comprises a read clock interconnect 514 receiving a read clock signal from the first semiconductor device 562, a read address interconnect 530 receiving a read address first semiconductor device 562, and a read data interconnect 540 transmitting data from the memory cells via a read data output 504 to the first semiconductor device 562. That is, the read data from the memory cells 504 is passed through the interface logic 568 to the read data interconnect 540. Similarly, the read address interconnect 530 is passed through the interface

logic 568 to the read address 508, which is used for accessing the memory cells. The read lock interconnect 514 is the clock that is sent to the memory cells and/or internal logic so that the interface logic can buffer the read data as presented to the read data interconnect 540.

[00118] The interface logic 568 can also utilizes a serial test data input 510, a test clock 512, and a serial test data output 566 for performing boundary scanning. These components enable the interface logic 568 to test the connectivity of interconnects and verify signal integrity. The interface logic 548 also includes boundary scan cells including a serial test data in 570 and a serial test data out 574. Optionally, a separate clock, e.g., test clock 574, can be used instead of the read clock 560. However, in some embodiments, the boundary scan cells may use the read clock 560. Thus, the connectivity from the interface logic 548 of the first semiconductor device 562 to the second semiconductor device 502 may be tested to make sure that the integrity of the connectivity therebetween is suitable.

[00119] A boundary scan is a testing technique used to verify the connectivity and integrity of interconnects within semiconductor devices. Thus, a boundary scan in testing the connectivity between the interface logic 548 of the first semiconductor device 562 and the interface logic 568 of second semiconductor device 502, may be used to ensure the suitability of the connectivity. Any, all, or some of the inputs and/or outputs for the interface logics 548, 568 may include boundary scan cells to control, modify, or test any, all, or some of the inputs and/or output.

[00120] The boundary scan test can be done by forming a boundary scan chain, connecting the boundary scan cells within each interface logic 548, 568 in a daisy-chain configuration. This creates a serial shift register arrangement, enabling controlled shifting of test data and return data through the boundary scan chain.

[00121] The boundary scan cells within the interface logics 548, 568 provide the control and capture capabilities to manipulate and observe the test data and return data within the boundary scan chain via a connected device. This can ensure reliable testing of the connectivity between the interface logic 548 of the first semiconductor device 562 and the interface logic 568 of the second semiconductor device 502. Thus, through the boundary scan test, the interconnects between the two interface logics 548, 568 can be thoroughly examined and validated to ensure that the connectivity is suitable and functioning as intended. The boundary scan cells within each interface logic 548, 568, can enable precise control over the test data and return data, allowing for comprehensive analysis and assessment of the connectivity between the two semiconductor devices.

[00122] During testing, various test patterns and data can be loaded into the boundary scan cells through the serial test data input 570 of the first semiconductor device's 562 interface logic 548 and/or the serial test data input 510 of the second semiconductor's 502 interface logic 568. These test patterns simulate different input scenarios and conditions, allowing for the examination of various connectivity scenarios between the two interface logics. The loaded test data is then shifted through the boundary scan chain using the test clocks 512, 574. Please note that the clocks may be tied together, synchronized, and/or other clocks may be used. With each clock cycle, the test data propagates through the serially connected boundary scan cells, advancing to the subsequent cells one by one. This shifting process allows the test data to traverse the interconnects between the two interface logics 548, 568, verifying the connectivity and integrity of the interconnects. This allows for subsequent analysis and comparison with the expected return data. By comparing the sampled return data with the expected values, the integrity of the connectivity between the two interface logics 548, 568 can be accurately assessed.

[00123] Also, at specific points within the boundary scan chain, the return data from the first semiconductor device's 562 interface logic 548 and/or the serial test data input 510 of the second semiconductor's 502 interface logic 568 is sampled into additional boundary scan cells. These boundary scan cells capture and retain the return data for further analysis and comparison.

[00124] Fig. 6 shows a diagram of two semiconductor devices 662, 602, such as two chiplets, that automatically test the connectivity of write interconnects 620, 624, 634 within a semiconductor device and the integrated connectivity in accordance with an embodiment of the present disclosure. The first semiconductor device 662 has several test signal connections 680, 682, 684 which can be used to test a path by examining how the signal is returned via a respective one of a return signal connections 658, 654, 650. In some embodiments, the write interconnects 620, 624, 634 may be integrated with the read interconnects 520, 524, 534 of Fig. 5 on the same interface logic.

[00125] As shown in Fig. 6, the stack 600 of two semiconductor devices 662, 602: an application chiplet (first semiconductor device 662) and a memory chiplet (second semiconductor device 602). The application chiplet 662 includes interconnect loopbacks 622, 632, 642 for interconnect testing before bonding. The interface logic 648 within the application chiplet facilitates communication with external circuitry and includes interconnect loopbacks 622, 632, 642 to test connectivity with conductive pads 618, 626, 636.

[00126] The interface logic 648 includes input/output interfaces for connectivity to the write address 624, the write clock 620, and the write data 634 of the first semiconductor device 662. These interfaces, along with interconnect loopbacks 622, 632, 642, enable testing of the connectivity between the interface logic 648 and the conductive pads (or bonds) 618, 626, 636 prior to bonding. Additionally, the conductive pads 618, 626, 636 of the first semiconductor device 662 may be electrically coupled to the conductive pads 616, 628, 638 of the second semiconductor device 602 such that the interface logic 648 can provide connectivity to write functionality of the memory found within the second semiconductor device 602.

[00127] The interface logic 648 consists of interconnects such as the write clock interconnect 620, connected to a write clock input 660, and terminating at conductive pad 618. It also includes interconnect loopback 622 and a buffer 656. The integrity of the circuit can be tested by applying a clock signal to the write clock input 660 and comparing it with the write clock output 658.

[00128] Similarly, the interface logic 648 includes a write address interconnect 624 connected to the write address input 664 and terminated at conductive pads 626. An interconnect loopback 632 coupled with buffer 652 allows for testing the write address 664.

[00129] The interconnect loopbacks 622, 632, 642 may include additional components such as comparators and delay circuits to ensure signal integrity and to test timing characteristics. The test signals and return signals for testing may include a write address 624, a write data 634, and a write clock signal 620. By applying these signals through interconnect loopbacks and comparing them with the expected values, the connectivity and integrity of the interconnects can be validated.

[00130] When the first semiconductor device 662 and second semiconductor device 602 are bonded together, their respective conductive pads (618, 616), (626, 628), (636, 638) are electrically coupled, enabling the transfer of electrical signals between them.

[00131] The second semiconductor device 602 has its own interface logic 668, which includes interconnects for a write clock 614, a write address 630, and write data 640. The write data applied to the write data 634 interconnect, is passed through the interface logic 668 to the write data 604, which is used to write to the memory cells addressed by the write address 608 on a write clock 606. The write clock interconnect 614 can receive the clock signal to control the writing to the memory cells and internal logic.

[00132] The interface logic 668 also incorporates components for boundary scanning, such as a serial test data input 610, a test clock 612, and a serial test data output 666. Boundary

scanning allows for testing the connectivity of interconnects and verifying signal integrity between the interface logics 648 and 668 of the two semiconductor devices.

[00133] The boundary scan test involves forming a boundary scan chain by connecting boundary scan cells in a daisy-chain configuration within each interface logic 648, 668. This enables controlled shifting of test data and return data through the boundary scan chain. The boundary scan cells provide control and capture capabilities to manipulate and observe the test data and return data within the boundary scan chain. This enables reliable testing of the connectivity between the interface logics 648 and 668. Some or all of the inputs and/or outputs of the interface logics 648, 668 may include boundary scan cells to facilitate the reading, writing, or recording of test data as known to one of ordinary skill in the relevant art.

[00134] During testing, test patterns and data are loaded into the boundary scan cells through the serial test data input 610, 670 of the interface logics 668, 648. These test patterns simulate different input/output scenarios, allowing examination of various connectivity scenarios between the two interface logics 668, 648. The loaded test data is then shifted through the boundary scan chain using the test clocks 612, 674. With each clock cycle, the test data propagates through the boundary scan cells, verifying the connectivity and integrity of the interconnects.

[00135] Return data from the interface logics is sampled into additional boundary scan cells within the boundary scan chain for analysis and comparison. By comparing the sampled return data with the expected values, the integrity of the connectivity between the two interface logics can be accurately assessed.

[00136] Fig. 7 shows a flow chart diagram of a method 700 for testing a semiconductor device 562 (or 662) and bonding together two semiconductor devices 502, 562 (or 602, 662) and performing an integration test after bonding in accordance with an embodiment of the present disclosure.

[00137] The method 700 includes acts 702-716. Act 702 forms a first semiconductor device 562 (or 662) having an interface logic 548 (or 648) with a plurality of interconnects 520, 524, 534 (or 620, 624, 634) electrically coupled to a surface of the first semiconductor device 562 (or 662). Act 704 activates an interconnect loopback (one or more of 522, 532, or 542 (or 622, 632, or 642)) that is coupled to an interconnect (one or more of 520, 524 or 534 (or 620, 624, or 634)) of the plurality of interconnects 520, 524, 534 (or 620, 624, or 634). Act 706 electrically couples a test signal to the interconnect (one or more of 520, 524, or 534 (or 620, 624, or 635)). The test signal may be, including by not limited to, a read address, read data, data, a clock signal, a read clock signal, etc. The test signals may be inputted into an interface

logic 548, 568 (or 648, 668) via a serial test data in, read data in, read address in, or external connects to the interface logic 548, 568 (or 648, 668) etc. A register, buffer, tri-state logic, clocks, comparators, delays, test patterns, etc. as disclosed herein or known by one of ordinary skill in the relevant art may be used for the test signal. Act 708 test a return signal returned from the interconnect loopback (one or more of 522, 532, or 542 (or 622, 632, or 642)) to thereby test a path from the interface logic 548 (or 648) through the interconnect (one or more of 520, 524, or 534 (or 620, 624, or 634)) and the interconnect loopback (one or more of 522, 532, or 542 (or 622, 632, or 642)) and back to the interface logic 548 (or 648). A register, buffer, tri-state logic, clocks, comparators, delays, test patterns, etc. as disclosed herein or known by one of ordinary skill in the relevant art may be used for the return test signal. Any of the test signals may be outputted to connections on an interface logic 548, 568 (or 648, 668) and/or read data out, serial test data out, read address out, read data out, etc.

[00138] A decision 710 determines if the tests indicate that the semiconductor device is of suitable quality. If not, the semiconductor is rejected at 712. If it is, the semiconductor passes and continues to act 714.

[00139] Act 714 bonds the first semiconductor device 562 to a second semiconductor device 502 (or 602). Act 716 bonds the interface logic 568 (or 668) of the second semiconductor device 502 (or 602) to the interface logic 548 (or 648) of the first semiconductor device 562 (or 662) by bonding the plurality of interconnects 514, 530, 540 (or 614, 630, 640) of the second semiconductor device 502 (or 602) to the plurality of interconnects 520, 524, 534 (or 620, 624, 634) of the first semiconductor device 562 (or 662). The bonds can be formed via conductive pads 516, 528, 538, 518, 526, 536 (or 616, 628, 638, 618, 626, 636) on the surfaces of the first and second semiconductor devices 502, 562 (or 602, 662). Act 718 performs a boundary scan to test electrical connections between the plurality of interconnects 520, 524, 534 (or 620, 624, 634) of the first semiconductor device 562 (or 662) and a plurality of interconnects 514, 530, 540 (or 614, 630, 640) of the second semiconductor device 502 (or 602). Act 720 performs a boundary scan to test a connectivity of the complementary interface (e.g., 568 or 668) logic to the interface logic (e.g., 548 or 648). For any boundary scan, a register, a buffer, tri-state logic, clocks, comparators, delays, test patterns, boundary scan cells, etc. as disclosed herein or known by one of ordinary skill in the relevant art may be used.

[00140] A decision 722 determines if the semiconductor device passes the boundary scan tests. If it has not, then the semiconductor is rejected at 724. If it has, then the semiconductor device is considered to be a known-good device 726.

[00141] Various alternatives and modifications can be devised by those skilled in the art without departing from the disclosure. Accordingly, the present disclosure is intended to embrace all such alternatives, modifications, and variances. Additionally, while several embodiments of the present disclosure have been shown in the drawings and/or discussed herein, it is not intended that the disclosure be limited thereto, as it is intended that the disclosure be as broad in scope as the art will allow and that the specification be read likewise. Therefore, the above description should not be construed as limiting, but merely as exemplifications of particular embodiments. And those skilled in the art will envision other modifications within the scope and spirit of the claims appended hereto. Other elements, steps, methods, and techniques that are insubstantially different from those described above and/or in the appended claims are also intended to be within the scope of the disclosure.

[00142] The embodiments shown in the drawings are presented only to demonstrate certain examples of the disclosure. And the drawings described are only illustrative and are non-limiting. In the drawings, for illustrative purposes, the size of some of the elements may be exaggerated and not drawn to a particular scale. Additionally, elements shown within the drawings that have the same numbers may be identical elements or may be similar elements, depending on the context.

[00143] Where the term "comprising" is used in the present description and claims, it does not exclude other elements or steps. Where an indefinite or definite article is used when referring to a singular noun, e.g., "a," "an," or "the," this includes a plural of that noun unless something otherwise is specifically stated. Hence, the term "comprising" should not be interpreted as being restricted to the items listed thereafter; it does not exclude other elements or steps, and so the scope of the expression "a device comprising items A and B" should not be limited to devices consisting only of components A and B. This expression signifies that, with respect to the present disclosure, the only relevant components of the device are A and B.

[00144] The term “stack” as used herein may mean any such coupling, bonding, securing, gluing, electrically coupling, physically coupling, signally coupling, optically coupling, or otherwise interfacing one or more devices together in any orientation such that they are secured together on any heterogeneous or homogenous surfaces between each other.

[00145] Furthermore, the terms "first," "second," "third," and the like, whether used in the description or in the claims, are provided for distinguishing between similar elements and not necessarily for describing a sequential or chronological order. It is to be understood that the terms so used are interchangeable under appropriate circumstances (unless clearly disclosed

otherwise and that the embodiments of the disclosure described herein are capable of operation in other sequences and/or arrangements than are described or illustrated herein.

[00146] Each of the characteristics and examples described above, and combinations thereof, may be said to be encompassed by the present disclosure. The present disclosure thus includes the following non-limiting numbered aspects:

[00147] 1. A method of making a known-good stack, the method comprising: forming a first semiconductor device having an interface logic with a plurality of interconnects electrically coupled to a surface of the first semiconductor device, activating an interconnect loopback configured to receive a first one of the plurality of interconnects and electrically communicate back to the interface logic through the interconnect loopback; electrically coupling a test signal to the first one of the plurality of interconnects; and testing a return signal returned from the interconnect loopback to thereby test a path from the first one of the plurality of interconnects and through the interconnect loopback back to the interface logic.

[00148] 2. The method according to aspect 1, wherein the interconnect loopback is activated by loading the test signal into a buffer.

[00149] 3. The method according to aspect 1, wherein the interconnect loopback is activated by activating a tri-state buffer coupled to one of the interconnect loopback and the first one of the plurality of interconnects.

[00150] 4. The method according to aspect 1, the method further comprising bonding the first semiconductor device to a second semiconductor device.

[00151] 5. The method according to aspect 4, the method further comprising using a boundary scan to test electrical connections between the plurality of interconnects of the first semiconductor device and a complementary plurality of interconnects of the second semiconductor device.

[00152] 6. The method according to aspect 4, the method further comprising: bonding a complementary interface logic of the second semiconductor device with a plurality of complementary interconnects electrically coupled to a surface of the second semiconductor device; and coupling the plurality of interconnects of the first semiconductor device to the complementary plurality of interconnects of the second semiconductor device.

[00153] 7. The method according to aspect 6, further comprising performing a boundary scan to test a connectivity of the complementary interface logic to the interface logic.

[00154] 8. The method according to aspect 1, wherein the act of electrically coupling the test signal to the first one of the plurality of interconnects comprises applying the test signal to the first one of the plurality of interconnects.

[00155] 9. The method according to aspect 1, wherein the act of electrically coupling the test signal to the first one of the plurality of interconnects comprises applying the test signal to the interconnect loopback.

[00156] 10. The method according to aspect 1, wherein: at least one conductive bond is disposed on the surface of the first semiconductor device; the first one of the plurality of interconnects is a conductive path configured to electrically couple the at least one conductive bond with the interface logic; and the interconnect loopback is another conductive path configured to electrically coupled to the interface logic.

[00157] 11. The method according to aspect 1, the method further comprising buffering the test signal in accordance with a clock.

[00158] 12. The method according to aspect 1, the method further comprising buffering the return signal in accordance with a clock.

[00159] 13. The method according to aspect 1, wherein the interface logic includes an external interface coupled to the first one of the plurality of interconnects.

[00160] 14. The method according to aspect 1, wherein the interface logic includes an external interface coupled to the interconnect loopback.

[00161] 15. The method according to aspect 1, wherein the interconnect loopback further comprises a comparator configured to compare the test signal with the return signal for determining signal integrity.

[00162] 16. The method according to aspect 1, wherein the interconnect loopback further comprises a delay circuit configured to introduce a controlled delay in the return signal for testing timing characteristics of the first one of the plurality of interconnects.

[00163] 17. The method according to aspect 1, the method further comprising dynamically adjusting the test signal based on predefined test patterns.

[00164] 18. The method according to aspect 1, the method further comprising: serially loading into a boundary scan cell a test data to thereby generate the test signal on the first one of the plurality of interconnects; sampling the return signal into a second boundary scan cell; and shifting the return signal.

[00165] 19. The method according to aspect 18, the method further comprising comparing the sampled return signal with an expected return signal.

[00166] 20. The method according to aspect 1, wherein: the first one of the plurality of interconnects is a read address interconnect; the test signal is a read address; and the return signal is a return read address returned from the first one of the plurality of interconnects through the interconnect loopback.

[00167] 21. The method according to aspect 20, the method further comprising: applying the return read address to a read data output bus of the interface logic of the first semiconductor device.

[00168] 22. The method according to aspect 20, the method further comprising: signaling a register clock signal into the interface logic; and buffering the return read address in a register.

[00169] 23. The method according to aspect 22, wherein the act of testing the return read address comprises testing an output of the register.

[00170] 24. The method according to aspect 20, wherein the interconnect loopback includes at least one buffer configured to selectively couple the interconnect loopback to the first one of the plurality of interconnects.

[00171] 25. The method according to aspect 1, wherein: the first one of the plurality of interconnects is a clock interconnect; the test signal is a clock signal; and the return signal is a return clock signal returned from the first one of the plurality of interconnects through the interconnect loopback.

[00172] 26. The method according to aspect 25, the method further comprising: applying the return clock signal to a read data output bus of the interface logic of the first semiconductor device.

[00173] 27. The method according to aspect 25, the method further comprising: signaling a register clock signal into the interface logic; and buffering the return clock signal in a register.

[00174] 28. The method according to aspect 27, the method further comprising testing the return clock signal in the register.

[00175] 29. The method according to aspect 25, wherein the interconnect loopback includes at least one tri-state buffer configured to selectively couple the interconnect loopback to the first one of the plurality of interconnects.

[00176] 30. The method according to aspect 1, wherein: the first one of the plurality of interconnects is a read data interconnect; the test signal defines read test data; and the return signal is a return read test data returned from the first one of the plurality of interconnects through the interconnect loopback.

[00177] 31. The method according to aspect 30, the method further comprising: applying the returned read test data to a read data output bus of the interface logic of the first semiconductor device.

[00178] 32. The method according to aspect 30, the method further comprising: signaling a register clock signal into the interface logic; and buffering the return read test data in a register.

[00179] 33. The method according to aspect 32, wherein the act of testing the return read test data comprises testing an output of the register.

[00180] 34. The method according to aspect 30, wherein the interconnect loopback includes at least one tri-state buffer configured to selectively couple the interconnect loopback to the first one of the plurality of interconnects.

[00181] 35. The method according to aspect 1, wherein: the first one of the plurality of interconnects is a write clock interconnect; the test signal defines a write clock signal; and the return signal is a returned write clock signal returned from the first one of the plurality of interconnects through the interconnect loopback.

[00182] 36. The method according to aspect 35, the method further comprising: applying the write clock signal to a read data output bus of the interface logic of the first semiconductor device.

[00183] 37. The method according to aspect 35, the method further comprising: signaling a register clock signal into the interface logic; and buffering the returned write clock signal in a register.

[00184] 38. The method according to aspect 37, wherein the act of testing the returned write clock signal comprises testing an output of the register.

[00185] 39. The method according to aspect 1, wherein: the first one of the plurality of interconnects is a write address interconnect; the test signal defines a write address; and the return signal is a returned write address returned from the first one of the plurality of interconnects through the interconnect loopback.

[00186] 40. The method according to aspect 39, the method further comprising: applying the returned write address to a read data output bus of the interface logic of the first semiconductor device.

[00187] 41. The method according to aspect 39, the method further comprising: signaling a register clock signal into the interface logic; and buffering the returned write address in a register.

[00188] 42. The method according to aspect 41, wherein the act of testing the returned write address comprises testing an output of the register.

[00189] 43. The method according to aspect 1, wherein: the first one of the plurality of interconnects is a write data interconnect; the test signal defines write test data; and the return signal is a returned write test data returned from the first one of the plurality of interconnects through the interconnect loopback.

[00190] 44. The method according to aspect 43, the method further comprising: applying the returned write test data to a read data output bus of the interface logic of the first semiconductor device.

[00191] 45. The method according to aspect 43, the method further comprising: signaling a register clock signal into the interface logic; and buffering the returned write test data in a register.

[00192] 46. The method according to aspect 45, wherein the act of testing the returned write test data comprises testing an output of the register.

[00193] 47. A stack system, the system comprising: a first semiconductor device, the first semiconductor device comprising: an interface logic having a plurality of interconnects electrically coupled to a surface of the first semiconductor device; an interconnect loopback configured to receive a first interconnect from the plurality of interconnects and electrically communicate back to the interface logic through the interconnect loopback; a test signal connection in electrical communication with the first interconnect; and a return signal connection for testing a path from the test signal connection, through the first interconnect, through the interconnect loopback, back to the interface logic, and to the return signal connection.

[00194] 48. The system of aspect 47, further comprising a second semiconductor device bonded to the first semiconductor device.

[00195] 49. The system of aspect 48, the second semiconductor device comprising a complementary plurality of interconnects bonded to the plurality of interconnects of the first semiconductor device, wherein the first and second semiconductor devices are configured to provide a boundary scan chain for testing electrical connections between the plurality of interconnects of the first semiconductor device and the complementary plurality of interconnects of the second semiconductor device.

[00196] 50. The system of aspect 48, further including a complementary interface logic on the second semiconductor device, the complementary interface logic having a plurality of complementary interconnects electrically coupled to a surface of the second

semiconductor device, wherein the plurality of interconnects of the first semiconductor device are coupled to the complementary plurality of interconnects of the second semiconductor device.

[00197] 51. The system of aspect 50, wherein the interface logic and the complementary interface logic are configured to provide a boundary scan to test connectivity therebetween.

[00198] 52. The system of aspect 51, wherein the interface logic and the complementary interface logic are coupled together to form an integration boundary scan to thereby implement the boundary scan.

[00199] 53. The system of aspect 47, the first semiconductor device further comprising a buffer coupled to the test signal from the interconnect loopback.

[00200] 54. The system of aspect 47, the first semiconductor device further comprising a tri-state buffer configured to drive the test signal onto the interconnect loopback.

[00201] 55. The system of aspect 47, wherein the test signal connection is electrically coupled to the first interconnect.

[00202] 56. The system of aspect 47, wherein the test signal connection is electrically coupled to the interconnect loopback.

[00203] 57. The system of aspect 47, wherein: the first interconnect is a conductive path configured to electrically couple a conductive bond on the surface of the first semiconductor device with the interface logic, and the interconnect loopback is a conductive path electrically coupled to the interface logic and the conductive bond.

[00204] 58. The system of aspect 47, wherein the interface logic includes an external interface coupled to the first interconnect.

[00205] 59. The system of aspect 47, wherein the interface logic includes an external interface coupled to the interconnect loopback.

[00206] 60. The system of aspect 47, wherein the interconnect loopback includes a comparator configured to compare the test signal with the return signal for determining signal integrity.

[00207] 61. The system of aspect 47, wherein the interconnect loopback includes a delay circuit configured to introduce a controlled delay in the return signal to thereby test timing characteristics of the first interconnect.

[00208] 62. The system of aspect 47, wherein the test signal connection is configured to dynamically adjust a test signal based upon a predefined test pattern.

[00209] 63. The system of aspect 47, further comprising: a boundary scan cell configured to generate the test signal on the first interconnect; and a second boundary scan cell configured to sample the return signal.

[00210] 64. The system of aspect 63, further comprising a comparator configured to compare the sampled return signal with an expected return signal.

[00211] 65. The system of aspect 47, wherein: the first interconnect is a read address interconnect, the test signal connection is configured to receive a read address, and the return signal is configured to be a returned read address from the first interconnect through the interconnect loopback.

[00212] 66. The system of aspect 65, the system further comprising a read data output bus configured to receive the returned read address.

[00213] 67. The system of aspect 65, further comprising a register configured to buffer the returned read address on a register clock signal.

[00214] 68. The system of aspect 67, further comprising a comparator configured to test the returned read address being outputted by the register.

[00215] 69. The system of aspect 47, wherein: the first interconnect is a clock interconnect, the test signal is a clock signal, and the return signal is a returned clock signal from the first interconnect through the interconnect loopback.

[00216] 70. The system of aspect 69, further comprising a read data output bus configured to receive the returned clock signal from the interface logic.

[00217] 71. The system of aspect 69, further comprising a register configured to buffer a returned clock signal upon receiving a register clock signal.

[00218] 72. The system of aspect 71, further comprising a comparator configured to compare the returned clock signal in the register to a predetermined value.

[00219] 73. The system of aspect 47, wherein: the first interconnect is a read data interconnect, the test signal connection configured to receive read test data, and the return signal is a returned read test data from the first interconnect through the interconnect loopback.

[00220] 74. The system of aspect 73, further comprising a read data output bus configured to receive the returned read test data.

[00221] 75. The system of aspect 73, further comprising: a register clock signal connection to the interface logic; and a register configured to buffer the returned read test data on a clock signal received via the register clock signal connection.

[00222] 76. The system of aspect 75, further comprising a comparator configured to test the returned read test data to a predetermined value.

[00223] 77. The system of aspect 73, further comprising at least one tri-state buffer configured to selectively couple the interconnect loopback to the first interconnect of the plurality of interconnects.

[00224] 78. The system of aspect 47, wherein: the first interconnect is a write clock interconnect, the test signal is a write clock signal, and the return signal is a returned write clock signal from the first interconnect through the interconnect loopback.

[00225] 79. The system of aspect 78, further comprising a read data output bus configured to receive the returned write clock signal from the interface logic.

[00226] 80. The system of aspect 78, further comprising: a register clock signal connector; and a register configured to buffer the returned write clock signal in response to a register clock signal from the register clock signal connector.

[00227] 81. The system of aspect 80, further comprising a comparator configured to compare the returned write clock signal to a predetermined value.

[00228] 82. The system of aspect 47, wherein: the first interconnect is a write address interconnect, the test signal is a write address, and the return signal is a returned write address from the first interconnect through the interconnect loopback.

[00229] 83. The system of aspect 82, further comprising a read data output bus configured to receive the returned write address from the interface logic.

[00230] 84. The system of aspect 82, further comprising: a register clock signal connection; and a register configured to buffer the returned write address upon a register clock signal received from the register clock signal connection.

[00231] 85. The system of aspect 84, further comprising a comparator configured to compare an output of the register to a predetermined value.

[00232] 86. The system of aspect 47, wherein: the first interconnect is a write data interconnect, the test signal comprises write test data, and the return signal is a returned write test data from the first interconnect through the interconnect loopback.

[00233] 87. The system of aspect 86, further comprising a read data output bus configured to receive the returned write test data from the interface logic.

[00234] 88. The system of aspect 86, further comprising: a register clock signal interface; and a register configured to buffer the returned write test data when a register clock signal is received via the register clock signal interface.

[00235] 89. The system of aspect 88, further comprising a comparator configured to compare an output of the register to a predetermined value.

[00236] 90. A method of manufacturing, the method comprising: forming a first semiconductor device according to one of aspects 47-89.

[00237] 91. A method of forming a stack of semiconductor devices, the method comprising: stacking a first semiconductor device according to one of aspects 47-89 on another semiconductor device.

[00238] 92. A method of forming a stack of semiconductor devices, the method comprising: providing a first semiconductor device according to one of aspects 47-89; and bonding another semiconductor device to the first semiconductor device.

[00239] 93. A method of using semiconductor devices, the method comprising: providing a first semiconductor device according to one of aspects 47-89; and testing one of the plurality of interconnects.

[00240] 94. A method of designing a semiconductor device, the method comprising: forming a digital representation of an interface logic in a first semiconductor device according to one of aspects 47-89.

[00241] 95. The method according to aspect 94, further comprising forming a photomask of the digital representation.

[00242] 96. A system comprising: a first semiconductor device according to one of aspects 47-89 having means for testing an interconnect of the plurality of interconnects.

What is claimed is:

1. A method of making a known-good stack, the method comprising:

forming a first semiconductor device having an interface logic with a plurality of interconnects electrically coupled to a surface of the first semiconductor device,

activating an interconnect loopback configured to receive a first one of the plurality of interconnects and electrically communicate back to the interface logic through the interconnect loopback;

electrically coupling a test signal to the first one of the plurality of interconnects; and

testing a return signal returned from the interconnect loopback to thereby test a path from the first one of the plurality of interconnects and through the interconnect loopback back to the interface logic.

2. The method according to claim 1, wherein the interconnect loopback is activated by loading the test signal into a buffer.

3. The method according to claim 1, wherein the interconnect loopback is activated by activating a tri-state buffer coupled to one of the interconnect loopback and the first one of the plurality of interconnects.

4. The method according to claim 1, the method further comprising bonding the first semiconductor device to a second semiconductor device.

5. The method according to claim 4, the method further comprising using a boundary scan to test electrical connections between the plurality of interconnects of the first semiconductor device and a complementary plurality of interconnects of the second semiconductor device.

6. The method according to claim 4, the method further comprising:

bonding a complementary interface logic of the second semiconductor device with a plurality of complementary interconnects electrically coupled to a surface of the second semiconductor device; and

coupling the plurality of interconnects of the first semiconductor device to the complementary plurality of interconnects of the second semiconductor device.

7. The method according to claim 6, further comprising performing a boundary scan to test a connectivity of the complementary interface logic to the interface logic.

8. The method according to claim 1, wherein the act of electrically coupling the test signal to the first one of the plurality of interconnects comprises applying the test signal to the first one of the plurality of interconnects.

9. The method according to claim 1, wherein the act of electrically coupling the test signal to the first one of the plurality of interconnects comprises applying the test signal to the interconnect loopback.

10. The method according to claim 1, wherein:

at least one conductive bond is disposed on the surface of the first semiconductor device;

the first one of the plurality of interconnects is a conductive path configured to electrically couple the at least one conductive bond with the interface logic; and

the interconnect loopback is another conductive path configured to electrically coupled to the interface logic.

11. The method according to claim 1, the method further comprising buffering the test signal in accordance with a clock.

12. The method according to claim 1, the method further comprising buffering the return signal in accordance with a clock.

13. The method according to claim 1, wherein the interface logic includes an external interface coupled to the first one of the plurality of interconnects.

14. The method according to claim 1, wherein the interface logic includes an external interface coupled to the interconnect loopback.

15. The method according to claim 1, wherein the interconnect loopback further comprises a comparator configured to compare the test signal with the return signal for determining signal integrity.

16. A stack system, the system comprising:

a first semiconductor device, the first semiconductor device comprising:

an interface logic having a plurality of interconnects electrically coupled to a surface of the first semiconductor device;

an interconnect loopback configured to receive a first interconnect from the plurality of interconnects and electrically communicate back to the interface logic through the interconnect loopback;

a test signal connection in electrical communication with the first interconnect; and

a return signal connection for testing a path from the test signal connection, through the first interconnect, through the interconnect loopback, back to the interface logic, and to the return signal connection.

17. The stack system of claim 16, further comprising a second semiconductor device bonded to the first semiconductor device.

18. The stack system of claim 16, the second semiconductor device comprising a complementary plurality of interconnects bonded to the plurality of interconnects of the first semiconductor device, wherein the first and second semiconductor devices are configured to provide a boundary scan chain for testing electrical connections between the plurality of interconnects of the first semiconductor device and the complementary plurality of interconnects of the second semiconductor device.

19. The stack system of claim 16, further including a complementary interface logic on the second semiconductor device, the complementary interface logic having a plurality of complementary interconnects electrically coupled to a surface of the second semiconductor device, wherein the plurality of interconnects of the first semiconductor device are coupled to the complementary plurality of interconnects of the second semiconductor device.

20. The stack system of claim 19, wherein the interface logic and the complementary interface logic are configured to provide a boundary scan to test connectivity therebetween.

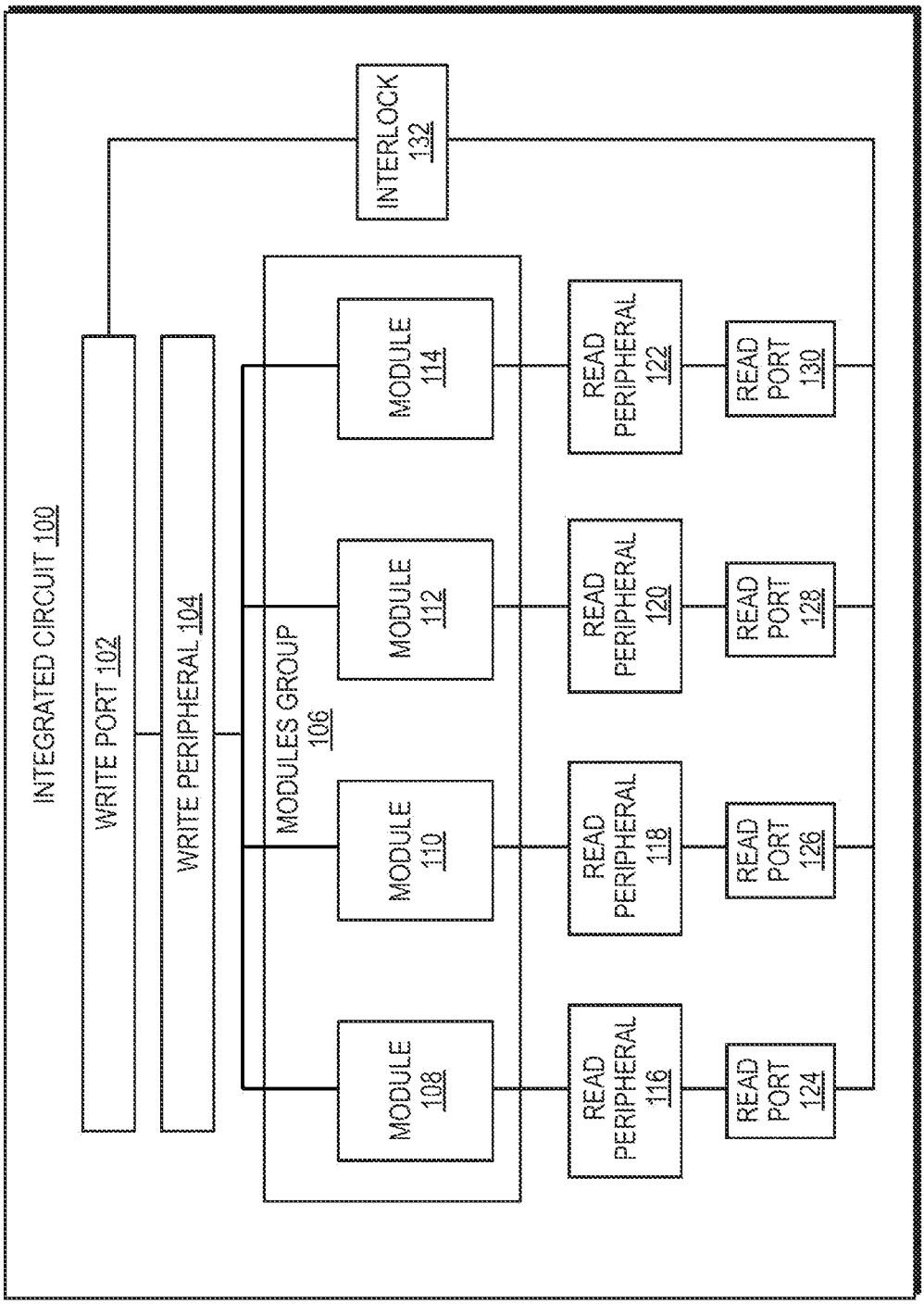

INTEGRATED CIRCUIT 100
WRITE PORT 102
WRITE PERIPHERAL 104
MODULES GROUP 106
MODULE 108
MODULE 110
MODULE 112
MODULE 114
INTERLOCK 132
READ PERIPHERAL 116
READ PERIPHERAL 118
READ PERIPHERAL 120
READ PERIPHERAL 122
READ PORT 124
READ PORT 126
READ PORT 128
READ PORT 130

FIG. 1

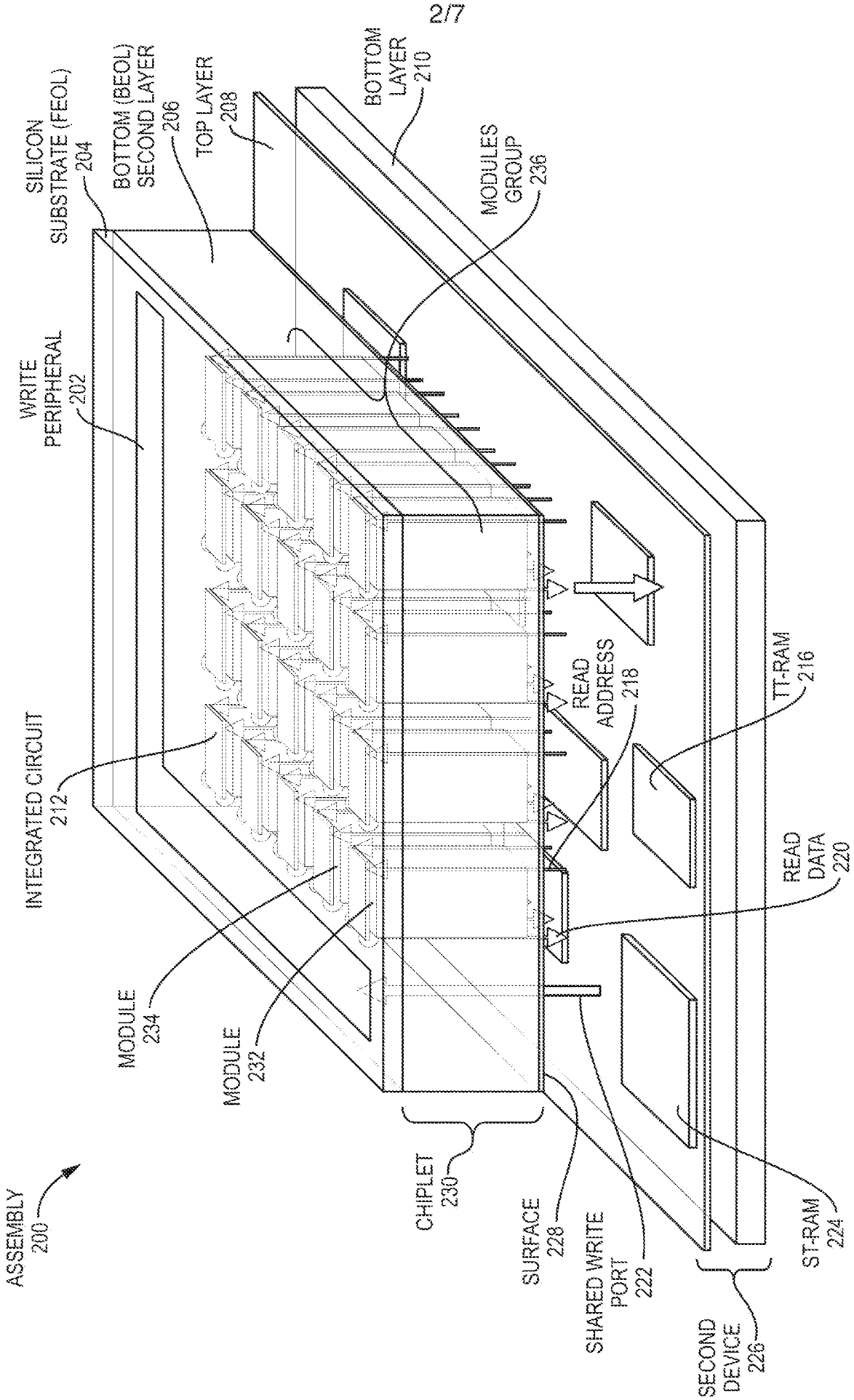

ASSEMBLY 200
SILICON SUBSTRATE (FEOL) 204
BOTTOM (BEOL) SECOND LAYER 206
TOP LAYER 208
BOTTOM LAYER 210
MODULES GROUP 236
WRITE PERIPHERAL 202
INTEGRATED CIRCUIT 212
MODULE 234
MODULE 232
CHIPLET 230
SURFACE 228
SHARED WRITE PORT 222
SECOND DEVICE 226
ST-RAM 224
READ ADDRESS 218
TT-RAM 216
READ DATA 220

FIG. 2

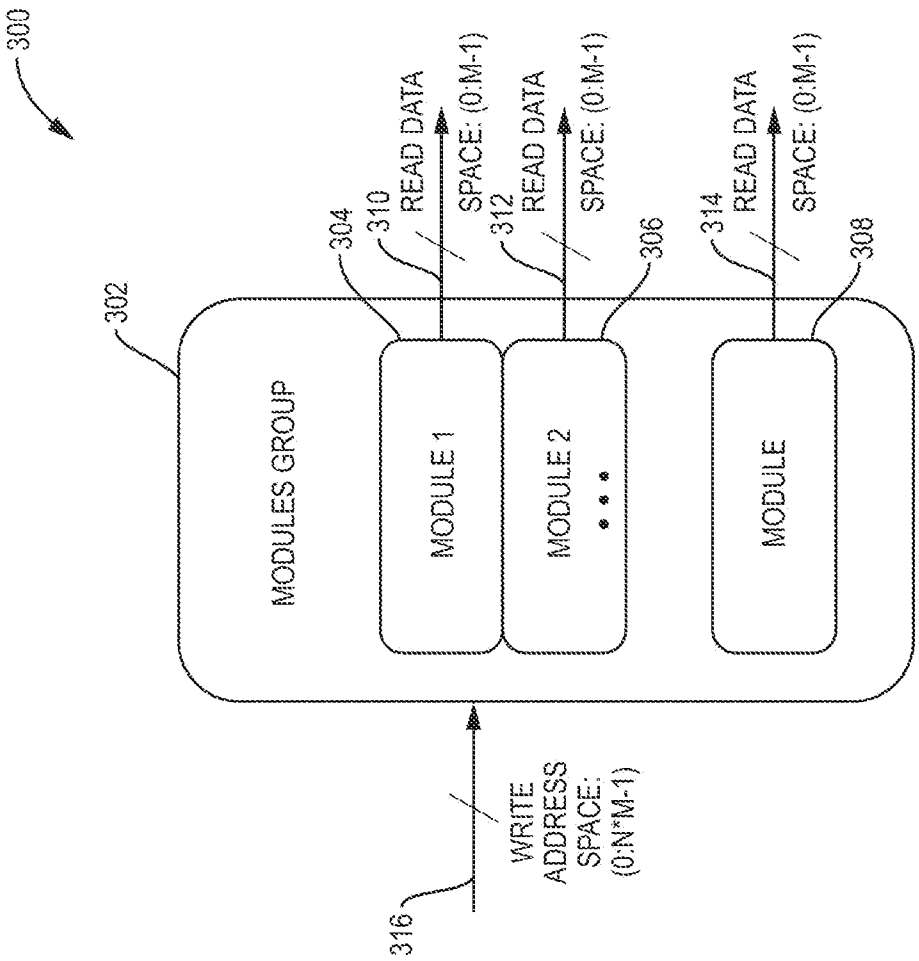

300
302
MODULES GROUP
MODULE 1
MODULE 2
• • •
MODULE
304
306
308
310
312
314
316
READ DATA
SPACE: (0:M-1)
READ DATA
SPACE: (0:M-1)
READ DATA
SPACE: (0:M-1)
WRITE ADDRESS SPACE: (0:N*M-1)

FIG. 3

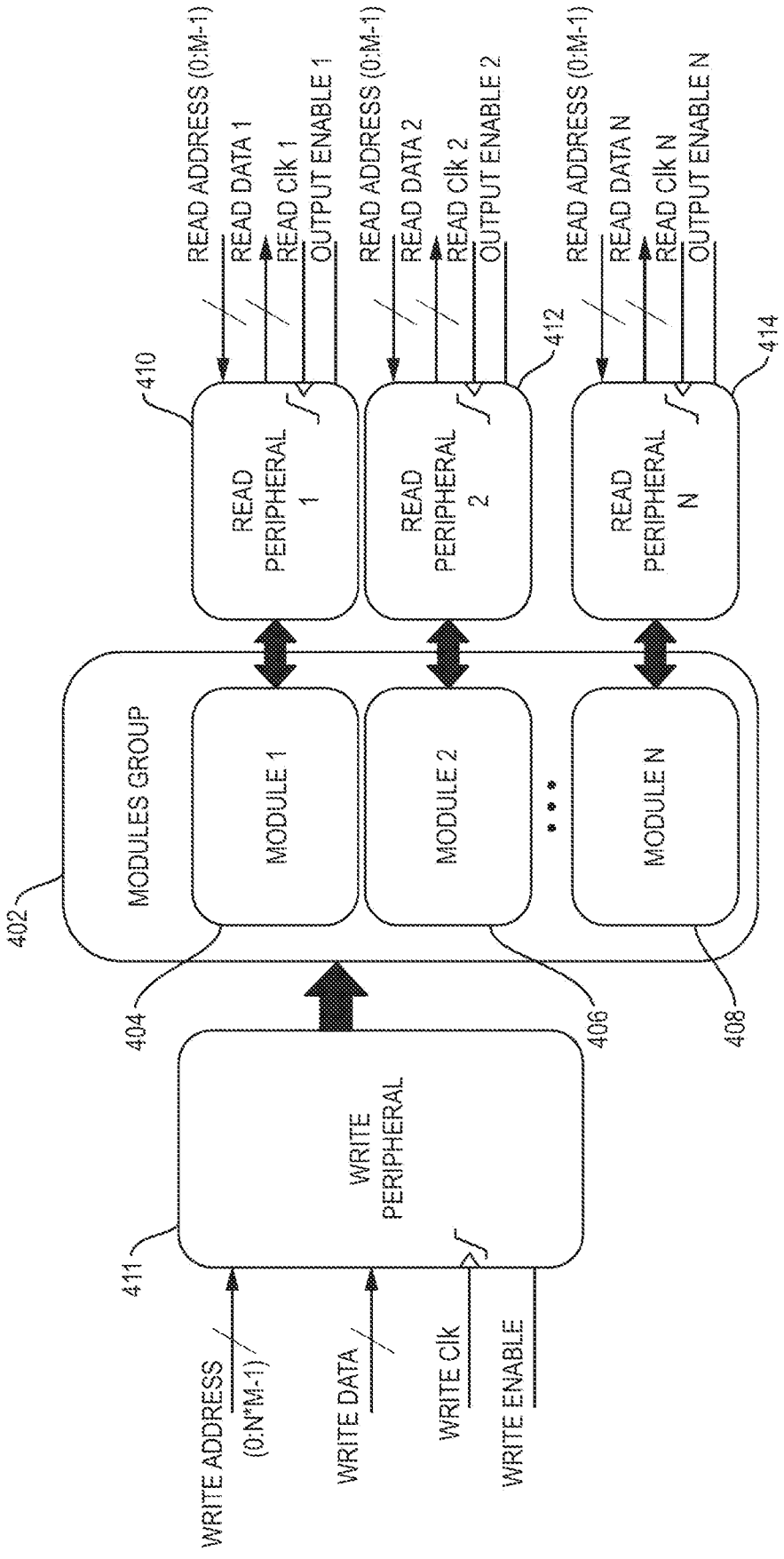

400
READ ADDRESS (0:M-1)
READ DATA 1
READ Clk 1
OUTPUT ENABLE 1
READ ADDRESS (0:M-1)
READ DATA 2
READ Clk 2
OUTPUT ENABLE 2
READ ADDRESS (0:M-1)
READ DATA N
READ Clk N
OUTPUT ENABLE N
410
412
414
READ PERIPHERAL 1
READ PERIPHERAL 2
READ PERIPHERAL N
MODULES GROUP
MODULE 1
MODULE 2
MODULE N
402
404
406
408
411
WRITE PERIPHERAL
WRITE ADDRESS (0:N*M-1)
WRITE DATA
WRITE Clk
WRITE ENABLE

FIG. 4

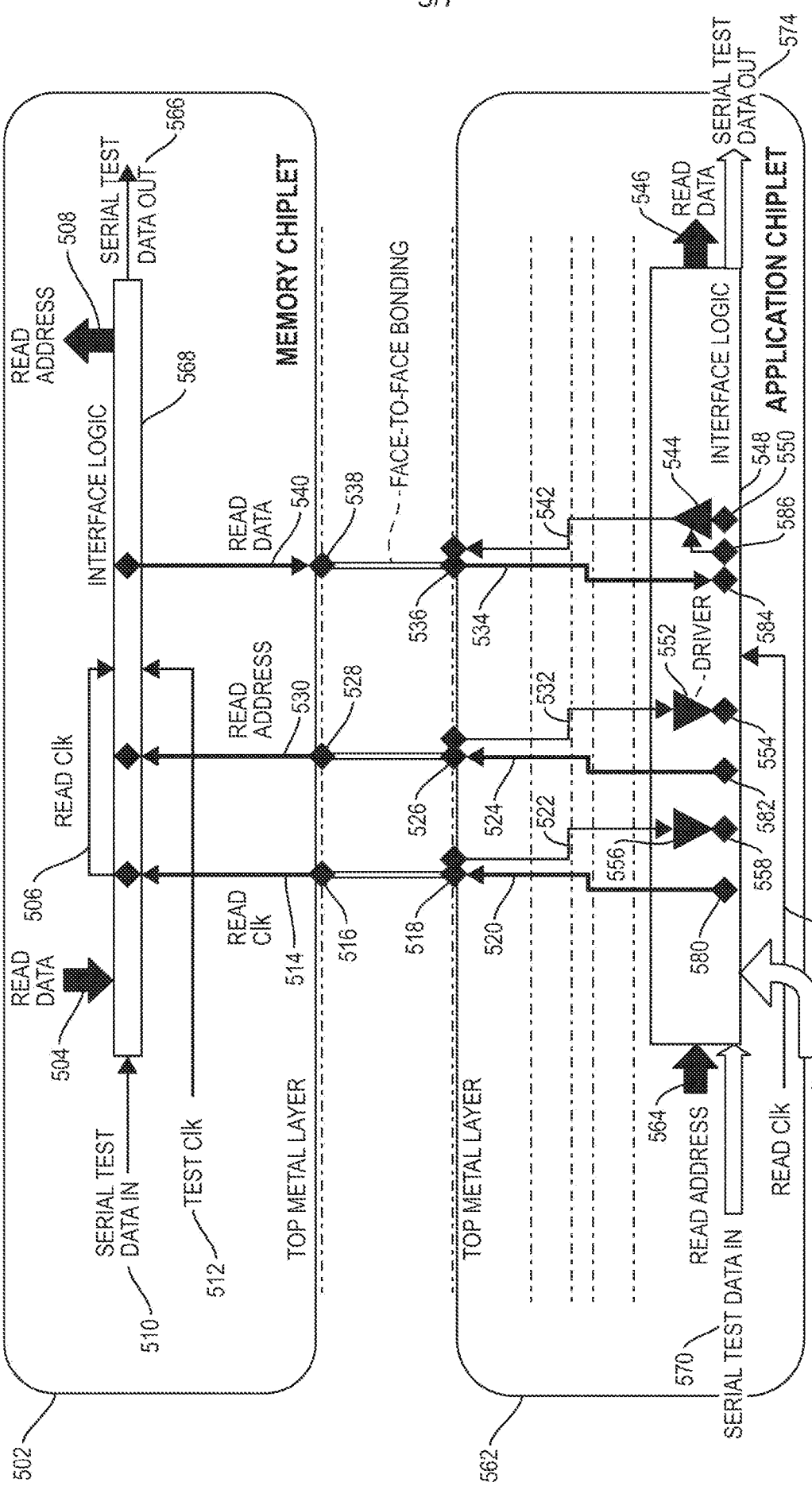

500
MEMORY CHIPLET
APPLICATION CHIPLET
FACE-TO-FACE BONDING
INTERFACE LOGIC
INTERFACE LOGIC
READ ADDRESS
SERIAL TEST DATA OUT
READ DATA
READ Clk
SERIAL TEST DATA IN
TEST Clk
TOP METAL LAYER
TOP METAL LAYER
DRIVER
READ ADDRESS
READ DATA
SERIAL TEST DATA OUT
READ Clk
TEST Clk
SERIAL TEST DATA IN
502
504
506
508
510
512
514
516
518
520
522
524
526
528
530
532
534
536
538
540
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FIG. 5

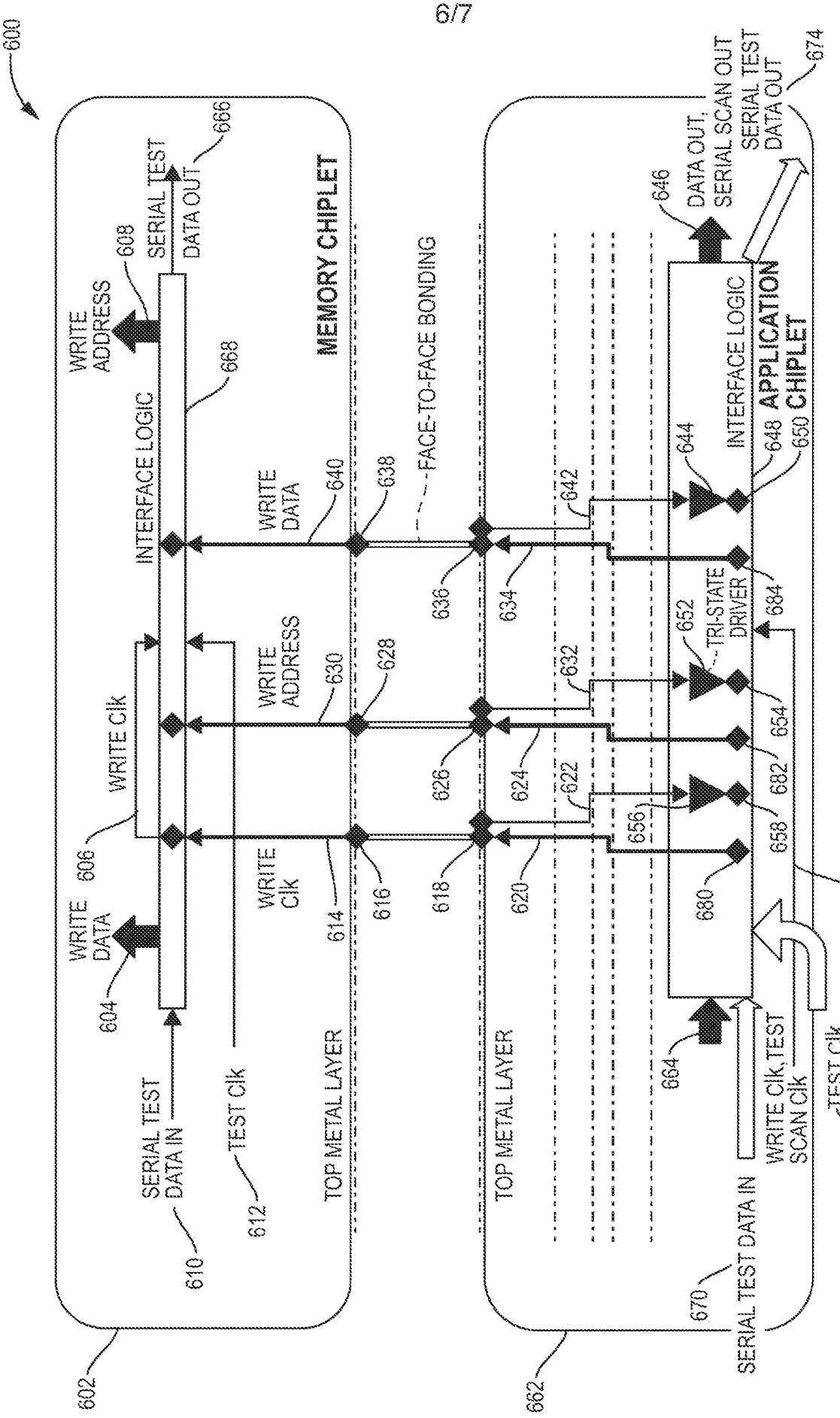

600
602
MEMORY CHIPLET
WRITE ADDRESS
608
SERIAL TEST DATA OUT
666
INTERFACE LOGIC
668
WRITE DATA
640
638
FACE-TO-FACE BONDING
WRITE Clk
606
WRITE ADDRESS
630
628
WRITE DATA
604
WRITE Clk
614
616
SERIAL TEST DATA IN
610
TEST Clk
612
TOP METAL LAYER
636
634
626
624
618
620
662
APPLICATION CHIPLET
646
DATA OUT, SERIAL SCAN OUT
SERIAL TEST DATA OUT
674
INTERFACE LOGIC
644
642
648
650
TRI-STATE DRIVER
652
632
684
654
682
622
656
658
680
660
664
WRITE Clk, TEST SCAN Clk
TEST Clk
674
670
SERIAL TEST DATA IN
TOP METAL LAYER

FIG. 6

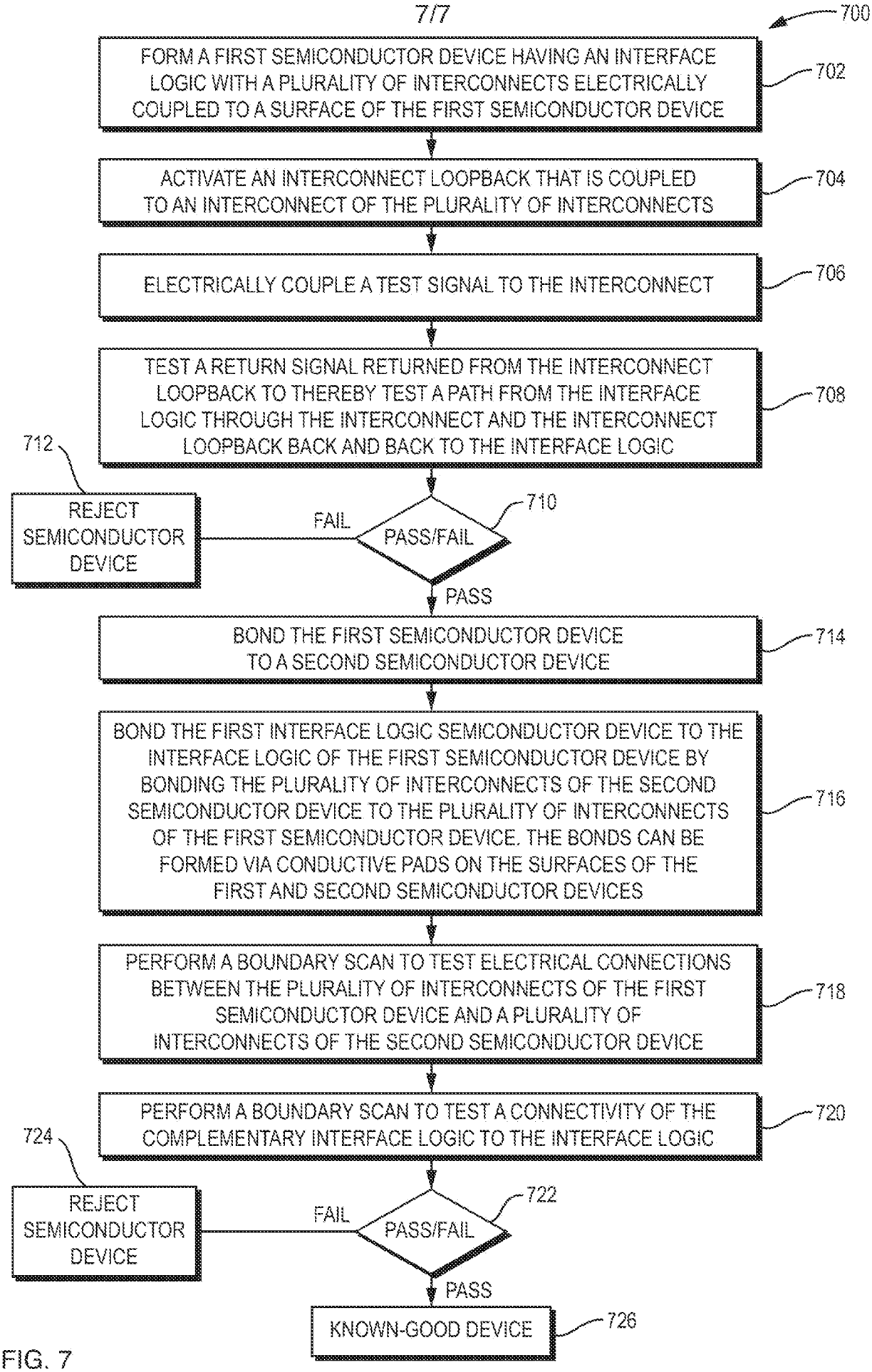

700
FORM A FIRST SEMICONDUCTOR DEVICE HAVING AN INTERFACE LOGIC WITH A PLURALITY OF INTERCONNECTS ELECTRICALLY COUPLED TO A SURFACE OF THE FIRST SEMICONDUCTOR DEVICE
702
ACTIVATE AN INTERCONNECT LOOPBACK THAT IS COUPLED TO AN INTERCONNECT OF THE PLURALITY OF INTERCONNECTS
704
ELECTRICALLY COUPLE A TEST SIGNAL TO THE INTERCONNECT
706
TEST A RETURN SIGNAL RETURNED FROM THE INTERCONNECT LOOPBACK TO THEREBY TEST A PATH FROM THE INTERFACE LOGIC THROUGH THE INTERCONNECT AND THE INTERCONNECT LOOPBACK BACK AND BACK TO THE INTERFACE LOGIC
708
712
REJECT SEMICONDUCTOR DEVICE
FAIL
PASS/FAIL
710
PASS
BOND THE FIRST SEMICONDUCTOR DEVICE TO A SECOND SEMICONDUCTOR DEVICE
714
BOND THE FIRST INTERFACE LOGIC SEMICONDUCTOR DEVICE TO THE INTERFACE LOGIC OF THE FIRST SEMICONDUCTOR DEVICE BY BONDING THE PLURALITY OF INTERCONNECTS OF THE SECOND SEMICONDUCTOR DEVICE TO THE PLURALITY OF INTERCONNECTS OF THE FIRST SEMICONDUCTOR DEVICE. THE BONDS CAN BE FORMED VIA CONDUCTIVE PADS ON THE SURFACES OF THE FIRST AND SECOND SEMICONDUCTOR DEVICES
716
PERFORM A BOUNDARY SCAN TO TEST ELECTRICAL CONNECTIONS BETWEEN THE PLURALITY OF INTERCONNECTS OF THE FIRST SEMICONDUCTOR DEVICE AND A PLURALITY OF INTERCONNECTS OF THE SECOND SEMICONDUCTOR DEVICE
718
PERFORM A BOUNDARY SCAN TO TEST A CONNECTIVITY OF THE COMPLEMENTARY INTERFACE LOGIC TO THE INTERFACE LOGIC
720
724
REJECT SEMICONDUCTOR DEVICE
FAIL
PASS/FAIL
722
PASS
KNOWN-GOOD DEVICE
726

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2024/041392

A. CLASSIFICATION OF SUBJECT MATTER

INV. G11C29/02 H01L29/66 H01L29/51 H01L29/78 G06F1/18
G01R31/3185 H01L29/04 H01L29/786 H01L21/28 H10B51/30
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	ARDALAN SHAHAB ET AL: "Bunch of Wires: An Open Die-to-Die Interface", 2020 IEEE SYMPOSIUM ON HIGH-PERFORMANCE INTERCONNECTS (HOTI), IEEE, 19 August 2020 (2020-08-19), pages 9-16, XP033821792, DOI: 10.1109/HOTI51249.2020.00017 [retrieved on 2020-09-08]	1-12, 15-20
Y	figures 1,2,7,8	13,14

-/--

[x] Further documents are listed in the continuation of Box C.

[ ] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance;; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance;; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 October 2024	15/11/2024

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Wolff, Norbert

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INTERNATIONAL SEARCH REPORT

International application No
PCT/US2024/041392

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	HUTNER M ET AL: "Special Session: Test Challenges in a Chiplet Marketplace", 2020 IEEE 38TH VLSI TEST SYMPOSIUM (VTS), IEEE, 5 April 2020 (2020-04-05), pages 1-12, XP033777297, DOI: 10.1109/VTS48691.2020.9107636 [retrieved on 2020-06-03] figure 11	13,14
A	ABDENNADHER SALEM: "Testing Inter-Chiplet Communication Interconnects in a Disaggregated SoC Design", 2021 IEEE INTERNATIONAL CONFERENCE ON DESIGN & TEST OF INTEGRATED MICRO & NANO-SYSTEMS (DTS), IEEE, 7 June 2021 (2021-06-07), pages 1-7, XP033951507, DOI: 10.1109/DTS52014.2021.9498132 [retrieved on 2021-07-27] abstract	1-20
A	ARDALAN SHAHAB ET AL: "An Open Inter-Chiplet Communication Link: Bunch of Wires (BoW)", IEEE MICRO, IEEE SERVICE CENTER, LOS ALAMITOS, CA, US, vol. 41, no. 1, 25 November 2020 (2020-11-25), pages 54-60, XP011833512, ISSN: 0272-1732, DOI: 10.1109/MM.2020.3040410 [retrieved on 2021-01-26] abstract; figure 1	1-20

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