# United States Patent

**Endo et al.**

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## [54] TRAFFIC SIGNAL CONTROL SYSTEM


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[52] **U.S. Cl.** ..... **340/40,** 340/35
[51] **Int. Cl.** ..... **G08g 1/00**
[58] **Field of Search** ..... 340/35



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[57] **ABSTRACT**

A system for controlling the traffic signals within a relatively wide district divided into a plurality of subdistricts, in each of which there are distributed many traffic signals at different places. A submaster controller coordinately controls many local controllers within each subdistrict, and a master controller controls all the submaster controllers within the wide district. The master controller gives the same cycle pulses and the same series of synchronizing pulses, but different offsets, to different submaster controllers, and each submaster controller provides a second series of synchronizing pulses, which are displaced in time from the first series of synchronizing pulses by the offset time given to the submaster controller, to the local controllers belonging to the submaster controller, so that the local controllers control their respective traffic signals on the basis of the synchronizing pulses received from the submaster controller. Thus, with proper different offsets given to the different submaster controllers, all the traffic signals in the wide district are coordinately controlled in accordance with the actual traffic conditions in the different subdistricts for establishment of smooth traffic flows throughout the wide district.


**4 Claims, 4 Drawing Figures**

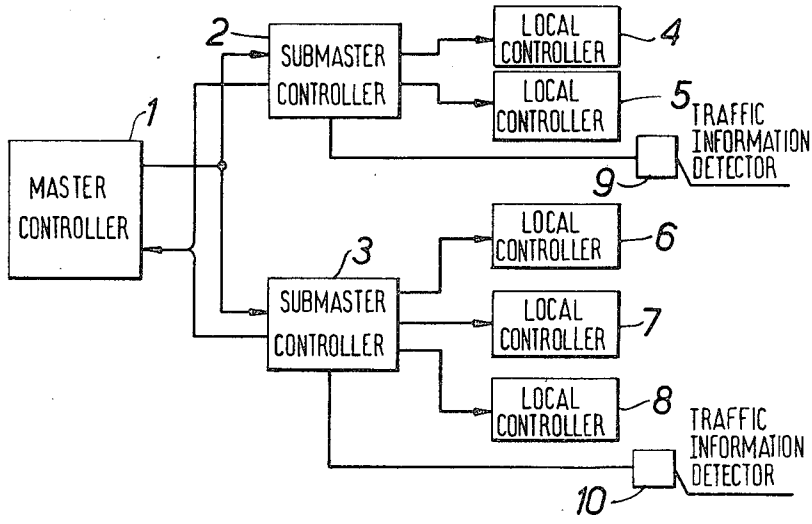

FIG. 1.

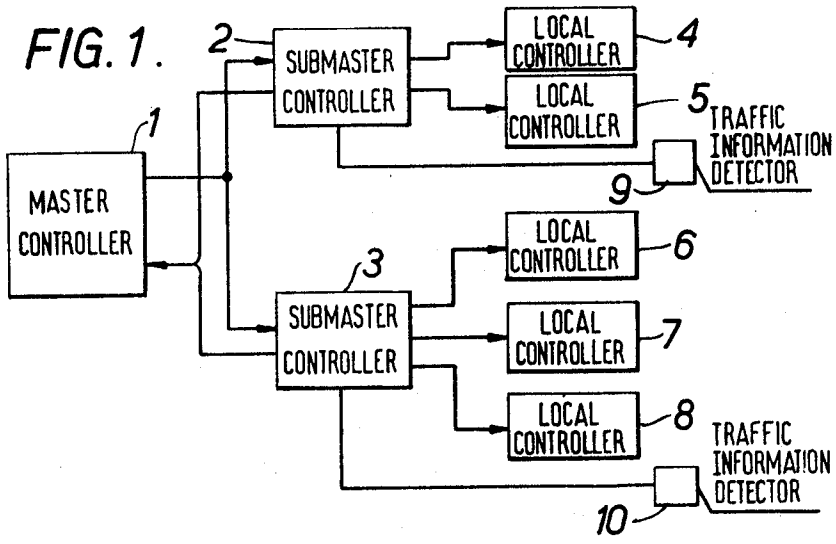


FIG. 2.

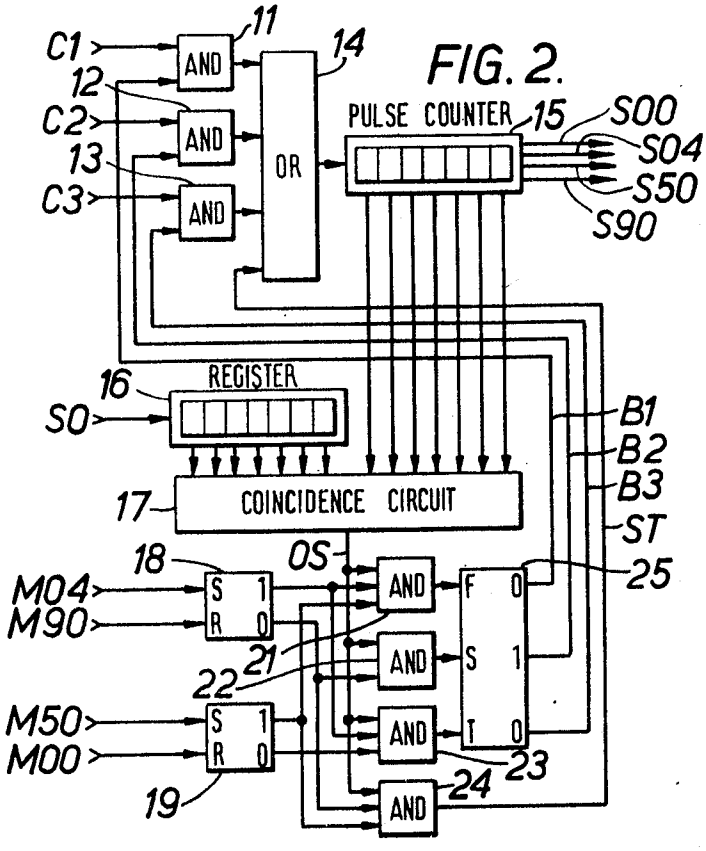


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FIG. 3.

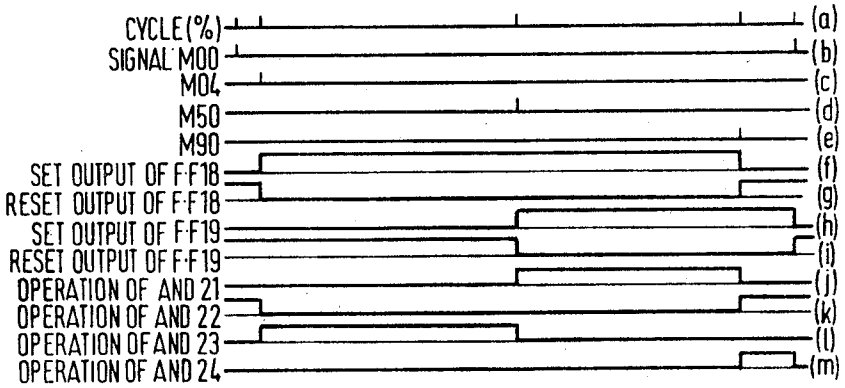
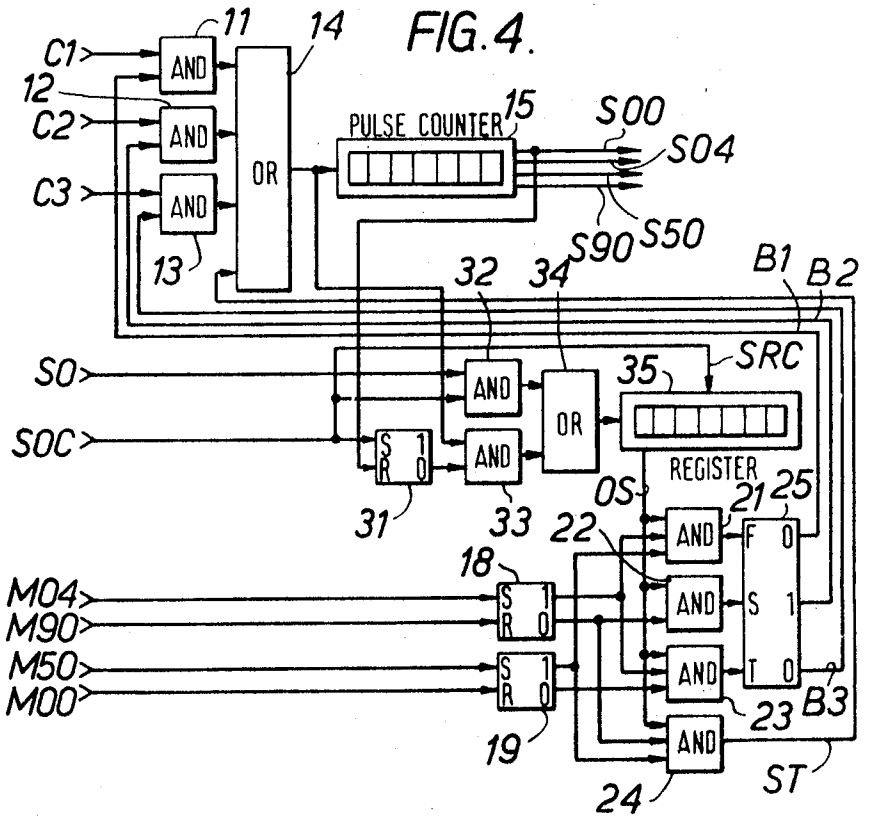



FIG. 4.

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# TRAFFIC SIGNAL CONTROL SYSTEM

This invention relates to a system for controlling the traffic signals within a relatively wide district.

There are known many systems which coordinately control many traffic signals distributed over a wide district. Suppose that the traffic signals within a certain area are coordinately controlled from a central controller and that the traffic signals within a different area adjacent to the first-mentioned area are also coordinately controlled from another central controller. If there is no reaction existing between the two central controllers, it is highly probable that confusion should arise to the traffic especially near the border between the two neighboring areas, thereby seriously impairing the effect of the coordinated signal control within the individual areas.

Accordingly, it is one object of the invention to provide a system for coordinately controlling the traffic signals in a wide district divided into a plurality of subdistricts for establishment of smooth traffic flows therebetween.

Another object of the invention is to provide a system for coordinately controlling the traffic signals in a wide district divided into a plurality of subdistricts, wherein there are provided a plurality of submaster controllers each for one of the subdistricts to coordinately control a plurality of local controllers directly controlling their respective traffic signals within the subdistrict, and wherein there is further provided a single master controller to coordinately control the submaster controllers for establishment of smooth traffic flows between the subdistricts.

In accordance with the invention, a relatively wide district within which the traffic signals are to be controlled is divided into a plurality of subdistricts, for each of which a submaster controller is provided to coordinately control many local controllers within the subdistrict. Each local controller controls the traffic signals belonging to it. A single master controller is provided to control all the submaster controllers within the wide district. The master controller gives the same cycle pulses and series of synchronizing pulses to all the submaster controllers. For coordinate control of the traffic signals between neighboring subdistricts, however, the master controller gives different offsets to different submaster controllers in neighboring subdistricts. Each submaster controller provides a second series of synchronizing pulses, which are displaced in time from the first series of synchronizing pulses by the offset time given to the submaster controller, to the local controllers belonging to the submaster controller, so that on the basis of these synchronizing pulses each local controller controls its own traffic signals. Thus, with suitable offsets given to different subdistricts, the traffic signals within the wide district can be coordinately controlled in accordance with the actual traffic conditions in the individual subdistricts.

The invention will be better understood from the following description of a preferred embodiment thereof with reference to the accompanying drawing, wherein;

FIG. 1 is a general layout of the system of the invention shown as an electrical block diagram;

FIG. 2 is a detailed electrical block diagram of the submaster controller used in the system;

FIG. 3 is a time chart of the various signals in the circuit of FIG. 2 for explanation of the operation thereof; and

FIG. 4 is a diagram similar to FIG. 2 but showing a modified form of the submaster controller.

In the embodiment of FIG. 1, it is assumed that the system covers two subdistricts, although in practice as many submaster controllers as are required may be controlled by a single master controller in a similar manner. One of the two subdistricts includes two local controllers 4 and 5, and the other, three local controllers 6, 7 and 8. As many local controllers as are required may be provided in each subdistrict. A submaster controller 2 is provided to control the local controllers 4 and 5; and a second submaster controller 3, to control the local controllers 6, 7 and 8. In practice, for example, the whole district of a city may be divided into as many subdistricts as are required so that a submaster controller is provided for each subdistrict to control the local controllers distributed at different places within the subdistrict.



In each subdistrict, a traffic information detector 9, 10 is provided to detect the present traffic conditions in the subdistrict. The submaster controller 2 coordinately controls the local controllers 4 and 5, with the splits and offsets as determined by the submaster controller on the basis of the traffic information received from the detector 9; and the submaster controller 3 coordinately controls the local controllers 6, 7 and 8, with their splits and offsets as determined by the submaster controller 3 on the basis of the traffic information received from the detector 10.

The submaster controllers 2 and 3 transmit the traffic informations received from the detectors 9 and 10, respectively, to a single master controller 1, which determines the signal cycle of all the traffic signals in the system and the offsets of the submaster controllers 2 and 3.

When the master controller has determined the signal cycle, it produces corresponding pulses (to be referred to as "cycle pulses") having a frequency inversely proportional to the cycle length. The submaster controllers operate on the basis of the cycle pulses received from the master controller, as will be described later, and at the same time transmit the cycle pulses to the local controllers 4, 5, 6, 7 and 8.

Besides the cycle pulses, the master controller 1 transmits to the submaster controllers those pulses which are in synchronism with each signal cycle (to be referred to as "SMC synchronizing pulses"), on the basis of which the submaster controllers operate, as will be described later in detail. The master controller also transmits to the submaster controllers the signals (to be referred to as "SMC offset signals") which command different offsets to be taken by different submaster controllers. The submaster controller 2 produces those synchronizing pulses (to be referred to as "LC synchronizing pulses") from which the SMC synchronizing pulses are displaced by the offset time taken by the submaster controller 2 and applies the LC synchronizing pulses to the local controllers 4 and 5; and the submaster controller 3 produces LC synchronizing pulses from which the SMC synchronizing pulses are displaced by the different offset time taken by the submaster controller 3 and applies these LC synchronizing pulses to the local controllers 6 – 8. Thus, the local controllers 4 and 5 in the first subdistrict and the local controllers 6 – 8 in the second subdistrict are controlled not by the same synchronizing pulses but by the synchronizing pulses displaced from the SMC synchronizing pulses to different degrees, so that the traffic signals in the first and second subdistricts are coordinately controlled.

FIG. 2 shows the details of the arrangement of each submaster controller of FIG. 1. The master controller applies cycle pulses of different frequencies to three terminals C1, C2 and C3. In the following pages, the line or terminal and the signal thereon will sometimes be referred to by the same reference numeral. The signal C1 has a frequency of 100 pulses per signal cycle; the signal C2, a lower frequency of 100 pulses per 1.25 signal cycle; and the signal C3, a higher frequency of 100 pulses per 0.875 signal cycle. The signals C1, C2 and C3 are applied as one input to AND elements 11, 12 and 13, respectively. A tri-stable circuit 25 applies its three outputs B1, B2 and B3 as the other input to the AND elements 11, 12 and 13, respectively, as will be described in detail later.

The output pulses from the AND elements 11 – 13 are applied through an OR element 14 to a pulse counter 15. The counter is so designed that whenever it has counted the 100th pulse applied thereto, it is returned to zero and at the same time produces an output on a line S00; and that when four, 50 and 90 pulses have been counted, it produces an output on lines S04, S50 and S90, respectively. In other words, as the counter 15 steps forward, it produces an output on the lines S00, S04, S50 and S90 upon lapse of times equal to 0 percent, 4 percent, 50 percent and 90 percent of one signal cycle length, respectively. These output signals are used as the LC synchronizing signals to be applied to the local controllers belonging to the submaster controller.

The SMC offset signal provided by the master controller is applied to a terminal S0 in the form of binary decimal code.

The coded signal S0 is stored in a 7-bit register 16 which is capable of storing decimal numbers up to 100. The previously mentioned counter 15 is of a construction similar to the register 16 and has seven output lines. The outputs corresponding to the 7 bits of the register 16 are applied to a coincidence circuit 17, to which the seven outputs from the counter 15 are also applied. The circuit 17 compares the value stored in the register 16 and the counted value on the counter 15 and produces an output on a line OS when the two values coincide. This signal OS is applied as one input to four AND elements 21 to 24.

The master controller also applies the SMC synchronizing pulses to terminals M00, M04, M50 and M90. The signal M00 is a pulse produced upon lapse of every one signal cycle, and the signals M04, M50 and M90 are pulses produced upon lapse of 4 percent, 50 percent and 90 percent of every one signal cycle, respectively, after the production of the signal M00. These signals M00 – M90 are shown in FIG. 3 (*a*) – (*e*), respectively.

The signal M04 is applied as a set input to a flip-flop 18, to which the signal M90 is applied as a reset input. Therefore, the flip-flop 18 is kept set during the period of time from 4 percent to 90 percent of one signal cycle length. The set and reset outputs from the flip-flop 18 are shown in FIG. 3 (*f*) and (*g*), respectively. The signal M50 is applied as a set input to a flip-flop 19, to which the signal M00 is applied as a reset input. Therefore, the flip-flop 19 is kept set during the period of time from 50 percent to 100 percent of one signal cycle. The set and reset outputs from the flip-flop 19 are shown in FIG. 3 (*h*) and (*i*), respectively.

The set output from the flip-flop 18 is applied as a second input to the AND element 21, to which the set output from the flip-flop 19 is applied as the third input. Therefore, as shown in FIG. 3 (*j*), the AND element 21 produces an output only when the signal 0S is produced by the coincidence circuit 17 during the period of time from 50 percent to 90 percent of one signal cycle length. In the following description, expressions such as "the period of time from 50 percent to 90 percent of one signal cycle length" will be expressed simply as "the 50 – 90 percent period of time." The reset output from the flip-flop 18 is applied as the other input to the AND element 22. Therefore, as seen from FIG. 3 (*k*) the element 22 produces an output only when the signal 0S is produced during the 90 – 100 percent period of time, or the 0 – 4 percent period of time of one signal cycle. The set output from the flip-flop 18 is applied as a second input to the AND element 23, to which the reset output from the flip-flop 19 is applied as the third input. Therefore, as seen from FIG. 3 (*l*) the AND element 23 produces an output only when the signal 0S is produced during the 4 – 50 percent period of time of one signal cycle. Finally, the reset output the flip-flop 18 is applied as a second input to the AND element 24, to which the set output from the flip-flop 19 is applied as the third input. Therefore, as seen from FIG. 3 (*m*) the AND element 24 produces an output only when the signal 0S is produced during the 90 – 100 percent period of time of one signal cycle.

The outputs from the AND elements 21 – 23 are applied as three inputs to the tri-stable circuit 25. When the output from the AND element 21 is applied as an input F to the circuit 25, it produces an output on a line B1; when the output from the AND element 22 is applied as an input S to the circuit 25, it produces an output on a line B2; and when the output from the AND element 23 is applied as an input T to the circuit 25, it produces an output on a line B3. Let it be assumed that in FIG. 2 the input S is applied to the circuit 25, which produces an output on the line B2.

The output ST from the AND element 24 is applied as one input to the OR element 14. Therefore, so long as the output ST continues to be applied through the OR element 14 to the counter 15, the counter 15 does not step forward even when any of the AND elements 11 – 13 applies pulses to the counter 15.

Suppose that on the basis of the traffic informations received from the detectors 9 and 10, the master controller has decided that is necessary to change the offsets in the subdistricts, and accordingly applies the signal SO expressing a new offset to the register 16 of the submaster controller 2 or 3 to be stored therein. At this time the counter 15 is stepping forward due to the normal cycle pulses C2 applied thereto through the AND element 12 and the OR element 14. When the counter 15 has reached the count which coincides with the new offset value stored in the register 16, the coincidence circuit 17 produces an output on the line OS, as previously mentioned. Naturally, the synchronizing relation between the signal OS and the SMC synchronizing pulses being applied to the terminals M04, M50, M90 and M00 now becomes different from that before the new offset has been stored in the register 16.

Suppose that the signal OS has been produced during the 50 – 90 percent period of time of the signal cycle. The moment the signal OS has been produced, the AND element 21 produces an output to be applied as the input F to the tri-stable circuit 25, so that the output B1 is produced to be applied to the AND element 11. Then, the counter 15 begins to count the cycle pulses applied thereto through the terminal C1. Since the frequency of these pulses C1 is lower by 12.5 percent than that of the standard cycle pulses C2, the time required for the counter 15 to count 100 pulses applied through the terminal C1 becomes 12.5 percent longer than the time required for the counter to count 100 pulses applied through the terminal C2. In other words, one signal cycle length has now become 12.5 percent longer than the normal signal cycle length. It will be easily seen that as this lengthened signal cycle is repeated three or four times at most, the signal OS comes to appear within the 90 – 100 percent or 0 – 4 percent period of time of the normal signal cycle length as defined by the SMC synchronizing pulses applied to the terminals M00 – M90.

In case the signal OS has appeared within the 90 – 100 percent period of time, the AND element 24 produces an output on the line ST to be applied through the OR element 14 to the counter 15. So long as this signal ST is being applied to the counter 15, it does not progress. During the 90 – 100 percent period of time, the AND element 22 produces an output so that the output B2 from the circuit 25 is applied to the AND element 12. This causes the pulses C2 to be applied through the AND element 12 and the OR element 14 to the counter 15. However, the continuous application of the signal ST to the counter 15 prevents the pulses C2 from progressing the counter 15. When the 90 – 100 percent period of time has elapsed, however, the signal M00 causes the signal ST to disappear, whereupon the counter 15 begins counting the cycle pulses C2. Since 100 pulses C2 are produced for every one normal cycle length, the counter 15 is returned to zero count upon lapse of every one normal cycle. Thus, the discrepancy between the SMC synchronizing pulse M00 and the LC synchronizing pulse S00 becomes equal to the new offset as stored in the register 16. From this time on the counter 15 produces LC synchronizing pulses on the basis of the new offset until the offset is again changed.

In case the signal ST has appeared within the 0 – 4 percent period of time, the AND element 22 produces an output on the line B2, whereupon the counter 15 begins counting pulses C2.

Suppose that the signal OS from the coincidence circuit 17 is produced within the 4 – 50 percent period of time of the signal cycle. Then, the AND element 23 produces an output to be applied to the input T of the tri-stable circuit 25, so that the circuit 25 produces an output on the line B3 to be applied to the AND element 13. This causes the counter 15 to count the cycle pulses C3 applied thereto through the OR element 14. Since the frequency of the pulses C3 is higher by 12.5 percent than that of the normal pulses C2, the time required for the counter 15 to count 100 pulses C3 becomes shorter by 12.5 percent than the normal signal cycle length. Therefore, while

the shortened signal cycle is repeated three times at most, the signal OS comes to appear within the 0 – 4 percent period of time of the signal cycle as defined by the SMC synchronizing pulses, or while the shortened signal cycle is repeated four times at most, the signal OS comes to appear within the 90 – 100 percent period of time of the normal signal cycle. Then the output S00 from the counter 15 is forwardly displaced from the signal M00 by the new offset as stored in the register 16. In other words, the counter 15 now produces LC synchronizing signals on the basis of the new offset.

The LC synchronizing signals, that is, S00, S04, S50 and S90 are transmitted to the local controllers belonging to the submaster controller. The submaster controller determines an offset for each of the local controllers. On the basis of the offset and the LC synchronizing signals received from the submaster controller, each local controller provides its own synchronizing signals to control the traffic signals belonging to it in a manner so well known in the art that no explanation thereof will be given.

FIG. 4 shows a modified form of the submaster controller shown in FIG. 2. Here, the register 16 and the coincidence circuit 17 in FIG. 2 are replaced by a circuit including a reversible register. In FIG. 4 the component parts corresponding to those in FIG. 2 are designated by the same reference numerals, and the following description will be limited to those portions which differ from the arrangement of FIG. 2.

The master controller applies an offset signal to a terminal SO. As in the case of FIG. 2, the signal SO is in the form of binary decimal code. Simultaneously with the application of the signal SO, the master controller also applies another signal to a terminal SOC. This signal SOC is a continuous signal unlike the signal SO. The two signals SO and SOC are applied to an AND element 32, so that the signal SO is applied through an OR element 34 to a reversible register 35 having a capacity of storing decimal numbers up to 100. Thus, the new offset value transmitted as the signal SO from the master controller is stored in the register 35. The register 35 is capable of storing the signal SO only while the signal SOC is being applied thereto as a continuous input through a line SRC. If the pulses from the OR element 34 are applied to the register 35 without the control input SRC, the register 35 subtracts a value corresponding to the pulses applied from the OR element 34 (which will be referred to as "subtraction pulses") from the value stored in the register 35 until the stored value is reduced to zero, whereupon the register 35 produces a signal on a line OS. After that time, if the OR element 34 further applies subtraction pulses to the register 35, the register 35 subtracts the applied subtraction pulses from 100.

The output signal OS from the register 35 is applied as one input to the AND elements 21 – 24 just as in the case of FIG. 2. The subtraction pulses applied to the register 35 are the pulses applied thereto from the OR element 14 through an AND element 33 and the OR element 34. A flip-flop 31 applies its reset output to one input of the AND element 33. The previously mentioned signal SOC is applied as a set input to the flip-flop 31, to which the output SOO from the counter 15 is applied as a reset input. Therefore, so long as the signal SOC exists, the AND element 33 produces no output, and when the signal SOO has appeared, the register 35 receives subtraction pulses to be subtracted from the value stored in the register 35. Thus, when after the production of the signal SOO, the new offset value stored in the register 35 has been reduced to zero, that is, when the new offset time as selected by the master controller has passed, the signal OS is produced. The operation of the embodiment of FIG. 4 will be so easily understood from the previous explanation of FIG. 2 that no further description will be required.

What we claim is:

1. A system for controlling the traffic signals within a wide district divided into a plurality of subdistricts, comprising: a plurality of local controllers to control the traffic signals provided at different places in each of said subdistricts, a submaster controller provided for each of said subdistricts for controlling said local controllers within each said subdistrict; and a single master controller for controlling said submaster controllers and including means for providing cycle pulses and a first series of synchronizing pulses to be applied to all said submaster controllers and means for providing a different offset signal to be applied to each of said submaster controllers; each said submaster controller including means for providing a second series of synchronizing pulses displaced from said first-mentioned series of synchronizing pulses by the offset time as determined by said offset signal, and means for applying said second series of synchronizing pulses to each said local controller, whereby each said local controller controls the traffic signals belonging thereto on the basis of said second series of synchronizing pulses received from each said submaster controller.

2. The system of claim 1, wherein each said submaster controller includes a register for storing said offset signal received from said master controller, a counter for counting said cycle pulses received from said master controller to produce said second series of synchronizing pulses as predetermined counts are reached, and circuit means for controlling said counter so that the time between the occurrence of said first and second series of synchronizing pulses becomes equal to said offset stored in said register.

3. The system of claim 1, wherein said submaster controller comprises a register for storing said offset signal, a counter for counting said cycle pulses to produce said second series of synchronizing pulses as predetermined counts are reached, a coincidence circuit operable to produce an output when the count on said counter has come to coincide with said offset stored in said register, means for detecting a discrepancy in occurrence between said output from said coincidence circuit and a first pulse in said first series of synchronizing pulses to produce an output, and means operable in response to said output from said detecting means to change the frequency of said cycle pulses to be applied to said counter.

4. The system of claim 1, wherein each said submaster controller comprises a first counter for counting said cycle pulses, a register for storing said offset signal, said register also receiving said cycle pulses to function as a second counter having the same counting capacity as said first counter to produce a signal when a predetermined count has been reached, means for detecting a discrepancy in occurrence between said signal from said second counter and a first pulse in said first series of synchronizing pulses to produce an output, and means operable in response to said last-mentioned output to change the frequency of said cycle pulses to be applied to said first counter.

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