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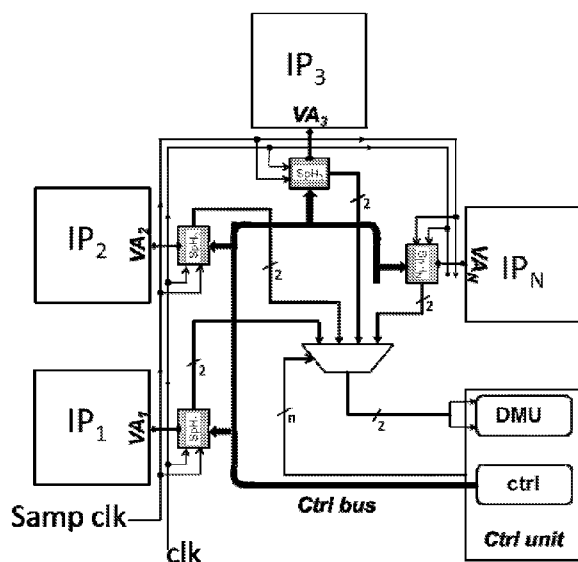


Figure 1a

(57) Abstract: Embodiments of the disclosure relate to a method and system for Built-in-Self- Test of analog signals with minimal area overhead, for measuring on-chip voltages in an all-digital manner. The method is well suited for a distributed architecture, where the routing of analog signals over long paths is minimized. A clock is routed serially to the sampling heads placed at the nodes of analog test voltages. This sampling head, present at each test node, which consists of a pair of delay cells and a pair of flip-flops, locally converts the test voltage to a skew between a pair of sub-sampled signals, thus giving rise to as many sub-sampled signal pairs as the number of nodes. To measure a certain analog voltage, the corresponding sub-sampled signal pair is fed to a Delay Measurement Unit (DMU) to measure the skew between this pair.



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SYSTEM AND METHOD FOR BUILT-IN SELF TEST (BIST) IN AN INTEGRATED CIRCUIT

TECHNICAL FIELD

Embodiments of the present disclosure relates to Built-in Self Test (BIST) in integrated circuits. More particularly, the embodiments relate to Built-in Self Test (BIST) of analog signals for measuring on-chip voltages.

BACKGROUND

Presently, bias variation is a common problem in analog circuits and is getting worse as the technology scales. The process variation is increasing and power supply is reducing which is causing this problem. With the increasing popularity of mixed signal integrated circuits (IC) designs in the deep sub-micron processes, it is required precisely measure analog voltages for test and debugging purposes. Such situations arise when measuring on-chip voltages for built-in-self-test (BIST) applications, voltages at the terminals of sleep transistors for power monitor applications and in measuring low bandwidth signals in sensor systems. These analog voltages could be potentially located all over the chip. It is desirable that the measurement circuitry employed in such situations occupies as less area as possible and be simple to design.

There exist few techniques of displaying analog signal waveforms using sub-sampling. These methods are well-suited for viewing waveforms in a laboratory but cannot be used directly for automated testing. An existing architecture of an Analog/RF BIST subsystem describes the maximum area permissible for the BIST subsystem for the total manufacturing and testing cost reduction. In those architectures, the DC voltages (of BIST sensors) of test nodes are all tied together to a common bus and digitized centrally through a 12-bit ADC. Even AC signals are converted to DC through an envelope detector circuit, but calibration is required in this case to map the digitized values to analog amplitudes. In such a case, one has to know the number of sensor nodes in advance or design for a worst-case scenario to ensure that the value on the bus settles within a specified time. Also, for the AC case, calibration puts a lower bound on the testing time required. It would be beneficial to have an approach where the design of driver for the bus can be made independent of the number of test nodes, and also eliminate the need for calibration in testing AC signals, which would reduce the time required for testing.

Techniques of analog routing, wherein voltages and/or currents to be measured in some internal circuitry are literally “scanned” out to test pins, but analog circuits are used to route analog voltages/currents, which can themselves lead to signal distortion while propagation. It is hence desirable to have testing circuitry which is simpler than those being tested.

Another existing technique is analog routing with digital interface, where an analog voltage is digitized and the bits are scanned out through a single pin. Similarly, one can also scan in digital bits and excite circuits with analog voltages using a DAC. But with reducing power supply voltages in the deep sub micron technology nodes, leading to reduction of available voltage headroom, designing conventional ADC architectures for such applications is becoming increasingly difficult. However, in the case of time based architectures, time resolution has improved since the transition time of digital signals has reduced with technology scaling. The all-digital nature of time-based approaches offers itself for scaling and suits stringent area and power specifications.

Recent techniques are focused on designing ADCs based on the methodology of time based architectures. The two main parts of such solutions are (a) ‘transducer’ to convert voltages into time pulses or delays, and (b) to measure time/delays. One way of implementing the transducer is to transform the input and reference voltages into time pulses, and measuring their duration was shown to yield a 9.4 ENOB SAR ADC. An extension of this technique is used to demonstrate a 10-bit ADC, working at a low supply voltage of 0.6 V, whereas conventional ADC architectures can go up to only 9 bits of resolution for a comparator noise of standard deviation of half LSB. But both these techniques do not yield themselves well for a distributed type of measurement as desired here.

Another technique uses voltage-to-time-to-digital and voltage-to-delay-to-digital architectures providing 4 bit resolution with power consumption of less than 2.4 mW. By implementing moving average filtering, a resolution of 12 μ V per LSB at a sampling rate of 10 kHz is achieved. This technique uses the delay of an inverter as LSB and their linearity is therefore limited by the matching between inverter elements.

Another digital approach which is gaining popularity is the VCO based approach. In this approach, the voltage to be quantized controls the frequency of the VCO, and the count of edges of the VCO output in a certain measurement time is the quantization of the analog voltage. Also, a sigma-delta ADC with the VCO as the quantizer is used to overcome the non-linearity of the voltage to frequency transfer curve. The voltage to be measured is tied to the control voltage of VCO, and as many VCOs are needed as test nodes. However, to reduce area overhead, the number of stages in the VCO needs to be small which increases its operating frequency and hence power.

In another existing technique, a ring oscillator ADC is implemented where a differential transistor pair drives two identical ring oscillators as a matched load. The voltage difference is digitized by the difference between the counters which capture the frequencies of the two oscillators. They report a bin size of 16 mV with 80 mV range and consuming a current of 37 μ A. However, while implementing two ring oscillators, there is a possibility of injection locking and adequate care has to be taken to avoid it.

For the task of measuring analog voltages distributed all over the chip, the techniques described above require the analog signals themselves to be routed to the measuring unit. The implementation of these techniques is costly as the analog signals will have to be shielded, which can take up considerable area.

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SUMMARY

The shortcomings of the prior art are overcome and additional advantages are provided through the provision of methods and systems of the present disclosure.

The present disclosure solves limitations of existing techniques by providing a built-in-self-test (BIST) at each node in an integrated circuit.

Additional features and advantages are realized through various techniques provided in the present disclosure. Other embodiments and aspects of the disclosure are described in detail herein and are considered as part of the claimed disclosure.

In one embodiment, the disclosure provides a system configured for built-in-self-test (BIST) at each node in an integrated circuit. The system comprises one or more nodes in the integrated circuit. The test voltage of each node is measured using BIST. Also, the system comprises one or more sampling head blocks to convert the test voltage at a node into time delay, wherein each sampling head is connected to each node. The system further comprises a control unit to control the operation of the one or more sampling head to perform the BIST corresponding to each node. Further, the system includes a delay measurement unit (DMU) to receive low-frequency signals from each sampling head block to calculate the time delay and thereby, the test voltage at each node by using interpolation on pre-computed calibration data.

In another embodiment, the disclosure provides a method to perform built-in self test (BIST) at each node of an integrated circuit. The method comprises the acts of converting test voltage of a predefined node of the integrated circuit and a reference voltage corresponding to said predefined node into time delay between a pair of low-frequency

signals by sub-sampling technique. The sub-sampling technique is performed using a sampling head. Next step of the method is calculating time delay corresponding to the difference between test voltage and the reference voltage to obtain a code word. Further, the method includes converting the code word into an analog value to obtain a differential voltage. The differential voltage is the difference between node voltage and reference voltage. Further, all the above steps are repeated for each node in the integrated circuit to perform BIST.

The foregoing summary is illustrative only and is not intended to be in any way limiting. In addition to the illustrative aspects, embodiments, and features described above, further aspects, embodiments, and features will become apparent by reference to the drawings and the following detailed description.

BRIEF DESCRIPTION OF THE ACCOMPANYING DRAWINGS

The novel features and characteristic of the disclosure are set forth in the appended claims. The embodiments of the disclosure itself, however, as well as a preferred mode of use, further objectives and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings. One or more embodiments are now described, by way of example only, with reference to the accompanying drawings wherein like reference numerals represent like elements and in which:

Fig. 1a is an exemplary block diagram of analog BIST, in accordance with one embodiment.

Fig. 1b is a block diagram showing blocks of sampling head (SpH), in accordance with one embodiment.

Fig. 2 shows a schematic circuit of current-starved voltage to delay cell (V2D), in accordance with one embodiment.

Fig. 3 shows a block diagram representation of analog BIST in an integrated circuit along with delay measurement unit (DMU), in accordance with an alternate embodiment.

Fig. 4 shows a timing diagram and sub-sampling in analog BIST, in accordance with one embodiment.

Fig. 5 shows a Behavioral model of voltage quantization employing the DMU, in accordance with one embodiment.

Fig. 6 shows a plot of OSR versus n , showing the existence of optimal OSR for a given f_{in} , in accordance with one embodiment.

Fig. 7 shows a plot of ‘offset-canceled’ differential delay versus differential voltage, in accordance with one embodiment.

Fig. 8 shows DNL and INL plots for the setting of entry 8 in Table 2, in accordance with one embodiment.

The figures depict embodiments of the disclosure for purposes of illustration only. One skilled in the art will readily recognize from the following description that alternative embodiments of the structures and methods illustrated herein may be employed without departing from the principles of the disclosure described herein.

DETAILED DESCRIPTION

The foregoing has broadly outlined the features and technical advantages of the present disclosure in order that the detailed description of the disclosure that follows may be better understood. Additional features and advantages of the disclosure will be described herein after which form the subject of the claims of the disclosure. It should be appreciated by those skilled in the art that the conception and specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present disclosure. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the disclosure as set forth in the appended claims. The novel features which are believed to be characteristic of the disclosure, both as to its organization and method of operation, together with further objects and advantages will be better understood from the following description when considered in connection with the accompanying figures. It is to be expressly understood, however, that each of the figures is provided for the purpose of illustration and description only and is not intended as a definition of the limits of the present disclosure.

Exemplary embodiments of the present disclosure provide system for performing a built-in-self-test (BIST) at each node in an integrated circuit. The system comprises one or more nodes in the integrated circuit. The test voltage of each node is measured using

BIST. Also, the system comprises one or more sampling head blocks to convert the test voltage at a node into time delay, wherein each sampling head is connected to each node. The system further comprises a control unit to control the operation of the one or more sampling head to perform the BIST corresponding to each node. Further, the system includes a delay measurement unit (DMU) to receive low-frequency signals from each sampling head block to calculate the time delay and thereby, the test voltage at each node by using interpolation on pre-computed calibration data.

In one embodiment the disclosure provides a method to perform built-in self test (BIST) at each node of an integrated circuit. The method comprises the acts of converting test voltage of a predefined node of the integrated circuit and a reference voltage corresponding to said predefined node into time delay between a pair of low-frequency signals by sub-sampling technique. The sub-sampling technique is performed using a sampling head. Next step of the method is calculating time delay corresponding to the difference between test voltage and the reference voltage to obtain a code word. Further, the method includes converting the code word into an analog value to obtain a differential voltage. The differential voltage is the difference between node voltage and reference voltage. Further, all the above steps are repeated for each node in the integrated circuit to perform BIST.

In one embodiment of the present disclosure, a small part of the measuring unit called sampling head (SpH) is placed at the measurement node, avoiding the routing of analog signals over long paths, as shown in fig. 1a. The sampling heads are placed at each node in integrated circuit in order to minimize the routing of analog signals routed over long paths. Each sampling head consists of a pair of identical delay cells (V2D) and a pair of flip-flops (DFF), as shown in fig. 1b. A clock signal is routed serially to all the sampling heads, which is fed to both the delay cells in the sampling head. The delay of one element of the pair is controlled by the analog voltage V_{Ai} , and that of the other by a reference voltage V_{ref} . Thus, a voltage difference between the node voltage and reference shows up as a delay difference in the clocks at the output of the delay cell pair. The pair of clocks is sampled by a slightly slower sampling clock, giving rise to a pair of beat frequency signals. The sub-sampled signals and the skew between them are amplified by the process of sub-sampling. Hence, there will be as many pairs of sub-sampled signals as there are test nodes. To measure a certain test node, the corresponding sub-sampled signal

pair has to be fed to the DMU with appropriate select signal to the multiplexer. Also, the design of a sampling head does not depend upon the number of test nodes desired, giving the advantage of scalability with respect to number of test nodes.

Fig. 1 shows both the input clock (clk) and sampling clock (samp clk) which are from a single point for each sampling head. Thus, cross-talk and coupling noise which may affect the clocks do not contribute to additional noise in the sampling head circuitry. Also, the output sub-sampled signal pair of the sampling head are low-frequency signals and the skew between them is already amplified by the 'sub-sampling' process, which makes the sub-sampled signal pair also immune to cross-talk and coupling noise. Also as shown in the fig. 1, reference voltage V_{ref} need not be the same for all the nodes.

One embodiment of the present disclosure is about measurement procedure. The delay cells of the system are non-linear and they need to be calibrated apriori. The delay cell pair, i , corresponding to VA_i is calibrated as follows: The multiplexer (MUXcal) as shown in the Fig. 1b is set high so that the calibration voltage is fed, instead of the local node voltage, to each of the delay cell pairs. The select signal $MUXsel_i$ of the multiplexer is set to 1 to provide this voltage to one of the delay cells in pair i . The other cell gets the reference voltage. The settling time of V_{cal} sets a bottleneck on the testing time in this mode.

As an example in one embodiment, let g_{i1} and g_{i2} are the voltage to delay functions of the two delay cells respectively, then the delay difference out of this cell pair, ΔD_i is given by

$$\Delta D_i = g_{i1}(V_{cal}) - g_{i2}(V_{ref})$$

Let, a function $f_i(\cdot)$ mapping ΔV_i to ΔD_i defined as

$$\Delta D_i = f_i(V_{cal} - V_{ref}) = f_i(\Delta V_i) \quad (1)$$

The calibration step measures the function $f(\cdot)$ at few points, which is used later to correct for non-linearity and bias. Calibration helps in mitigating mismatches, if any, between the delay cell pairs. The delay at the input of the delay measurement unit (DMU) is given as:

$$\Delta D_{DMU} = \Delta D_i + \Delta D_{residual} \quad (2)$$

wherein $\Delta D_{residual}$ is the delay difference in the clock pair, accrued in the rest of the path. The delay difference will be independent of the voltage at node i and hence can be easily calibrated out.

During the measurement process, the multiplexer (MUXcal) is set low. To measure VA_i , the corresponding sub-sampled signal pair is selected by the multiplexor. Thus, the delay cell pair i will create a delay differential given as :

$$\Delta D_i = g_{i1}(VA_i) - g_{i2}(V_{ref}) \quad (3)$$

$$:= f_i(VA_i - V_{ref}) \quad (4)$$

The input delay difference at the DMU is as shown in the expression 2. From the calibration data, VA_i can be inferred directly or by interpolation. The input delay difference at the DMU as shown in expression 2, from the calibration data VA_i can be inferred directly or by interpolation.

Fig. 2 shows a schematic circuit of current-starved Voltage to Delay cell (V2D). The target measurement range for BIST in an integrated circuit is 0 to 100 mV. Hence, PMOS controlled current starved inverters is used as shown in Fig. 2. However, alternative delay cell architectures may be used for other applications as the specifications desire. The area of the pair of delay cells chosen for this application and taped out is $8.2 \mu\text{m} \times 8.4 \mu\text{m}$ in about 130nm UMC CMOS process, in one embodiment.

As shown in the fig. 2, the voltage influences only the delay of the rising edge, while the delay of the falling edge is uncontrolled. Hence, input clock period of T and duty ratio D provides the range of the system, i.e. the value of V_{in} which gives an absolute delay of D_r , wherein $D_r = D \times T$, the maximum rising edge delay possible. As an example for a clock period of 125 ns, duty ratio of 0.5, let 120 mV provides a delay of 62.5 ns, then the range of the system is 120 mV.

One embodiment of the present disclosure provides design considerations of the system. The sizing of the delay cell circuitry is critical, so the capacitance between the analog voltage and the input clock is about 2 fF. With a decoupling capacitor of 4 pF, the kickback will be less than 0.6 mV. For smaller kickback, either the decoupling capacitor

has to be increased or cascoding has to be implemented. With a transistor of gain 20 in cascode, the decoupling capacitor can be as less as 0.1 pF.

The delay of every cell is sensitive to supply voltage, variations in supply voltage directly impacts the voltage measurement. The power supply will have a distribution profile across the chip. This profile will get calibrated out provided the power supply does not change too much with time. To combat time varying supply voltage, delay cells are used with a good power supply rejection ratio or to use regulated power supply. Placing a transistor in cascade helps to mitigate the effect of power supply noise on delay.

The measurement of bias voltages is dependent on V_{cal} for the calibration and interpolation. Hence, the generation of V_{cal} have to be accurate and has to be shielded well so that noise coupled onto V_{cal} will not impact the measurement. The noisy currents of the voltage-to-delay converter contribute to jitter on the clocks. If N delay cells are used in cascade to generate the delay difference, assuming the jitter added by each to be independent of one another, the jitter grows as $\sqrt{N}$, while the total delay grows as N . Hence, from a noise perspective, it is advantageous to employ more delay stages. But this leads to bandwidth limitation and increased kick-back to the analog test node.

In one embodiment for a given measurement time, the resolution of measurement of delay difference that can be obtained be 6σ (where σ is the standard deviation of the measured delay values). Then, the required voltage-to-delay ratio is calculated based on the desired voltage resolution. Based on the total delay required, one can choose the number of delay stages needed.

For example, suppose that a resolution of 10 ps can be achieved in a given measurement time and the voltage resolution desired is 1 mV. Then the voltage-to-delay converter has to provide a differential delay of 10 ps/mV. Suppose a single delay cell is designed to provide this delay and If 0.1 mV resolution is desired with the available system architecture and measurement time, then ten such delay cells can be used.

Fig. 3 shows the block diagram of the system implemented to evaluate the concept. The system comprises of voltage-to-delay circuitry, an on-chip sampling head and a DMU. The system is used to measure a single analog voltage, shown as the pin named ' V_{in} '. It is used first for calibration (by feeding known voltages) and then to measure test

voltages. There is a provision to select the output of either of a single or a series of 13 voltage-to-delay cells, giving a handle on the voltage-to-delay transfer.

In one embodiment of the system, a sub-sampling based delay measurement unit (DMU) is used. The V2D cells set up a delay between the clocks at nodes Da_i and Db_i , which has to be measured. Since the objective is to measure delay digitally, the clock pair is sampled by another clock. To perform sampling, a sampling clock with a frequency which is much larger (about $100\times$) that of the clock pair can be used. But, practical measurements show that the standard deviation of the measured delay, and therefore of voltage is too high. The system here uses a sampling frequency which is slightly less or slightly more than that of the clock pair which is known as sub-sampling.

The sampling rate is about 2 times lesser than Nyquist frequency, which means that the full signal cannot be reconstructed back. But, if the parameter of interest can be made periodic with a known frequency, then this technique can still be used to reconstruct the parameter of interest. For example, an on-chip analog oscilloscope where a high frequency periodic analog signal is sub-sampled and the samples are digitized. The sampling clock has a frequency which is slightly less than that of the input signal to be displayed, so that the original signal becomes time expanded, thereby significantly reduces the required bandwidth of the ADC that follows.

As shown in Fig. 3, if the frequencies of sampling clock and core clock pair are rationally related that happens when one of them is derived from the other, then the resolution of measurement is lower bounded by a non-zero quantity, determined by the parameters T and ΔT . This means that, in spite of increasing the measurement time, the accuracy (standard deviation) of measurement does not improve beyond a certain value. In such cases, adding some additional jitter onto the clocks, by way of frequency modulation for instance, improves the resolution.

Further, when the frequencies of sampling and core clock pair are irrationally related, there is no such fundamental limit on resolution. But, it comes with the rider that this sampling clock has to be generated from a separate crystal. For this particular application, the tester can be made to feed this second clock signal. In this setup, the jitter of the clocks comes in as a hindrance and is mitigated by averaging.

Fig. 4 illustrates of timing diagram and the concept of Sub-sampling. As shown, the input clock pair Da_i and Db_i (of period T) is sampled by an asynchronous sampling clock of period $T+\Delta T$. As a result, the two outputs will be beat clocks with period given as $T_b = (T+\Delta T) \times T/\Delta T$. The period of ideal Qa and Qb is as shown in Fig. 4. Here, there is time amplification by a factor $T/\Delta T$. Hence, the skew δ between these two clocks which has to be measured will also be amplified by the same amount $Tsk = [(T+\Delta T) \times \delta/\Delta T]$, shown as skew between ideal Qa and ideal Qb . Due to jitter on the clocks and meta-stability issues of the samplers, the sampled outputs will be bouncy as shown in the waveforms for Qa and Qb . Hence, the skew has to be estimated by averaging the delay difference between the two rising edges of Qa and Qb across many instances. Since Qa and Qb are synchronous to sampling clock, their delay difference will always be some multiple of sampling clock period and hence a simple up/down counter suffices to estimate this difference. Further, the same counter can be used for averaging across multiple periods of Qa and Qb . Such an averaging yields an unbiased estimate of the skew as a fraction of the clock period T [20]. The falling edge related bounces is ignored and hence the clean clocks CQa and CQb are generated which are fed to the up/down counter as shown in Fig. 4.

In one embodiment of the present disclosure, the system uses needs two clocks i.e. a core clock and a sampling clock, of slightly different frequencies. Generation and routing of such close frequency clocks is obtained using a pair of signal generators independently. In a real-world BIST scenario, one of the clocks can be provided while the other can be generated on-chip. A sub-harmonic of the sampling clock does practically no change to this system of sub-sampling and hence eliminates the issue of injection-locking.

Fig. 5 shows the behavioral model of voltage quantization employing the DMU. Let T and $T+\Delta T$ be the time periods of core clock and sampling clock respectively. Then, the duration of the beat period is given by $T_b = (T+\Delta T) \times T/\Delta T$, which will consist of $T/\Delta T$ sampling clock periods. Hence, the resolution of the quantizer in measuring time, in principle, is $\Delta T/T$. Therefore, the maximum number of bits of this quantizer, b_{max} and conversion time T_b are given by:

$$b_{max} = \log_2\left(\frac{T}{\Delta T}\right)$$

$$T_b = (T + \Delta T) \times T / \Delta T \quad (5)$$

If d_{max} is the maximum delay given by the voltage-to-delay converter corresponding to the maximum voltage input, then the number of bits b available is given by:

$$b = \log_2\left(\frac{d_{max}}{\Delta T}\right) = \log_2\left(c \frac{T}{\Delta T}\right) \quad (6)$$

where c is the maximum delay as a fraction of the time period T .

If the total measurement time is M beat periods, the variance reduces by a factor of M , and hence the SNR increases by about $3 \log_2(M)$ dB. Hence, doubling the measurement time improves the SNR by about 3 dB. The bandwidth of measurement is $1/2T_b$. Hence, clearly there is a bandwidth-accuracy trade-off in the choice of parameters T and ΔT . The overall SNR of the complete system for a sinusoidal input of amplitude V_{inmax} is given by:

$$SNR = 10 \log_{10}\left(\frac{A^2}{2} \cdot \frac{1}{12} \cdot c^2 \frac{(\Delta T)^2}{T^2} \cdot M\right) \quad (7)$$

where $A = kV_{inmax}$ with k being the voltage to delay gain i.e. assuming voltage to delay conversion being linear. Thereby, assumes that sample-and-hold circuitry is available which can hold the sampled values for a period of the measurement time (t_m), given by

$$t_m = M \cdot (T + \Delta T) \times T / \Delta T \quad (8)$$

In one embodiment, let f_c and f_s be the frequencies of the core and sampling clocks respectively. Then, the frequency of the beat signal is given by $f_b = f_c - f_s$. The above equations can now be re-written as:

$$\frac{T}{\Delta T} = \frac{f_s}{f_b} \quad (9)$$

$$\Delta T = \frac{f_b}{f_c f_s} \quad (10)$$

$$b = \log_2 \left(\frac{c f_s}{f_b} \right) \quad (11)$$

$$\text{Conversion rate} = f_b \quad (12)$$

In order to simplify the design in this case of distributed voltage measurement, the use of a sample-and-hold at the voltage nodes is avoided. Hence, this renders data conversion at Nyquist rate impossible, but the methodology of over-sample-and-average can be used. Basically, the sampling rate should be high enough so that the signal of interest does not change beyond an LSB within the conversion time. Assuming an input sinusoid $V_{in} = A \sin(2\pi f_{in} t)$, an LSB a and conversion rate f_b , the maximum change in V_{in} within an interval of $1/f_b$ should not exceed a , i.e.,

$$\frac{2\pi A f_{in}}{f_b} \leq a \quad (13)$$

Let $OSR = f_b / (2f_{in})$ and $2A/a = 2^{n_1}$ for n_1 effective bits of conversion. Then, OSR sets a limit on the number of effective bits (n_1) that can be obtained, as given by

$$n_1 \leq \log_2 \left(\frac{OSR}{\pi} \right) + 1 \quad (14)$$

A second limit on the number of effective bits (n_2) available is set by the number of bits available at each conversion, which reduces with increased oversampling. Using (11),

$$\begin{aligned} n_2 &\leq b + \frac{1}{2} \log_2 (OSR) \\ &\leq \log_2 \left(\frac{c f_s}{2 f_{in} \sqrt{OSR}} \right) \end{aligned} \quad (15)$$

The actual number of bits (n) that one can obtain is given by

$$n = \min(n_1, n_2) \quad (16)$$

Fig. 6 shows a plot indicating the existence of an optimal OSR along with the optimal OSR which reduces for a higher input bandwidth and also yields lesser number of effective bits.

In one embodiment, as an example, a set of 32 measurements are taken to compute the mean and standard deviation of the delay count for each V_{in} value. The error-bars obtained is as shown in Fig. 7 as plots, which represents a value of $\pm\sigma$ on each side of the mean. The accuracy of voltage measurement is defined as the range of voltage values corresponding to $\pm 3\sigma$. This is obtained by the dividing standard deviation of delay by the local slope at each point in Fig. 7.

Fig. 6 is the plot of OSR versus n , showing the existence of optimal OSR for a given f_{in} . The other parameters of the equations are taken from the settings described in Table 2. The dots indicate the results summarized in Table 2. The gap between the modeled and measured behavior is because the differential delay generated is a small fraction of the clock time period, and the resolution improves as the ratio of differential delay to time period increases. Table 1 shows a summary of measured results for DC input.

Table 1

Sl. No.	VDD (V)	f_c (MHz)	f_s (MHz)	MT (s)	DR (ns)	σ_{max} (ps)	Bin-size (mV)
1	0.75	8.0	7.6	4.42	6.77	32.1	1.50
2	1.2	10.0	9.8	3.42	1.53	10.1	2.05
3*	1.2	8.0	7.9	4.25	11.25	30.5	0.82
4	0.75	8.0	7.99	4.20	7.80	29.0	1.60
5	0.75	8.0	7.99	16.80	7.30	15.0	0.85
6†	1.0	37.0	36.927	0.056	2.97	9.77	2.10
7†	1.1	37.0	36.927	0.056	2.13	9.92	1.03
8†	1.2	37.0	36.927	0.88	1.20	3.87	1.25

wherein * is 13 V2D cells and † is measurement time strictly integer number of beat periods, f_c - Input Clock Frequency, f_s - Sampling Clock Frequency, MT - Measurement Time, DR - Dynamic Range of delay, σ_{max} - Maximum standard deviation of delay values, Bin-size - Accuracy of measurement

Fig. 8 shows plots of ‘offset-canceled’ differential delay versus differential voltage for the settings mentioned. Refer Table 1 for the settings of #1,2,3.

Table 2: Summary of Measured Results for Sine wave input

Sl.	f_{in}	f_c	f_s	OSR	SNR	ENOB
No.	(Hz)	(MHz)	(MHz)		(dB)	(bits)
1	30	37	36.999	16.67	9.61	1.30
2	30	37	36.9975	41.67	17.57	2.63
3*	30	37	36.995	41.67	17.37	2.59
4*	30	37	36.9925	62.50	19.54	2.95
5*	30	37	36.99	83.33	16.51	2.45
6*	30	37	36.98	166.67	9.01	1.20
7	10	37	36.999	50.0	17.76	2.63
8*	10	37	36.927	1825	33.61	5.29

wherein * is one measurement over two beat periods; f_{in} - Frequency of input sine wave, f_c - Core clock Frequency, f_s - Sampling Clock Frequency, OSR - Over-sampling Ratio, SNR - Signal to Noise Ratio, ENOB - Effective Number Of Bits.

Table 1 and Fig. 7 presents a summary of measured results, which shows that delay increases with reducing supply and increasing number of V2D cells. The delay versus voltage plots of Fig. 8 are for the settings presented in the rows 1, 2 and 3 of Table 1. An accuracy of about 1 mV can be obtained by proper choice of parameters and measurement time. One can easily obtain desired accuracies by suitably altering the measurement time. Except entry 3, other entries of Table 1 correspond to the single V2D case. Entries 4 and 5 show that the accuracy improves with measurement time. For a four-fold increase in measurement time, the accuracy improves by a factor of two, which goes well with the

theory. Entries 6 to 8 are taken for a measurement time strictly integer number of beat periods. The bin-size obtained in lesser duration is comparable to other entries acquired over a larger measurement time. The differences in the delay ranges for the similar settings are present because they were measured on different days and hence conditions like supply voltage and temperature could be different. However, the measurements taken with the same setting about couple of hours apart (after offset-cancellation) is stable enough.

In one embodiment, a sine wave of frequency 30 Hz is applied to the system directly without sample-and-hold circuitry. A set of 16,384 data points are collected for the SNR measurements. SNR measurements are determined without calibrating the data points. The summary of results obtained is shown in Table 2. It is observed that the SNR degrades for both low and high OSR in accordance with Fig. 6. Entries number 7 and 8 of the Table 2 confirms that the SNR is higher for a lower bandwidth signal with rest of the settings being similar. Fig. 8 shows the plot of DNL and INL for setting 8 of Table 2, obtained by code density test. The maximum values of DNL and INL are found to be less than 1 LSB.

The theoretical analysis shows that a resolution of 12 bits is possible in this approach, as shown in Fig. 6, but the measured results show a maximum of 5.29 bits. The limitation in the resolution is because the delay in this case is a small fraction of the time period of core clock. So, in order to get a better resolution, a core clock of higher frequency has to be used. But the poor rise time of the presently designed voltage-to-delay (V2D) converter limits the frequency of the clock that can be used.

Also, since the oversampling rate is closely related to the difference of the core and sampling clock frequencies, both these clock frequencies need to be accurately controlled. Entries 1 and 3 of Table 2 show that the SNR drops by about 8 dB for a change in the third decimal place of the sampling clock frequency. Hence, the use of this system necessitates precise control of the sampling clock frequency. This may be achieved by deriving this sampling clock from the core clock and mimicking asynchrony by artificially introducing frequency modulation. Also, a PLL may be used to precisely control the oversampling rate or beat frequency and accordingly adjust the sampling clock frequency.

The present disclosure is not to be limited in terms of the particular embodiments described in this application, which are intended as illustrations of various aspects. Many modifications and variations can be made without departing from its spirit and scope, as will be apparent to those skilled in the art. Functionally equivalent methods and apparatuses within the scope of the disclosure, in addition to those enumerated herein, will be apparent to those skilled in the art from the foregoing descriptions. Such modifications and variations are intended to fall within the scope of the appended claims. The present disclosure is to be limited only by the terms of the appended claims, along with the full scope of equivalents to which such claims are entitled. It is also to be understood that the terminology used herein is for the purpose of describing particular embodiments only, and is not intended to be limiting.

With respect to the use of substantially any plural and/or singular terms herein, those having skill in the art can translate from the plural to the singular and/or from the singular to the plural as is appropriate to the context and/or application. The various singular/plural permutations may be expressly set forth herein for sake of clarity.

In addition, where features or aspects of the disclosure are described in terms of Markush groups, those skilled in the art will recognize that the disclosure is also thereby described in terms of any individual member or subgroup of members of the Markush group.

While various aspects and embodiments have been disclosed herein, other aspects and embodiments will be apparent to those skilled in the art. The various aspects and embodiments disclosed herein are for purposes of illustration and are not intended to be limiting, with the true scope and spirit being indicated by the following claims.

We claim:

1. A system configured for built-in-self-test (BIST) at each node of an integrated circuit comprising:
 - one or more nodes in the integrated circuit, wherein a predefined test voltage of each node is measured using BIST;
 - one or more sampling head blocks to convert the predefined test voltage at a node into time delay, wherein one sampling head is connected to each node;
 - a control unit to control the operation of the sampling heads to perform the BIST corresponding to each node; and
 - a clock module comprising two clocks, called core and sampling clocks, of slightly different frequencies, where a predefined time delay is captured between the pair of core clock signals of predefined frequency, the pair of core clocks are sampled by sampling clock to digitize the time delay to produce sub-sampled signal pairs; and
 - delay measurement unit (DMU) to receive sub-sampled signals from each sampling head block to calculate the time delay and thereby, the test voltage at each node by using interpolation on pre-computed calibration data.
2. The system as claimed in claim 1, wherein the integrated circuit comprises sampling head blocks equal to number of nodes.
3. The system as claimed in claim 1, wherein the clock module comprises of two clocks, one clock carries the predetermined delay information and the other clock performs sampling operation to produce a pair of sub-sampled signals.
4. The system as claimed in claim 1, wherein the predetermined information is time delay information.
5. The system as claimed in claim 1, wherein each sampling head block comprises:
 - a pair of delay cells (V2D) which takes the test voltage of the corresponding node connected to the sampling head block as input, and correspondingly delays an input clock triggering said V2D; and
 - a pair of flip flops connected to the pair of delay cells, each flip flop has input from the corresponding delay cell, said delay flip flops are triggered using a sampling

clock to generate pair of sub-sampled signals, the delay between which carries information about the test voltage.

6. The system as claimed in claim 1, wherein the control unit supplies reference voltage, calibration voltage to each sampling head and selects one of either calibration or measurement phase via a control bus.
7. The system as claimed in claim 1, wherein the control unit determines the test node to be measured by selecting the corresponding sub-sampled output pair to be fed to the DMU using a multiplexer.
8. A method to perform built-in self test (BIST) at each node of an integrated circuit comprising:
 - converting test voltage of a predefined node of the integrated circuit and a reference voltage corresponding to said predefined node into time delay between a pair of low-frequency signals by sub-sampling technique, wherein said sub-sampling technique is performed using sampling head;
 - calculating said time delay corresponding to the difference between test voltage and the reference voltage to obtain a code word; and
 - converting the code word into an analog value to obtain a differential voltage, said differential voltage being the difference between node voltage and reference voltage;
 - repeating all above step for each node in the integrated circuit to perform BIST.

AMENDED CLAIMS
received by the International Bureau on 06 August 2013 (06.08.2013)

1. A system configured to perform built-in-self-test (BIST) at each node of an integrated circuit, said system comprising:
 - said integrated circuit comprising one or more nodes, wherein a predefined test voltage of each of the one or more nodes is measured using BIST;
 - one or more sampling head blocks to convert the predefined test voltage into a time delay, wherein the one or more sampling head blocks are in one to one connection with the one or more nodes;
 - a control unit to control operations of the one or more sampling heads to perform the BIST corresponding to each node; and
 - a clock module comprising two clocks, a core clock and a sampling clock, with different frequencies, wherein a predefined time delay is captured between a pair of core clock signals of predefined frequency, the pair of core clocks are sampled by the sampling clock to digitize time delay to produce sub-sampled signal pairs; and
 - delay measurement unit (DMU) to receive sub-sampled signals from each sampling head block to calculate the time delay and thereby, the test voltage at each node by using interpolation on pre-computed calibration data.
2. The system as claimed in claim 1, wherein the core clock carries predetermined delay information and the sampling clock performs sampling operation on the predetermined delay information to produce a pair of sub-sampled signals.
3. The system as claimed in claim 2, wherein the predetermined information is time delay information.
4. The system as claimed in claim 1, wherein each sampling head block comprises:
 - a pair of delay cells (V2D) to receive the test voltage of a node connected to the sampling head block as input, and correspondingly delays an input clock triggering said V2D; and
 - a pair of flip flops in one to one connection with the pair of delay cells (V2D), each of said pair of flip flops has input from the corresponding delay cell, said pair of flip flops are triggered using the sampling clock to generate pair of sub-sampled signals, the delay between the generated pair of sub-sampled signals provides information about the test voltage.

5. The system as claimed in claim 1, wherein the control unit supplies reference voltage, calibration voltage to each sampling head and selects one of either calibration or measurement phase using a control bus.
6. The system as claimed in claim 1, wherein the control unit determines the test node to be measured by selecting the corresponding sub-sampled output pair, which is fed to the DMU using a multiplexer.
7. A method of performing built-in self-test (BIST) at each node of an integrated circuit, said method comprising:
 - converting test voltage of a predefined node of the integrated circuit and a reference voltage corresponding to said predefined node into a time delay between a pair of low-frequency signals by performing sub-sampling using a sampling head;
 - calculating said time delay corresponding to the difference between test voltage and the reference voltage to obtain a code word; and
 - converting the code word into an analog value to obtain a differential voltage, said differential voltage being the difference between node voltage and reference voltage;
 - repeating all above step for each node in the integrated circuit to perform BIST.

STATEMENT UNDER ARTICLE 19 (1)

The Applicant acknowledges the receipt of the ISR&WO dated 10th June, 2013 issued by the EPO with respect to the aforementioned matter and responds to the objections raised by the learned Authorized Officer are under Article 19.

The instant PCT application discloses a system configured for built-in-self-test (BIST) at each node of an integrated circuit. The system comprises one or more sampling head blocks to convert the predefined test voltage at a node into time delay; a control unit controls the operation of the sampling heads to perform said conversion and the BIST at each node; a clock module comprising two clocks, core and sampling clocks with slightly different frequencies, the pair of core clocks time signals are sampled by sampling clock to digitize the time delay and produce sub-sampled signal pairs; and delay measurement unit (DMU) receives sub-sampled signals from each sampling head block to calculate the time delay and thereby, the test voltage at each node by using interpolation on pre-computed calibration data. The cited document Rajath et al, hereinafter referred as D1, does not talk about pair of core clocks sampled at each test node and digitizing time delay; and in cited document, sub-sampling of the core clock pair is not done at each node; the delay between the core clock pair gets accumulated as the core clock pair is daisy-chained through all the test nodes, for which separating out the contributions due to each test node has to be made.

Each sampling head block comprises a pair of delay cells (V2D) which takes the test voltage of the corresponding node as input and correspondingly delays, an input clock triggering said V2D; and a pair of flip flops connected to the pair of delay cells, each flip flop has input from the corresponding delay cell, said delay flip flops are triggered using a sampling clock to generate pair of sub-sampled signals. However, D1 does not talk about pair of flip flops in a sampling head.

A method to perform built-in self-test (BIST) at each node of an integrated circuit comprising converting test voltage of a predefined node of the integrated circuit and a reference voltage corresponding to said converting of predefined node into time delay between a pair of low-frequency signals by sub-sampling technique, wherein said sub-

sampling technique is performed using sampling head. However, D1 does not talk about a predefined node into time delay between a pair of low-frequency signals by sub-sampling technique.

The Applicant is of the opinion that the claims amendments and aforementioned details are successful in overcoming the novelty, inventiveness and clarity issues raised by the learned Authorized Officer. Therefore, the learned Authorized Officer is requested to consider the same and issue a favourable International Preliminary Report on Patentability.

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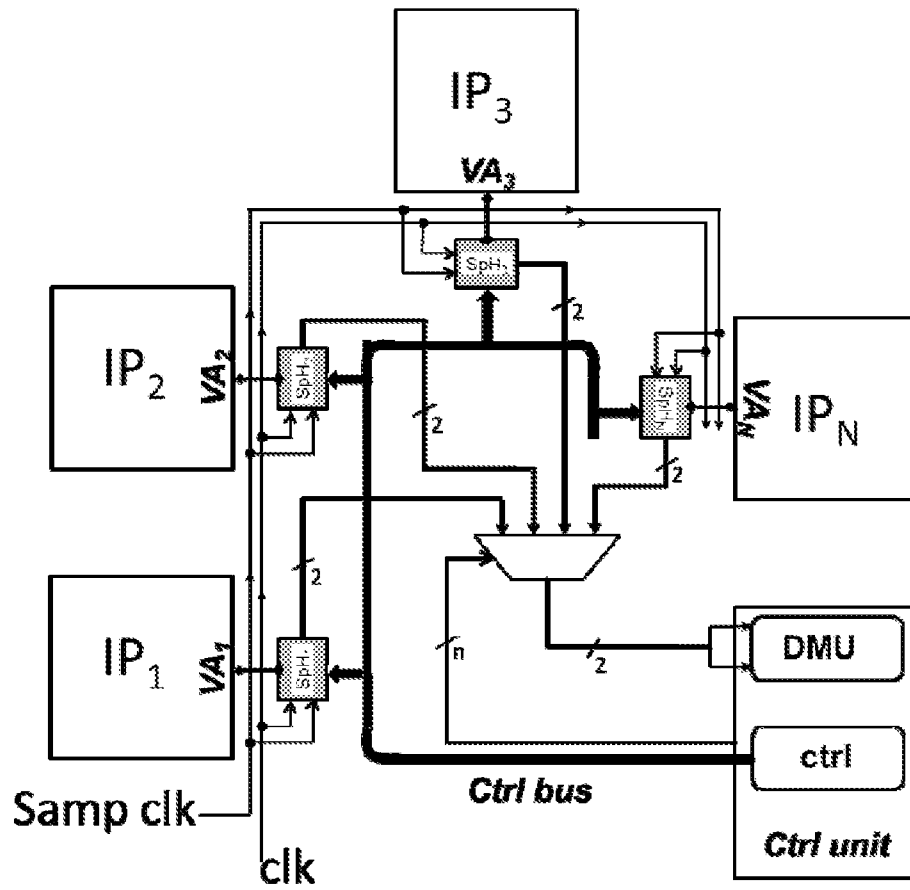


Figure 1a

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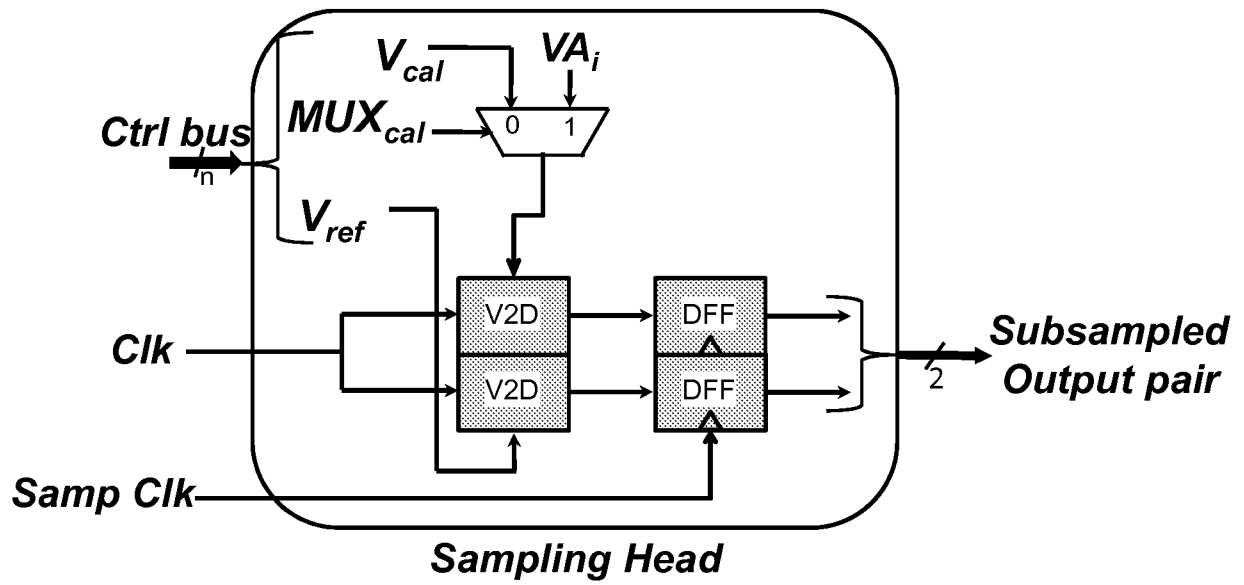


Figure 1b

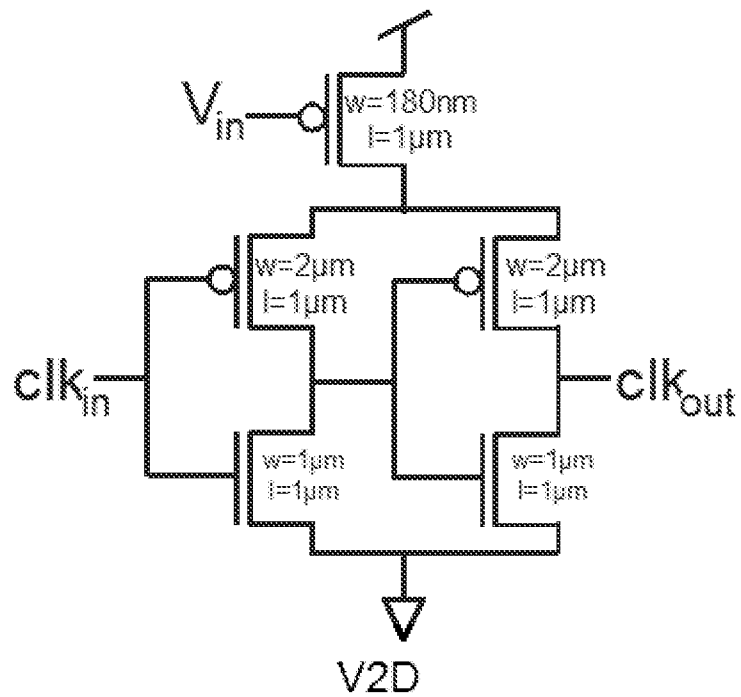


Figure 2

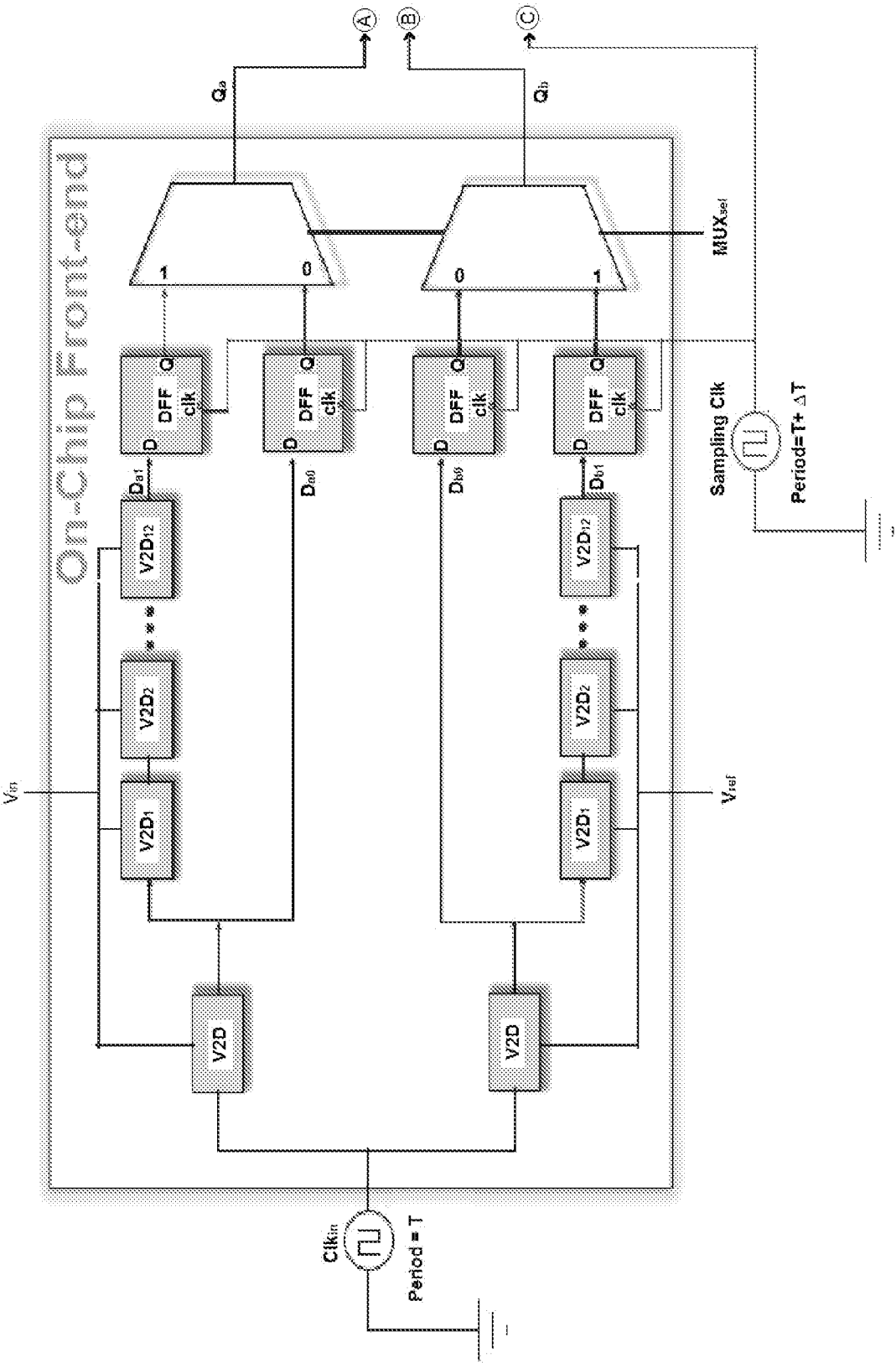


Figure 3

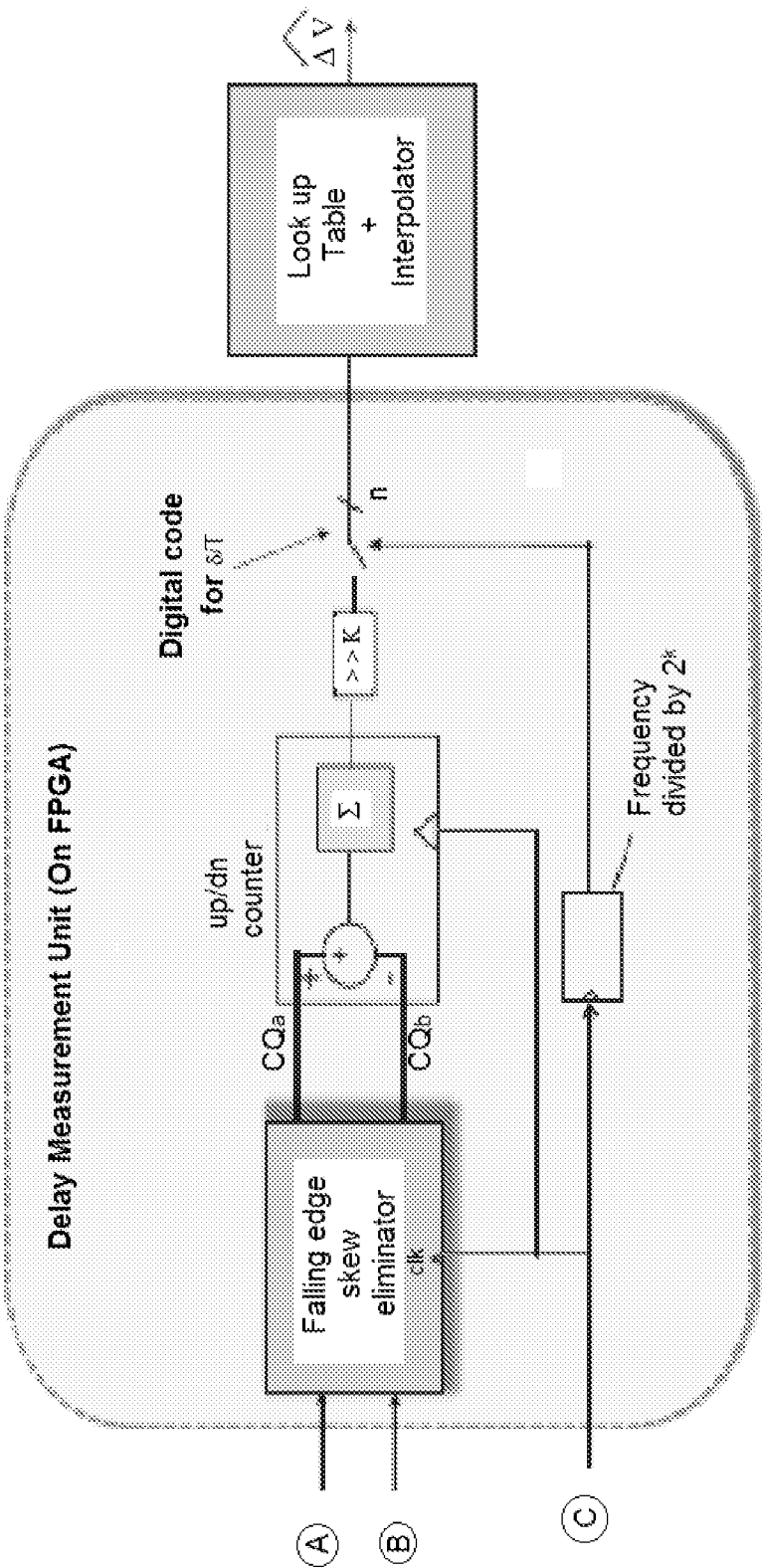


Figure 3 (Contd.)

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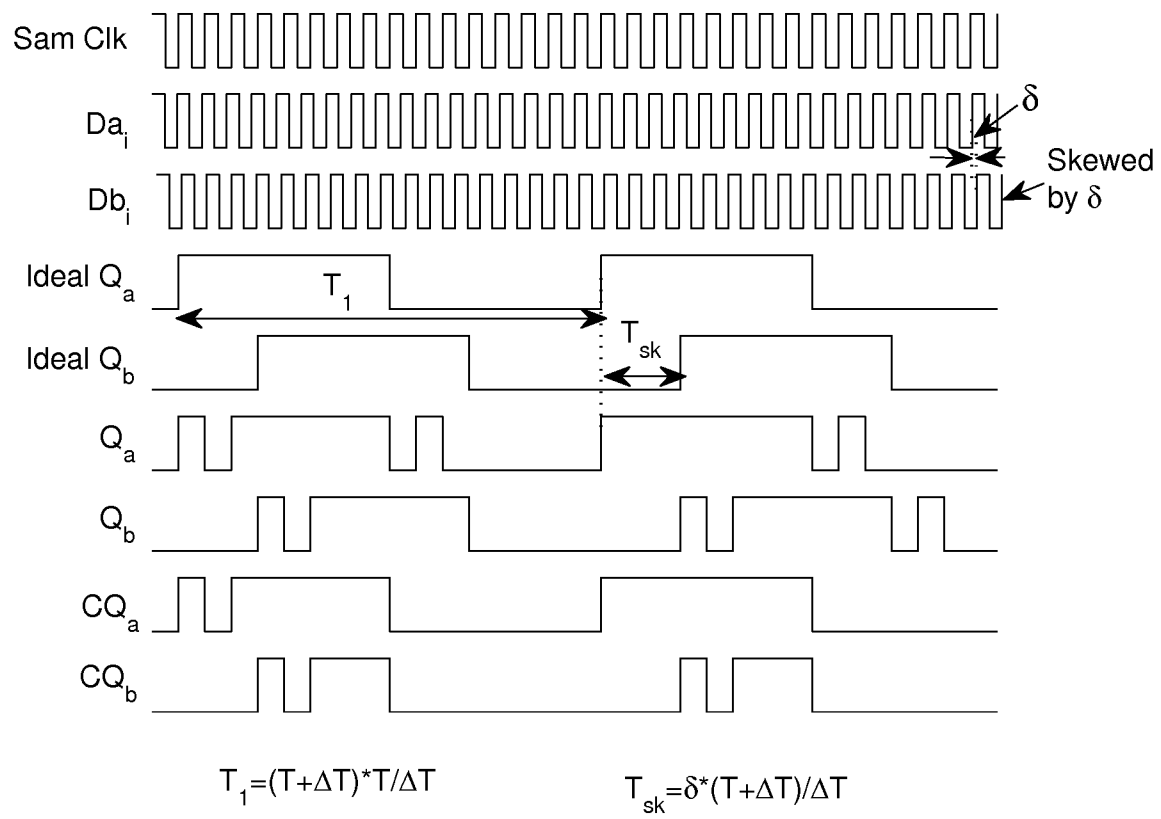


Figure 4

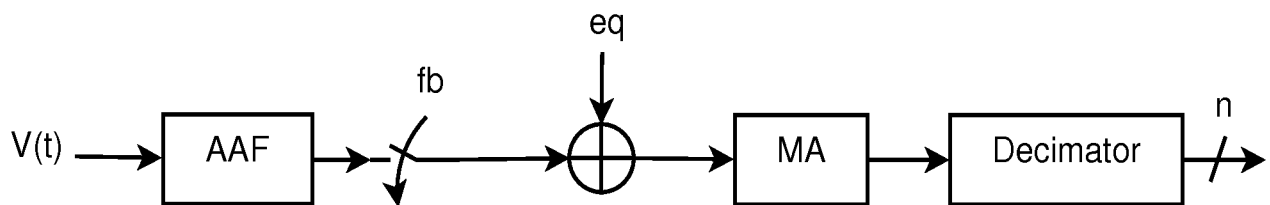


Figure 5

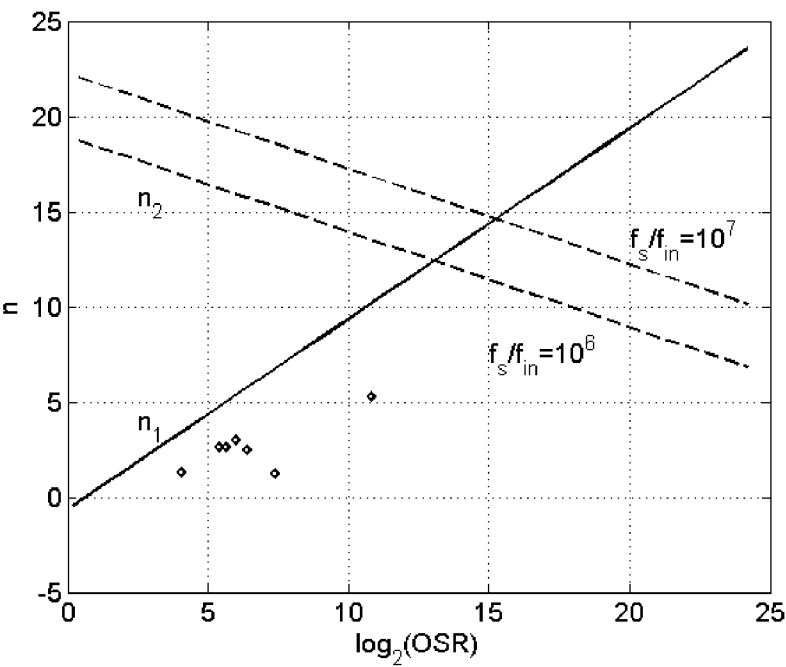


Figure 6

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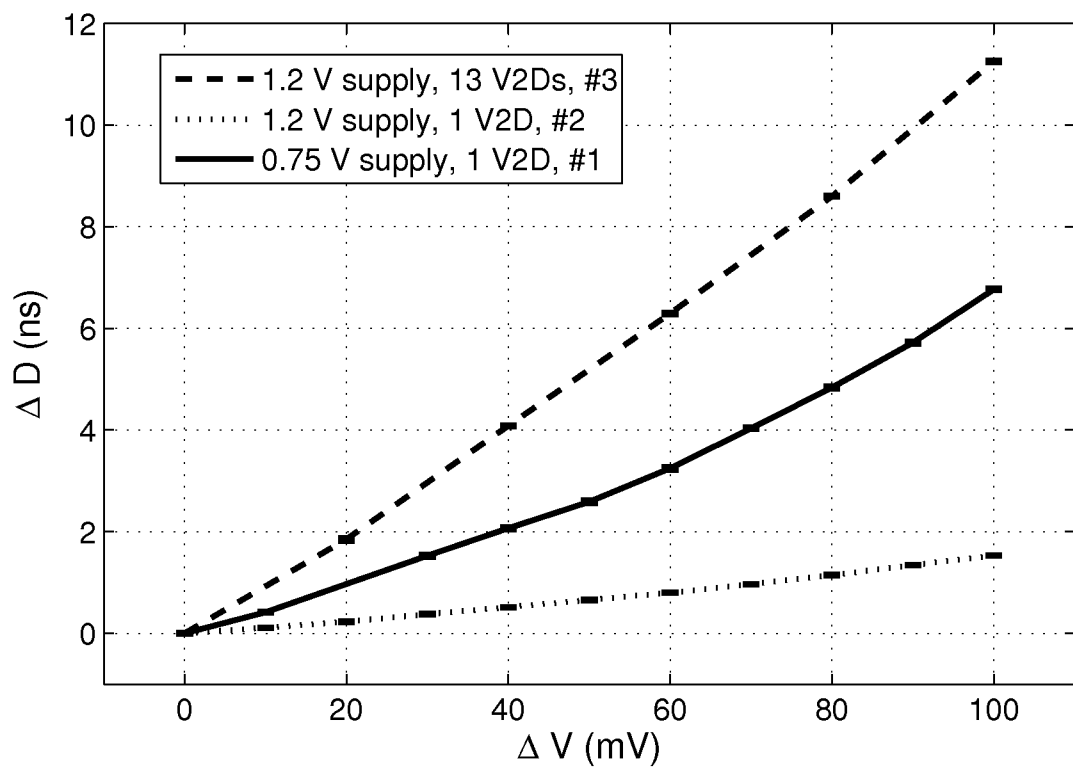


Figure 7

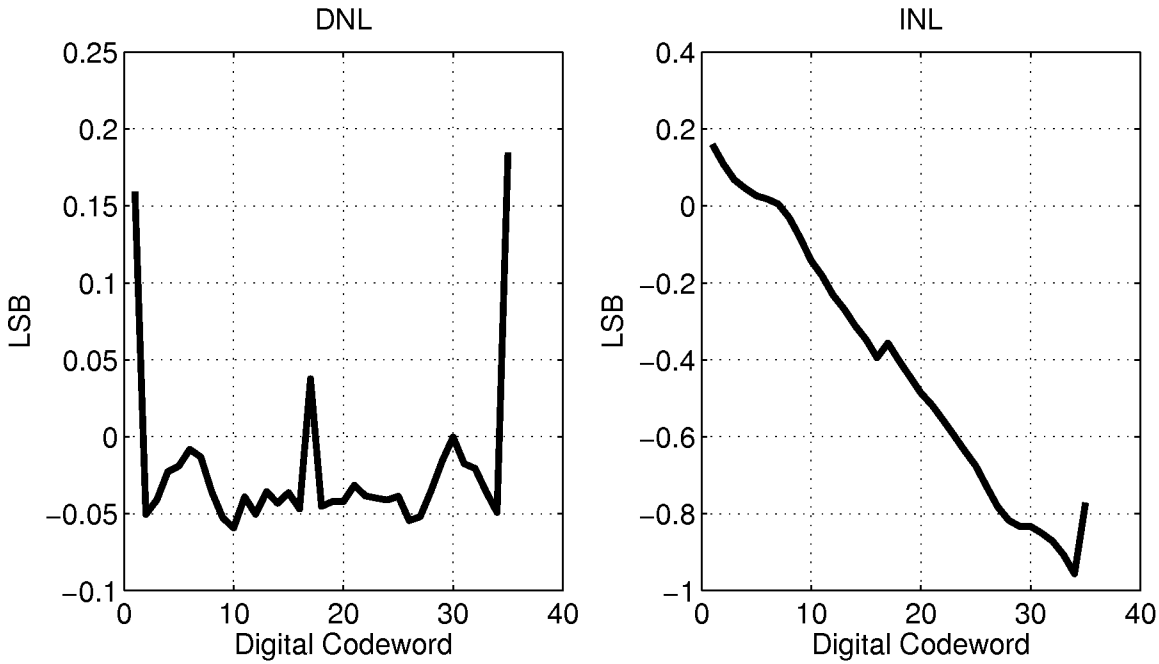


Figure 8

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2012/057462

A. CLASSIFICATION OF SUBJECT MATTER
INV. G01R31/3187 G01R19/00 G01R31/3167
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	<p>RAJATH VASUDEVAMURTHY ET AL: "A mostly-digital analog scan-out chain for low bandwidth voltage measurement for analog IP test", CIRCUITS AND SYSTEMS (ISCAS), 2011 IEEE INTERNATIONAL SYMPOSIUM ON, IEEE, 15 May 2011 (2011-05-15), pages 2035-2038, XP031998053, DOI: 10.1109/ISCAS.2011.5937996 ISBN: 978-1-4244-9473-6 cited in the application the whole document</p> <p style="text-align: center;">----- -/-</p>	1-8



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

31 May 2013

Date of mailing of the international search report

10/06/2013

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
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Fax: (+31-70) 340-3016

Authorized officer

Meggyesi, Zoltán

INTERNATIONAL SEARCH REPORT

International application No

PCT/IB2012/057462

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	<p>CHIN-LONG WEY: "BUILT-IN SELF-TEST (BIST) STRUCTURE FOR ANALOG CIRCUIT FAULT DIAGNOSIS", IEEE TRANSACTIONS ON INSTRUMENTATION AND MEASUREMENT, IEEE SERVICE CENTER, PISCATAWAY, NJ, US, vol. 39, no. 3, 1 June 1990 (1990-06-01), pages 517-521, XP000129130, ISSN: 0018-9456, DOI: 10.1109/19.106284 cited in the application the whole document</p>	1-8
A	<p>RON HO ET AL: "Applications of on-chip samplers for test and measurement of integrated circuits", VLSI CIRCUITS, 1998. DIGEST OF TECHNICAL PAPERS. 1998 SYMPOSIUM ON HONOLULU, HI, USA 11-13 JUNE 1998, NEW YORK, NY, USA, IEEE, US, 11 June 1998 (1998-06-11), pages 138-139, XP010291219, DOI: 10.1109/VLSIC.1998.688033 ISBN: 978-0-7803-4766-3 cited in the application the whole document</p>	1-8
A	<p>GAURAB BANERJEE ET AL: "Analog/RF Built-in-Self-Test Subsystem for a Mobile Broadcast Video Receiver in 65-nm CMOS", IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE SERVICE CENTER, PISCATAWAY, NJ, USA, vol. 46, no. 9, 1 September 2011 (2011-09-01), pages 1998-2008, XP011381461, ISSN: 0018-9200, DOI: 10.1109/JSSC.2011.2159055 cited in the application Sections I-IV on p. 1998-2003</p>	1-8