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 [73] Assignee **Medeko Incorporated**  
**Wood Dale, Ill.**

[54] **DATA HANDLING SYSTEM**  
 13 Claims, 45 Drawing Figs.

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 [51] Int. Cl. .... G06F 3/00  
 [50] Field of Search ..... 340/172.5,  
 150, 151, 152, 154; 235/157, 61.6, 61.7

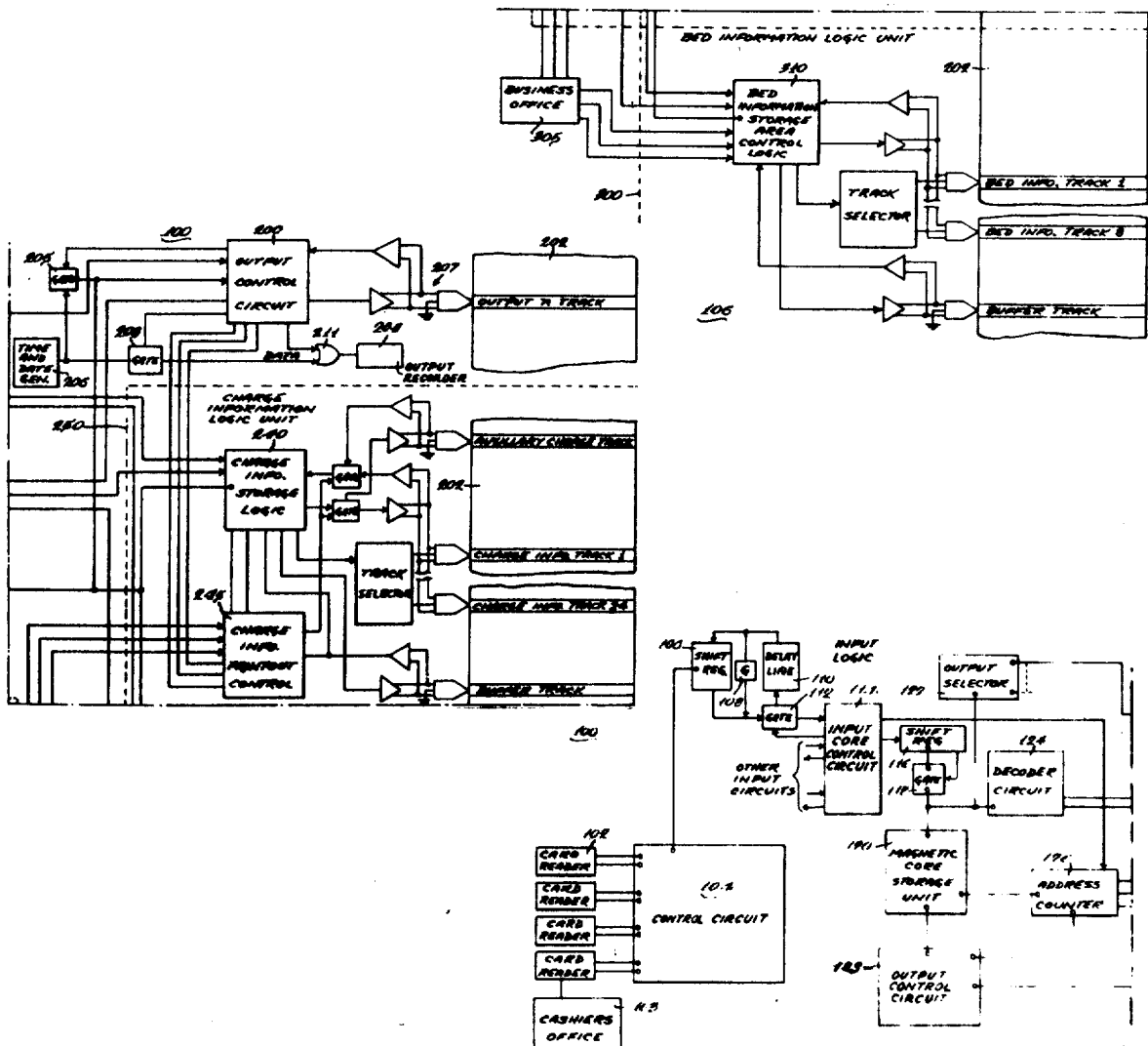
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Primary Examiner—Raulfe B. Zache  
 Attorney—Mason, Kolehmainen, Rathburn and Wyss

**ABSTRACT:** The application discloses a hospital data handling system which transmits and receives all message information normally required in hospital operations and automatically withdraws from the transmitted messages all data necessary for establishing such items as bed status data, inventory records, patient charges, etc. The system input is derived from permanent punch cards containing all necessary message and control information and disposable punch cards containing variable data, such as patient identifying cards made, for instance, when a patient is admitted. A printer and a card reader are located at each message originating location or station in the hospital to provide messages which are placed in a delay line input storage shared by a group of card readers. As the delay line data is transferred to a core storage unit shared by all the readers, a printer selector checks each message for printer addresses, and a control decoder checks for the type of operation to be performed on the message. If only output recording is required and if all addressed printers are available, the message is cleared from the delay line storage and read out from the core storage unit to the printers through individual buffer tracks on a drum in a central processor. Alternatively, if all the printers are not available, the message is retained in the delay line until the printers are available. If the control decoding indicates that data operations are to be performed on the message, the message is sent from the core storage unit to the drum in the central processor.



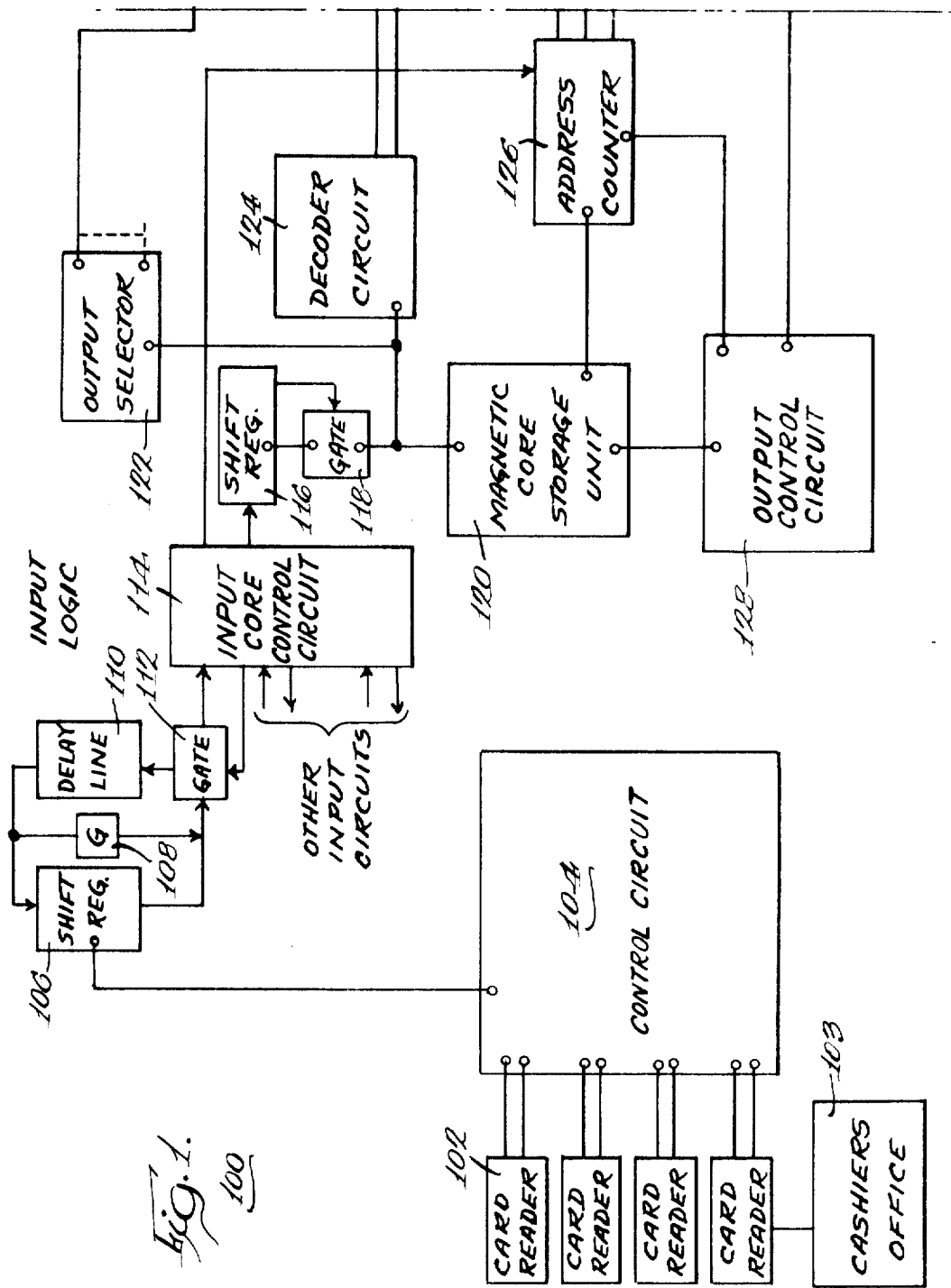
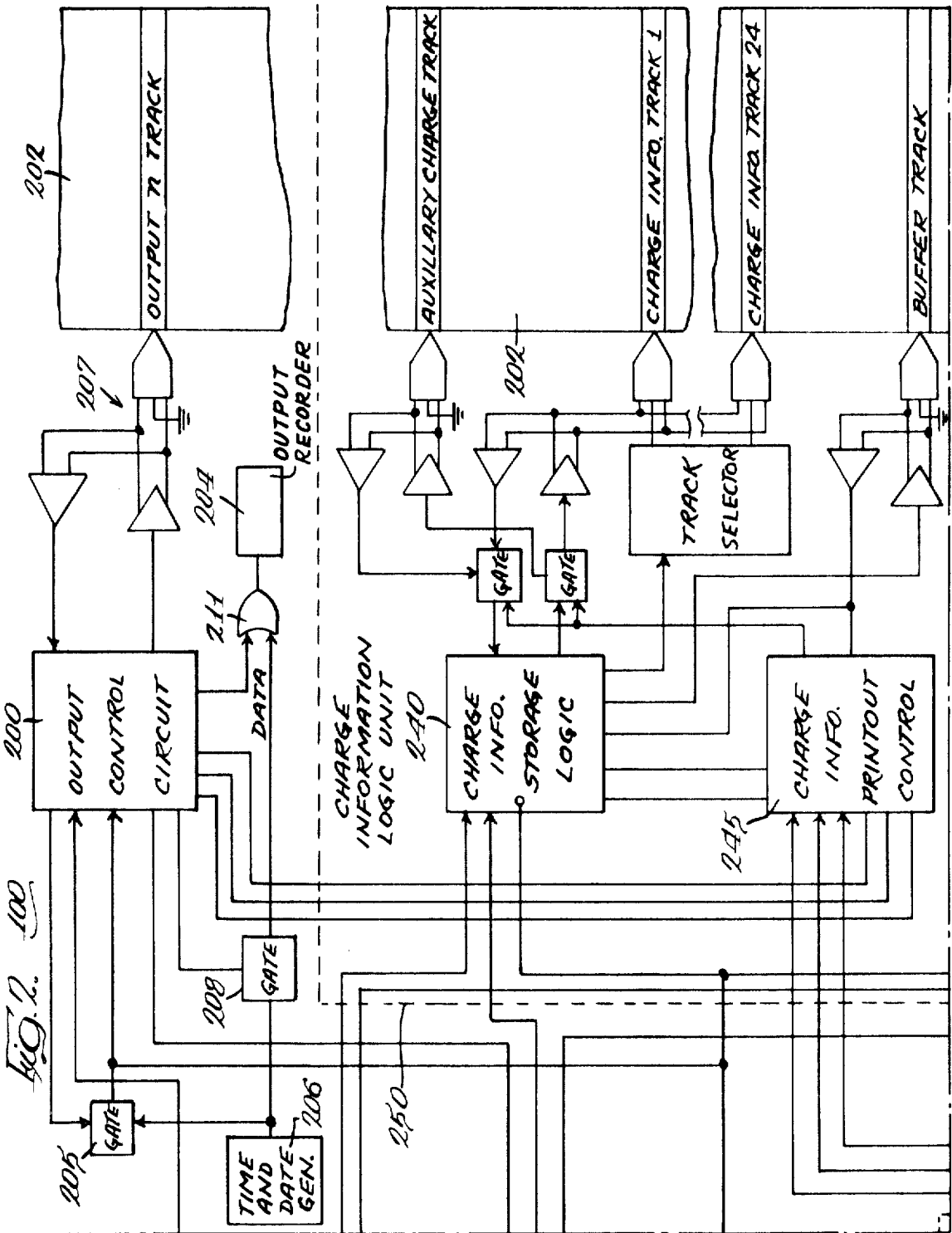


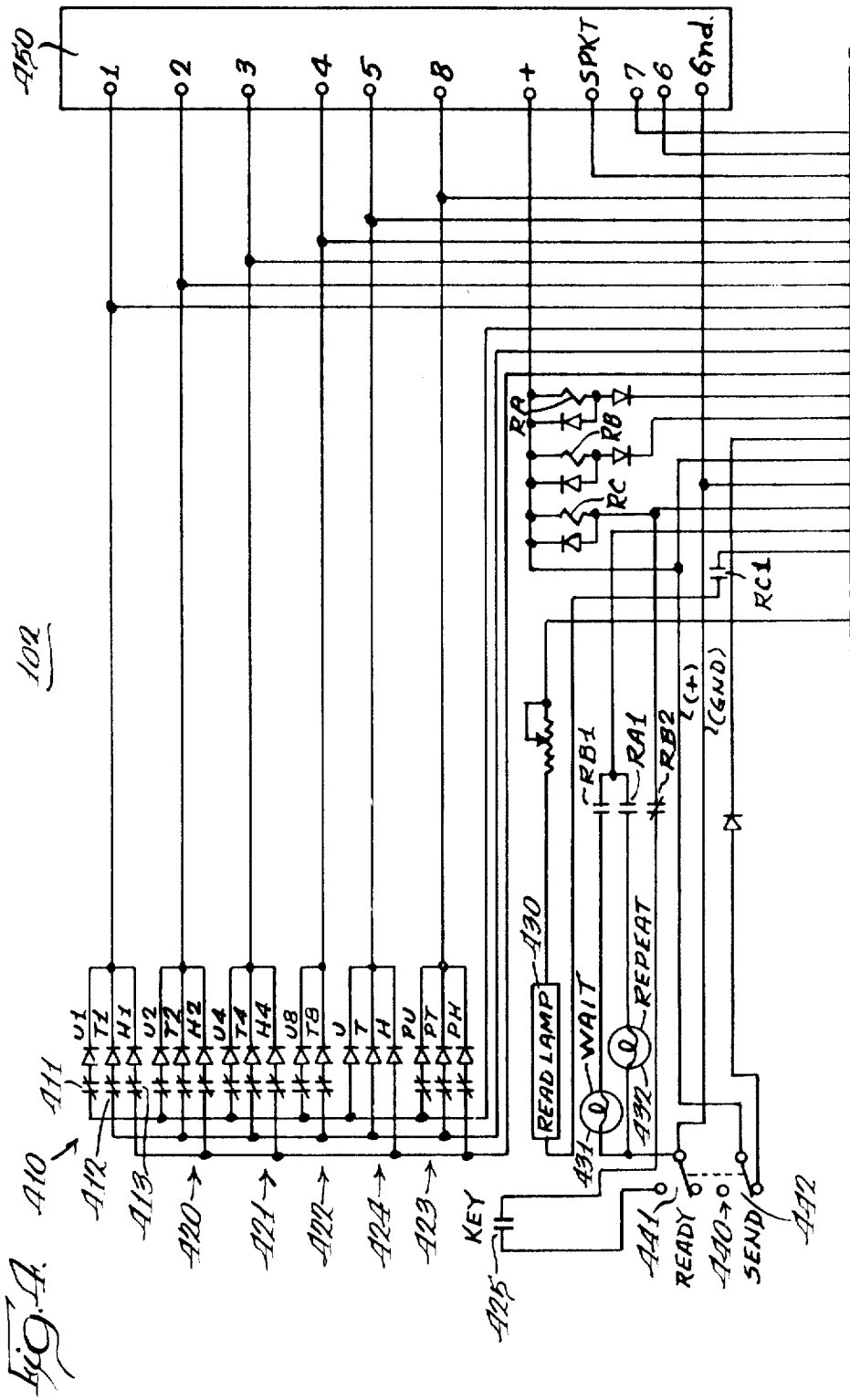
Fig. 1.  
100

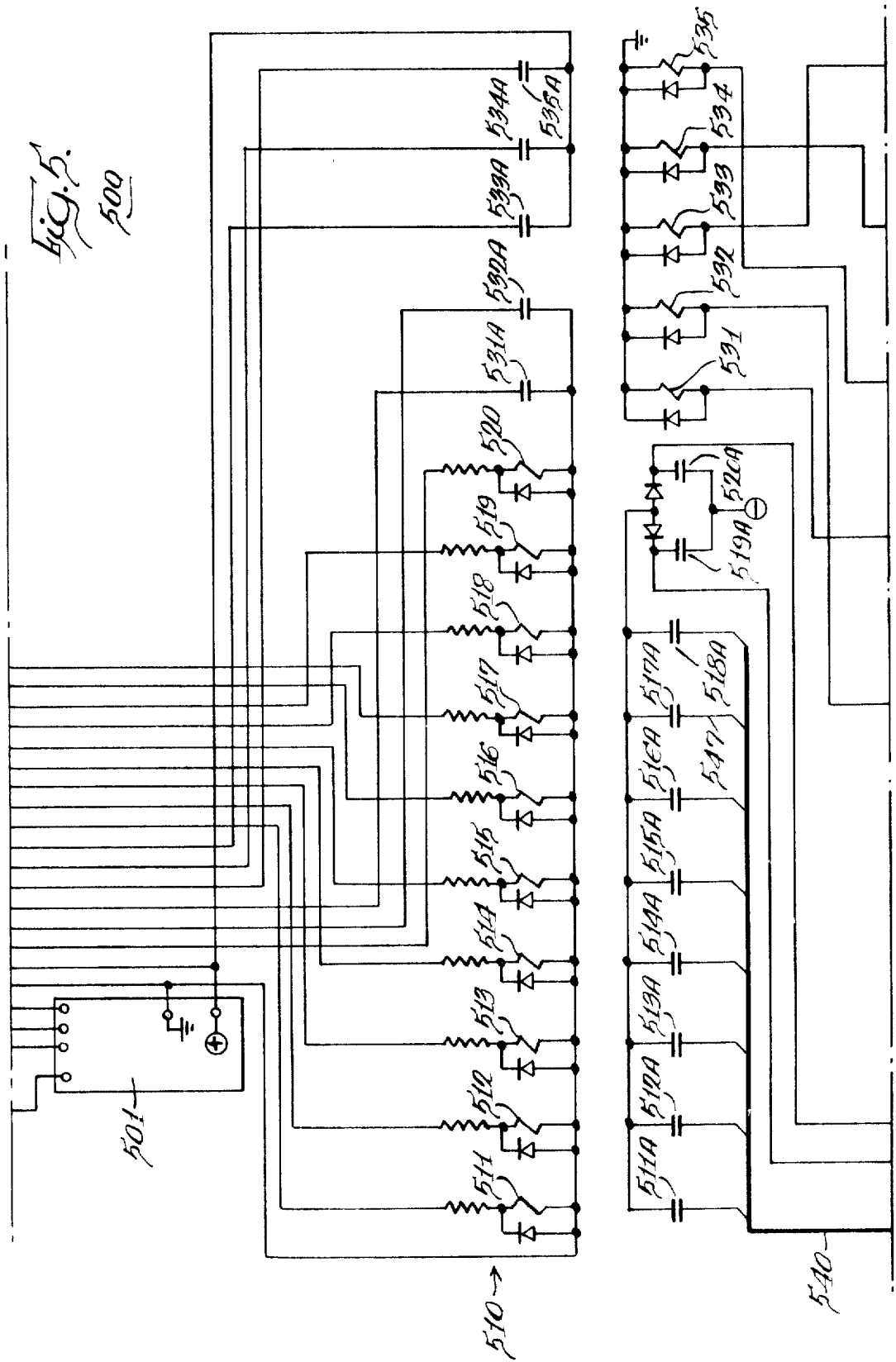
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Eugene A. Staria  
By

Mason, Kolchmainen, Rathburn & Wyss  
Attys









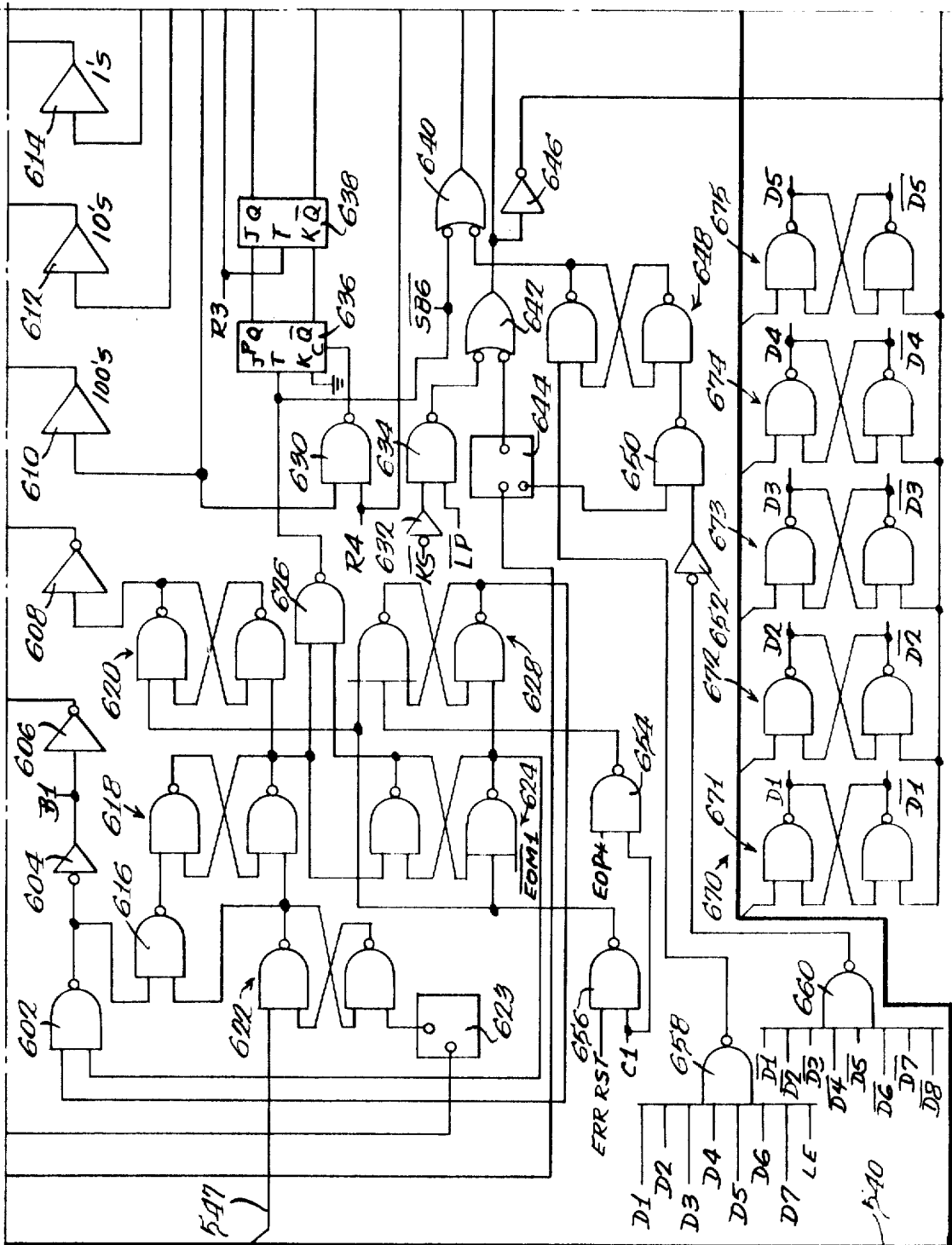


Fig. 6.

10A →

Fig. 7

10A

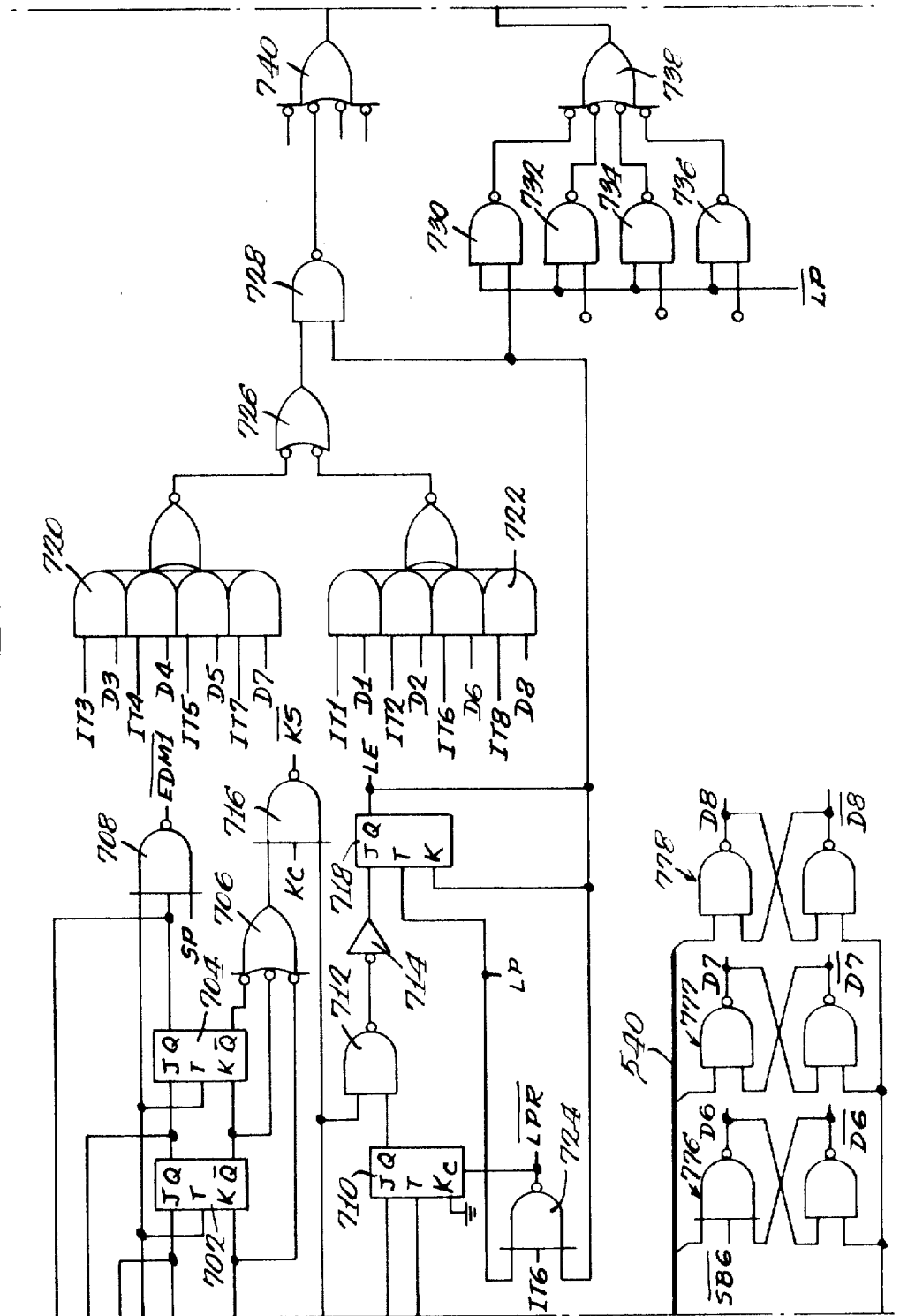
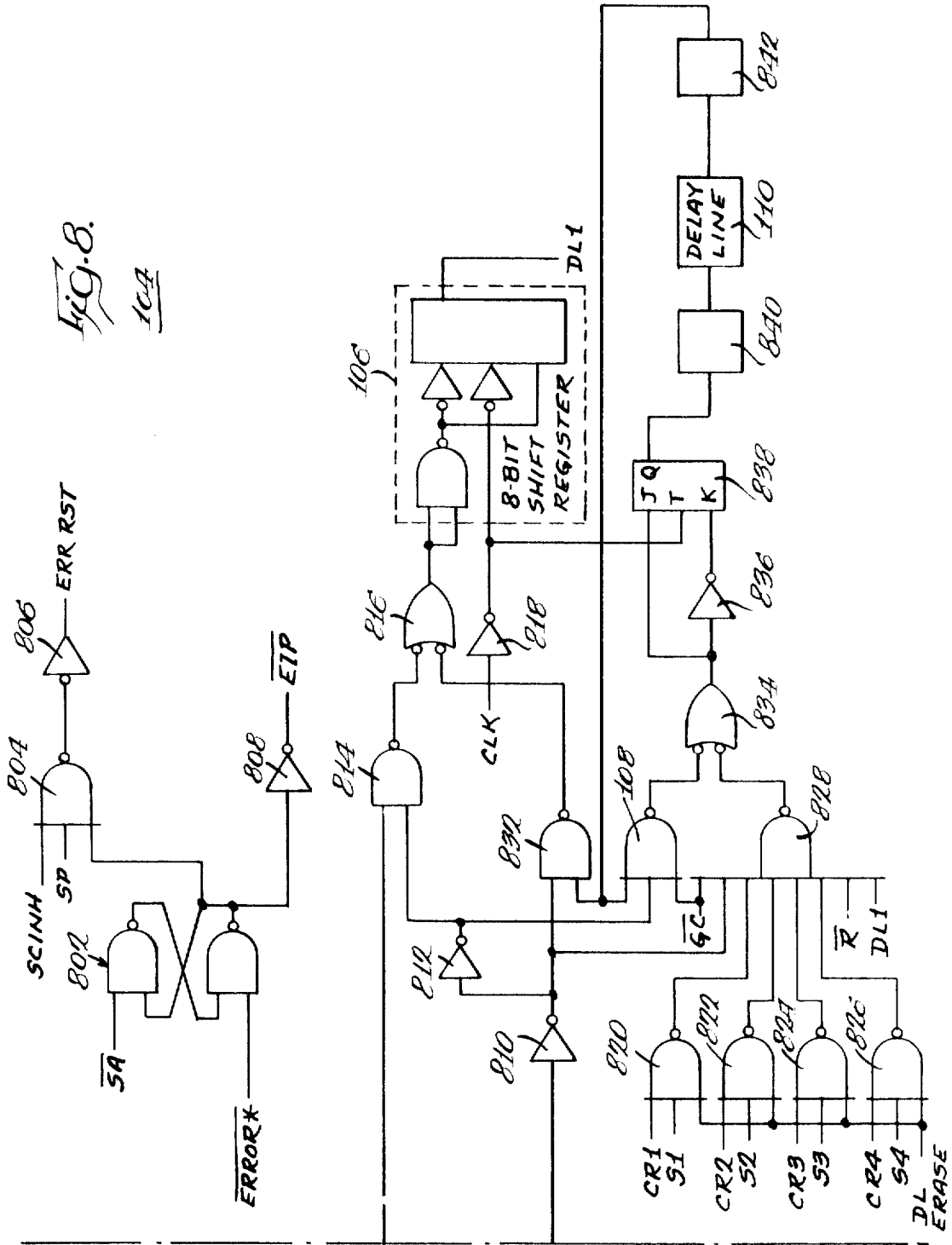


Fig. 8.  
10A



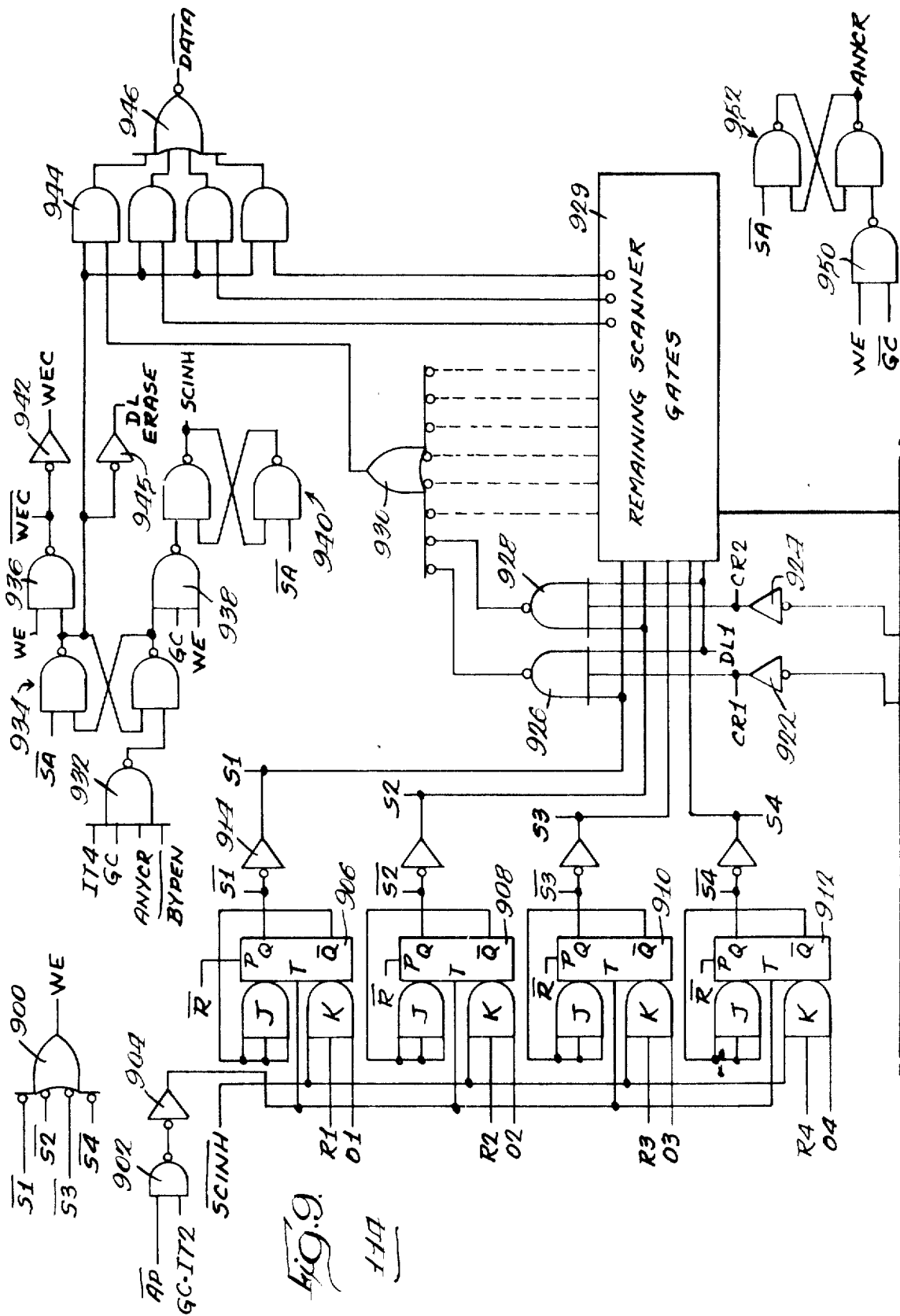
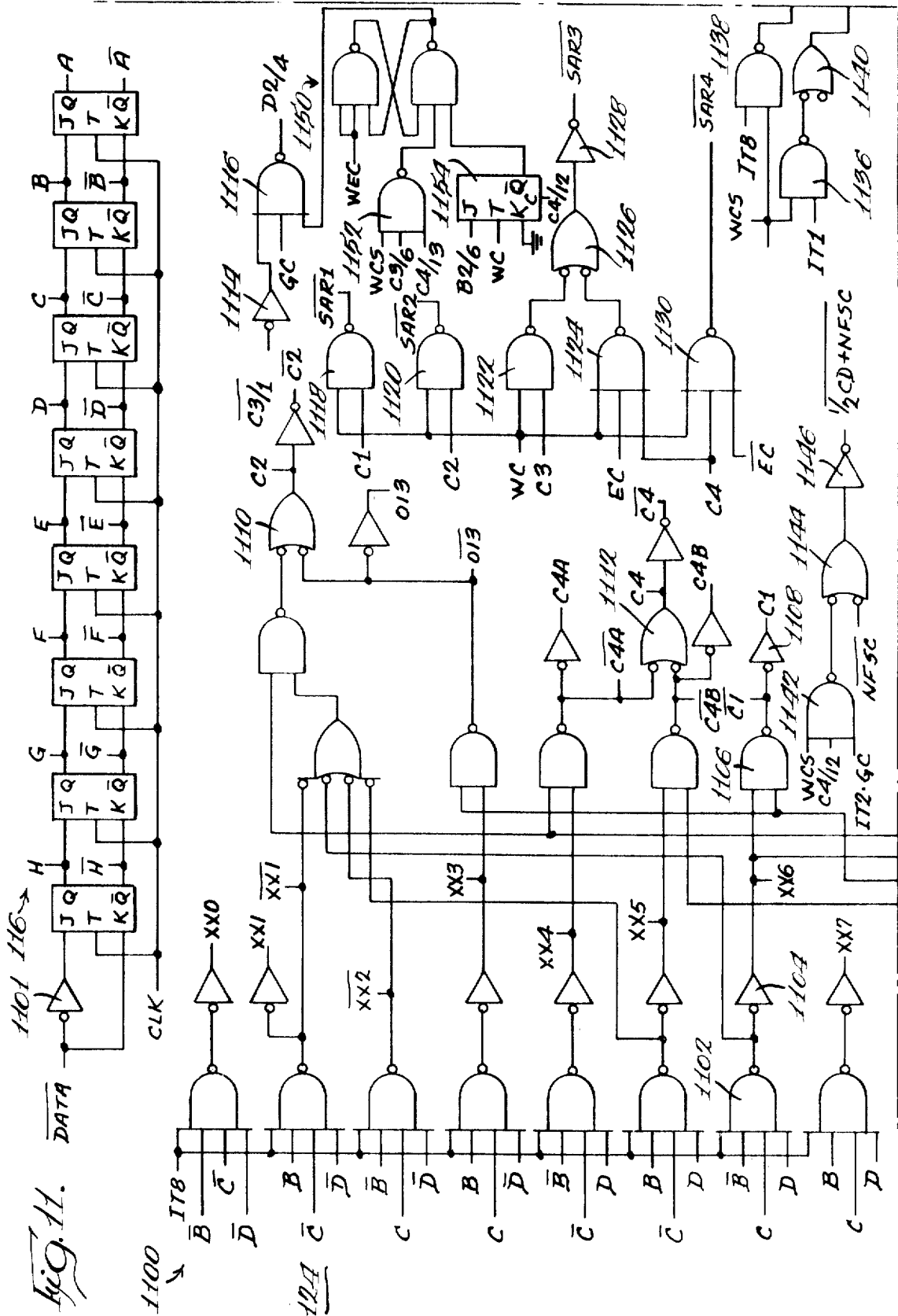
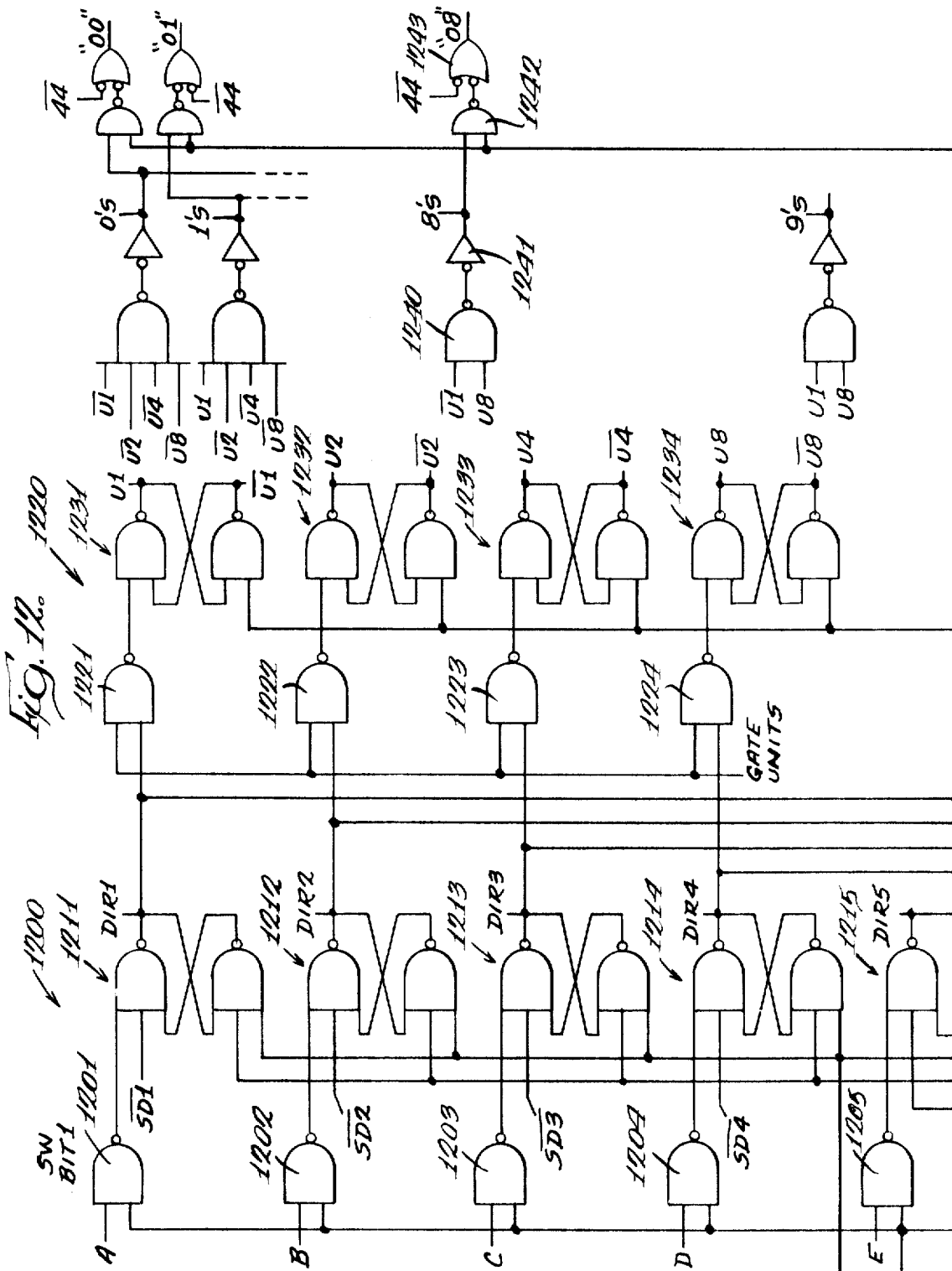


Fig. 9  
117









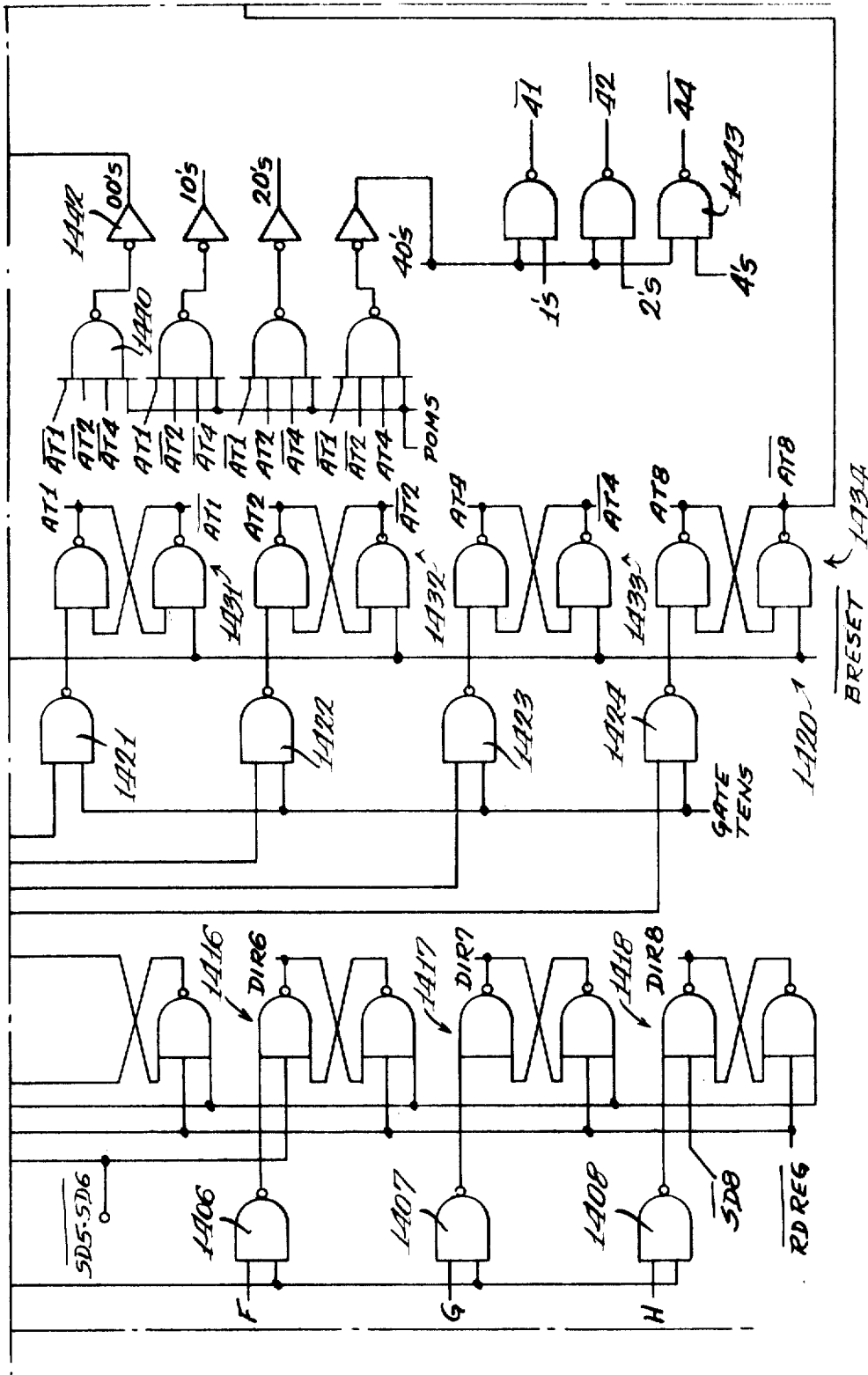
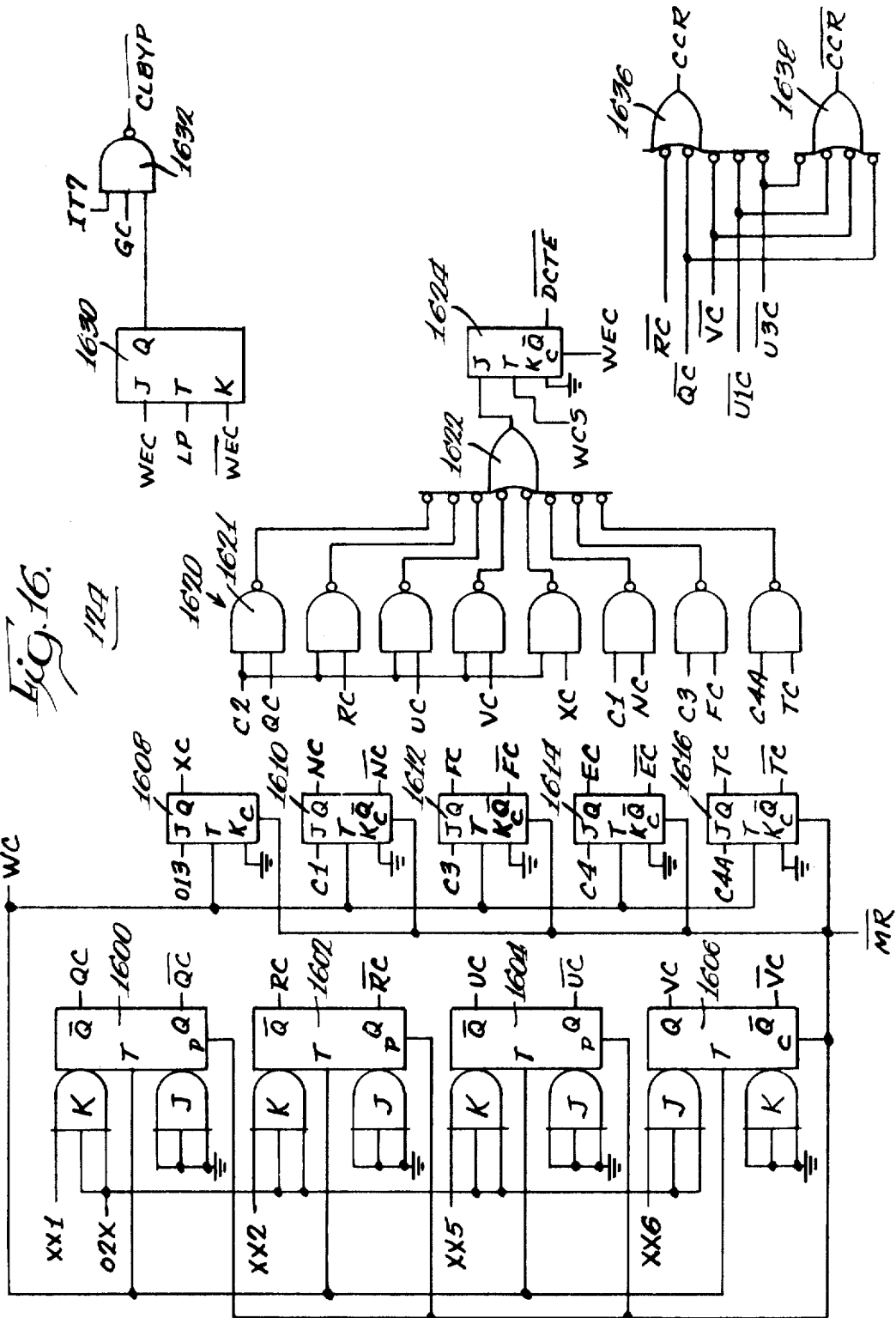


FIG. 1A







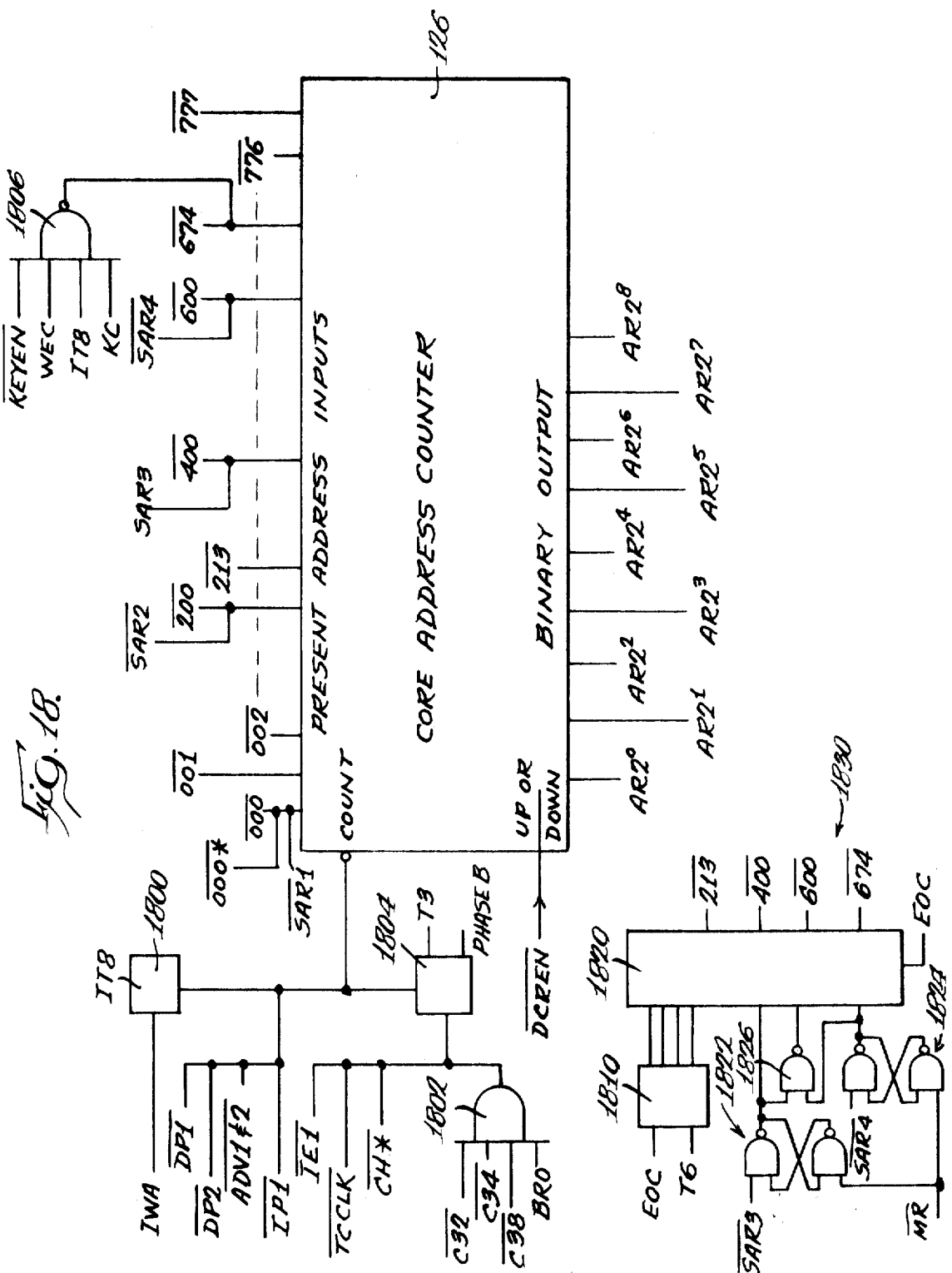


Fig. 19.

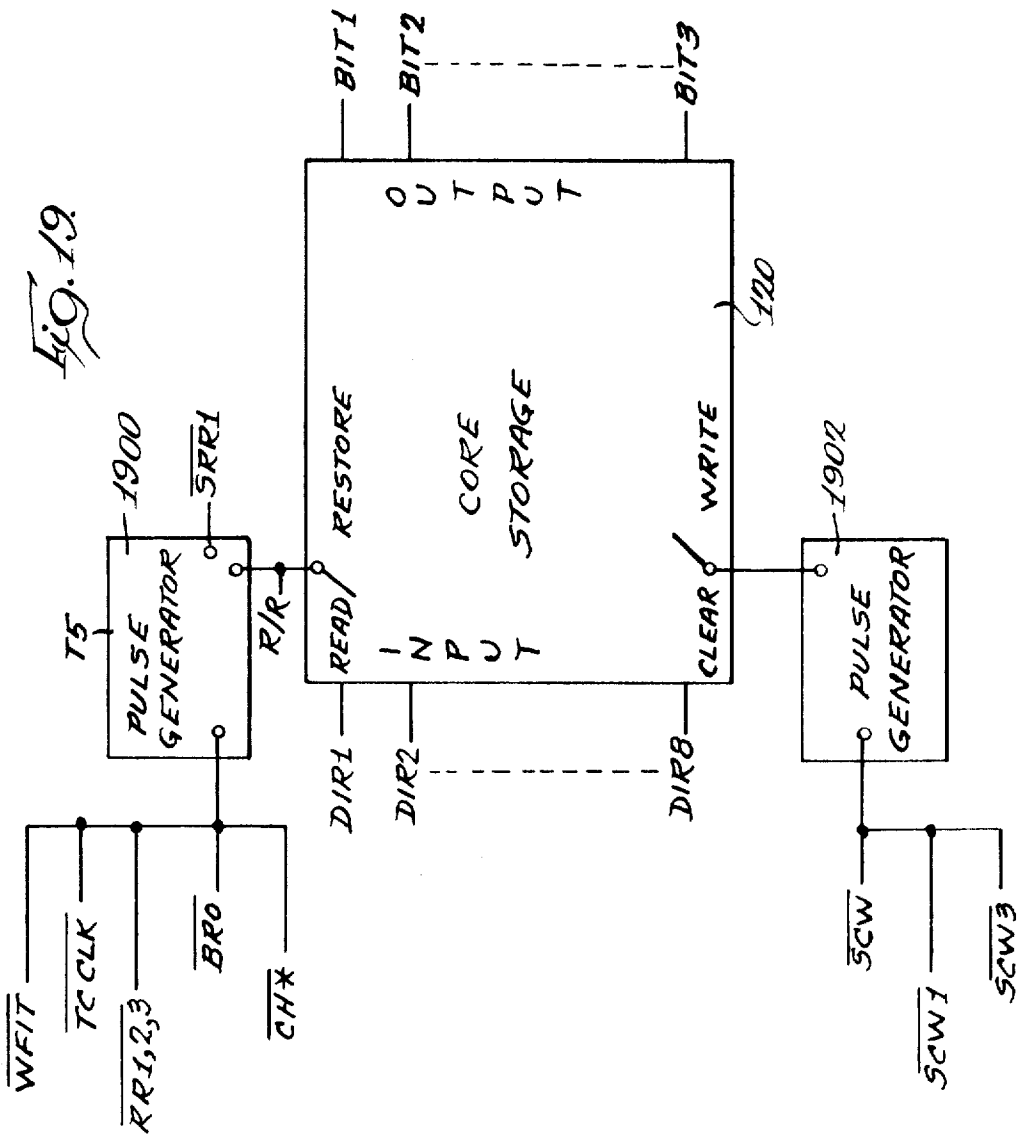


Fig. 20.

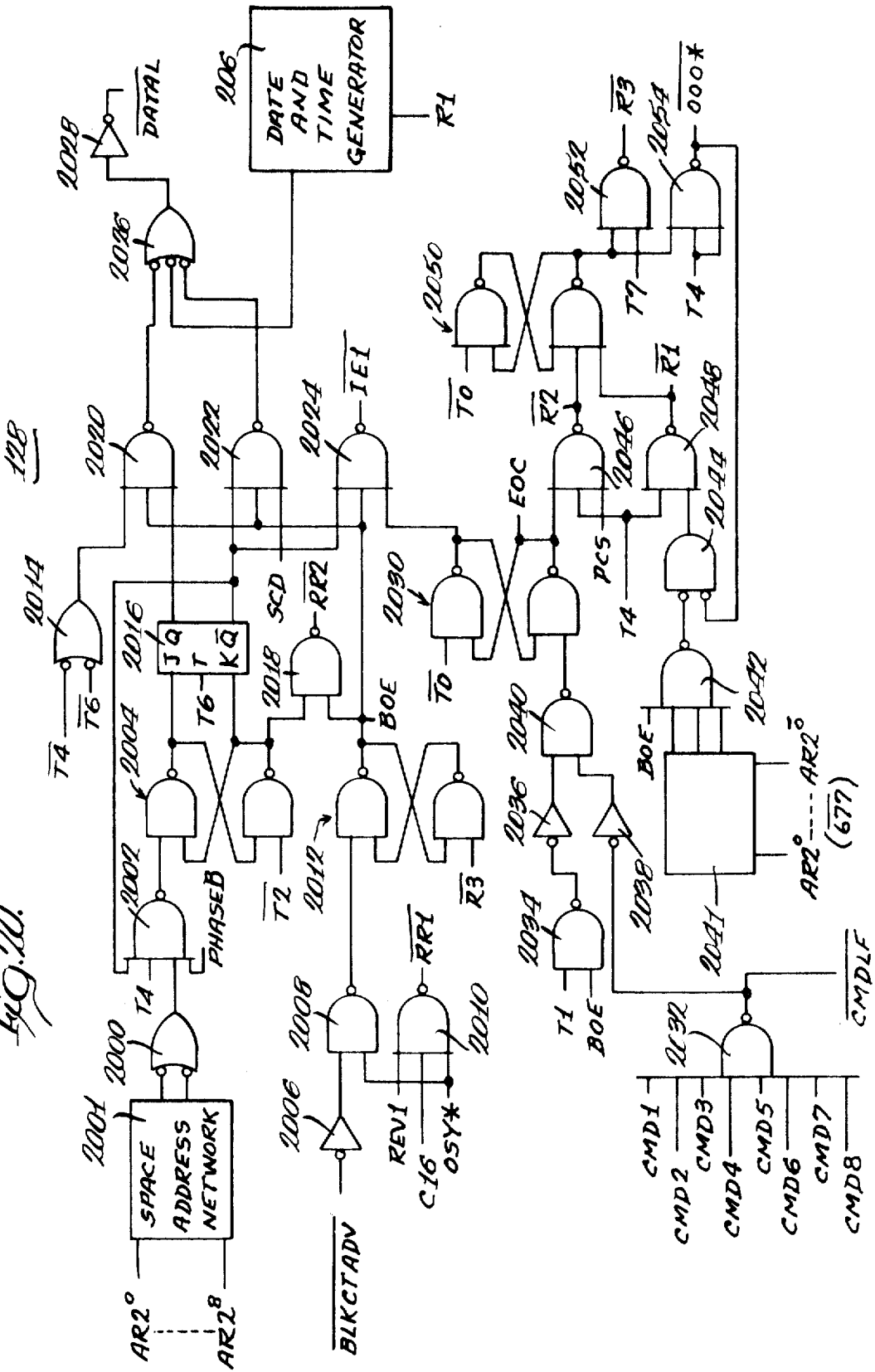


FIG. 21.

128

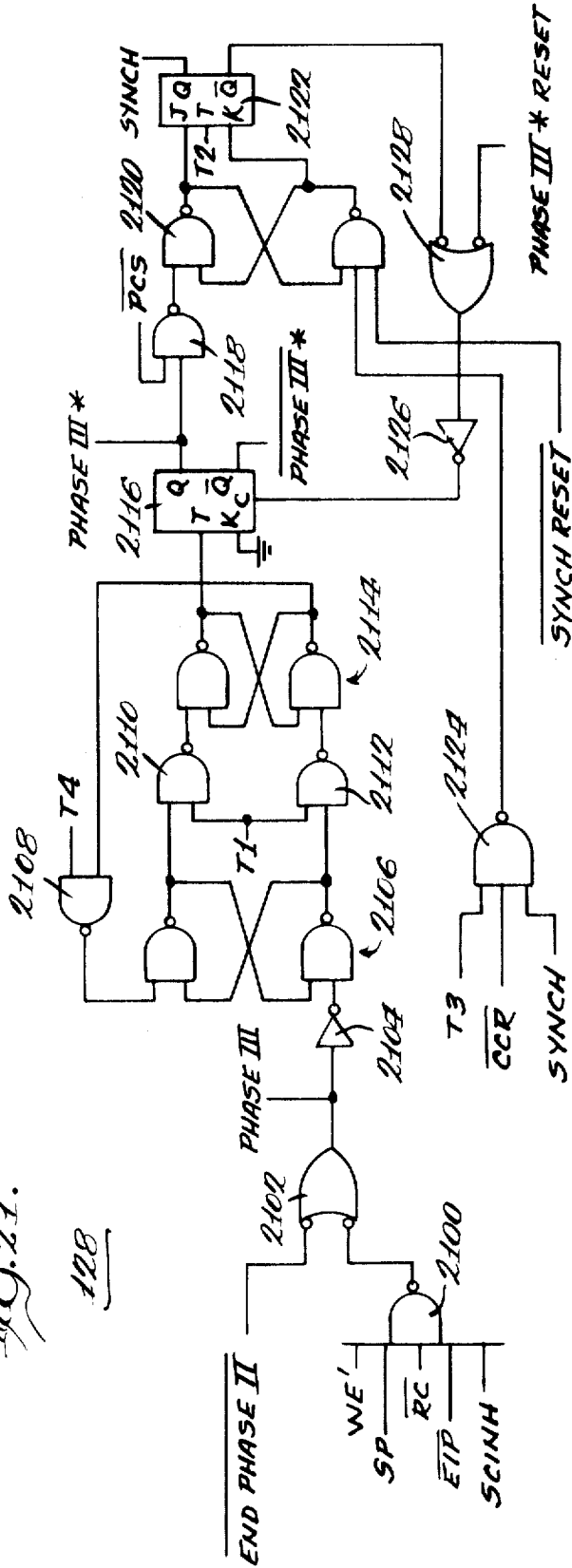
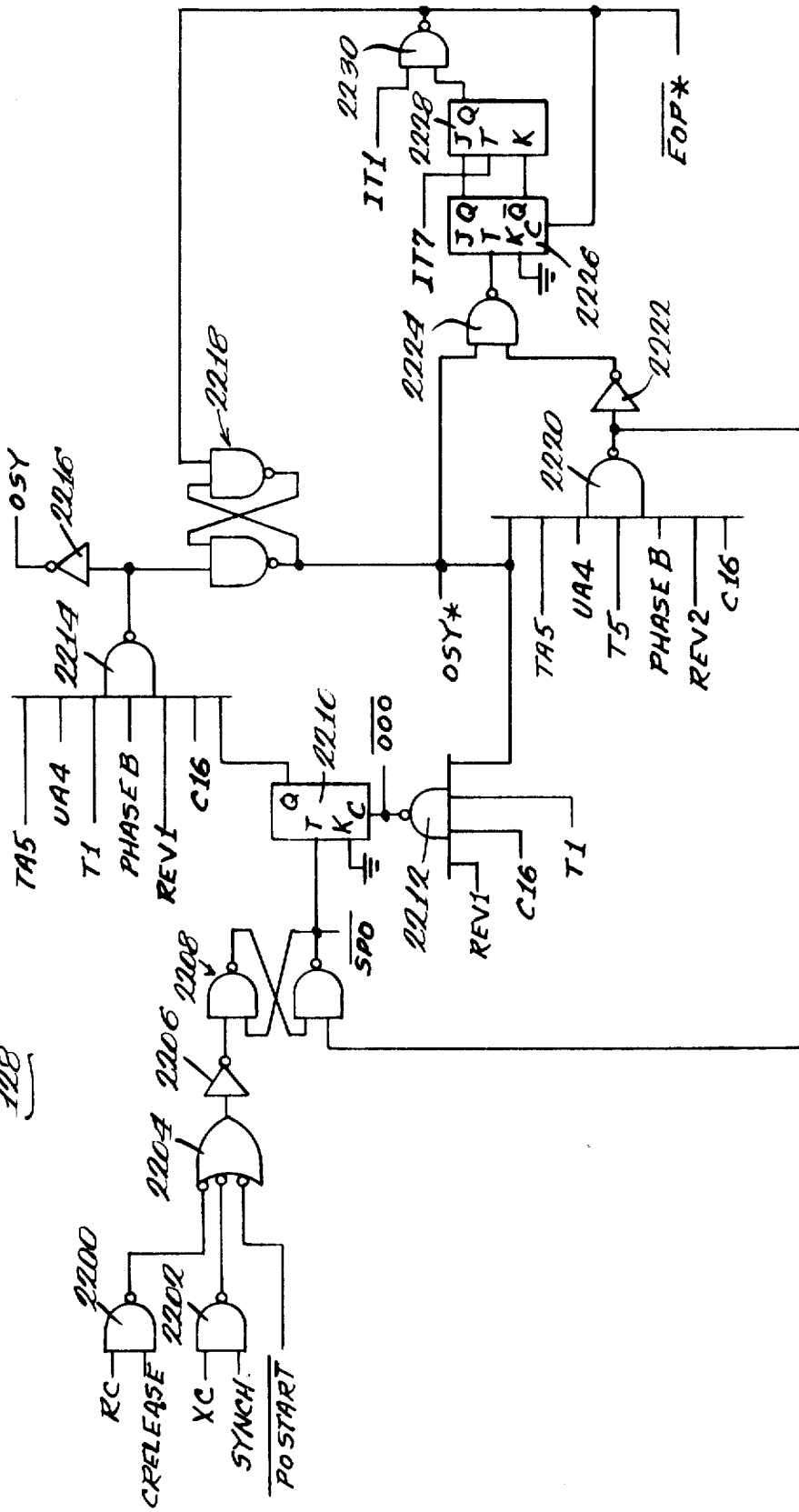


FIG. 22.

128





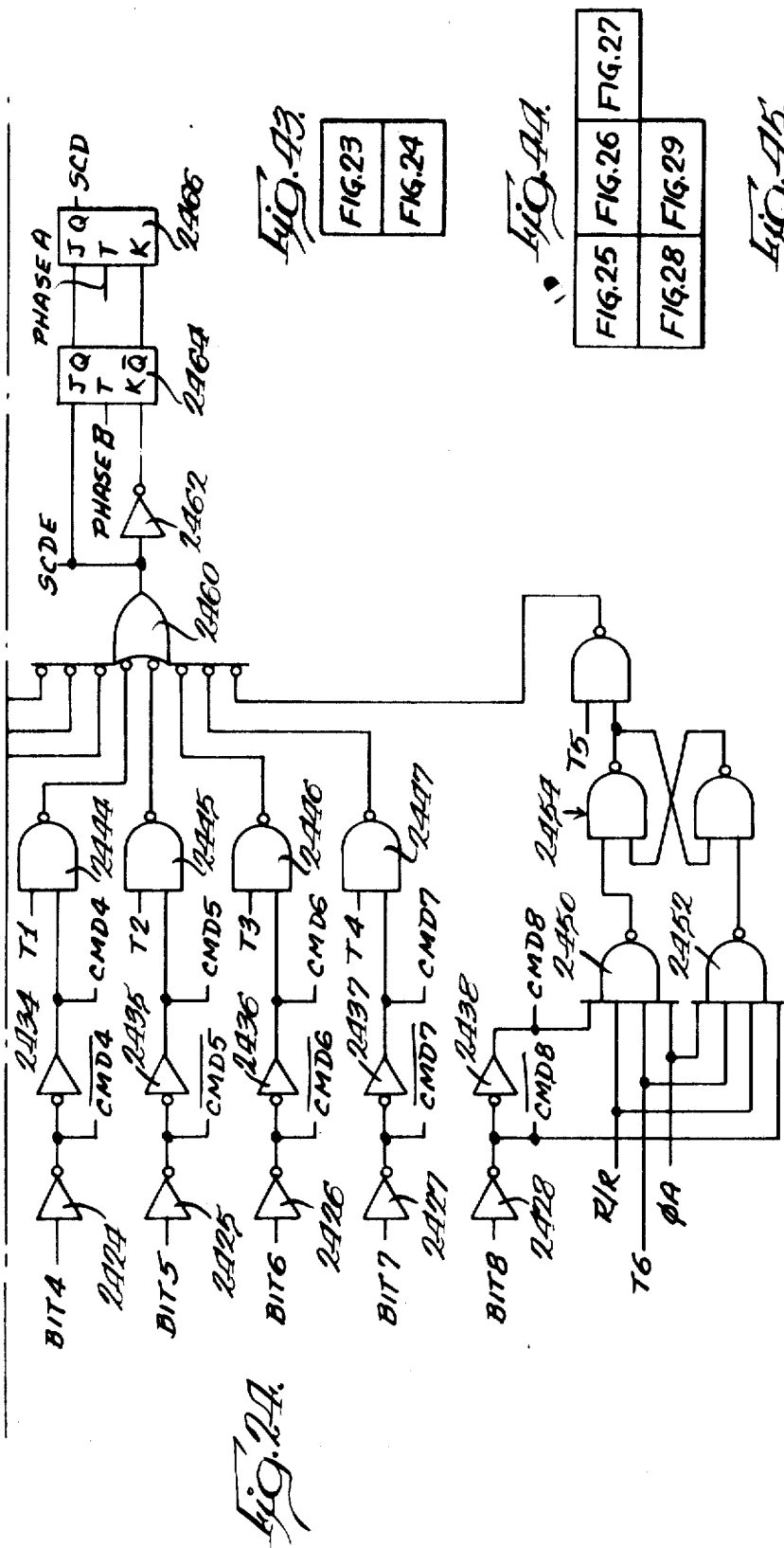
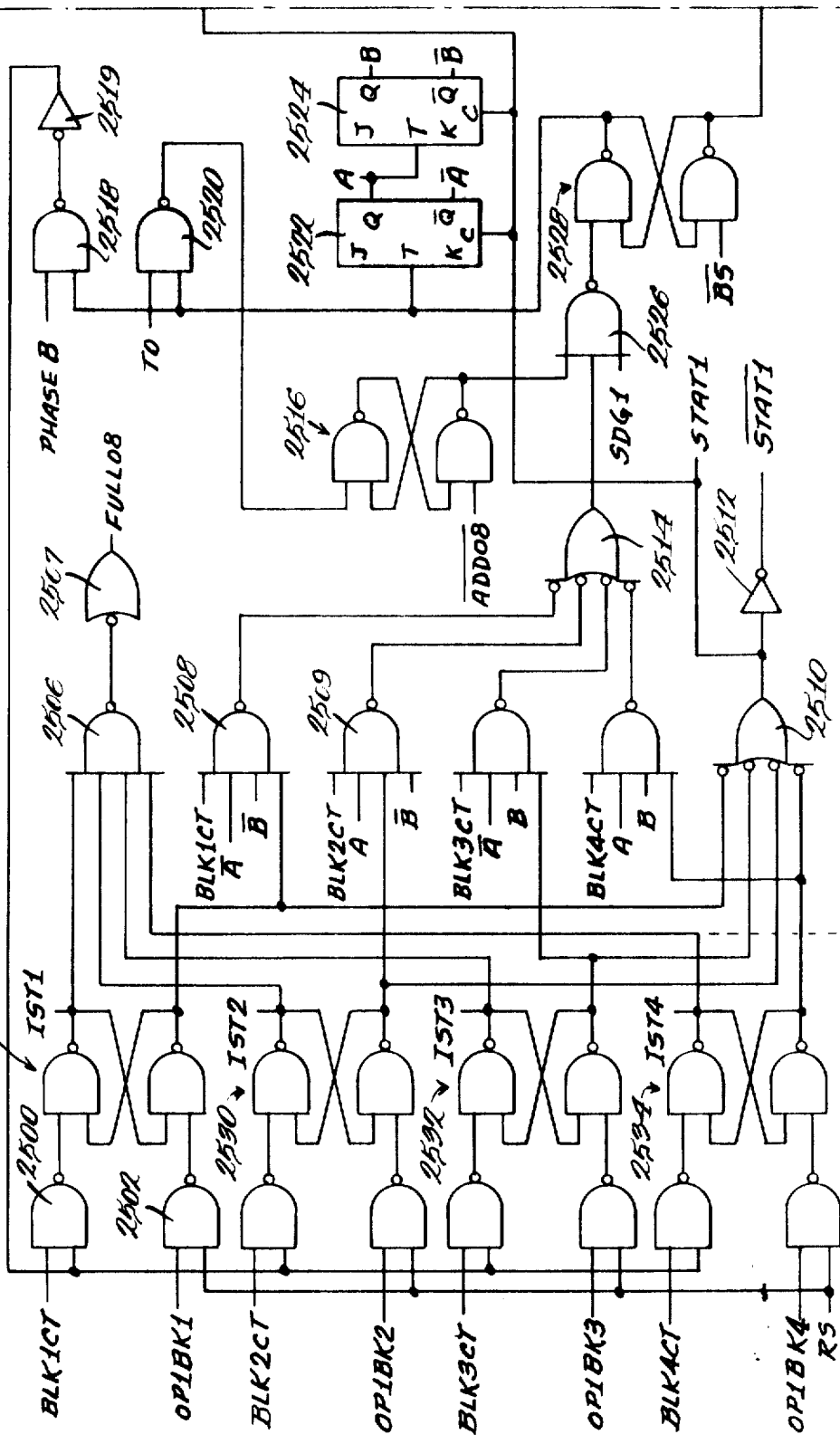


FIG. 23  
FIG. 24

FIG. 44  
FIG. 25  
FIG. 26  
FIG. 27  
FIG. 28  
FIG. 29

FIG. 30  
FIG. 31  
FIG. 32

Fig. 25. 200



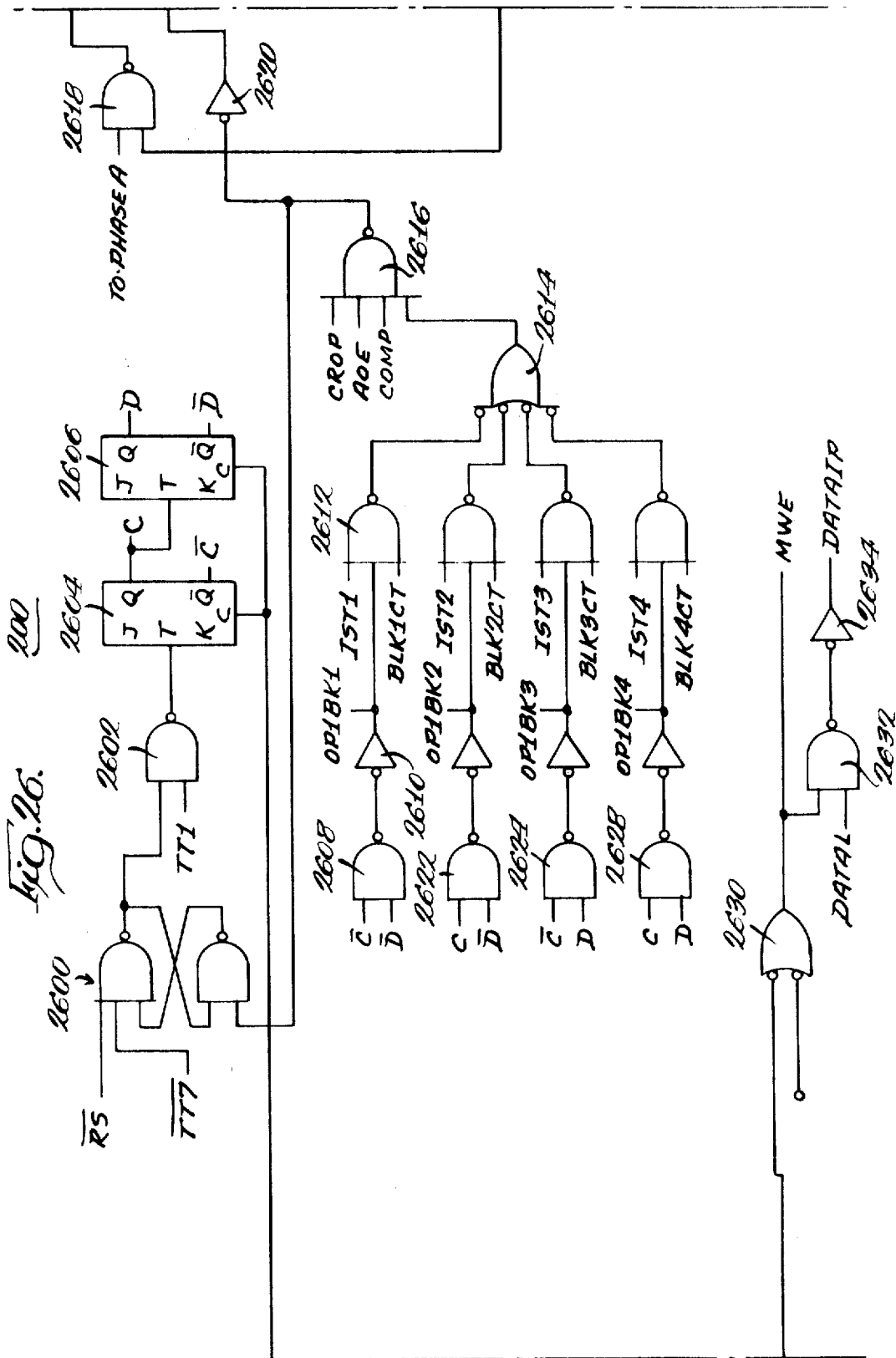


Fig. 27.  
200

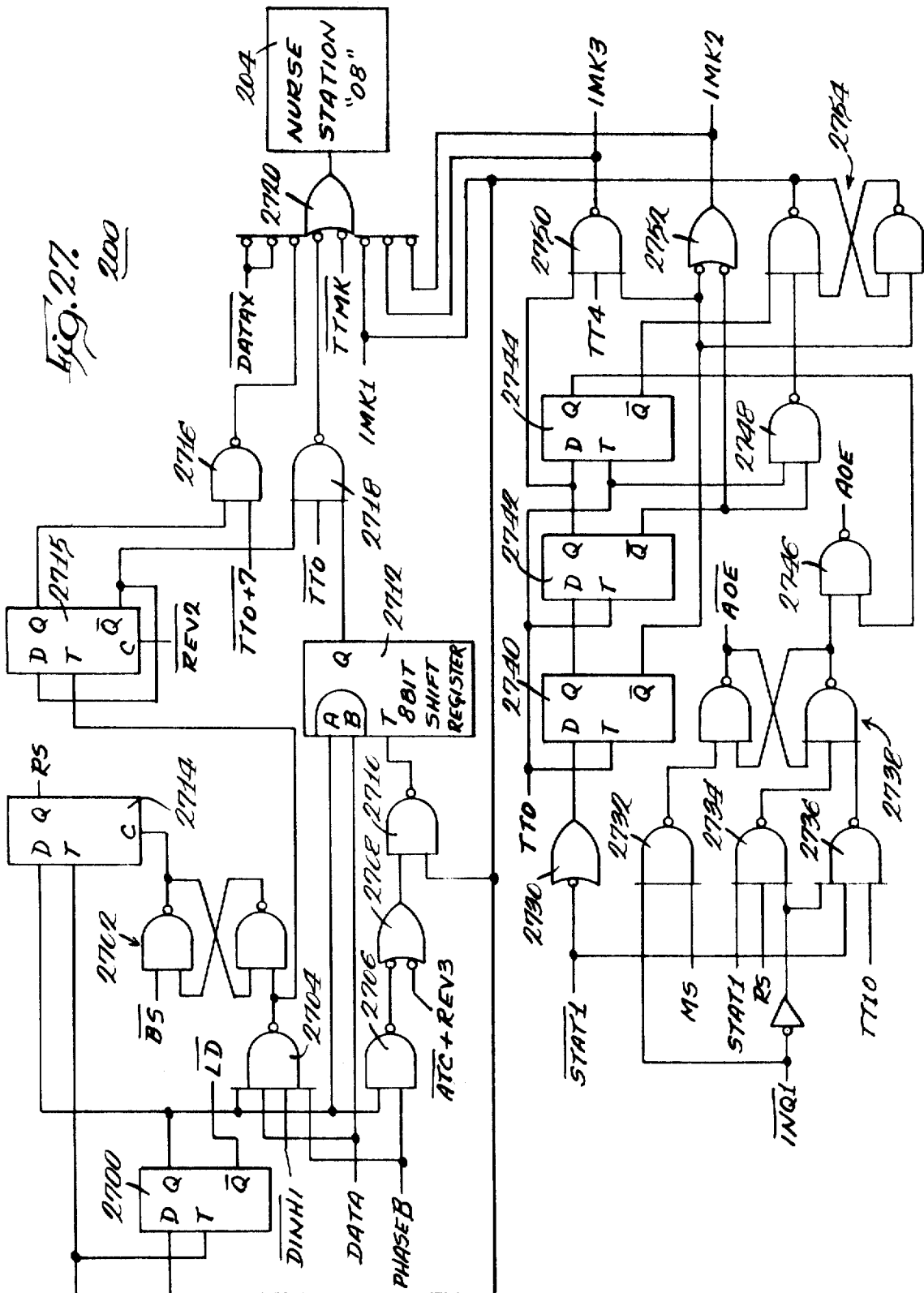
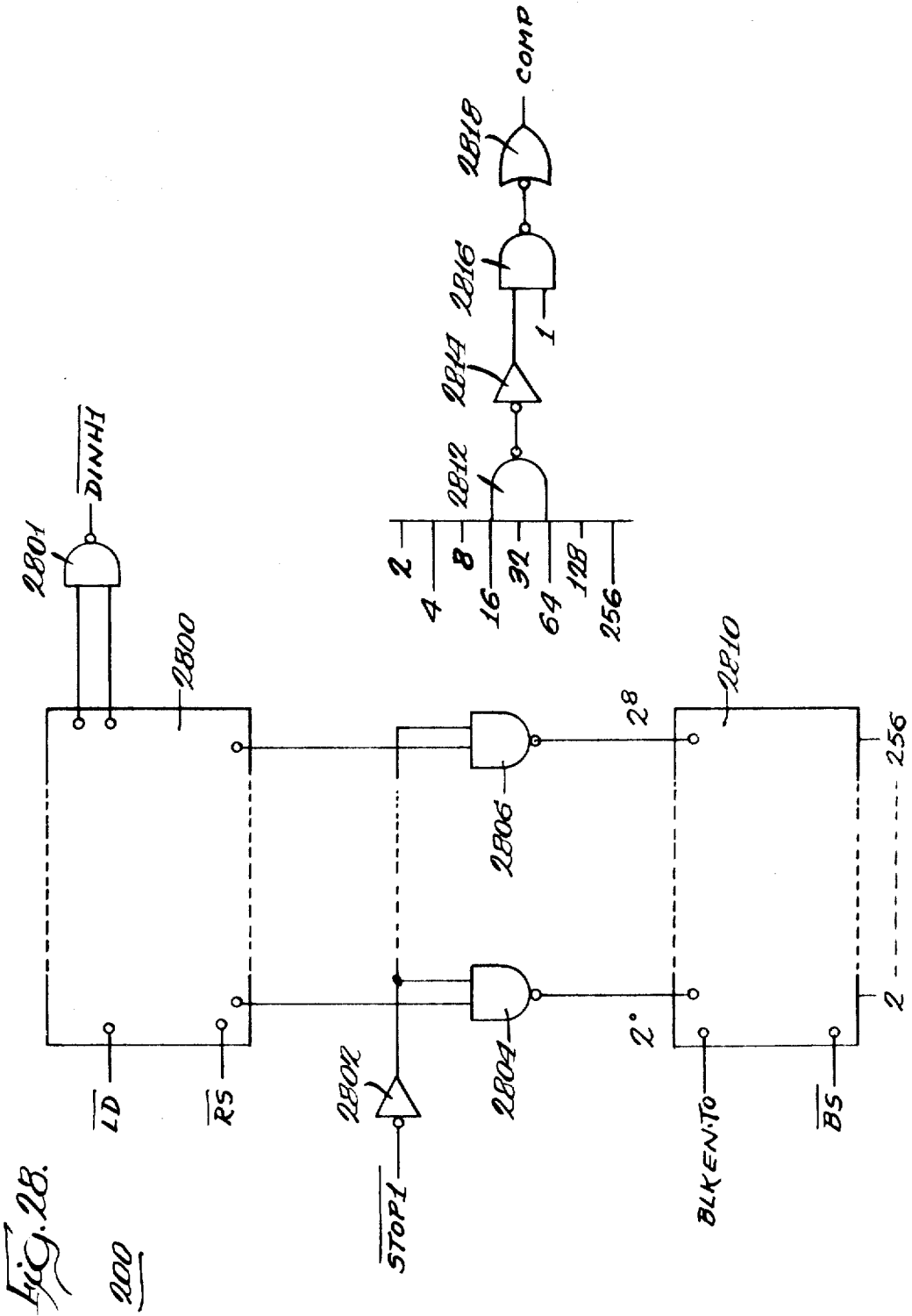


Fig. 28.



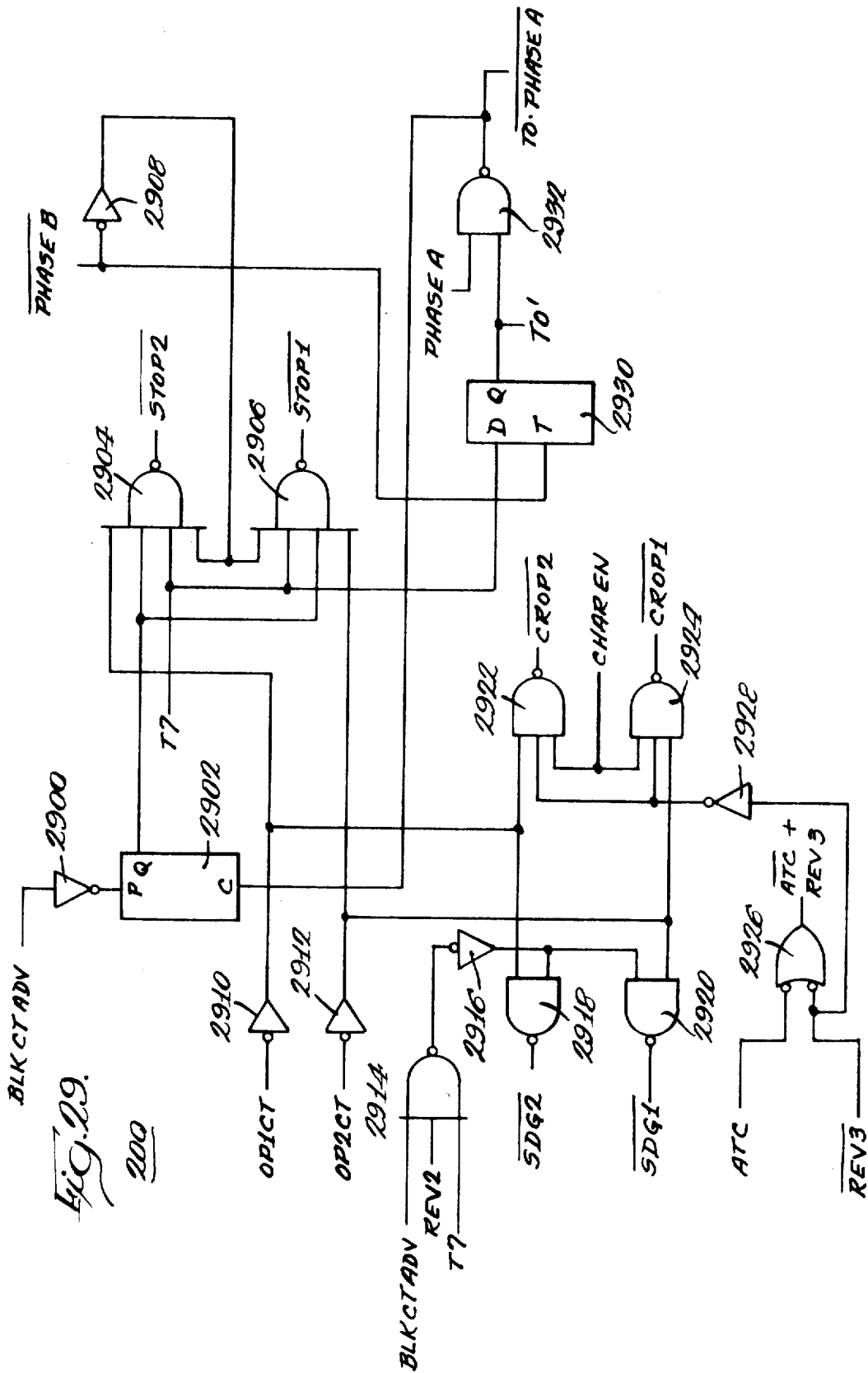
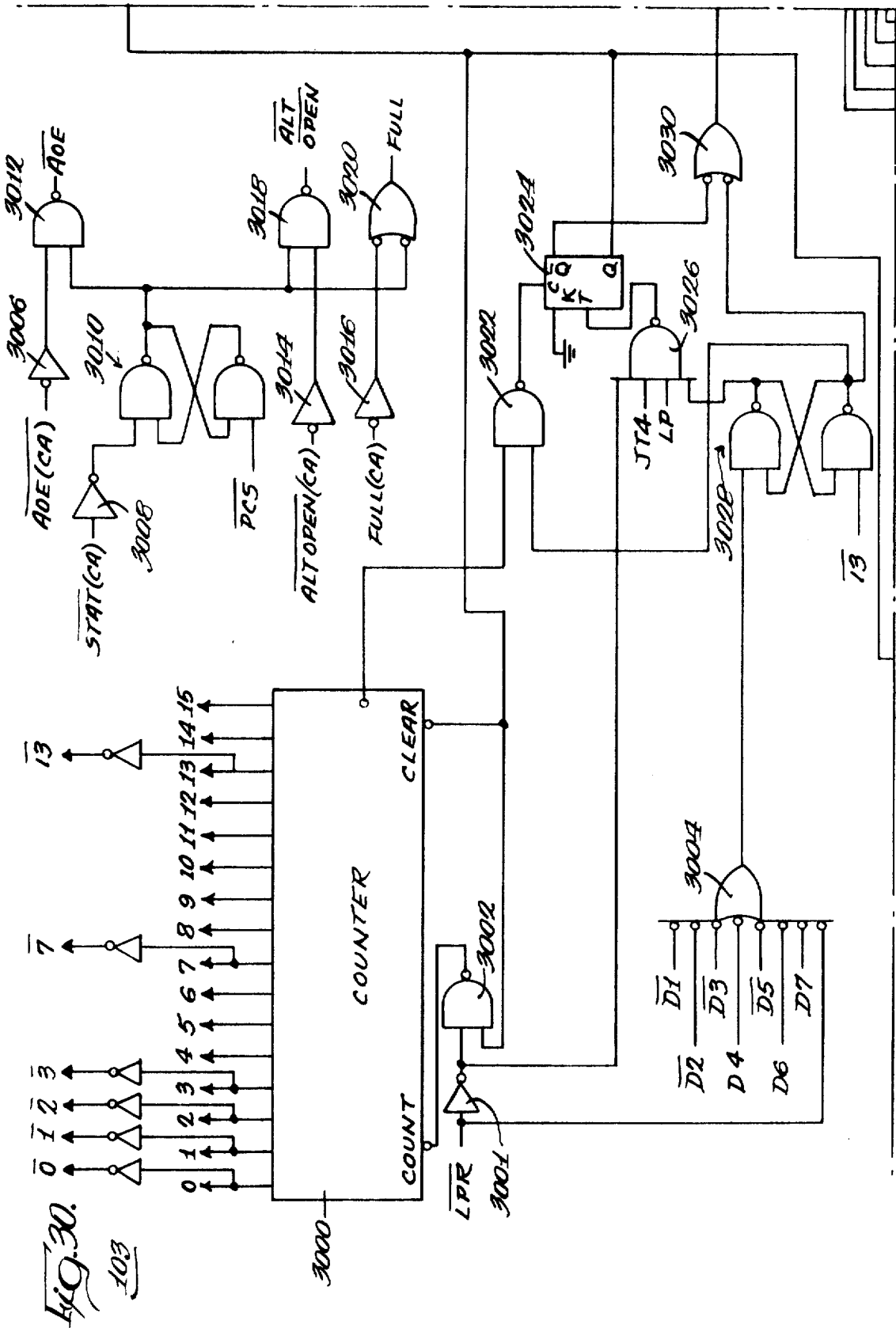
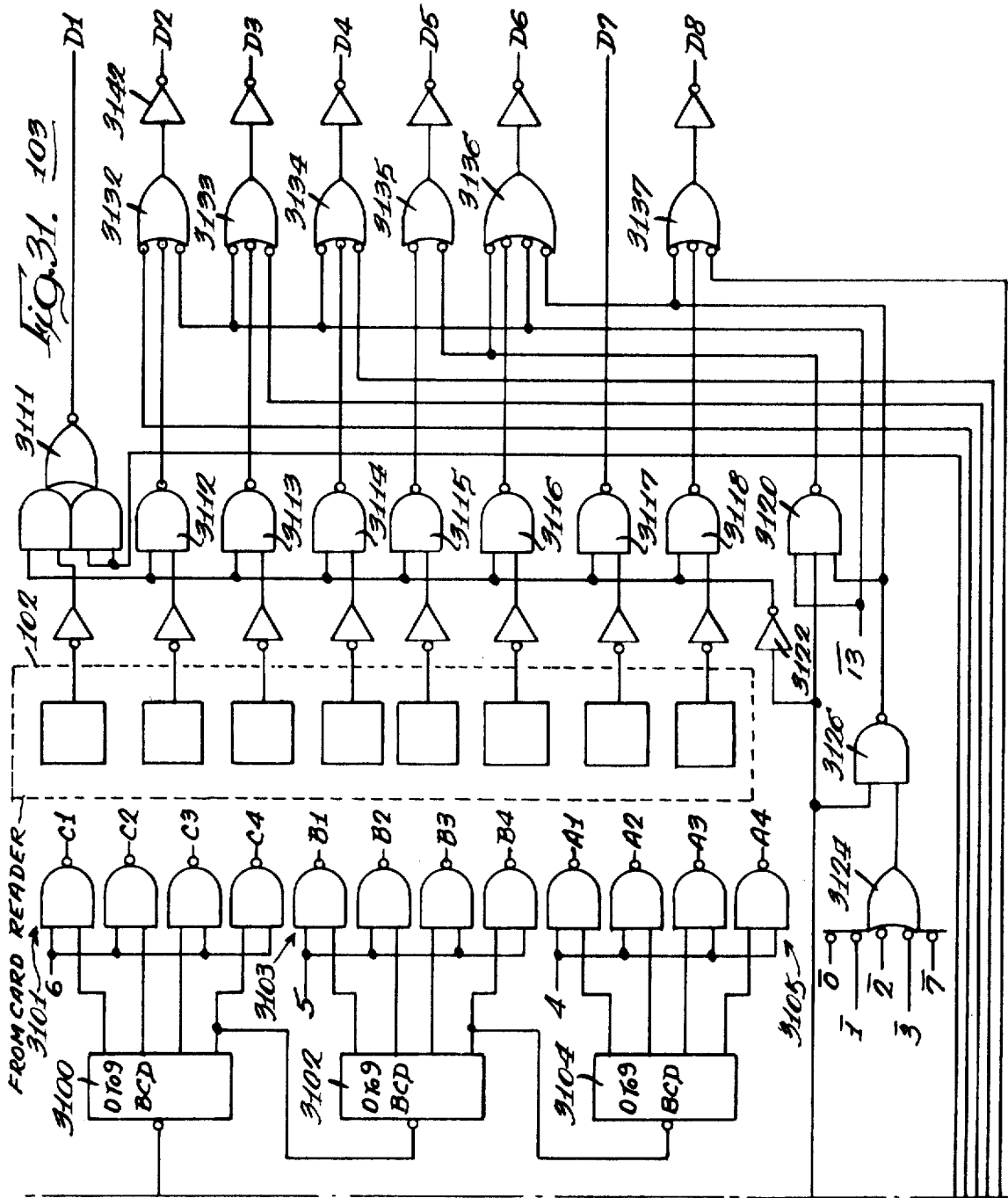
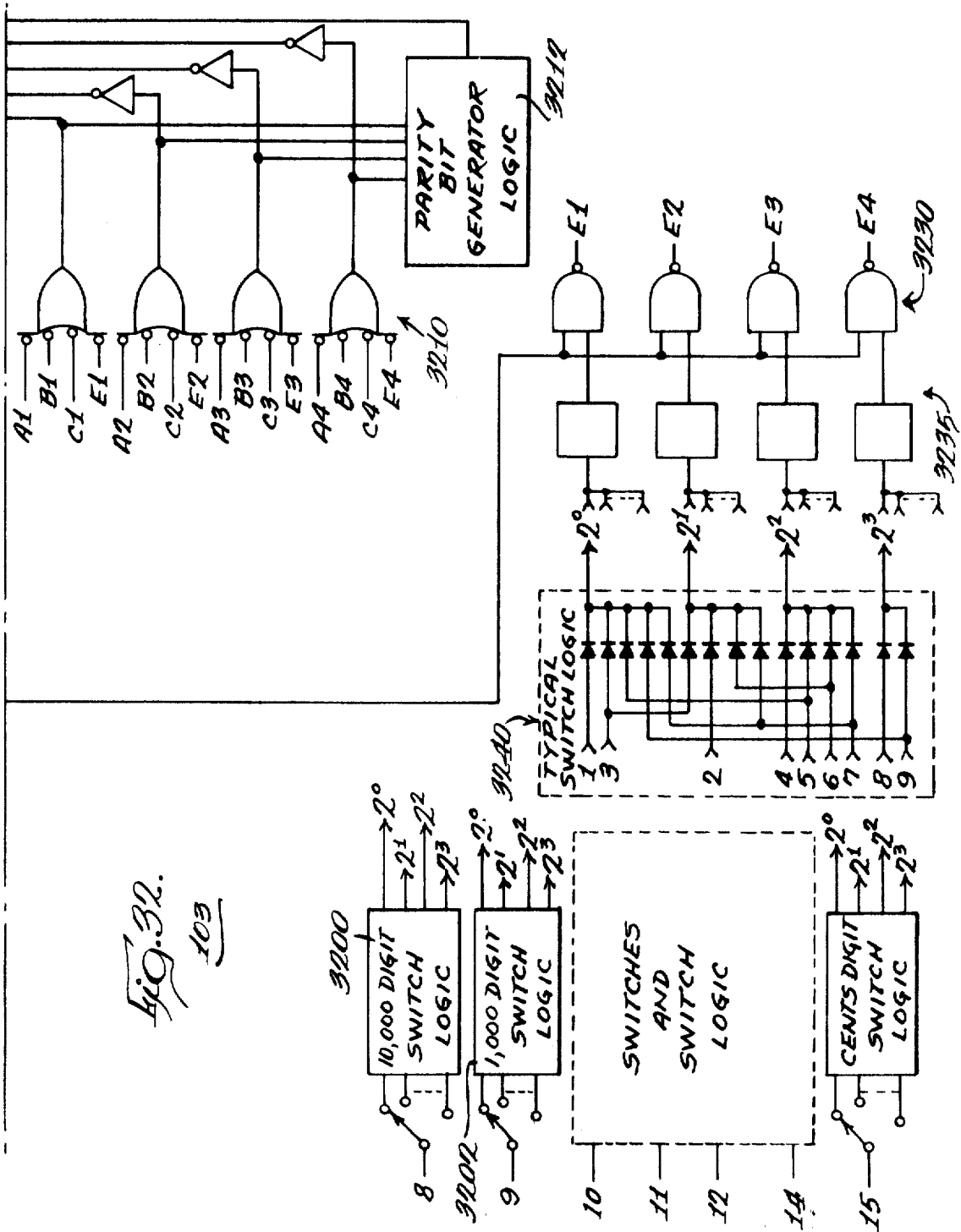


Fig. 29.

200







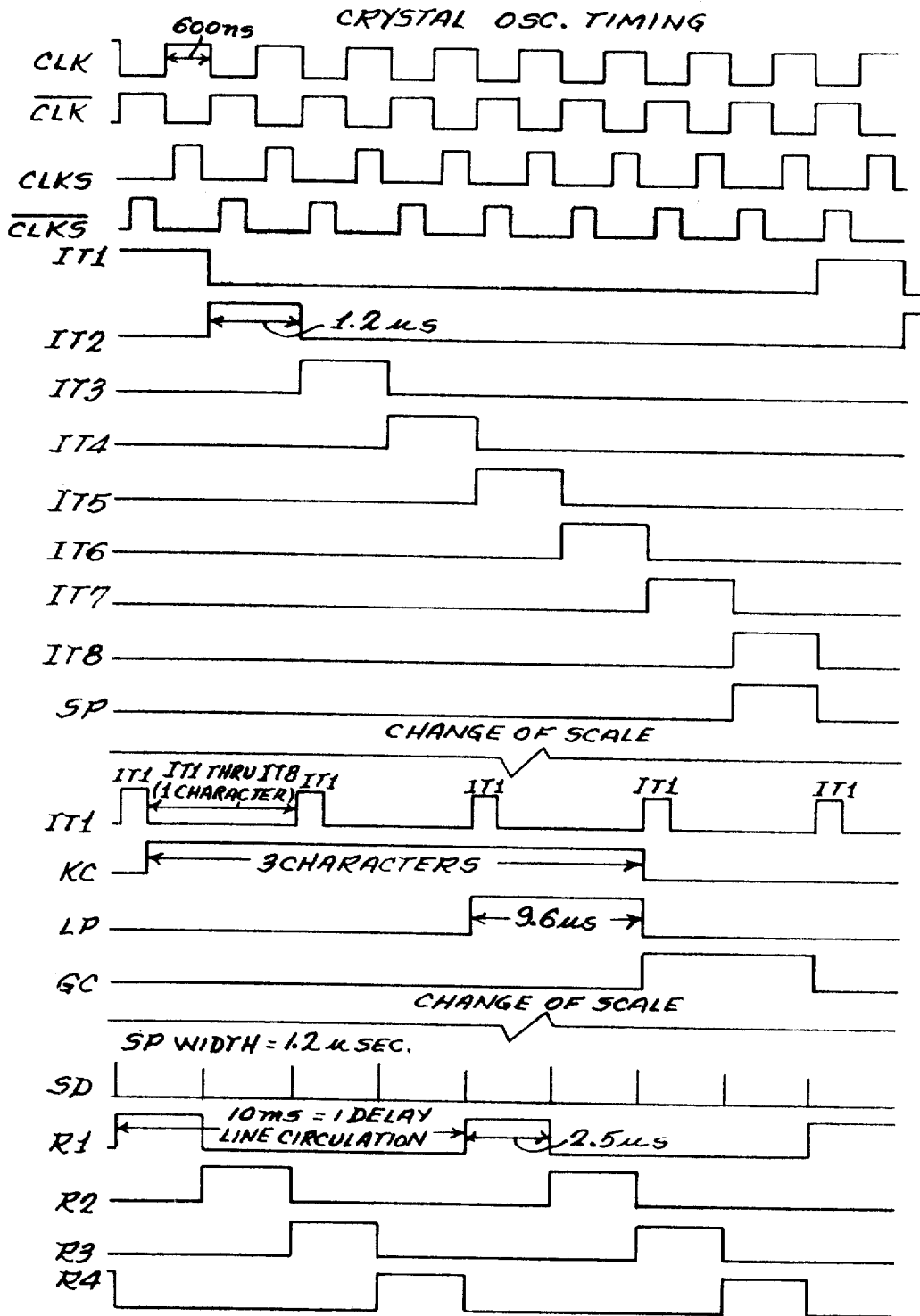


Fig. 33.

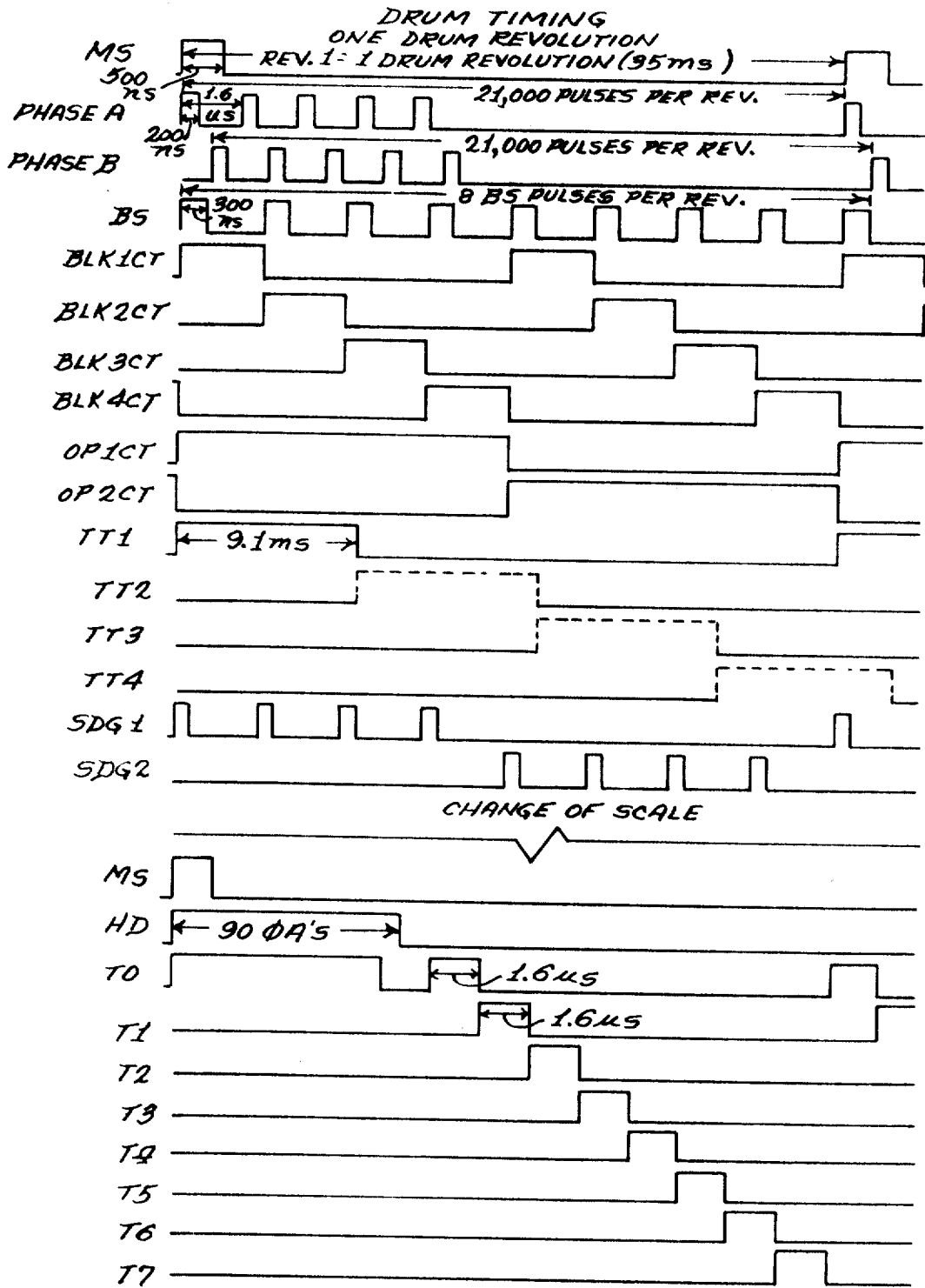


Fig. 3A.

CHANGE OF SCALE  
(3 DRUM REVOLUTIONS)

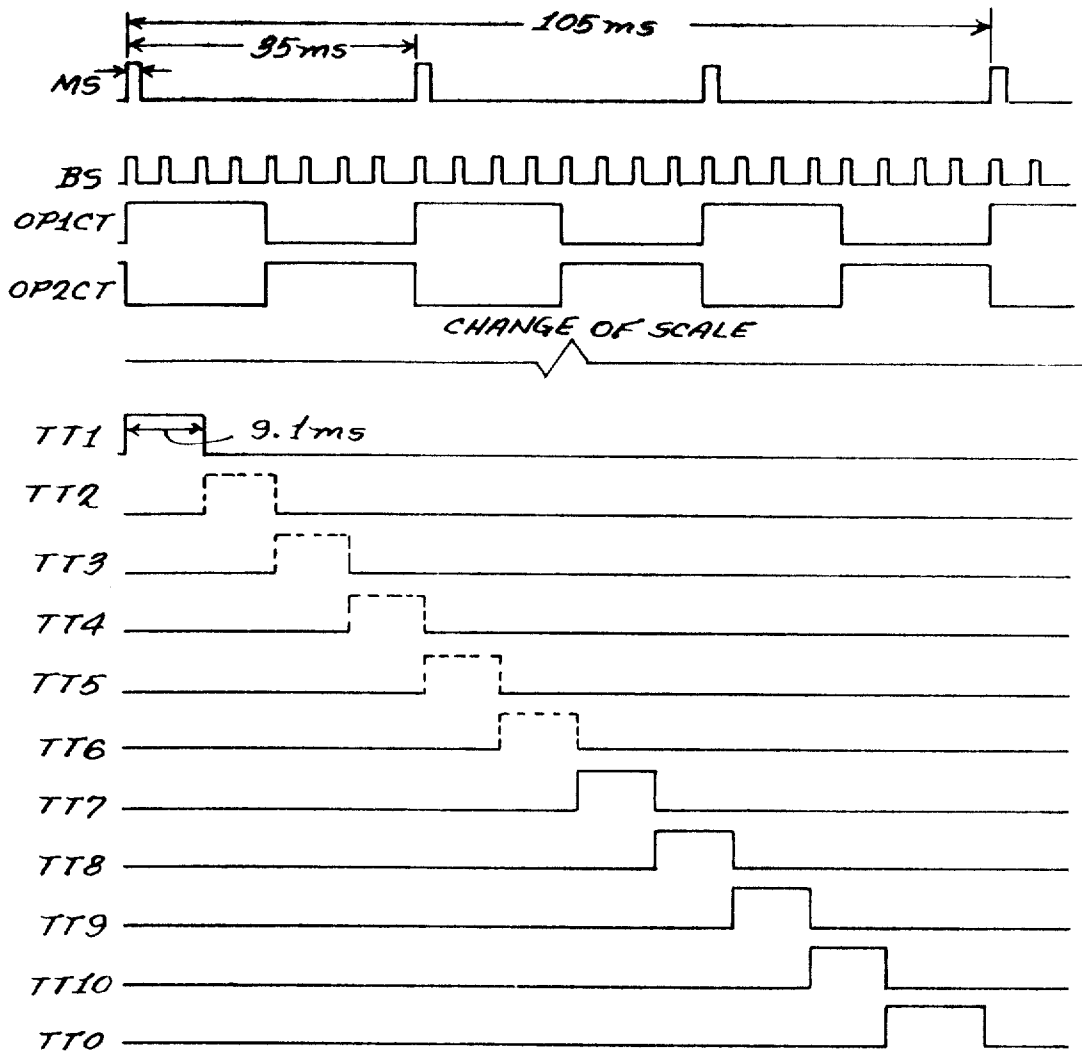


Fig. 35.

Fig. 36.

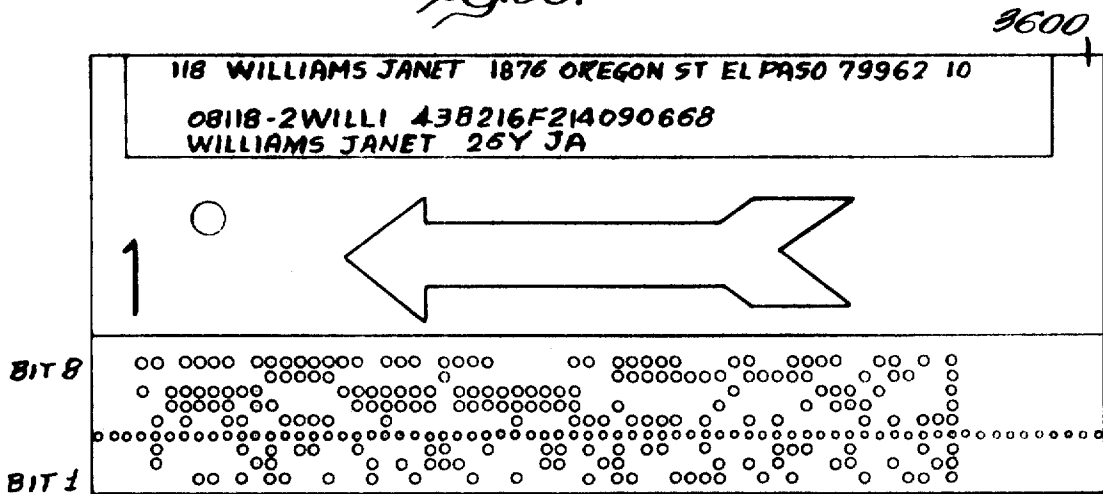
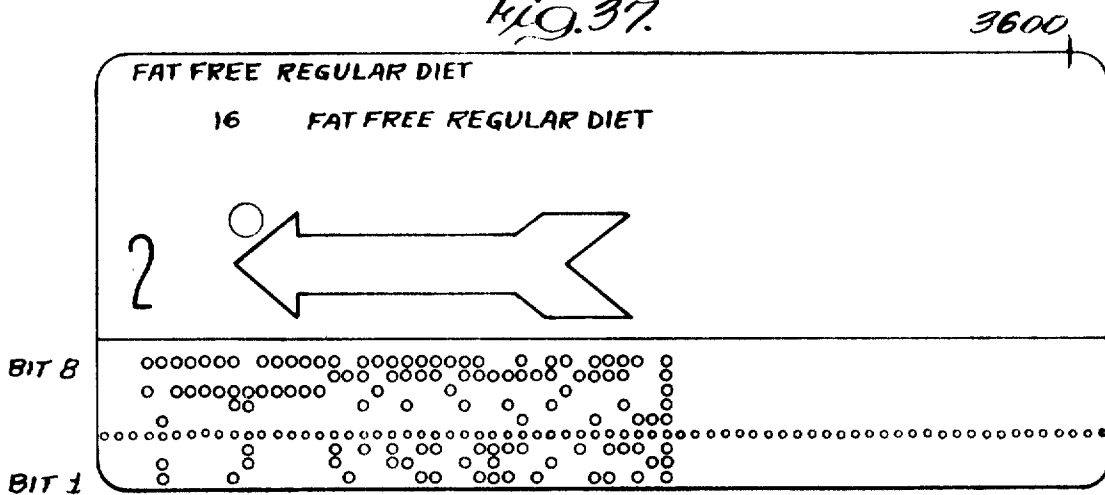


Fig. 37.



08 118-2 WILLI 438216 F 214 0906 68  
 WILLIAMS JANET 26Y JA  
 FAT FREE REGULAR DIET  
 054 9/ 6/68 10:45 PM

Fig. 38.

**DATA HANDLING SYSTEM**

**SUMMARY OF THE INVENTION**

**CROSS-REFERENCE TO RELATED APPLICATION**

The central data processor unit used with the system of this invention is disclosed and claimed in a contemporaneously filed application Ser. No. 761,042 of E. A. Stanis and L. E. Philipps, which application is assigned to the same assignee as the present application.

**TABLE OF CONTENTS**

Background of the invention.....	Col. 1
Summary of the invention.....	2
Brief description of the drawings.....	3
Description of the preferred embodiment.....	4
Introduction.....	4
Logic diagram and symbols.....	6
Timing signals.....	7
Typical card input and printout.....	8
Transfer of data from card reader to delay line through input control circuit.....	10
Transfer of data from the delay line to the core storage unit through the control circuit 114.....	16
Magnetic core storage unit, core address counter, output selector, and decoding circuit.....	19
1. Writing data from delay line into core storage unit.....	20
2. Output selector.....	23
3. Control code decoding.....	27
4. Error detection.....	28
Reading data out of the core storage unit using the control circuit 128.....	30
Output control circuit.....	36
1. Assigning block on drum and writing data from core storage unit into selected block.....	36
2. Transferring data from the drum to the output printer.....	38
Cashier's office.....	43

**BACKGROUND OF THE INVENTION**

This invention relates to a data handling and processing system and, more particularly, to a system for automatically collecting, compiling, and performing arithmetic operations on data such as data relating to hospital operations.

The operation of a hospital with even a small number of beds involves the preparation and transmission of a very large number of rather short messages relating to virtually every phase of hospital operation ranging from pharmacy orders, requests for laboratory tests, and admitting or discharging instructions to requests for repair of a broken window. In some hospitals, a written order is made only when the nature of the service demands it, and other functions such as maintenance or bed status are requested by oral communication. Further, many of the operations or items covered by the messages require a charge to be made frequently against several entities, e.g., inventory and a patient. These charges are collected either by using the primary written message or by making secondary records frequently in machine code based on a primary message.

However, the use of written orders and messages is time consuming, requires manual transmission or conveyance to perhaps a number of points of use, and is subject to error in preparation when read and translated to secondary records. The compilation and calculation of charges or inventory records requires the physical presence of all of the records, and it has been determined that errors arise not only from record loss but from charges entered for services requested that are not actually performed. The time involved in collecting and translating the records and messages frequently causes a delayed billing for charges not available on discharge and delays the submission of charges to other paying bodies such as insurance companies. Further, because of the time required by written messages, there is a temptation to use oral requests when the nature of the requested service or item does not demand a written record.

The data handling and processing system of the present invention does away with written messages and orders and insures the collection, calculation, and compilation of all charges on any desired periodic basis. Messages and charges are free of transmission errors and provide legible permanent copy for medical records. In addition, skilled hospital personnel are freed from time consuming clerical duties and from acting as messengers with the resultant increase in their availability for professional services.

In general, the system includes a central processing unit which receives data from and supplies data to a plurality of remote stations each located at a point from which messages or orders are normally received and to which this data is normally directed. Each remote station includes a data recorder such as a teleprinter and a data transmitter. The data transmitter comprises a card or record reader which is enabled for operation by the insertion and actuation of a key identifying the station operator such as a technician or nurse and which is adapted to send plural card messages to selected points. Each station includes prepared cards containing all of the message information normally required by the department and other cards individually identifying each patient. By inserting the cards forming a plural card message into the reader, the patient and requested service information is automatically transmitted to one or more points in the hospital as required for each service or message, and any data relating to charges or other data compilations is collected in storage in the central processing unit. During message transmission from the card or record reader, a digital signature identifying the key that enabled the card reader is automatically transmitted to identify the person responsible for originating the message. The system also includes special equipment at such locations as the business office and cashier's office, which include manual data entry means in addition to a card reader. The business office station also possesses controls by which periodic or daily charge, credit and payment totals, and specific or complete listings of patient charges, can be retrieved from the system and the system cleared of all data printed out.

The basic system organization includes a plurality of card readers, groups of which time-share different delay lines providing input buffers. The delay lines are scanned for complete messages to enable transfer of a complete message to a magnetic core storage unit. The data in core storage is then either transferred to a magnetic drum storage unit, or is transmitted to one or more of the remote stations, or both, depending upon the nature of the received information and the functions required to be performed on the data designated by control characters on each card. If the message requires nothing more than transmission to one or a group of stations, the data is transferred from the core storage unit to tracks on the drum which function as an output buffer, and then is delivered over output lines to the addressed stations. If the message relates to items such as chargeable services or reflects changes in the allocation or status of beds, the data from core storage is transferred to a bed information storage area or a charge information storage area on the drum, perhaps after processing in an arithmetic section which has access to the core storage unit.

The bed information storage area includes a storage location for each bed containing information of the patient occupying the bed, and also containing information as to the condition or status of the bed. This information is updated continuously with information transmitted into the system from the remote stations. The system includes bed information search logic for compiling listings of the information stored in this area, such as lists by nursing station of beds which need attention, lists by nursing station of beds which are in a particular status (available, occupied, etc.), lists of patients admitted on a particular day, and the like.

The charge information storage area includes numerous storage locations into each of which a record of a cash or inventory transaction can be placed. A complete record of each

individual charge against a patient, payment of account, and withdrawal from or addition to inventory is maintained. The system includes charge information searching logic for compiling listings of the information stored in this area, such as tally lists by department of changes in inventory, listings of charges allocable to a particular patient, and a complete breakdown of all charges by patient number. This latter list is called an all patient charges list, and is usually printed out at the end of the day just prior to the time when the record of that day's transaction is erased to make room for the next day's transactions. The tally inventory lists are by item number. A special tally arithmetic unit calculates the total quantity of each item debited or credited to the inventory of each department, so the tally lists are summarized and are not broken down into individual transactions.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Many other objects and advantages of the present invention will become apparent from considering the following detailed description in conjunction with the drawings in which:

FIGS. 1—3 form a block diagram of the data handling and processing system embodying the present invention;

FIGS. 4—10 disclose in logic schematic form a data input unit including a card reader and a control circuit for taking message data from the card reader, placing it in a delay line storage unit, and reading the data out of the delay line for transmission to a core storage unit,

FIGS. 11—17 disclose in logic schematic form a control circuit for writing data into the core storage unit and for performing decoding and output selection operations on the data supplied to the core storage unit;

FIGS. 18—22 disclose in block and logic schematic form the core storage unit, a core storage address counter, and a control circuit for reading data out of the core storage unit;

FIGS. 23 and 24 disclose in logic schematic form a circuit for converting data read out of the core storage unit from parallel to serial form;

FIGS. 25—29 disclose in logic schematic form a control circuit for supplying data to a storage drum and for transferring data from the drum to an output recorder;

FIGS. 30—32 form a logic diagram of a chashier's office forming an input to the system;

FIGS. 33—35 are timing diagrams of certain control and clock signals used in the system;

FIGS. 36 and 37 are illustrations of cards used to provide a data input to the system;

FIG. 38 is an illustration of a typical record produced by the system;

FIG. 39 is a block diagram illustrating the manner in which FIGS. 1—3 are placed adjacent each other to form a complete circuit diagram;

FIG. 40 is a block diagram illustrating the manner in which FIGS. 4—10 are placed adjacent each other to form a complete circuit diagram;

FIG. 41 is a block diagram illustrating the manner in which FIGS. 11—17 are placed adjacent each other to form a complete circuit diagram;

FIG. 42 is a block diagram illustrating the manner in which FIGS. 18—22 are placed adjacent each other to form a complete circuit diagram;

FIG. 43 is a block diagram illustrating the manner in which FIGS. 23 and 24 are placed adjacent each other to form a complete circuit diagram;

FIG. 44 is a block diagram illustrating the manner in which FIGS. 25—29 are placed adjacent each other to form a complete circuit diagram; and

FIG. 45 is a block diagram illustrating the manner in which FIGS. 30—32 are placed adjacent each other to form a complete circuit diagram.

#### DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now more specifically to FIGS. 1—3 of the drawings, therein is disclosed a block diagram of a system 100 embodying the present invention. The system 100 is capable of transmitting and receiving all of the communications, orders, and requests normally handled in a hospital and of automatically compiling and computing all necessary data relating to patient charges and the status of the beds in the hospital, as well as providing a running inventory control. To insure against the presence of errors, virtually all input messages are made by selecting records in machine readable code from a prepared supply thereof containing all of the messages and service requests normally required in a hospital. The patient information is derived from records prepared in machine readable code on admittance to the hospital.

Normal entry to the system is obtained through a card reader 102 which is supplied with two or more punchcards or permanent records containing patient identifying information, message information, and one or more control codes. Each of the card readers 102 is enabled by the actuation of a key individual to the operator or the person responsible for transmitting the message into the system 100. The actuation of this key appends a plural digit identifying designation to the message transmitted from each reader. A group of card readers 102 share a common delay line 110 which provides a buffer storage unit to which access is obtained through a control circuit 104. The delay line 110 is divided into a number of time slots equal to the number of card readers 102 having access to the delay line. When message data is to be loaded into the delay line 110, the control circuit 104 selects one of the card readers 102 to which it has access and transfers the information character by character into the delay line 110.

Message data stored in the delay line 110 is normally circulated through the shift register 106 and a gate 112. However, when new message information is to be added to the delay line 110, a gate 108 is enabled to bypass the shift register 106. This time shifts the message information a single character position and permits the new message material in the shift register 106 to be added to the delay line 110.

After a complete message has been stored in one of the time slots in the delay line 110, the gate 112 is selectively enabled under the control of an input core control circuit 114 which is common to a number of delay lines 110 to transfer a complete message character by character to an input shift register 116. When a complete character has been transferred from the delay line 110 to the shift register 116, it is transferred through a gate 118 to the input of a magnetic core storage unit 120. The control circuit 114 controls an address counter 126 to place each character from the shift register 116 in a predetermined address location in the storage unit 120.

As each message is shifted through the register 116 into the magnetic core storage unit 120, an output selector 122 examines the incoming message for address codes and performs one or a plurality of output selection operations to select one or a group of output controls 200 each individual to a single output such as a recorder or teleprinter 204. Each of the output control circuits 200 has access to a plurality of buffer storage blocks on a track of a magnetic drum 202 forming a part of a central processor unit consisting essentially of a charge information logic unit 250 and a bed information logic unit 300. If at least one of the buffer storage areas on the drum 202 of an addressed output control circuit is available, the output recorder 204 is considered idle or not as busy, and the magnetic core storage unit 120 is permitted to receive the entire message, and this message is erased from the delay line 110. Alternatively, if any one of the output control circuits 200 selected by the output selector 122 does not have available buffer storage space, the message is not stored in the unit 120 because it cannot be immediately processed, and the message is retained in the delay line 110 without erasure.

The system 100 also includes a decoder circuit 124 which also monitors the data supplied by the shift register 116 to the

magnetic core storage unit 120 in selected locations to detect and decode certain control codes that advise the system 100 of the nature of the operation to be performed on the incoming message information. The decoder circuit 124 supplies the decoded information to the charge information logic unit 250 and the bed information logic unit 300 to indicate the disposition to be made of the message information. If the message information requires processing or relates to the operations performed by the units 250 and 300 forming the central processor unit, this information is transferred out of the magnetic core storage unit 120 to the processor unit. Alternatively, if the message indicates that no operations on the data are to be performed, and it is to be supplied to an output recorder 204, an output control circuit 128 controls the address counter 126 to select the desired information and transfers this information through the circuit 128 to the output control circuit 200 with the timing required to write this information onto the buffer track of the drum 202 through conventional drum reading and writing electronics indicated generally as 207. The control circuit 200 selects an idle buffer block on the track for receiving the message information. Incident to this transfer, the output control circuit 200 enables a gate 205 so that date and time information from a date and time generator 206 can be added to the message. Further, by controlling the addresses primed into the counter 126, the output control circuit 200 can control the makeup and content of the message placed in storage on the drum. When a complete message has been stored on the drum 202, the output control circuit 200 reads the data character by character from the buffer storage block with drum timing and supplies this data through an output gate 211 with the timing required by the recorder 204 to control the recorder to produce an output message.

If the message stored in the core storage unit 120 requires processing by the central processor, this information is supplied through a charge information storage logic circuit 240 for storage on the tracks of the drum 202 assigned to the unit 250 or through a bed information storage logic circuit 310 for storage on the tracks of the drum 202 assigned to the unit 300. The patient charge and bed information is processed in the units 250 and 300 and transferred by a charge information printout control circuit 245 to the output control circuit 200 which is directly addressed by the circuit 245. This data does not go into buffer storage associated with the various control circuits 200, but is directly transferred to the output recorder. If desirable or necessary, the selected output control circuits 200 can enable the gate 208 to add date and time information to the message supplied from the units 250 and 300 under the control of the control circuits 245.

The units 250 and 300 which comprise the central processor unit perform a variety of operations on the message data such as automatically establishing charges, maintaining inventory control, providing lists of various types, providing a current indication of the status of each bed in the hospital. The central processor unit is shown and described in detail in the contemporaneously filed Stanis et al. application.

A cashier's office 103 and a business office 305 are equipped with special inputs to the system 100 that may or may not be associated with a card reader 102. The business office 305 can initiate requests for totals of charges and control the erasure of information from the drum 202. The business office 305 can also initiate a search for the room location of a patient by admission date, or by code number, and inventory searches for all items received and distributed by a particular department. These searches are initiated by pushbutton, and some by card reader. The cashier's office includes a facility for manually adding a record of payments on account to the data assembled by the cashier's office card reader, and also is able to obtain an up to date listing of all charges allocable to a particular patient so that departing patients can be presented with a completely updated statement at the time of their departure. The admitting office (not shown) is able to obtain special listings of available beds in a specified nursing station as an aid in assigning new patients to available beds.

At the request of individual nursing stations, a list of all beds requiring service or attention can be compiled. This listing is requested by card reader, and is printed out at the nursing station that requested the list.

An arithmetic unit (not shown), associated with the magnetic core unit 120, is used to carry out arithmetic manipulation of input data, and also to keep a running total of each day's charges, credits, and payments on account.

This arithmetic unit has access to the magnetic core storage unit 120 and uses the core storage unit 120 as a source of data. The details of the arithmetic unit are set forth in detail in the above identified Stanis et al. application

## LOGIC DIAGRAMS AND SYMBOLS

In accordance with the preferred practice of electronic circuit designers, the details of the system 100 are represented by logic diagrams rather than by circuit diagrams. In physically constructing the system 100, each logic element shown is replaced by an equivalent electrical circuit that performs the logical task defined by the logic element. The use of logic elements emphasizes that any of the many differing electrical circuits capable of performing a logical task may be used in constructing the present invention.

To facilitate locating the various elements used in the system, the hundreds or thousands and hundreds digit of each reference number assigned to each element designates the Figure of the drawing on which the element is located or was first identified. As an example, a NAND gate 602 appears on FIG. 6. As an additional example, a delay line identified as 110 in the block diagram of FIG. 1 is similarly identified in the detailed logic diagram appearing in FIG. 8.

In the system 100, a high level or more positive potential normally represents a "1," "TRUE," or "PRESENT" signal, and a low level or more negative potential normally represents a "0," "FALSE," or "ABSENT" signal. Throughout this specification, the names of signals are written entirely in capitals. As an example, a store core inhibit signal generated in FIG. 9 is designated as "SCINH." Signals are often encountered in an inverted form. This is indicated in the drawings by an overline or bar drawn over the signal name. As an example, the inverted store core inhibit signal "SCINH" also appears in FIG. 9 as  $\overline{\text{SCINH}}$ . In this specification, this inversion is indicated by placing the word "inverted" before the name of the signal. In this case of an inverted signal, a low level potential represents a "1," "TRUE," or "PRESENT" signal, and a high level potential represents a "0," "FALSE," or "ABSENT" signal.

The preferred embodiment of the system 100 is constructed almost entirely from transistor-transistor integrated circuit logic elements manufactured by Texas Instruments Incorporated, of Houston, Texas. The fundamental element in the transistor-transistor logic system is the NAND gate, such as a NAND gate 602 shown in FIG. 6. The NAND gate 602 has two inputs into and a single output from the D-shaped figure which is used as the standard logic symbol for a NAND gate in this description. The circle separating the D-shaped figure from the output lead signifies an inversion of the output signal. The output lead from this unit is high or at a more positive potential at all times except when all of the inputs are at a high or more positive potential at which time the output drops to a more negative or low potential.

Inverters (NOT gates) are represented by a triangular amplifier symbol with a circle at the input or output lead to indicate inversion. These are conveniently formed from NAND gates having their inputs wired together in parallel. An example of an inverter is an inverter 604 in FIG. 6.

A typical AND-NOR device 720 is shown in FIG. 7. This device includes a series of two input AND gates, the outputs of which are fed into a NOR gate. The output of this device is normally high or positive. It goes to a low level whenever both of the inputs to any one of the AND gates are at a high level.

A typical NOR gate 640 is shown in FIG. 6. The output of the NOR gate 640 is low or negative if and only if both of the input leads are at a high or more positive potential. If either of the input leads is at a low level, the output rises to a high level potential.

Two general types of flip-flops are used in the system 100. The first type is constructed by cross-connecting the outputs of two NAND gates with one input of each of the gates. A typical example is a flip-flop 622 in FIG. 6 constructed from two cross-connected NAND gates.

The second general type of flip-flop is provided by a D-type flip-flop or a JK flip-flop, such as a flip-flop 636 shown in FIG. 6. The JK flip-flops can have up to seven leads or terminals J, K, T, C, P, Q, and  $\bar{Q}$ . These designations appear in the rectangular block of the logic symbol only when they are used in the circuit but have all been applied to the symbol for the flip-flop 636 as an illustration.

When a clock or toggle input T of the JK flip-flop is at a high potential, data applied to the J and K input terminals is stored. When the clock lead T goes negative, this data is transferred to the Q and  $\bar{Q}$  outputs and becomes the flip-flop output. When both of the J and K terminals are either open circuited or connected to a high level signal, the flip-flop toggles or reverses the state of the Q and  $\bar{Q}$  terminals whenever the clock input T goes from positive to negative. If both of the J and K terminals are connected to a low level potential, the flip-flop remains in its prior state when the T input goes negative and does not toggle. When a prime or clear terminal is included in a flip-flop, the flip-flop may be set directly to a desired state. A flip-flop is cleared by applying a low level signal to the C terminal to cause a more positive potential to appear at the  $\bar{Q}$  output and a low level signal to appear at the Q output. A flip-flop is set or primed by applying a low level signal to the P terminal to cause a high level signal to appear at the Q terminal and a low level signal to appear at the  $\bar{Q}$  terminal.

The internal circuitry of the individual logic elements is not relevant to the present invention and is therefore not disclosed in the present application. Chapter 11 of the book *Integrated Circuit Engineering-Basic Technology*, Fourth Edition, by the staff of Integrated Circuit Engineering Corporation, Glen R. Mudland et al., published in 1966 by Boston Technical Publisher Incorporated, Cambridge, Massachusetts, gives a rather complete explanation of digital integrated circuits suitable for use in the system 100. Additional background on the use of logic diagrams and integrated circuits can be found on pages 149 through 162 of *Electronics*, Vol. 40, No. 5, March 6, 1967.

#### TIMING SIGNALS

The system 100 in general operates off of two sets of synchronized timing signals which are asynchronous with respect to each other. The first set of timing signals are those used to control the input of data from the card readers 102 through the delay lines 110 to the core storage unit 120 (see FIG. 33), and the second set are those used in feeding data into and out of the drum 202 and in supplying output signals to the printers 204 (see FIGS. 34 and 35). These signals are developed by standard components and circuits, and the circuitry for obtaining these signals is not illustrated or described.

The input timing signals shown in FIG. 33 are related to the circulation time of the delay line 110 and are, for example, easily developed using a crystal controlled oscillator driving a group of frequency dividing counters. The delay lines have a circulation time of the order of 10 ms. which is time divided into four separate segments or sectors of 2.5 ms. shown as R1, R2, R3, and R4. Each of these sectors or segments in the delay line is assigned to a single card reader to receive and store a message of no more than 246 characters each comprising eight bits.

To provide character bit timing, the clock circuit develops a series of character bit timing pulses or signals IT1—IT8 each

having a duration on the order of 1.2  $\mu$ sec. An additional control pulse SP is generated concurrent with the eighth bit timing pulse IT8. Each slot or segment defined by the signals R1—R4 includes at its beginning a guard character signal GC of a 9.6  $\mu$ sec. duration corresponding to one character interval. Each segment is also terminated by a KC signal of three characters duration appearing in the 244th 245th and 246th character positions and a load pulse or LP signal of one character duration occurring at the very end of the slot or segment in the 246th character position.

The bit timing signals IT1—IT8 are developed from a clock signal CLK developed in the clocking circuit. These circuits also supply a secondary signal CLKS of the same periodicity as the clock signal CLK but of a duration shorter than the 600 nsec. duration of the positive-going half of the clock signal CLK. An inverted secondary clock signal CLKS symmetric with the inverted clock signal CLK is also provided.

The drum or output timing waveforms are shown in FIGS. 34 and 35 of the drawings and are derived from a clock or timing track or a plurality thereof on the drum 202. The signal is shown on the first four lines of FIG. 34 of the duration and periodicity indicated thereon. The signals BS appear at the beginning of each block on a drum track. The next four signals BLK1CT, BLK2CT, BLK3CT, and BLK4CT define four blocks or segments on a track on the drum occurring twice during a drum revolution. When combined with the next two signals, i.e., OPICT and OP2CT, these six signals effectively define eight separate blocks or segments on each drum track. The SDG1 and SDG2 signals are developed using the OPICT, OP2CT signals and the signal BS during the second revolution of a three revolution drum cycle.

The timing signals T0—T7 are used for timing bit operations with respect to the drum and have a width of 1.6  $\mu$ sec. with a repetition rate of 12.8  $\mu$ sec. In the illustration, the initial positive-going portion of the T0 signal arises from the adjacent head delay signal HD and does not recur after the drum is placed in operation. The signals TT1—TT10 and TT0 are of 9.1 msec. duration and are used to clock and control the output of signals to the output printer.

#### TYPICAL CARD INPUT AND PRINTOUT

Two typical cards 3600 which can be applied to the card reader 102 to provide an input message to the system 100 are shown in FIGS. 36 and 37 of the drawings, and a typical or representative message provided at an output printer 204 from the two cards 3600 shown in FIGS. 36 and 37 is illustrated in FIG. 38. The insertion of the two cards 3600 into the card reader at nursing station "08" causes the message shown in FIG. 38 to be printed at the output printers at the originating nursing station which is assumed to be designated "08" and in the diet kitchen which is assumed to be designated as output "16."

In general, a message from a card reader can include two, three, or four cards containing no more than a total of 243 characters to which are added three characters from the key inserted in the card reader to identify the operator. Each of the cards in the message contains as a first significant character, a control character designating the type of operation or function to which the card of the message on the card relates. The various types of cards for which the system 100 is designed for use include the following:

1. control N—patient, bed, or nursing station number, in-patient, out-patient, or out of the hospital person
2. control R—charge card
3. controls R & W—paid on account card and correction to paid on account card
4. control V—bed status card which may include secondary control D, S, or P characters signifying new admission to bed, patient discharged from bed, or miscellaneous bed status information such as maid working or out of service. The control D, S, and P characters if present appear in 15th information character on card.
5. control Q—reserve or cancel reserve information

6. control U—request for list of items. This card may include a secondary control character in the 17th position specifying the nature of the list required.
7. control K—diet order card, maintenance order card, single card message, lab results, X-ray results
8. control F—quantity or frequency of administration
9. control T—credit for service card or return for credit card
10. control E—message card

Using the above types of cards, there are three proper two card combinations, one proper three card combination, and one proper four card combination. A proper two card message affecting bed information would include an N card and either a Q card or a V card. A valid two card message affecting charge information would include an N card and either an R card or an R & W card. With this message, one or two control E cards which are message cards can be added. The third proper two card message relays the transmission of information only and includes an N card and a K card to which one or two control E cards may be added. A proper three card combination includes an N card and an R card and either an F card or a T card. With this three card message, a fourth message or control E card may be added. A proper four card message includes an N card and an R card and an F card and a T card. In addition, the system will accept a message consisting of a single card bearing the information normally carried on two or more cards if the format and sequence of data on the single card is that of the individual cards.

To illustrate the operation of the system 100, it is assumed that the diet kitchen at output station 16 is to be advised that Janet Williams a patient in room 118, bed 2, located at nursing station "08" is to be provided with a fat-free regular diet. Since this involves only the transmission of information and does not affect charges or bed status, the cards necessary to perform the operation include only a control N card which is a card in every message and a control K card.

FIG. 36 of the drawings illustrates a control N card relating to the patient Janet Williams which is prepared on admission and stored at nursing station "08." The top printed line of the card includes the patient's room number "118" followed by the patient's name, address, and miscellaneous information. This printed information facilitates the selection of the card for use in the reader. The second and third printed lines are a printed record of significant or selected portions of the information stored in coded form along the lower edge of the card.

More specifically, the second printed line includes the digits "08" identifying the nursing station involved, and the following digits "118-2" designate the patient occupies bed 2 in room 118. The following information "WILLI 438216" is the patient identification insofar as the data processing system is concerned. The next character "F" indicates that the patient is female. The next three characters "214" form a numerical designation of the attending physician. The remaining digits "090668" specify the month, day, and year of some reference date such as the date of admission.

With respect to the third printed line, this information is contained in the message portion of the card and comprises the full name of the patient and any additional information expressed in code such as the religious preference of the patient.

Referring now more specifically to the coded portion of the record shown in FIG. 36 contained along the lower edge thereof, these records are coded in ASCII code in which the lower line of perforations represents bit "1" and the upper line of perforations represents bit position 8. Each card must begin with a space code consisting of perforations in the sixth and eighth bit levels, and the second character on each card is a control character. Since the card shown in FIG. 36 is a control N card, the perforations representing mark conditions are present in the second, third, and fourth bit positions. The eighth bit position is used to provide even parity, and thus a perforation is provided in the eighth bit position for the control N character. The next 29 characters comprise the information contained in the second printed line on the card including a space code between the "I" in "WILLI" and the "4"

in the remainder of the line. Following these characters, a carriage return code and a line feed code are provided. The remaining characters are a coded representation of the third line of the printed message including the indicated spaces, and the message terminates with a carriage return, a line feed, and a code delete or "RUB OUT" code comprising perforations in all eight bit positions.

The second card of the illustrative message comprises a control K card which is illustrated in FIG. 37. The top printed line is provided to facilitate selection of the card containing the desired message, and a second printed line contains the station to which the message is to be directed together with the complete test of the message. In the coded portions appearing along the lower edge of the card, the first character comprises the required space code, and the second character comprises the required control character, in this case a control K. The next 10 characters are provided to select up to five 2-digit stations. Since only one station is to be selected, space codes fill this area of the card except for the two characters providing a coded representation of the diet kitchen designation "16." The remainder of the card consists of the printed message shown in the second line of the card, and the card is terminated with a carriage return code, a line feed code, and a delete code.

the message produced by feeding the cards shown in FIGS. 36 and 37 into the system 100 is shown in FIG. 38. This message is produced at both the nursing station "08" at which the message originated and at the diet kitchen station "16." The first line of the printed message includes the second printed line of information from the card shown in FIG. 36 with spaces inserted by a format generator in the system 100. The second line of the printed message shown in FIG. 38 includes the information shown in the third printed line on the card illustrated in FIG. 36. The third line of the message includes data from the second printed line on the card shown in FIG. 37 with the station designation "16" omitted.

The last line of the message shown in FIG. 38 includes the numerical designation "054" which is appended to the message transmitted at the station "08" and which was derived from the key number of the nurse or other operator placing the message. The remaining portion of the fourth line of the message is generated by the date and time generator 206 in the system 100.

#### Transfer of Data From Card Reader 102 to Delay

##### Line 110 Through Input Control Circuit 104

Assuming that the message including the two cards shown in FIGS. 36 and 37 is to be transmitted through the system 100, these two cards are placed in the card reader 102 (FIG. 4) at nursing station "08," and the nurse who is assumed to be identified by the designation "054" inserts her key into the card reader 102. This key can either comprise a perforated record or badge or can comprise a key or more or less conventional appearance, the coded profile of which selectively presents the assigned digital designation. When the key is inserted into the reader 102, a pair of normally open contacts 425 are closed, and four groups of normally closed contacts 410 and 420—423 are selectively actuated to provide a coded representation of the designation "054."

More specifically, the contact group 410 includes three normally closed contacts 411—413 representing the binary weight "1" in the units, tens, and hundreds denominations. With the assumed nurse designation, the contacts 411 and 413 would be opened indicating an absence of a "1" bit in the units and hundreds denominations, and the contacts 412 would remain closed representing the presence of a binary weight "1" in the tens denomination. The contact groups 420—422 are similarly actuated in accordance with a coded representation of the operator's identifying number. The contacts in the group 423 are selectively actuated to provide even parity. A group 424 of three diodes selectively provides the "5" bit required of all numbers in the ASCII code.

To initiate the card reading operation, the operator actuates a switch 440 to close a pair of normally open contacts 441 and to open a pair of normally closed contacts 442. The opening of the contacts 442 interrupts the operating circuit for a normally operated relay 520 in a group 510 of input relays 511—520 in an interface circuit 500 to supply control data from the card reader 102 to the input control circuit 104. The release of the relay 520 opens a pair of normally closed contacts 520A to remove a negative potential which is supplied through a pulse shaping circuit 623 to one input of a flip-flop 622. The status of the flip-flop 622 in the control circuit 104 is not changed at this time, but this flip-flop is freed for subsequent control.

The closure of the contacts 441 forwards ground potential from a card reader control circuit 501 through the normally closed contacts 425 and a pair of normally closed contacts RB2 to complete an operating circuit for a relay RC. The operation of the relay RC closes a pair of normally open contacts RC1 to connect a read lamp 430 in the card reader 102 to a source of potential in the control circuit 501. This provides a source of illumination for photoelectrically reading the perforated card 3600. The ground signal forwarded through the closed contacts 425 is also forwarded to the control circuit 501 to energize a drive motor for advancing the perforated cards through the card reader 102 during which they are photoelectrically sensed.

More specifically, as the cards move through the card reader 102, each successive transversely extending line of perforations is photoelectrically scanned in a conventional photoelectric scanner unit 450 to provide a more positive potential at each of the numbered terminals on the unit 450 corresponding to a bit position at which a perforation or mark signal is present. As an example, the space code which is the first item sensed on the control N card includes perforations in the sixth and eighth bit positions, and positive signals are applied to the sixth and eighth terminals by the reader 450. This reader also sensed the line of sprocket holes in the card shown in FIGS. 36 and 37 intermediate the third and fourth bit positions and thus supplies a positive gating signal at a sprocket terminal SPKT for each character read.

The positive signals provided at the output of the photoelectric sensing unit 450 are selectively applied to the operating windings of the bit output relays 511—518 and the winding of the sprocket relay 519. These relays close corresponding contacts 511A—519A. The contacts 511A—518A are connected over a cable 540 to the corresponding set terminals of eight flip-flops or bistables 671—675 and 776—778 forming an input register 670. Since the first code read by the card reader 102 is a space code, the contacts 516A and 518A are closed to apply a more negative or low level potential to the set terminals of the flip-flops 776 and 778.

When the contacts 519A are closed representing the presence of a sprocket pulse, a more negative potential is applied through a pulse shaping and delay network 644 to provide a positive-going pulse at the output of a gate 642. This pulse is inverted in an inverter 646, the output of which is connected to the reset terminals of all of the flip-flops 671—675 and 776—778. This pulse resets the register 670 to a normal state, and at the trailing edge of this pulse the clamp is removed from the flip-flops in the register 670 to permit these flip-flops to be set in accordance with the input signal. Since the input signal is a space code, the flip-flops 776 and 778 are set, and the remaining flip-flops in the register 670 remain in a reset condition.

A gate 660 is provided for decoding the receipt of a space code and provides a more negative signal at its output in response to the received space code which is inverted in an inverter 652 and applied to one input of a gate 650. The circuit 644 supplies a second enabling input at this time so that the output of the gate 650 drops to a more negative potential to set a flip-flop 648 to a condition in which a more negative potential is applied to one input of the gate 640, the output of which is connected to the J input of a flip-flop 710. Thus, when the trailing negative-going edge of the pulse from the

gate 642 is applied to the clock terminal of the flip-flop 710, this flip-flop is set so that a more positive potential is applied at its Q output. This enables one input to a gate 712.

If it is assumed that the card reader 102 is assigned the first time slot of the time slot defined by R1 timing in the associated delay line 110, the other input to the gate 712 is enabled by the R4 signal so that during this interval the gate 712 is effective through the inverter 714 to apply a more positive potential to the J terminal of a flip-flop 718. During the last character interval of the R4 signal at the termination thereof which effectively terminates a fourth time slot, the trailing edge of an LP signal applied to the clock terminal of the flip-flop 718 sets this flip-flop to a condition in which a more positive potential is applied to its Q terminal to develop an LE or load enable signal. This signal is returned to the K input of the flip-flop 718 as well as to one input of each of three gates 724, 728, and 730. The signal LE is used to control the bypassing of the shift register 106 to provide a one character shift in the delay line 110 during the first time slot defined by the R1 signal to permit the character stored in the register 670 to be added to the delay line 110.

More specifically, during normal operation of the delay line, the output signals supplied through an output interface 842 are returned to a gate 832 and a gate 816 to be shifted through the eight bit shift register 106 under the control of the CLK signal applied to an inverter 818. The output of the shift register 106 appears as a DL1 signal which is connected to one input of an otherwise fully enabled gate 828. Thus, the signal is returned through a gate 834 and applied in direct and inverted form to J and K terminals of a flip-flop 838, the Q terminal of which is coupled to the input of the delay line 110 through an input interface 840. Thus, signals in the line 110 are normally circulated through the shift register 106 and clocked by the CLK signal to insure synchronization.

However, when the LE signal is applied to one input of the gate 730, the other input of this gate is enabled by the inverted LP signal and an inverter 810 applies an inhibit to the gates 832 and 828 to prevent circulation of signals through the line 110 starting at the beginning of the first time slot defined by the R1 signal. The output of the inverter 810 is, however, inverted by an inverter 812 to enable the bypass gate 108 at the conclusion of the initial guard character during which this gate is inhibited by the inverted GC signal. Thus, the signals in the delay line 110 are directly returned to the input interface 840 through the gates 108 and 834 bypassing the shift register 106. During this entire interval, the LE signal also enables one input to the gate 728, the other input of which is connected to the output of a pair of AND-NOR circuits 720 and 722 through a gate 726. The gates 720 and 722 include a plurality of AND gates, one input of which is supplied with the output from the flip-flops in the register 670 and the other of which is supplied with bit timing pulses IT1—IT8. Thus, during this entire interval, the space character stored in the register 670 is being shifted into the shift register 106 through the fully enabled gate 814. It cannot be shifted out of the register 106 because the gate 828 to which the output of the register 106 is connected is inhibited.

However, when the LP signal in the first slot defined by R1 timing is reached, the inverted LP signal applied to the gate 730 inhibits this gate to cause the gate 108 to be inhibited and the gates 832 and 828 to be enabled. Thus the next character coming out of the delay line 110 is returned by the gate 832 to the input of the shift register 106, and the character stored therein which is the character stored in the register 670 is shifted into the input of the delay line 110 through the gates 828 and 834. Accordingly, the character received from the reader 102 and stored in the register 670 has now been shifted into the first time slot in delay line 110 to which the reader 102 is assigned.

At the beginning of the LP interval in which the first character or space code is shifted out of the register 106 into the delay line 110, the gate 724 is fully enabled during the bit interval defined by the signal IT6 to provide a negative-going

signal that clears or resets the flip-flop 710 so that a more negative potential is applied to its Q terminal to inhibit the gate 712. The negative-going trailing edge of the LP pulse clocks the flip-flop 718 to set the Q terminal at a more negative potential and thus terminate the LE signal. The control circuit 104 remains in this condition until the next character is read by the card reader 102 and stored in the register 670.

At this time the sprocket pulse is again effective through the circuit 644 and the gate 642 to clock the flip-flop 710. This in turn causes the flip-flop 718 to be set with the Q terminal high on the next LP pulse during the fourth slot defined by signal R4 so that during the following time slot defined by the signal R1 the shift register 106 is again bypassed and the second character, in the illustrative example a control N, is inserted into the delay line 110. This operation continues until the entire message on the control N card has been placed in circulating storage in the delay line 110.

Since the message on each card terminates with a code delete, the last item supplied from the first card placed in the reader 102 sets all of the flip-flops in the register 670, and this code delete character is read into the delay line 110 in the manner described above. However, during the interval defined by the signal R1 in which the code delete character is read into the delay line 110, the LE signal completes the enabling of a gate 658 so that the low potential output from this gate resets the flip-flop 648 to a condition in which a high potential is connected to the connected input of the gate 640. Thus, additional information cannot be loaded into the delay line 110 until the space flip-flop 648 is set by the initial space code on the second card in the message transmitted by the card reader 102.

When this next initial space code is supplied from the card reader 102 to the register 670, the flip-flop 648 is again set and the information stored on the second card is stored in the delay line 110 in the first time slot defined by the signal R1 in the manner described above. Thus, the characters from the two cards forming the message are now stored in the delay line 110 in the first segment or time slot therein, and the flip-flop 648 has been reset by the code delete character terminating the message on the second card. The next operation performed by the control circuit 104 is to enable the card reader 102 to transmit the hundreds, tens, and units digit of the key designation for storage in the delay line 110.

During the reading of the first and second card, the appearance of any alphabetical character causes the operation of the relay 517 to close the contacts 517A because each alphabetical character includes a seventh bit. The closure of the contacts 517A sets the flip-flop 777 in the register 670 but also supplies a more negative signal over a conductor 547 which extends through the cable 540 to an input of the flip-flop 622. Thus, the flip-flop 622 is set to apply a more positive potential to the connected input of a gate in a flip-flop 618 and also to the lower input of a gate 616. The upper input of the gate 616 is enabled at this time by the output of a gate 602, and a more negative potential is supplied by the gate 616 to set the flip-flop 618 so that this flip-flop applies a more negative potential to the upper input to a flip-flop 624 so that this flip-flop is set to apply an enabling potential to one input of a gate 626, the other input of which is inhibited by the flip-flop 618. The setting of the flip-flop 624 also sets the flip-flop 628 so that an enabling potential is applied to the upper input of the gate 602. The gate 602 remains inhibited, however, because of the inhibiting potential supplied from the output of the flip-flop 624.

The control circuit 104 remains in this condition at the conclusion of the reading of the second card message into the delay line 110. At this time the operator at the card reader 102 returns a switch 440 to the position illustrated in FIG. 4, and this actuation of the switch 440 reads the three key characters or digits into the delay line 110 and initiates the transfer of the message from the delay line 110 through the scanner or core input control 114 to the core storage unit 120. More specifically, when the switch 440 is returned to the position shown in

FIG. 4, the operating circuit for the relay RC is opened so that the contacts RC1 are opened to terminate the illumination of the read lamp 430. Further, the control circuit 501 in the card reader 102 is stopped.

When the contacts 442 are closed, a positive potential is again applied to the winding of the relay 520 to operate this relay so that a more negative potential is applied to the pulse shaping circuit 624 to reset the flip-flop 622. The reset flip-flop 622 inhibits the gate 616 and resets the flip-flop 618. When the flip-flop 618 is reset, both inputs to the gate 626 are enabled, and the output of this gate drops to a more negative potential and clocks a flip-flop 636. Since the K terminal of the flip-flop 636 is tied to ground, the Q terminal of the flip-flop 636 rises to a more positive potential, and the Q terminal drops to a more negative potential, these potentials being applied to the JK terminals of a flip-flop 638. The negative potential at the output of the gate 626 is also forwarded through the gate 640 to hold the J terminal of the flip-flop 710 at a more positive potential. The output of the gate 626 is also applied as an inverted SB6 signal to one input on one of the gates in the flip-flop 776 to hold this bistable set during the card reading.

On the trailing edge of the next following R3 signal, the flip-flop 638 is clocked so that its Q output drops to a lower potential and its Q output rises to a high level. This high level signal is applied to the input of a relay driver 610 and to one input of a gate 630. The low output of the Q terminal is inverted in a gate 706 and applied as one enabling input to the gate 716.

The more positive signal applied to the input of the line driver 610 causes the operation of the relay 535 to close the contacts 535A so that ground potential is applied to the hundreds contacts in the groups 410 and 420—423 and to the hundreds diode in the diode group 424. Thus, the relays in the group 510 corresponding to the bits "1," "2," "3," "4," "5," and "8" are selectively operated in accordance with the code for the value of the hundreds digit and selectively operate the bistables in the register 670 in accordance therewith. In this connection, the ASCII code for numerals requires bits "5" and "6." The "5" bit is provided from the card reader 102 by the diode group 424, and the bit "6" is provided by the inverted SB6 signal derived from the output of the gate 626 in the control circuit 104. By selectively supplying one bit from the card reader 102 and one bit from the control circuit 104, a check is made to insure that the character stored in the register 670 is a valid character arising from reading the key in the card reader 102.

The leading edge of the R4 signal defining the fourth slot in the delay line 110 completes the enabling of the gate 630, and the output of this gate clears or resets the flip-flop 636 so that a low level signal is provided at the Q terminal and a high signal at the Q terminal. The R4 signal also partially enables the gate 712 and further enables the gate 716. At the beginning of the last three character spaces in the fourth time slot, the gate 716 is fully enabled by the KC signal to provide an inverted KS signal which is forwarded through an inverter 632 to enable one input of a gate 634. The other input of this gate is enabled by the inverted LP signal so that the gate 634 provides a more negative input to the gate 642. This performs the same function as the signal provided by the circuit 644 and is effective through the inverter 646 to reset the register 670. At the beginning of the LP signal in the fourth time slot defined by the R4 signal, the gate 634 is inhibited, and the reset signal for the register 670 provided by the inverter 646 is removed permitting the register 670 to store the hundreds digit of the key designation derived from the card reader 102. The negative-going pulse provided by the gate 642 at this time also clocks the flip-flop 710 to initiate the loading of the hundreds digit of the key designation in the delay line 110 during the next following first time slot defined by the R1 signal in the manner described above. Thus, the gates 634 and 642 provide an artificial sprocket signal to clock the key characters into the delay line 110 in the same manner that this function is performed by the sprocket signals derived from the card.

Since the input flip-flop 636 has been cleared, the trailing edge of the next following R3 signal shifts a "1" into a flip-flop 702 and clears the flip-flop 638. This disables the line driver 610, removes the enabling from the gate 630, and operates a line driver 612 to operate the relay 534 to close the contacts 534A. Thus, the tens digit of the key designation is now read in the card reader 102 and stored in the delay line 110 in the manner described above. During the next cycle, the R3 signal clears the flip-flop 702 and sets a "1" into a flip-flop 704 to disable the tens line driver 612 and to operate the units line driver 614 so that the relay 533 is operated to read the units digit of the key designation into the delay line 110.

The setting of the last flip-flop 704 also partially enables a gate 708 so that during the SP signal occurring during the next following R3 signal, i.e., after the loading of the units key digit in the delay line 110, the gate 708 is fully enabled to provide an inverted EOM1 signal which is returned to one input of a gate in the flip-flop 624. The termination of the R3 pulse also shifts the "1" out of the flip-flop 704 so that the shift register counter including the flip-flops 638, 702, and 704 is cleared.

The inverted EOM1 signal resets the flip-flop 624 so that an inhibiting signal is applied to one input of the gate 626 which aids in restoring the circuit 104 to a normal condition. The high level signal from the flip-flop 624 completes the enabling of the gate 602 so that its output drops to a more negative potential to inhibit one input of the gate 616. This signal is also effective through an inverter 604 to apply a more positive signal to a line driver 606 which operates the relay 532 to close the contacts 532A. The closure of the contacts 532A operates a relay RB in the card reader 102 to open the contacts RB2 and to close a pair of normally open contacts RB1. The closure of the contacts RB1 illuminates the wait lamp 431 to provide a visible indication that the card reader 102 cannot be used until the message stored in the assigned time slot 1 of the delay line 110 has been transferred to the core storage unit 120. The opening of the contacts RB2 prevents the initiation of a card reading operation in the event that the switch 440 is operated to again close the contacts 441.

The B1 signal provided at the output of the inverter 604 also advises the core load control circuit 114 (FIGS. 9 and 10) that a complete message has been stored in the sector of the delay line 110 assigned to the card reader 102 which should be transferred to the core storage unit 120.

If the storage of data proceeds satisfactorily, the control circuit 104 is supplied with a signal indicating the satisfactory transfer, and this circuit as well as the connected card reader 102 are restored to a normal condition. More specifically, at this time, a high level C1 signal is supplied from the control circuit 114 (FIGS. 10), and a high level signal EOP\* (FIG. 22) is supplied to fully enable a gate 654. The low level output from the gate 654 resets the flip-flop 628 so that an inhibiting potential is applied to the upper input of the gate 602. This removes the signal B1 and releases to restore the card reader 102 and the control circuit 104 to a normal condition.

In the event that an error is encountered during the transfer of data from the delay line 110 to the core storage unit 120, the lower input to a gate 656 is enabled by the C1 signal, and an error reset signal ERR RST is supplied from FIG. 8 to fully enable the gate 656. The more negative output from the gate 656 resets the flip-flops 624 and 628 and sets a flip-flop 620. The resetting of the flip-flops 624 and 628 produces the functions described above including the termination of the illumination of the wait lamp 431. The setting of the flip-flop 620 enables a relay driver 608 so that the relay 531 is operated to close the contacts 531A. The closure of the contacts 531A operates a relay RA to close a pair of contacts RA1. The closure of the contacts RA1 illuminates the repeat lamp 432 to provide a visible indication that the message previously transmitted by the card reader 102 must be retransmitted because of an error. The flip-flop 620 is reset when the flip-flop 618 is next set by the gate 616 by the receipt of a bit "7" from the card reader 102 indicating the transmission of alphabetical information.

As indicated above, the delay line 110 is shared by a group of four card readers. The control circuit 104 includes three additional circuits similar to those shown on FIG. 6 and the left-hand portion of FIG. 7, the outputs of which are supplied to the terminals of the gates 732, 734, and 736 and the terminals of the NOR gate 740 so that all four card readers have access to the delay line 110.

#### TRANSFER OF DATA FROM THE DELAY LINE 110 TO THE CORE STORAGE UNIT 120 THROUGH THE CONTROL CIRCUIT 114

The control circuit 114 (FIGS. 9 and 10) basically consists of a scanner which continuously searches for a complete message stored in any of the time slots in any of the delay lines in the system 100. This scanner includes a series of three gates for each card reader or data source in the system. As an example, a group of three gates 1022, 1026, and 926 are provided for the data source or card reader 102 assigned to slot 1 in the delay line 110 and a series of three gates 1024, 1028, and 928 assigned to the card reader whose data is stored in slot of delay line 110. The gates for the other data sources similar to the sets illustrated in FIGS. 9 and 10 are schematically indicated at 929. These gates are scanned in sequence by a conventional shift register counter 1000 which is so connected as to shift a series of "1"s through the shift register followed by a series of "0"s and then a series of "1"s. The interface in the shift register between the "1"s and "0"s provides enabling for the gates so that only a single gate is enabled at any one time.

As an example, the gate 1022 is assumed to be the first gate in the chain and is fully enabled by an inverted counter reset signal CRS\* and the inverted A signal of the first stage in the counter 1000 which this counter is reset by a main reset in the event of, for instance, a power failure. When the first operating or shift pulse is applied to the counter 1000, the "0" is shifted to a second or B stage. Thus, the first gate 1022 is inhibited by the inverted A signal, and the second gate 1024 is enabled by the A signal and an inverted B signal, i.e., the interface between "1"s and "0"s is between the A and B stages.

The shift register counter 1000 is advanced by register advance signals SA developed under the control of a gate 1006. The upper four inputs to the gate 1006 are enabled whenever no delay line is supplying data to the core storage unit 120. The lower two leads to the gate 1006 are enabled during the fourth bit timing signal IT4 and the clock signal CLK. When the gate 1006 is fully enabled, an inverted register advance signal SA is generated and inverted by inverter 1020 to provide the SA signal, the trailing edge of which advances the register 1000. Thus, the register 1000 is continuously advanced so long as an inhibit is not applied to the gate 1006.

Assuming that the shift register counter 1000 arrives at its initial or first setting in which the gate 1022 is enabled to supply a low level signal which is inverted to develop the positive-going signal C1, one input to the gate 1026 is enabled. If a complete message has been stored in the first time slot of the delay line 110, which message is received from the card reader 102, the B1 signal is present and the gate 1026 is fully enabled to develop an inverted CR1 signal. This signal is inverted in an inverter 922 to provide a CR1 signal which also enables one input to the gate 926. A second input to the gate 926 is connected to the DL1 output lead from the shift register 106 associated with the delay line 110 and continuously receives data pulses from the output of the shift register 106 as they are returned to the input of the delay line 110.

The inverted card reader 1 signal CR1 is applied to one input of a gate 1002 to develop a signal "01" which is applied to one input of a gate 1004. The other input of this gate is supplied with an inverted SCOV signal derived from a flip-flop 1034. The flip-flop 1034 is set to a condition supplying the inverted SCOV signal once during each character by an inverted eighth bit timing signal IT8. Thus, the gate 1004 is fully enabled to generate an inverted "01" signal which applies an in-

hibit to the gate 1006 and thus prevents further advance of the shift register counter 1000 now that a complete message for transfer to the core storage unit 120 has been found. The inverted "01" signal is also applied through a gate 1001 to develop a  $\bar{1}$  signal. The signal  $\bar{1}$  provides a more or less master control for the system 100 indicating that the system 100 is engaged in the operation of transferring data into the core storage unit 120.

The first "01" signal developed by the gate 1002 is applied to one input to an AND gate connected to the K terminal of a flip-flop 906. Another input to this AND gate is enabled by an inverted signal SCINH and the third input to this gate is enabled at the beginning of the first time slot by the R1 signal. Thus, a more positive signal is applied to the K input of the flip-flop 906 as well as three other flip-flops 908, 910, and 912 used in conjunction with the second, third, and fourth slots in all of the delay lines. These flip-flops are clocked under the control of a gate 902 and an inverter 904. The upper input to the gate 902 is supplied with an inverted AP signal from the logic circuits shown in the Stanis et al. application so that the upper input to the gate 902 is enabled at all times that the core storage unit 120 is not in use by these logic circuits. The lower input to the gate 902 is fully enabled during each guard character in the second bit interval by a signal formed by combining the signals GC and IT2 to form a signal GC-IT2. When the gate 902 is fully enabled, the output from the inverter 904 clocks the flip-flop 906 so that a more positive output is returned from the Q output to all of the inputs of the J AND gate and the Q output supplies a more negative potential which forms the inverted signal S1. This signal is again inverted to provide the signal S1 by an inverter 914. The signal S1 completes the enabling of the gate 926 during the guard character signal GC at the beginning of slot 1 so that data from the shift register 106 is free to pass through the gate 926 and a gate 930 to one input of the gate 944 at the end of the guard character interval.

The inverted signal S1 is forwarded through a gate 900 to provide the signal WE which is used to enable the writing of information from the delay line 110 into the core storage unit 120. More specifically, a flip-flop 934 is set by the inverted SA signal each time that the shift register counter 1000 is advanced so that an enabling potential is applied to the lower input of the gate 936. The upper input of this gate is enabled by the signal WE so that the output of this gate provides an inverted WEC signal which is inverted by an inverter 942 to provide a signal WEC. The more positive potential at the output of the upper gate in the flip-flop 934 completes the enabling of the gate 944 so that data from the shift register 106 is supplied to a gate 946 to provide an inverted DATA signal used as an input to the core storage unit 120. During the interval that data in the first time slot is supplied through the gate 946 as the inverted DATA, this information is also circulated through the gates 828 and 834 to be returned to the delay line 110. The data is not erased from the delay line 110 as it is first read into the core storage unit 120 to preserve this data for subsequent transmission to the unit 120 in the event that this becomes necessary.

A flip-flop 952 is reset on each advance of the shift register counter 1000 by the inverted SA signal. However, when the write enable signal WE appears indicating that data is to be transmitted from a delay line to the core storage unit 120 and after the termination of the guard interval preceding the flip-flop from which data is being withdrawn, a gate 950 is fully enabled by the inverted signal GC to set the flip-flop 952 and provide an output signal ANYCR which is applied to one input of a gate 1032 and one input of a gate 932.

At the end of the first time slot at which time all of the message information in the first time slot has been transferred from the delay line 110 to the storage unit 120, the signal GC-IT2 again clocks the flip-flop 906 so that the Q terminal rises to a positive potential and removes the inverted signal S1 and the signal S1. The removal of the inverted S1 signal removes the WE signal at the gate 900, and the removal of the

signal S1 applies an inhibit to the gate 926 to prevent any further transmission of the inverted data signal DATA. The removal of the signal WE also removes the inverted signal WEC and the signal WEC which serve as enabling signals in the control circuit 114.

During this same guard interval in the following bit "4" timing provided by the signal IT4, a gate 932 is fully enabled to reset the flip-flop 934 so that an inhibit is supplied to the gate 944. This inhibiting signal from the output of the flip-flop 934 is inverted in an inverter 945 and applied to the gates 820, 822, 824, and 826 to partially enable these gates.

On the following circulation interval of the delay line 110, the signal R1 is returned to the K gate of the flip-flop 906, and this flip-flop is clocked by the signal GC-IT2 during the timing for bit "2" to again set this flip-flop so that the inverted signal S1 and the signal S1 are provided, and thus the signal WE. This enables the gate 926, but the inverted data signal DATA which would cause a second read-in in the core storage unit 120 is not provided because of the inhibit applied to the gate 944 by the flip-flop 934. Instead, the reappearance of the signal S1 causes the data previously transferred from the first slot in delay line 110 to the core storage unit 120 to be erased from the delay line 110.

More specifically, the upper input to the gate 820 is enabled by the signal CR1, the second input to this gate is enabled by the signal S1, and the third input is enabled by the signal DLERASE. With the gate fully enabled, an inhibit is applied to the gate 828 during the first time slot defined by the signal R1. The previously transferred information in the first time slot is erased from the delay line 110.

The control circuit 114 remains in this condition until the signal EOP\* enables the gate 654 in the manner described above to cause the removal of the signal B1. The removal of the signal B1 removes the inverted signal CR1 which is effective through the gates 1002 and 1004 to remove the inhibit from the gate 1006. The gate 1006 is now enabled to develop the inverted signal SA and the signal SA to advance the shift register counter 1000 to search for the next complete message to be transferred to the core storage unit 120. The appearance of the inverted SA signal resets the flip-flop 952 to remove the signal ANYCR and resets the flip-flop 934 to remove the DLERASE signal and to enable the gate 944 as well as the gates connected in parallel therewith controlled by the remaining scanner gates indicated generally as 929. The flip-flop 906 was reset by the GC-IT2 signal at the beginning of the second time slot following the erasure of the first time slot. Thus, the circuit 114 is now enabled to search for and read out the next complete message stored in any of the delay lines associated with the control circuit 114.

This resetting of the circuit 114 also removes the inhibit applied by the gate 820 to permit the circulation of data through the delay line 110 and the shift register 106 through the gates 828 and 834.

The control circuit 114 also controls the provision of the error reset signal ERR RST to the control circuit 104. More specifically, a flip-flop 802 is normally reset by the inverted SA signal each time that the shift register counter 1000 is advanced. If an error is present, an inverted signal ERROR\* sets the flip-flop 802 to provide an inverted signal EIP through an inverter 808. The set flip-flop 802 also enables one input to a gate 804. Another input to this gate is enabled during the eight bit timing of the signal SP once during each of the slot defining signals R1—R4. The remaining lead of the gate 804 is enabled by a signal SCINH which is provided by a flip-flop 940. The flip-flop 940 is set by the signals GC and WE whenever the flip-flop 934 has been set by the gate 932 to provide the erase signal DLERASE. When the gate 804 is fully enabled, an inverter 806 connected to the output of this gate provides the error reset signal ERR RST. This performs the functions set forth above of lighting the repeat light 432 and advancing the shift register counter 1000 by removing the signal B1.

The system 100 also includes means for preventing the transfer of data from the delay line 110 to the core storage

unit 120, in the event that any of the receiving printers 204 to which a message being transferred from a delay line 110 to the core storage unit 120 is to be transmitted is unavailable. More specifically, if during the transfer of addresses from a delay line 110 to the core storage unit 120 the decoding of the addresses in unit 122 results in the selection of a printer 204 to which immediate access may not be obtained, the inverted signal **BYPEN** appears to apply a low level signal to the K terminal of a flip-flop 1048 and a more positive signal to the J terminal of this flip-flop. The flip-flop 1048 is toggled under the control of another flip-flop 1040 which is clocked to set its Q terminal positive with bit "8" timing under the control of the signal **IT8** and reset by secondary clock signals **CLKS**. The flip-flop 1040 enables one input to a gate 1042, the other input of which is enabled during the guard character interval by the signal **GC**. Thus, during the eighth bit of the guard interval defined by the signal **GC**, the gate 1042 drives an inverter 1044 to clock the flip-flop 1048. When the flip-flop 1048 is set, the  $\bar{Q}$  terminal goes negative and is effective through the gate 1050 to provide a master reset signal **MR** which is used to restore portions of the circuit associated with reading data into the core storage unit 120.

The positive-going signal at the Q terminal of the flip-flop 1048 enables one input of the gate 1032. The top input to the gate is enabled by the signal **ANYCR** if the circuit 114 is in the process of supplying data from a delay line 110 to the core storage unit 120. The enabling of the gate 1032 is completed by the signals **IT2** and **GC** during the second bit timing of the guard character in the time slot immediately following the one in which the condition giving rise to the inverted **BYPEN** signal arose. When the gate 1032 is fully enabled, the flip-flop 1034 is set to drive the inverted signal **SCOV** negative and inhibit all four of the gates 1004, 1010, 1014, and 1018. This removes the inhibit from the gate 1006 provided by the seizure of a delay line for readout and permits the shift register counter 1000 to advance in search of another message since the message then being transmitted could not be forwarded to its destination. The message is not lost, however, for the reason set forth above that the delay line is not erased until after the data has been stored in the unit 120 and found to be proper.

The set output of the flip-flop 1034 also partially enables the gate 1036 which is fully enabled during bit "6" timing by the signal **IT6**. The output of the gate 1036 provides an inverted **RBE** signal which is returned to the clear terminal of the flip-flop 1048 to clear this flip-flop and thus remove one enabling potential from the gate 1032 and terminate the master reset signal **MR**. During eighth bit timing, the inverted signal **IT8** resets the flip-flop 1034 to drive the inverted **SCOV** signal to a positive level and partially enable the gates 1004, 1010, 1014, and 1018.

When the shift register counter 1000 is advanced in the manner described above under the control of the inverted **BYPEN** signal, the circuit 114 is restored to its normal state and searches for the next available complete message stored in one of the delay lines 110. During these subsequent scanning operations, the delay line containing the message which could not be serviced and which gave rise to the inverted **BYPEN** signal can again be seized and an attempt made to read the complete message out of this delay line.

#### MAGNETIC CORE STORAGE UNIT 120,

#### CORE ADDRESS COUNTER 126, OUTPUT SELECTOR 122,

#### AND DECODING CIRCUIT 124.

The portion of the circuit shown on FIGS. 11-17 of the drawings writes the data received from the delay line 110 into the core storage unit 120 (FIG. 19) under the control of the core address counter 126 (FIG. 18). In addition, the circuits shown in FIGS. 11-17 detect the addresses in the message material supplied from the delay line 110 as it enters the core

storage unit 120 and control the output selector 122 to select the desired output stations on messages of the type requiring a recorded output. In addition, these circuits include the decoding circuit 124 which not only searches for and detects the presence of control codes but also detects and provides indications of errors in the input data.

#### 1. Writing Data from Delay Line 110 into Core Storage Unit 120

The inverted signal **DATA** (FIG. 9) from the delay line 110 is directly applied to the K terminal and applied by an inverter 1101 to the J terminal of an input stage of the eight bit shift register 116 (FIG. 11), and this data is shifted into the register by the signal **CLK**. From the register 116, the data is supplied in parallel form to the core storage unit 120 (FIG. 19) and is decoded while in the register 116 and checked for errors by the circuit 124. The control codes detected by the circuit 124 also are used to prime addresses into the core address counter 126 to control the location in the core storage unit 120 in which various types of messages are stored.

The first character received in any message is a space code which is shifted through the register 116 and is not stored in the core storage unit 120. The second character in every message is a control code, and this code is detected or decoded by two networks 1100 and 1300 consisting of gates and output inverters. Each character is decoded on an octal basis and, since the last bit into the shift register 116 is a parity bit, the codes can be detected when only the first seven bits of the character have been shifted into the register 116. The circuit is arranged to examine a first octal group of shift register stages providing B, C, and D outputs representing the binary weights "1," "2," and "4." The second and third octal groups are examined concurrently and comprise a second octal group examining the outputs of the shift register stages providing the E, F, and G output signals of binary weights "1," "2," and "4" and a third group consisting of a single output signal H of a binary weight "1."

As an example and assuming that the first seven bits of the control N code from the first card in the illustrative message have been shifted into the first seven stages of the register 116, these bits will occupy the indicated position at the end of the **IT7** signal. At the beginning of the **IT8** signal, all of the gates in the group 1100 are partially enabled by the **IT8** signal. This means that the stages providing the output signals C, D, and E will be set, and the stages providing the output signals B, F, G, and H will be reset. A gate 1102 is fully enabled by the signals **IT8**, B, C, and D to provide a lower potential signal which is forwarded through an inverter 1104 to enable one input to a gate 1106. Thus, the decoding of this first octal group is "XX6" or that the value of the binary weights in the first octal group produced by the presence of a C signal and the presence of a D signal, i.e., "2" and "4" is "6." Similarly, a gate 1302 is fully enabled by the signals E, F, G, and H to provide a more negative signal which is forwarded through an inverter 1304 to enable the other input of the gate 1106. The signal provided by the gate 1302 and the inverter 1304 represents an octal decoding of "01X" representing the presence of a binary weight "1" in the second octal group and a binary weight "0" in the third octal group.

The enabling of the gate 1106 essentially combines the two octal decodings "01X" and "XX6" to provide "016" which is the octal coding for control N. Since the control N character is always associated with only a first card, the output of the gate 1106 provides an inverted first card signal C1, and an inverter 1108 provides a signal C1. In a similar manner, the remaining gates in the detecting networks 1100 and 1300 provide a second card signal C2 at the output of a gate 1110, a third card signal C3 at the output of an inverter 1306, and a fourth card signal C4 at the output of a gate 1112. In view of the fact that a number of different control codes are used on the second and fourth cards, the second card signal C2 and the fourth card signal C4 arise from multiple translations. The

designations of the various decoded octal groups are shown on FIGS. 11 and 13.

The operations involving the writing of data from the delay line 110 into the core storage unit 120 use essentially delay line timing. Accordingly, when data is to be written into the core storage unit 120 from the delay line, the signal WEC (FIG. 9) is supplied as one enabling input to three gates 1308, 1312, and 1314, the other inputs of which are supplied with the signal CLKS, the inverted signal CLKS, and the signal CLK, respectively, to provide in conjunction with two inverters 1310 and 1316 the signal WCS, the inverted signal WCS, and the signal WC.

As set forth above, the circuit 124 provides the signal C1 in response to the receipt of the control N code. The signal C1 indicates that a first card message is being transmitted from a delay line 110. This first card message is to be stored in a particular location in the core storage unit 120. Accordingly, a gate 1118 is fully enabled by the signal C1 and the signal WC to provide an inverted signal SARI. This signal is supplied to the core address counter 126 (FIG. 18) and primes the counter 126 to a predetermined setting such as "000" in which a particular combination of octal output signals AR2<sup>0</sup>—AR2<sup>7</sup> are provided. These signals are translated in a conventional decoding network (not shown) to address a predetermined location in the core storage unit 120 to receive the first stored character.

To supply the bits of the character stored in the shift register 116 to the input of the core storage unit 120, a gating and storage network 1200 is provided including eight gates 1201—1205 and 1406—1408 which are used to set eight bistables 1211—1215 and 1416—1418. One input to each of the gates 1201—1205 and 1406—1408 is supplied with the indicated one of the output signals A—H from the shift register 116. The character is completely shifted into the register 116 during the last bit timing signal IT8. On the following first bit timing signal IT1, a gate 1136 is enabled by the signal WCS to forward a more positive signal from the gate 1140 to complete the enabling of the gates 1201—1205 and 1406—1408 in dependence on the character stored in the register 116. Those of the input gates that are fully enabled set the corresponding flip-flops 1211—1215 and 1416—1418 to supply the core input signals DIR1—DIR8. These signals are applied to the input of the core storage unit 120 (FIG. 19). 19).

To write the signals DIR1—DIR8 into the core storage unit 120, a gate 1351 supplies a more positive potential to the J terminal of a flip-flop 1354 whenever one of the card signals C1—C4 is present. The flip-flop 1354 is clocked by the signal WC to set the Q terminal more positive and the  $\bar{Q}$  terminal more negative whenever a card signal is present. The more negative signal at the  $\bar{Q}$  terminal of the flip-flop 1354 inhibits a gate 1362 supplies an output signal C4/13, and clocks a flip-flop 1364, the K terminal of which is returned to a more negative potential. Thus, the flip-flop 1364 is set so that a low potential is applied to one input to a gate 1366 to generate a more positive signal IWA. The signal IWA is applied as an enabling signal to a pulse generator 1800 which is also supplied with the last timing bit signal IT8. The pulse generator 1800 supplies a count pulse to the core address counter 126 to advance this counter at the end of each character timing cycle or as each character is read into the core storage unit 120.

The more positive potential provided at the output of the gate 1366 enables a gate 1368 so that when the signals IT1 and WC are present, an inverted store core write signal SCW is generated. This signal which is generated at the beginning of the character timing cycle is applied as an enabling input to a pulse generator 1902 which is coupled to the clear/write input of the core storage unit 120. Thus, at the beginning of each character timing cycle, the character represented by the signal DIR1—DIR8 is written into the core storage unit 120, and at the end of the character timing cycle the pulse generator 1800 advances the core address counter 126 to its next setting to direct the next character to the next address location. In this connection, an inverted signal DCREN applied to the core ad-

dress counter 126 controls the up or down direction in which the counter 126 operates.

The bistables 1211—1215 and 1416—1418 which provide the input signals DIR1—DIR8 are reset during the last bit timing provided by the signal IT8 as the core address counter 126 is advanced. More specifically, a gate 1138 is provided at its input with the signals IT8 and WCS. The output of the gate 1138 is connected to one reset input terminal of each of the flip-flops 1211—1215 and 1416—1418 to reset these flip-flops during the last bit timing signal IT8.

In this manner, the characters of the first card message are stored in the core storage unit 120. At the end of the first card message as well as at the end of every card message, a code delete code is stored in the input register 116. This is translated to enable a gate 1350 so that an inverter 1352 generates a signal C3/6 and also applies a more positive potential to the K terminal of the flip-flop 1354. When this flip-flop is clocked by the signal WC, a signal C4/12 goes negative, and the signal C4/13 provided at the  $\bar{Q}$  terminal goes positive. This signal completes the enabling of the gate 1362 when the inverted signal CLKS and the last bit timing signal IT8 are present. The output of the gate 1362 resets the flip-flop 1364 so that a more positive potential is applied to the input of the gate 1366. This terminates the signal IWA and the inverted signal SCW to prevent further advance of the core address counter 126 or the writing of additional information into the core storage unit 120.

The circuit remains in this condition until the next card is received. Assuming that it is a second card, a gate 1120 is fully enabled to provide an inverted signal SAR2 which is applied to the preset address input of the core address counter 126 to advance the counter to the setting at which the second card information is to be stored in the core storage unit 120. Further, the presence of the inverted second card signal C2 again controls the setting of the flip-flops 1354 and 1364 so that the core advance enabling signal IWA and the inverted store core write signal SCW are provided. The second card information is then stored in the core storage unit 120 in the manner described above. At the end of the message on the second card, the code delete code is again detected to reset the flip-flops 1354 and 1364 to prevent writing additional information into the core storage unit 120.

When a third card is read out of a delay line 110, the signal C3 enables a gate 1122 to provide a signal which is forwarded through a gate 1126 and an inverter 1128 to provide the third card address inverted signal SAR3 which is applied to one of the preset address inputs of the core register counter 126 in the manner described above to prime this counter to a setting representing the address in the core storage unit 120 at which the message on the third card is to be provided. However, this same address provided by the inverted signal SAR3 is used when the decoding of the control character indicates that a control E or message card has been detected, this control also being decoded to provide the fourth card signal C4. Thus, the signals EC and C4 enable a gate 1126 to provide the inverted signal SAR3. In this instance, either of the signals C3 or C4 causes the setting of the flip-flops 1354 and 1364 to permit the writing of information in the core storage unit 120 through the provision of the inverted signal SCW and also enables the incremental advance of the core address counter 126 by the provision of the enabling signal IWA.

If there is a fourth card present in the message, the signal C4 enables one input to a gate 1130, and if this card is not a control E or message card, the inverted signal EC enables another input to the gate 1130. This gate is fully enabled by a signal WC to provide the inverted fourth address signal SAR4 which is applied to the indicated preset address input on the core address counter 125. Thus, the counter 126 is primed to a condition in which the characters of the fourth card message are fed into the core storage 120 starting at a fourth preset address. The flip-flops 1354 and 1364 again provide the signal IWA to enable the incremental advance of the counter 126 and the inverted signal SCW to enable the the pulse generator 1902 to

supply clear/write signals to the core storage unit 120 for writing the fourth card characters into the storage unit 120. The code delete at the end of the fourth card again clears the flip-flops 1354 and 1364 to inhibit the advance count pulse generator 1800 for the core address counter 126 and the clear/write pulse generator 1902 for the core storage unit 120.

The last item of information in a message comprises the three digits of the designation of the key, and as set forth above these three digits occur during the timing signal KC which occupies the last three character spaces of any slot in a delay line 110. Accordingly, the circuit 124 includes a flip-flop 1318, the J and K terminals of which are provided with the signal KC and the inverted signal KC, respectively. The flip-flop 1318 is clocked from the last timing bit signal IT8 to develop a key enable signal KEYEN and its inverted signal. The inverted signal KEYEN is forwarded through the gate 1366 to provide the count enabling signal IWA and to enable the gate 1368 to provide the inverted store core write signal SCW. The signals used to enable the network 1200 provided by the gate 1140 and to reset the network 1200 provided by the gate 1138 are not dependent on the detection of a control character, and thus these signals are available to transfer the key characters into storage. A gate 1806 momentarily enabled by the inverted signal KEYEN and the signals WEC, IT8, and KC primes a known key digit address into the counter 126 (FIG. 18). At the end of the signal KC, the flip-flop 1318 is reset by the last bit timing signal IT8.

Since it is also necessary to store data in the core storage unit 120 under the control of the central processor unit, each of the flip-flops 1211—1215 and 1416—1418 is provided with an additional inverted input signal SD1—SD8 in the manner shown in the copending Stanis et al. application. Further, this application provides an inverted resetting signal RDREG for resetting these flip-flops.

To permit this writing into the core storage unit 120 from the central processor unit, the copending Stanis et al. application also includes circuits for providing inverted store core write signals SCW1 and SCW3 (FIG. 19). Further, to permit the core address counter 126 to be advanced to settings selecting the addresses at which information is to be stored in the unit 120 by the central processor unit, the digitally designated preset address inputs shown in FIG. 18 are provided. The central processing unit shown in this copending application provides the inverted signals DP1, DP2, ADV1&2, and IP1 to supply count signals to the counter 126. This application also provides an inverted up/down control signal DCREN to control the direction and operation of the counter.

During the last character interval of the time slot in which data is being transferred from the delay line 110 into the core storage unit 120, the signal WEC and the inverted signal WEC are read into the J and K inputs of a flip-flop 1630. At the end of the signal LP, the flip-flop 1630 is clocked to apply a more positive potential from the Q terminal to one input of the gate 1632. The gate 1632 is fully enabled by the signals GC and IT7 of the next following time slot to develop an inverted CLBYP signal. This signal is used in the copending application.

## 2. Output Selector 122

The output selector 122 (FIGS. 12, 14, and 15) is continuously supplied with the signals being supplied to the core storage unit 120 by the network 1200 and selectively translates only those signals representing address codes to effect the selection of the output recorders 204 required by each message. This output selection operation is performed as information is being read from the delay line 110 into the core storage unit 120 so that the output selector 122 or circuits associated therewith can determine the availability, i.e., idle/busy status, of the output recorders. If all of the output recorders 204 required by a given message are not available at the time that the message information is applied to the core storage unit 120, the message is not erased from the delay line and this delay line is bypassed in the manner described above

to permit the message to be retransmitted to the core storage unit 120 at a subsequent time in the hope that all of the output recorders 204 required by the message will then be available.

With the cards used in the system 100, address codes occupy the third and fourth character positions on a first or control N card and may occupy one or all of the third through 13th character positions on a second card. Output addresses are not provided on third and fourth cards. Thus, the output selector 122 examines the information being supplied by the network 1200 to the input of the core storage unit 120 during the third and fourth characters of a message derived from a first card and during the third through 13th characters of a message derived from a second card.

In the illustrative example, the first or control N card contains the nurse's station address "08" in the third and fourth character positions comprising a tens address digit "0" and units address digit "8." The units digit information is collected by a network 1220 including four input gates 1221—1224, the outputs of which are connected to four storage flip-flops 1231—1234 and the inputs of which are supplied with the core input signals DIR1—DIR4, respectively. The tens digit information is supplied by a network 1420 including four input gates 1421—1424, the outputs of which are coupled to four storage flip-flops 1431—1434 and the inputs of which are supplied with the core input signals DIR1—DIR4, respectively.

To provide means for selectively enabling the units input gates 1221—1224 and the tens input gates 1421—1424, the four gates 1518, 1522, 1524, and 1528 are provided. These gates are selectively enabled under the control of the settings of the core address counter 126 which provides an indication of the position in the message occupied by the data signals DIR1—DIR4 then being supplied to the input of the core storage unit 120. The gate 1518 selects the tens digit of the single address on a first card, and the gate 1524 selects the units digit of the single address on a first card. The gate 1522 selects the tens digit of up to five addresses on a second card, and the gate 1528 selects the units digit of up to five addresses on a second card.

More specifically, the gate 1518 is partially enabled through a gate 1506 and an inverter 1508 by the inverted signal AR2' and the signal AR2<sup>o</sup> derived from the core address counter 126. A second enabling for the gate 1518 is derived from a gate 1514 and an inverter 1516 under the control of the inverted signals AR2<sup>o</sup>—AR2<sup>o</sup>. The two gates 1506 and 1514 are thus fully enabled in the second address which, since the initial space is dropped, is the first or tens character of the address on the first card. The gate 1518 is clocked or rendered fully enabled under the control of a gate 1502 and an inverter 1504 under the control of the signals WEC, IT1, and CLK during the first bit position in the character timing, i.e., concurrently with the inverted store core write signal SCW. When the gate 1518 is fully enabled, a tens gate 1520 provides a signal GATE TENS to enable the gates 1421—1424. Thus, the flip-flops 1421—1434 are selectively set under the control of the signals DIR1—DIR4 to provide the signals AT1, AT2, AT4, and AT8. These signals correspond to the binary weights "1," "2," "4," and "8" of the binary coded tens decimal digit. At the end of the signal IT1, the enabling potential from the tens gates 1421—1424 is removed.

When the units digit of the address on the first card is supplied to the flip-flops 1211—1215 to provide the signals DIR1—DIR4, the core address counter 126 is advanced to its next setting to inhibit the gate 1506 and to enable a gate 1510 so that an inverter 1512 partially enables the gate 1524. The input to the gate 1510 is provided with the inverted signal AR2<sup>o</sup> and the signal AR2'. The enabling of the gate 1524 is completed by the gates 1502 and 1514 so that a more negative potential at the output of the gate 1524 is forwarded through a gate 1526 to provide a signal GATE UNITS. This signal enables the gates 1221—1224 so that the binary coded units decimal digit of the station address is stored in the flip-flops 1231—1234. In the illustrative example in which the address

on the first card is "08" identifying the transmitting card reader 102, all of the flip-flops 1431—1434 are reset representing the tens digit "0," and only the flip-flop 1234 is set in the network 1220 representing the units digit "8."

The units digit is immediately translated into decimal marking in a series of gates, some of which are shown to the right in FIG. 12. A gate 1240 is provided with the inverted signal U1 and the signal U8 and is fully enabled by the digit "8" stored in the flip-flops 1231—1234. An inverter 1241 provides an output signal 8's and partially enables a gate 1242.

The translation of the settings of the tens storage flip-flops 1431—1434 is delayed until the units digit is read. More specifically, a gate 1534 and an inverter 1536 control the enabling of a group of tens translating gates including a gate 1440 by the selective application of an enabling signal POMS. Since the number of output recorders 204 used in the system 100 does not require the use of the binary weight "8" for the tens digit, flip-flop 1434 is always reset and supplies one enabling signal to the gate 1534. The other input to the gate 1534 is supplied from the Q terminal of a flip-flop 1532, the clock input of which is connected to the gate 1526. The clear terminal of the flip-flop 1532 is clocked by a gate 1530 to the input of which the signals IT8 and WCS are supplied. Thus, the flip-flop 1532 is cleared to a setting in which a more negative potential is applied to the Q terminal at the end of each character interval by the signal IT8. However, the K terminal of this flip-flop is connected to ground, and this is read into the flip-flop 1532 when the signal GATE UNITS is provided. When the address register counter 126 advances, the gate 1524 is no longer enabled, and a negative-going signal is applied to the clock terminal of the flip-flop 1534. This sets the flip-flop so that a more positive potential is applied by the Q terminal to the connected input of the gate 1534. When the signal IT4 of the following character appears, the gate 1534 is fully enabled and applies the signal POMS to a translating gate including the gate 1440.

Since in the illustrative example, the value of the tens digit is "0," the gate 1440 is fully enabled by the flip-flops 1431—1434, and an inverter 1442 completes the enabling of the gate 1242 so that a gate 1243 supplies a more positive output signal representing the nurse's station "08." This signal is forwarded through an inverter 1560 to set a flip-flop 1562 to provide an output signal OD08 representing that the nurse's station identified as "08" is to receive the message. The setting of the flip-flop 1562 also partially enables a gate 1564.

When the seventh bit timing signal IT7 is provided in the same character interval in which the gate 1534 was enabled, a gate 1538 is fully enabled to provide an inverted signal BRESET. This signal is supplied to all of the flip-flops 1231—1234 and 1431—1434 to reset the tens and units digit storage bistables and prepare them for storing the next address code. During the eighth or last bit timing period defined by the signal IT8, the gate 1530 clears the flip-flop 1532 and applies an inhibit to the gates 1534 and 1538 which persists until the next address characters are read.

As indicated above, a second card can include up to five addresses occupying the third through 13th character positions on a second card. When a second card is provided, the signal C2 permits the flip-flop 1520 to be set to provide a more positive output on a Q terminal when the flip-flop 1540 is clocked by the signal WC. This is shifted into a flip-flop 1542 on the next succeeding signal WC and enables the gate 1544, the other input of which is supplied with the last bit timing signal IT8. The two flip-flops 1540 and 1542 in addition to detecting the presence of a second card signal C2 provide a one character delay in combination with a flip-flop 1550 so that the flip-flop 1550 is set under the control of a gate 1544 and 1546 on the timing of the signal IT8. The more positive signal supplied at the Q terminal of the flip-flop 1550 partially enables the two second card gates 1522 and 1528. In the odd character positions from the card, the gate 1552 is enabled by a decade counter shown generally as 1556, and the gate 1528 is enabled by this decade counter on the even numbered

character positions on the second card. Thus, when the tens digit of the first address is presented by the output signals DIR1—DIR4, the gate 1552 is fully enabled to read the tens digit into the flip-flops 1431—1434. At the end of this interval on the signal IT8, a gate 1552 is fully enabled and is effective through an inverter 1554 to advance the decade counter 1556 a single step, thus reversing the normally negative output signal provided at a terminal A from the counter 1556 to a more positive signal. This more positive signal completes the enabling of the gate 1528 and is effective through an inverter 1527 to inhibit the gate 1522. Thus, the units digit of the address appearing in an even numbered character position on the card is stored in the flip-flops 1231—1234. The flip-flop 1532 controls the reading of the tens storage flip-flops 1431—1434 in the manner described above and then resets these flip-flops in the manner described above.

During the eight following character intervals, the decade counter 1556 alternately enables the two gates 1522 and 1528 so that the remaining addresses are read into the storage flip-flops 1231—1234 and 1431—1434, translated by the gates similar to the flip-flop 1562. At the end of the translation of the units digit in the fifth address, a gate 1548 is fully enabled to clear the flip-flop 1542 and thus prevent further enabling of the input gates 1221—1224 and 1421—1424 until the second card signal C2 is again applied to the input flip-flop 1540.

In the illustrative example, only a single address is provided in the five possible locations for addresses on the second card, and this address designates the output recorder 204 in the diet kitchen, which is a departmental recorder rather than a nursing station recorder. Thus, a flip-flop similar to the flip-flop 1562 is set representing the designation "16" identifying the diet kitchen recorder, and this set flip-flop provides an output signal OD16 representing the demand for this recorder. This signal partially enables a gate 1580 similar to the gate 1564 which is partially enabled by the requested output recorder at the nursing station identified as "08." A given address, such as "44" can be used to request all or a group of the recorders through a gate 1443.

The signals OD08 and OD16 are forwarded to a comparison network 2300 (FIG. 23) at which a comparison of these signals with busy signals FULL 08 and FULL 16 is made to determine whether or not recording facilities are available for all of the addressed stations by a group of gates 2302, 2304, 2306, 2310. If not, the inverted signal BYPEN is generated and forwarded to control circuit 114 shown in FIG. 10 to cause the bypass operation described above as well as the resetting of certain of the components in the circuit shown in FIGS. 11—17 under the control of the master reset signal MR. Further and as described above, the presence of the inverted signal BYPEN develops the inverted signal RBE.

This signal is applied to one input of a flip-flop 1590 and sets this flip-flop so that a more negative signal is forwarded through a gate 1591 to a J terminal of the flip-flop 1592. This flip-flop is clocked on the inverted signal IT1 so that its Q terminal rises to a more positive potential and is effective through an inverter 1593 to reset the flip-flop 1562 and the corresponding flip-flop providing the signal OD16 and thus remove the stored indication of the required addresses "08" and "16." As set forth above, the bypass operation leaves the message stored in the originating delay line 110 and permits the message to be accessed and an attempt made to secure the necessary outputting facilities at a subsequent time. The inverted output signal RDB1 from the inverter 1593 is also returned to an input of the flip-flop 1590 to reset this flip-flop and permit the flip-flop 1592 to be reset by the inverted IT1 signal. This frees the flip-flops similar to the flip-flop 1562 to be set under the control of the next addresses supplied to the circuit 122.

Assuming that the output facilities for the required stations "08" and "16" are available so that the message stored in the core storage unit 120 can be transferred to the drum 202, a circuit shown in FIG. 22 develops an output synchronizing signal OSY which is applied to a pair of gates 1570 and 1574.

A signal from the gate 1574 is forwarded through an inverter 1576 to enable the other input to the gate 1580 to develop the signal ADD16. The signal applied to the gate 1570 normally completes enabling of this gate so that an inverter 1572 completes the enabling of the gate 1574 to provide the signal ADD08.

The signal OSY could be used to enable both of the gates 1564 and 1580 except that certain types of outputs derived from the central data processing unit are not to be supplied to nurse's stations or certain of the output stations such as the nurse's station identified as "08." Accordingly, if any of the inverted signals WCL, U2C, or U3C which identify these particular types of list operations are to be performed, a gate 1566 and an inverter 1568 inhibit the gate 1570 to prevent the enabling of those stations to which lists are not to be transmitted. On the other hand, it does not effect the enabling of stations in departments such as the diet kitchen identified as "16" which can be enabled by the gates 1574 and 1580.

The appearance of the OSY signal which provides the output signals ADD08 and ADD16 as well as the corresponding signals for the other stations also causes the resetting of the storage flip-flops similar to the storage flip-flop 1562. These output flip-flops are also reset in the event of an occurrence of an error. More specifically, the gate 1591 is supplied with an inverted signal OSY and an inverted signal ERROR\* which effect the resetting of the flip-flops similar to the flip-flop 1562 in the manner described above to remove the output request.

### 3. Control Code Decoding

The circuit 124 decodes and stores a number of control characters located in different positions on the cards of the incoming message to supply control signals to the central processing unit specifying the type of operation that is to be performed on the message information being received from the delay line 110 and stored in the core storage unit 120. In general, this decoding takes place on the second character of a received message which includes the control code, and in certain special applications when a certain code appears prior in the message, also examines a subsequent character position in the message or card to look for the presence of a second or additional control character.

FIG. 16 of the drawings illustrates a series of flip-flops 1600, 1602, 1604, 1606, 1608, 1610, 1612, 1614, and 1616, all of which are cleared by the inverted main reset signal MR and clocked by the signal WC.

The K input to the flip-flop 1600 decodes the octal coding "021" to provide the signal QC representing a Q control.

The K input to the flip-flop 1602 decodes the octal code "022" to set the flip-flop 1602 to provide the control R signal RC.

The K gate to the input of the flip-flop 1604 decodes the octal code "025" and sets the flip-flop 1604 to provide the control U signal UC.

The J input to the flip-flop 1606 decodes the octal group "026" and sets the flip-flop 1606 to provide the control V signal VC. In a similar manner the decoding networks 1100 and 1300 supply the input signals O13, C1, C3, C4, and C4A to set the flip-flops 1608, 1610, 1612, 1614, and 1616 to provide the output signals XC, NC, FC, EC, and TC, respectively. The signal XC represents the presence of a control K. The signal NC represents a first card. The signal FC represents a third card requiring a multiplier. The signal EC represents a message card, and the signal TC represents a correction card.

The circuit shown on FIG. 17 of the drawings, in the lower portion thereof, affords means for detecting control characters that are conditioned on the prior appearance of another control character. As an example, cards carrying an initial control U or an initial control V provide the inverted signals UC and VC and are effective through a gate 1718 and an inverter 1720 to clock a flip-flop 1722, the K input of which is tied to ground. Thus, if a control U or a control V is detected, the flip-flop 1722 is set to enable one input to a gate 1724. The

remaining inputs to these gates are enabled by the signals AR2<sup>2</sup>—AR2<sup>3</sup> representing a given address in the core address counter 126 and thus specifying a specific location at which additional secondary control characters should be detected. The flip-flop 1722 is reset on the inverted signal AR2<sup>4</sup>.

When the gate 1724 is fully enabled, an inverter 1726 partially enables six flip-flops 1728, 1730, 1732, 1734, 1736, and 1738. The J and K gates of these flip-flops thus look at the shift register 116 for the codes "020," "004," "023," "061," "062" to provide the output signals PC, DC SC, U1C, U2C, and U3C, respectively when clocked by the signal WC. These flip-flops are cleared by the inverted main reset signal MR (FIG. 10) on a bypass condition or when the processing operation has been terminated as signified by the presence of the inverted signals EOP\* and EAPC.

Three flip-flops 1740, 1742, and 1744 are provided for detecting and storing a pair of control codes supplying output signals WCL and XCL, respectively. These signals indicate the paid on account operation (WCL) and a correct paid on account operation (XCL).

More specifically, the J input to the flip-flop 1740 is enabled by the octal decoding "027" and is clocked by the signal WC to provide the output signal WCL and the inverted signal WCL. When the inverted WCL signal appears, the flip-flop 1742 is clocked and has its K input returned to ground. Thus, the Q output of the terminal 1742 rises to a more positive potential to partially enable one of the K inputs to the flip-flop 1744. When the octal group "130" is found in the shift register 116 subsequent to the detection of a "027," the signal WC clocks the flip-flop 1744 to provide the output signal XCL. The flip-flop 1742 is cleared by the inverted signal AR2<sup>5</sup>, and the flip-flops 1740 and 1744 are cleared or primed on the inverted signal MR.

A pair of gates 1636 and 1638 provide two output signals CCR and CCR̄ by decoding the inverted signals shown connected to their inputs.

### 4. Error Detection

The circuit 124 includes a number of circuits for checking various errors in the incoming information. The detection of any of these errors results in the production of the inverted signal ERROR\*, and this signal as described above causes the illumination of the lamp 432 at the input card reader 102 to advise the operator that a retransmission of the message is necessary.

One of the errors detected by the circuit 124 is the presence of an improper combination of control characters, and this is performed by a decoding or translating network 1620. The gates of the network 1620 are supplied with the indicated pairs of input signals which are not proper combinations. As an example, if the flip-flop 1600 has been set to provide the signal QC representing the presence of a Q control character and a subsequent character stored in the shift register 116 is any one of the combinations resulting in the second card signal C2, a gate 1621 is fully enabled and is effective through a gate 1622 to apply a more positive potential to the J terminal of a flip-flop 1624. This flip-flop is clocked on the signal WCS and provides at the Q̄ terminal an inverted signal DCTE representing the fact that two control characters have been received in a single message. The flip-flop 1624 is reset on the signal WEC.

The circuit 124 also includes means for checking for the presence of an incorrect combination. This checking is performed by three gates 1324, 1326, and 1328, one input to the gates 1326 and 1328 being supplied by a gate 1322. The three gates 1324, 1326, and 1328 are partially enabled at the end of the message by the signal KEYEN which is generated in the manner described above. If the combination of control characters represented by the signals TC, EC, and WCL and the inverted signals TC, FC, and RC have been received during the message, one of the three gates 1324, 1326, or 1328 is fully enabled indicating that an incorrect or improper group of

cards has been received during the message. A gate 1330 and an inverter 1332 clock a flip-flop 1334 at this time to set this flip-flop so that a more negative potential appears at its  $\bar{Q}$  terminal, the K input terminal being strapped to ground. The setting of the flip-flop 1334 which is cleared by the signal WEC stores the fact that the message contained an improper card group.

The circuit 124 also includes means for checking or determining whether or not a first and a second card have been received inasmuch as any proper message includes both a first and second card. This circuit includes a flip-flop 1356 which is set by the signal WC to provide a more positive output at the Q terminal when a second card signal C2 is applied to its J terminal. This enables one input to a gate 1358. When a first card is provided, the signal C1 applies a more positive potential to the J input of a flip-flop 1370 which is also clocked on the signal WC. The presence of a first card sets the flip-flop 1370 so that a more positive signal is applied from its Q terminal to the other input of the gate 1358. Thus, when both a first card and a second card have been included in the message, the gate 1358 is enabled to apply an inhibit to one input of a gate 1360. If, on the other hand, both a first card and a second card have not been received, the upper input to the gate 1360 is enabled, and this gate is fully enabled by the signal WEC and a signal formed by combining the signals GC and IT2 to provide the signal GC-IT2. Thus, when both a first card and a second card have not been included in the message, the gate 1360 provides the inverted signal NFSC.

The circuit 124 includes another circuit for determining whether a complete message has been included on each of the input cards. This circuit includes a gate 1142, one input of which is enabled by the signal WCS. Another input is supplied with the signal C4/12 which is positive whenever the flip-flop 1354 has been set in the manner described above to provide an indication that a first, second, third, or fourth card is present as represented by the inverted signals C1-C4. The last input to the gate 1142 is enabled by the signal GC-IT2 which appears only at the beginning of the time slot next following the one from which the message is transmitted. Thus, if a code delete code which must terminate every message has not been received to reset the flip-flop 1354, the gate 1142 is enabled to provide a lower potential output which is supplied to one input of a gate 1144. The other input to this gate is supplied by the inverted signal NFSC. The output of the gate 1144 is forwarded through an inverter 1146 to provide the inverted signal 1/2 CD+NFSC.

This signal, the inverted signal DCTE, and the signal from the flip-flop 1334 all representing an error of one type or another are applied to the inputs of a gate 1336 to be forwarded through an inverter 1338, a gate 1340, and an inverter 1342 to provide the inverted signal PS. This signal is applied to the clear terminal of a flip-flop 1714 and clears this flip-flop so that a more positive enabling potential is applied to one input of a gate 1716. The remaining two inputs of the gate 1716 are enabled by the signals GC and IT2 to provide the inverted ERROR\* signal indicating the presence of an error and causing the operations described above. The flip-flop 1714 is primed to its reset condition by a gate 1712 by the signals GC and IT3 at the beginning of each time slot. The gate 1712 also resets a flip-flop 1700 which is used to provide an error signal for a parity error in any received character.

More specifically, the J and K terminals of a flip-flop 1710 are connected to the signal H provided from the first stage of the shift register 1116. The flip-flop 1710 is clocked by the signal WC so that the flip-flop 1710 counts "0/1" transitions. The flip-flop 1710 is cleared by two gates 1702 and 1706 and an inverter 1708 from the signals WCS and IT2 during each character. Thus, if the flip-flop 1710 provides a more positive output at its Q terminal, the K gate to the flip-flop 1714 is enabled during any character in which a parity error occurs, and the flip-flop 1714 is clocked by the inverted signal WCS to set the flip-flop 1714 to a state in which the  $\bar{Q}$  output terminal enables the gate 1716. This provides the inverted error signal

ERROR\* in the manner described above after the transmission of a complete message.

The flip-flop 1700 provides a means for clearing the flip-flop 1710 when the flip-flop 1714 is cleared or primed by the gate 1712 immediately following the transmission of a message. More specifically, when the flip-flop 1700 is set by the gate 1712, a gate 1704 becomes enabled on the next write in to the core when the signals WC and IT1 become available. The lower potential output of the gate 1704 is effective through the gate 1706 and the inverter 1708 to clear the flip-flop 1710. When, however, the flip-flop 1364 is set to provide the signals IWA and SCW in the manner described above in response to the receipt of an inverted card signal C1, C2, C3, or C4, an inverted signal B5/13 is provided which resets the gate 1700 and inhibits the gate 1704. Thus, the gate 1704 is used only during the parity check of the first received character in a message.

The circuit 124 also includes means for detecting the presence of two control characters or two code deletes during what appears to be a single card transmission. More specifically, this control is provided by a flip-flop 1150 having one input connected to the  $\bar{Q}$  terminal of a flip-flop 1154 which detects dual control characters. The C terminal of this flip-flop is supplied with a signal C4/12 from the Q terminal of the flip-flop 1354. The Q terminal of the flip-flop 1354 resets the flip-flop 1154 whenever a code delete is received at the end of a message. Thus, when the flip-flop 1354 is set on the receipt of the first control code during the reading of a card, a more positive potential is applied to the terminal C of the flip-flop 1154. If during the interval the C terminal is held at a more positive potential, another signal is received which translates to one of the signals C1-C4 a more positive potential in the form of a signal B2/6 and applied to the J terminal of the flip-flop 1154. This flip-flop is clocked by the signal WC so that the  $\bar{Q}$  terminal drops to a more negative potential and sets the flip-flop 1150 so that an enabling potential is applied to one input of a gate 1116.

To provide means for detecting the presence of two code deletes in which appears to be a single card message, a gate 1152 is provided, the output of which is connected to one input of the flip-flop 1150. The flip-flop 1154 on being cleared by a code delete in the manner described above develops a more positive signal C4/13 which is supplied to one input of the gate 1152. If another code delete is detected before the flip-flop 1354 is cleared so that the signal C3/6 is provided, this signal completes the enabling of the gate 1152 during the timing provided by the signal WCS, and the flip-flop 1150 is also set.

The setting of the flip-flop 1150 by either the gate 1152 or the flip-flop 1154 enables one input to the gate 1116. Another input to this gate is enabled during the guard character of the next following time slot by the signal GC, and the remaining input of the gate 1116 is enabled through an inverter 1114 by the inverted signal C3/1 during the timing signal IT1. The fully enabled gate 1116 provides an inverted output signal D2/4 which is connected to one input of the gate 1340. The application of the inverted signal D2/4 to the input of the gate 1340 causes the production of the inverted error signal ERROR\* in the manner described above by setting the flip-flop 1714. The flip-flop 1150 is cleared or reset by the signal WEC.

#### READING DATA OUT OF THE CORE STORAGE UNIT 120

##### USING THE CONTROL CIRCUIT 128

The core address counter 126 (FIG. 18) and the core storage unit 120 (FIG. 19) are controlled by the control circuit 128 (FIGS. 20, 21, and 22) to read data in the magnetic core storage unit 120 to the drum 202. This operation is initiated either under the control of an inverted END PHASE II signal derived from the central processing unit shown in the copending Stanis et al. application or at the conclusion of the

satisfactory storage of data from a delay line 110 into the core storage unit 120. More specifically, a gate 2100 is fully enabled by the signals WE, SP, and SCINH and the inverted signals RC and EIP, when delay line data has been stored in the core storage unit 120 and if an input error has not occurred or a control R operation is not required. The output of the gate 2100 or the inverted signal END PHASE II is effective through a gate 2101 to develop a signal PHASE III. This signal is effective through an inverter 2104 to set a flip-flop 2106 to enable one input to a gate 2112. This gate is enabled during the first drum bit timing signal T1 to set a flip-flop 2114. When the flip-flop 2114 is set, a flip-flop 2116 is clocked to provide the signal PHASE III \* and its inverted signal. The setting of the flip-flop 2114 also enables one input to a gate 2108 so that the flip-flop 2106 is reset on the signal T4 through the gate 2108. The resetting of the flip-flop 2106 is effective through a gate 2110 to reset the flip-flop 2114.

The setting of the flip-flop 2116 enables one input to a gate 2118, the other input of which is enabled if a patient charge search is not being performed in the central processor unit as represented by an inverted patient charge search signal PCS. The enabling of the gate 2118 sets a flip-flop 2120 so that a more positive potential is applied to the K terminal of this flip-flop. The flip-flop 2122 is clocked by the drum bit signal T2 to provide a synchronization signal SYNCH.

The setting of the flip-flop 2122 is also effective through a gate 2128 and an inverter 2126 to clear the flip-flop 2116 and terminate the signal PHASE III \*. The flip-flop 2116 can also be reset through the inverter 2126 and the gate 2128 by the signal PHASE III \* RESET.

The signal SYNCH developed by the flip-flop 2122 persists until the flip-flop 2122 is reset at the time that the flip-flop 2120 is reset. The flip-flop 2120 is reset by the inverted signal SYNCH RESET or under the control of a gate 2124. The gate 2124 is fully enabled to reset the flip-flop 2120 by the inverted signal CCR and the signals T3 and SYNCH. The signal CCR (FIG. 16) is present on all operations requiring the use of the central processor unit or when the inverted signal RC, QC, VC, U1C, or U3C is present. Thus, in the illustrative example in which the significant control signal is a signal XC representing a message, the inverted signal CCR enables the gate 2124 to remove the signal SYNCH after one character period.

The signal SYNCH is combined with the message control signal or the signal XC in a gate 2202 to fully enable this gate and set a flip-flop 2208 through a gate 2204 and an inverter 2206 to provide the inverted signal SPO. This signal is also provided by an inverted signal PO START and two signals RC and C RELEASE applied to the input of a gate 2200 from the central processor unit.

When the flip-flop 2208 is set, its negative-going output clocks a flip-flop 2210 whose K terminal is connected to ground so that the Q output of the flip-flop 2210 enables one input of a gate 2214. The remaining inputs to this gate are enabled by the signals TA5, UA4, T1, PHASE B, REV1, and C16. These signals are developed under the control of drum timing and specify a particular address or location of the drum to provide a reference point. Thus, when the gate 2114 is fully enabled at this reference point with respect to drum rotation, an inverter 2216 provides the output synchronization signal OSY which enables the development of the address signals such as the signals ADD08 and ADD16 (FIG. 15). This signal OSY disappears at the end of the signal PHASE B.

However, the output of the gate 2214 also sets a flip-flop 2218 to provide a special output synchronization signal OSY\*. This signal enables one input to a gate 2212, the other inputs of which are also enabled by the drum position identifying signals REV1, C16, and T1. Accordingly, the enabling of the gate 2212 clears the flip-flop 2210 and also develops an inverted address signal 000. Concurrent with the development of this signal, a gate 2010 enabled by the signals REV1, C16, and OSY\* develops an inverted signal RR1. The inverted signals RR1 and 000 initiate the readout of data from the core storage unit 120.

More specifically, the inverted signal 000 is applied to the like designated input of the core address counter 126 (FIG. 18) to prime the counter to its initial setting in which is stored the first bit of information derived from the first card in the message now stored in the core storage unit 120. The inverted signal RR1 is applied as an enabling input to a pulse generator 1900 (FIG. 19) which supplies read-restore signals R/R to the core storage unit 120 clocked by the fifth drum bit timing signal T5. The pulse generator 1900 is also enabled by the inverted signals WFIT, TC CLK, RR2, RR3, BRO, and CH\*, all of which are provided by the data processor unit except the inverted signal RR2. The generator 1900 is clocked by the timing signal T5 when enabled by any of these signals and is directly enabled by an inverted signal SRR1 provided from the central processor unit.

The read restore signal R/R reads the eight bit character out of the core storage unit 1200 located at the address defined by the signal 000 as eight output signals BIT 1—BIT 8 representing the eight bits of a character. These signals are applied to the inputs of eight corresponding inverters 2321—2323 and 2424—2428 which provide eight inverted output signals CMD1—CMD8. These signals are also forwarded through a second set of inverters 2331—2333 and 2434—2438 to provide the output signals CMD1—CMD8. These signals are applied to one input of seven gates 2341—2343 and 2444—2447 which are clocked by the drum bit timing signals T6, T7, and T0—T4, respectively. These gates are connected to the inputs of a gate 2460.

The eighth bit represented by the signal BIT 8 is stored in a bistable 2454, the output of which enables one input to a gate 2448 which is clocked during the fifth bit timing signal T5. It is desirable to store the BIT 8 signal in the bistable 2454 because of the fact that the read-restore signal R/R is generated with bit timing signal T5. The flip-flop 2454 is set by two gates 2450 and 2452 which are selectively enabled or disabled with the timing provided by the signals R/R, T6, and PHASE A in dependence on the absence or presence of the parity bit signal BIT 8.

The output of the gate 2460 provides a serialized core data output signal SCDE which is applied to the J terminal of the flip-flop 2464, and this signal is inverted by an inverter 2462 and applied to the K terminal of the flip-flop 2464. The flip-flop 2464 is clocked by the signal PHASE B to control the input supplied to a flip-flop 2466 which is clocked on PHASE A. The output derived from the Q terminal of the flip-flop 2466 provides a serialized core data signal SCD. Since the bit timing signals T0—T7 are clocked from the PHASE A signal, the use of a PHASE B clock for the flip-flop 2464 and a PHASE A clock for the flip-flop 2466 provides a one bit time delay so that bit "I" of the character, although clocked by the timing signal T6, appears as a component of the output signal SCD in the seventh time slot defined by the signal T7.

As set forth above, the transfer of data to the core storage unit 120 cannot be accomplished unless a buffer section on the drum 202 is available. Further, to provide adequate buffer storage for each output printer 204, four separate sections of buffer storage on a given output track of the drum 202 are provided. Since each track contains eight buffer sections, four available to one output printer 204 and four available to another output printer 204, it is necessary to read the data stored in the core storage unit 120 to the buffer track on the drum 202 eight separate times even though the data will be rendered effective and written onto the track in only one of the blocks, which block is preselected in response to the receipt of the address signal such as the signal ADD08 by the output control circuit 200. Further, it is thus necessary to synchronize the writing of data from the core storage unit 120 with the advance of the successive blocks of the assigned storage track on the drum 202. To accomplish this, an inverted block counter advance signal BLK CT ADV is developed by the drum clocking logic and is provided at the beginning of each of the eight blocks of the output buffer track of the drum 202. This signal is forwarded through an in-

verter 2006 to enable a gate 2008, the other input of which is supplied with the output synchronization signal OSY\*. The enabling of the gate 2008 sets a flip-flop 2012 to develop an output signal BOE and to partially enable four gates 2018, 2020, 2022 and 2024. One input of the gate 2022 is normally enabled from the Q terminal of a flip-flop 2016, and the other terminal of the gate 2022 is supplied with the serialized core data signal SCD. Thus, the gate 2022 repeats the data derived from the core storage unit 120 through a gate 2026 and an inverter 2028 to provide the inverted output signal DATA L. This signal is forwarded to the output control circuit 200 in which it is gated into the head of the drum 202 at the assigned track only during the block previously allotted by the control circuit 200 for this message.

The setting of the flip-flop 2012 also completes the enabling of a gate 2018, the other input of which is enabled by a reset gate 2004 to provide an inverted output signal RR2. The signal RR2 provides an additional enabling for the pulse generator 1900 when the inverted signal RR1 disappears. The setting of the flip-flop 2012 also completes the enabling of a gate 2024, the other two inputs of which are enabled by the flip-flop 2016 and a flip-flop 2030 so as to develop an inverted output signal IE1. The signal IE1 is returned to the input of a count pulse generator 1804 which is clocked with the signals PHASE B and T3. The pulse generator 1804 is thus enabled to advance the core address counter 126 from the preset address specified by the signal 000 and to access the second character of the message. The pulse generator 1804 is also enabled by a gate 1802, the input of which is derived from the central processor and by the inverted signals TC CLK and CH\* derived from the central processor.

Thus, the core address counter 126 is advanced on the timing signal T3, and the read-restore signals R/R are generated by the signal T5 to read the successive characters from the first card of the message from the core storage unit 120 and to convert these signals into serial form in the inverted output signal DATA L. Since it is desirable to have certain items of information in the message separated by spaces in the printed record, the circuit 128 includes means for inserting space codes where desirable. As an example, the first data entry on the first card 3600 includes "08118," whereas it is desirable to separate the designation of the nurse's station "08" from the room number "118" on the printed record shown in FIG. 38. Accordingly, when the core address counter 126 reaches a given setting representing the place at which the space is to be inserted, a space address network 2001 is enabled by the input signals AR2<sup>1</sup>-AR2<sup>n</sup> to supply a signal through a gate 2000 to partially enable a gate 2002. One input to this gate is enabled from the signal supplied at the Q terminal of the flip-flop 2016, and the remaining inputs are enabled with the timing signals T4 and PHASE B. The enabling of the gate 2002 sets the flip-flop 2004.

When the flip-flop 2004 is set, one input to the gate 2018 is inhibited to remove the inverted signal RR2 during the fourth bit timing interval and before the pulse generator 1900 is clocked on the signal T5. On the trailing edge of the signal T6, the flip-flop 2016 is set to provide a more positive potential at the Q terminal and a more negative potential at the Q terminal. The more negative potential at the Q terminal inhibits the gate 2022 to prevent the transmission of core data to the gate 2026 and also inhibits the gate 2024 to remove the inverted signal IE1 and prevent advance of the core address counter 126. This signal from the Q terminal of the flip-flop 2016 also inhibits one input to the gate 2002.

The setting of the flip-flop 2016 in providing a more positive potential at the Q terminal partially enables a gate 2020, one input of which is connected to the output of a gate 2014. The input to this gate is supplied with the inverted signals T4 and T6 so that the gate 2020 supplied mark bits to the input of the gate 2026 in the fourth and sixth bit timing intervals defined by the signals T4 and T6. As set forth above, the data supplied in the signal SCD has been time delayed a single timing pulse, and thus mark pulses in the fourth and sixth timing intervals

correspond to bits 6 and 8 and represent a space code. The flip-flop 2004 is reset by the inverted signal T2 during the same character interval in which the space code is generated, and the flip-flop 2016 is clocked on the trailing edge of the signal T6 to its reset condition to restore the circuit to its prior condition. Thus, further data from the signal SCD is supplied to the inverted output signal DATA L. In this manner, spaces are inserted at any desired point in the message by translating or decoding the setting of the core address counter 126.

When an end of message code is received at the end of the message material on the first card, the signals CMD1-CMD8 fully enable a code delete gate 2032 to provide an inverted signal CMDLF. This signal is inverted in an inverter 2038 and partially enables a gate 2040. A gate 2034 is enabled by the signals T1 and BOE and is effective through an inverter 2036 to complete the enabling of the gate 2040. This resets the flip-flop 2030 to inhibit the advance of the core address counter 126 by removing the inverted signal IE1. This resetting or setting of the flip-flop 2030 also develops an end of card signal EOC which is used to control the setting of the core address counter 126 to the address at which is located the next character to be taken out of the core storage unit 120.

More specifically, a network or circuit 1830 is provided for presetting the core address counter 126 to various settings on the receipt of each end of card signal EOC in dependence on the number of cards comprising the message then stored in the core storage unit 120. The circuit 1830 includes a flip-flop 1822 set by the inverted signal SAR3 which represents, for example, the address at which a third card message is stored. This circuit 1830 also includes a flip-flop 1824 which is set by the inverted signal SAR4 if a fourth card is included in the message. As set forth above, the inverted signals SAR3 and SAR4 are used to prime the counter 126 to the starting location or address for storing the message on third and fourth cards, respectively. Thus, when the flip-flop 1822 is set, a translating network 1820 is provided with a signal indicating the presence of a third card in the message. Similarly, when the flip-flop 1824 is set, the circuit 1820 is provided with an indication that a fourth card is included in the message. A gate 1826 which is fully enabled when both of the flip-flops 1822, 1824 are set provides an indication that the message does not terminate with a third card, and that a fourth card is included. The circuit 1830 also includes a two stage binary counter 1810 advanced on the timing signal T6 when the end of card signal EOC is present. Thus, the counter 1810 provides the circuit 1820 with a changing pattern of binary related signals indicating the number of end of card signals received from the circuit 128.

As set forth above, the second cards included in a message comprise control or address characters through the twelfth character of the message that is stored in the core storage unit 120. Since these addresses do not form any part of the desired output message and since the second card information is required in any valid message, the first signal EOC applied to the counter 1810 controls the translating network 1820 to supply an inverted output signal 213 which is applied to the corresponding preset address input to the counter 126. The second message was stored in the core storage unit 120 beginning at the preset address represented by the inverted signal SAR2 or 200. Thus, by presetting the counter 126 to the address provided by the inverted signal 213, the address characters are skipped. This information is also gated out of the circuit 1820 on the signal EOC.

The flip-flop 2030 is reset by the inverted signal T0 to terminate the end of card signal EOC. The resetting of the flip-flop 2030 also returns the enabling potential to the gate 2024 so that the inverted signal IE1 is provided to permit incremental advance of the core address counter 126 from the address to which it was preset by the inverted signal 213. Thus, the circuit 128 now transmits the material on the second card of the message.

This operation continues in the manner described above until the next end of card is signified by the detection of the

code delete. At this time, the flip-flop 2030 is again set to develop the end of card signal EOC. This time the network 1830 controls the circuit 1820 to provide one of two output addresses. If a third card is included in the message, the inverted output signal 400 is provided to reset the counter 126 to this setting. Alternatively, if the flip-flop 1822 has not been set, the receipt of the second end of card signal EOC advises the circuit 1820 that the core address counter 126 should be jumped to the setting at which are located the three digits of the key identification, i.e., at the address represented by the inverted signal 674. After the core address counter 126 is primed to this new address, the flip-flop 2030 is reset, and the message from the third card or from the key is read out of the core storage unit 120.

If a fourth card is provided, the flip-flop 1824 is set so that on receipt of the next end of card signal EOC, the counter 126 is primed to the address provided by the inverted signal 600 corresponding to the address at which this counter was set when the fourth card was read into the core storage unit 120. The fourth card message is then read out of the core storage unit 120 followed by another end of card signal EOC. At the termination of the second and third card messages, in dependence on the length of the messages, the circuit 128 always primes the core address counter 126 to the position provided by the inverted signal 674 to read the three digits of the key designation out of the core storage unit 120.

When the digits identifying the key have been read out of the core storage unit 120, the core address counter 126 is advanced to a predetermined position, and in the illustrative example, it is the position set by the inverted priming signal 677. At this time, a network 241 translates the binary output signals AR2<sup>a</sup>—AR2<sup>b</sup> and fully enables the gate 2042 so that a more negative potential is applied to one input of a gate 2044, the enabling of the gate 2042 being completed by the signal BOE. The other input to the gate 2044 is normally held at a more positive potential at the output of a gate 2054. Accordingly, when the output of the gate 2042 drops to a lower potential, the output of the gate 2044 becomes more positive and fully enables a gate 2048 during the signal T4. This provides an inverted output signal R1 which sets a flip-flop 2050 and also supplies a momentary start signal to the date and time generator to add the date and time information shown on the last line of FIG. 38 to the inverted signal DATA L.

The setting of the flip-flop 2050 partially enables the gate 2054 so that during the signal T4, an inverted output signal 000\* is generated to prime the core address counter 126 back to its initial starting position in which is accessed the first character of the message on the first card. The inverted signal 000\* is also forwarded through the gate 2044 to briefly hold the inverted signal R1 on during the signal T4 and until the counter 126 is set. During the following timing signal T7, a gate 2052 is enabled to provide an inverted signal R3 which resets the flip-flop 2012 to remove the inverted signals IE1 and RR2 and the signal BOE. This arrests reading of the unit 120 and any advance of the counter 126. The flip-flop 2540 is reset by the inverted signal TO, and only date and time are supplied to the inverted signal DATA L until the start of the next drum track block.

At that time, the inverted signal BLK CT ADV again sets the flip-flop 2012 to return the signal BOE and the inverted signals IE1 and RR2. The core storage unit 120 is now read as the counter 126 is advanced. The control circuit 128 now reads the entire message stored in the core storage unit 120 and adds the date and time data a second time in the manner described above. This is repeated six more times so that the message stored in the core storage unit 120 is read out as the inverted signal DATA L eight times in total during the eight blocks forming a single revolution of the drum 202.

When the drum initiates the next following revolution defined by the signal REV2 a gate 2220 is enabled at the same reference point defined by the signals TA5, UA4, T5, PHASE B, and C16. The enabling of the gate 2220 resets the flip-flop 2208 and terminates the inverted signal SPO. Further, the out-

put of the gate 2220 is effective through an inverter 2222 to complete the enabling of a gate 2224 so that a negative-going clock pulse is applied to the T terminal of a flip-flop 2226. The K terminal of this flip-flop is returned to ground, and the output from the gate 2224 sets the flip-flop so that a more positive potential is applied from its Q terminal to the J terminal of a flip-flop 2228. During the following timing signal IT7, the flip-flop 2228 is clocked to enable one input to a gate 2230. During the following timing signal defined by the signal IT1, the gate 2230 is fully enabled to reset the flip-flop 2218. This removes the special output synchronization signal OSY\*. It also generates the inverted signal EOP\* and clears the flip-flop 2226 so that the flip-flop 2228 is thereafter cleared and an inhibit applied to the gate 2230 to terminate the inverted signal EOP\*. As set forth above, the signal EOP\* is used to reset the circuit 104 and provides an indication that the data from the card reader 102 has been satisfactorily transferred through the delay line 110 and the core storage unit 120.

#### OUTPUT CONTROL CIRCUIT 200

The control circuit 200 (FIGS. 25—29) takes the serialized core storage data in the form of the inverted signal DATA L and writes this data onto one of the four blocks in the buffer track on the drum 202 assigned to each of the output stations such as the station including the printer 204. When this data has been stored on the buffer track on the drum 202, the circuit 200 then initiates an outputting operation during which the data stored on any block containing a complete message is transferred off the drum 202, converted to telegraph signal timing, and forwarded to a selected output printer such as the printer 204. In addition, the control circuit 200 inserts certain control signals in the message information derived from the drum 202.

#### I. Assigning Block on Drum 202 and Writing Data from Core Storage Unit 120 into Selected Block

As set forth above, the output buffer tracks on the magnetic drum 202 are each effectively divided into two halves by the signals OP1CT and OP2CT, and each of these halves of the track is divided into four separate storage blocks each capable of storing a complete message by the timing signals BLK1CT—BLK4CT. FIGS. 25—28 of the drawings illustrate the portion of the control circuit 200 assigned to data recorder 204 at the nurse's station identified as "08" to which is assigned four blocks in the first half of a given output buffer track defined by the signal OP1CT. A portion of this circuit illustrated in these Figures of the drawings is shared by a similar circuit to which is assigned the four blocks of buffer storage occupying the second half of the track defined by the timing signal OP2CT.

The circuit 200 includes for each of the outputs a counting circuit such as a counting circuit including two flip-flops 2522 and 2524 which is in a setting representing an idle block on the assigned output track at any given time. Assuming that all four of the blocks available to output to the nursing station identified as "08" are empty, the counter including the flip-flops 2522 and 2524 is cleared to its normal setting in which the inverted output signals A and B of these flip-flops are at a more positive potential. A gate 2508 is partially enabled by the inverted input signals A and B. Further, if all of the blocks are empty, four status storage flip-flops 2504, 2530, 2532, and 2534 representing blocks one, two, three, and four are all reset, and the third input to the gate 2508 is enabled.

When the nurse's station identified as "08" is addressed in the manner described above, the inverted signal ADD08 is applied to one input of a flip-flop 2516, and this flip-flop is set to partially enable a gate 2526. Another input to the gate 2526 is supplied by the signal SDG1. This signal is generated on FIG. 29 of the drawings by a gate 2920. One input of the gate 2920 is supplied with the signal OP2CT which defines the second block on the track through an inverter 2912. Thus, one input

to the gate 2920 is enabled only during the first half of the track when the signal OP2CT is not present. The other input to the gate 2920 is supplied by a gate 2914 and an inverter 2916. The gate 2914 is enabled by the signals T7, REV2, and BLK CT ADV. The signal REV2 defines the second revolution of a three revolution cycle of the drum 202, and the signal BLK CT ADV appears for a short duration at the beginning of each of the eight blocks and is also used to advance the counter in the drum clock logic which provides the block defining signal BLK1CT—BLK4CT. Thus, with this timing, the inverted signal SDG1 is provided by the gate 2920, and a gate 2918 provides the same signal during the second half of the track.

Thus, the gate 2526 is enabled by the signal SDG1 at the beginning of each of the four blocks during the first half of the storage track assigned to the address "08." When the first block signal BLK1CT appears following the setting of the flip-flop 2516, the gate 2508 is fully enabled and is effective through a gate 2514 to complete the enabling of the gate 2526. The gate 2526 sets a flip-flop 2528 so that a more positive enabling potential is applied to two gates 2520 and 2518. When the PHASE B signal appears, the gate 2518 is fully enabled and is effective through an inverter 2519 to complete the enabling of a gate 2500, the other input of which is also supplied with the first block signal BLK1CT.

The enabling of the gate 2500 sets the flip-flop 2504 to generate the signal IST1. When the flip-flop 2504 is set, the gate 2508 is disabled to apply an inhibit to one input to the gate 2526. During the timing interval defined by the signal TO, the gate 2520 is fully enabled to reset the flip-flop 2516 and thus removes another enabling signal from the gate 2526.

The more positive output signal from the set flip-flop 2504 which indicates that the first block has been seized to receive a message enables one input to a gate 2506, the output of which is forwarded to a gate 2507. When all of the flip-flops 2504, 2530, 2532, and 2534 are set, thus indicating that all of the blocks available to output to the nursing station identified as "08" have been seized for use, the gate 2506 is fully enabled, and the gate 2507 develops the full or busy signal FULL08. The more negative signal provided by setting at least one of the flip-flops such as the flip-flop 2504 is also forwarded through a gate 2510 to provide the signal STAT1 which indicates that at least one message has been or is being stored in one of the blocks assigned to the station. The output from the gate 2510 is also forwarded to an inverted 2512 to provide the inverted signal STAT1.

When the bistable 2528 is set, the lower potential output from this flip-flop is forwarded through a gate 2630 to enable one input of a gate 2632. The other input of this gate is supplied with the signal DATA L which is the serialized data from the core storage unit 120. The output of the gate 2632 is coupled through an inverter 2634 to provide the signal DATA IP which is applied to the head of the buffer storage track on the drum 202 assigned to the indicated station. The other input to the gate 2630 is supplied from the flip-flop similar to the flip-flop 2528 in the circuit assigned to the second half of the same storage track on the drum. The output of the gate 2630 also supplies a signal MWE which is used to enable the associated drum head.

At the beginning of the next block, an inverted block strobe signal BS is applied to the flip-flop 2528 to return this flip-flop to its reset condition. This removes the enabling potential for the gate 2632 and prevents any further writing of data onto the drum since it has been stored in the first block thereon. As set forth above, a signal DATA L includes the same message repeated eight times, but only one of these messages is transferred to the drum 202.

The resetting of the flip-flop 2528 also clocks the input flip-flop 2522 so that in the illustrative example the Q terminal of this flip-flop rises to a more positive potential. This removes the partial enabling from the gate 2508 and partially enables the gate 2509 assigned to the second block in the first half of the buffer drum track. Thus, the next message will be stored in

the second block whenever the inverted address signal ADD08 next appears indicating the presence of a message in the core storage unit 120 for transmission to the output printer 204.

## 2. Transferring Data from the Drum 202 to the Output Printer 204

The circuit shown on FIGS. 26—28 of the drawings transfers the data derived from the drum 202 with drum bit timing to the output printer 204 with telegraph timing. The circuit 200 includes a counter including two flip-flops 2604 and 2606 which is advanced one step for each teletype character. More specifically, an input flip-flop 2600 is set by the inverted telegraph timing signal TT7 to partially enable a gate 2602. This gate is fully enabled by the telegraph timing signal TT1 to clock the input stage 2604. Thus, the counter including the stages 2604 and 2606 is advanced on each output character.

The Q and  $\bar{Q}$  terminals of the flip-flops 2604 and 2606 are connected to the inputs of four gates 2608, 2622, 2624, and 2628 so that these gates are enabled in successive settings of the counter. When the gate 2608, for instance, is fully enabled, an inverter 2610 develops an output signal OP1BK1 and partially enables a gate 2612. The remaining inputs to the gate 2612 are provided by the signals BLK1CT and IST1. The presence of the signal IST1 indicates that a message has been stored in the first block which requires transfer to the printer 204. The signal BLK1CT times the gate 2612 to enable this gate during only the first block. When the gate 2612 is fully enabled, a more negative output from this gate is forwarded through the gate 2614 to enable one input to a gate 2616. The remaining inputs to the gate 2616 are provided by the inverted signal AOE and the signals COMP and CROP1.

Each time that the master strobe signal MS appears at the beginning of each drum revolution, a gate 2732 is enabled by the signal MS and the inverted signal INQ1. The low output from the gate 2732 sets a flip-flop 2738 to provide the inverted signal AOE. Thus, this signal also partially enables the gate 2616.

The signal CROP1 is developed by a gate 2924 having one input enabled during the first block on the drum or whenever the signal OP2CT is not supplied to the input of the inverter 2912. A second input to the gate 2924 is enabled by a character enabled signal CHAR EN developed by drum clock logic in the interval between the block strobe pulses or signals BS. The remaining input to the gate 2924 is enabled by an inverted signal REV3 applied to the input of an inverter 2928. The signal REV3 is generated during the third revolution of the three revolution cycle of the drum 202. When the gate 2924 is fully enabled, an inverted signal CROP1 is developed. A gate 2922 develops an inverted signal CROP2 with timing during the second half of the track. Thus, the signal CROP1 partially enables the gate 2616 during the third revolution of the drum after the disappearance of the block strobe signal BS. The last input to the gate 2616 provided by the signal COMP is enabled whenever the drum has been advanced to the location at which is located the next character to be supplied to the output printer 204.

The inverted signal STAT1 which is supplied through a gate 2730 to apply a more positive potential to the D input of the first of three D-type flip-flops 2740, 2742, and 2744 causes the automatic generation of a sequence of signals for supplying a start code to the printer 204 to prepare this printer for receiving the following message or messages. Thus, when the leading edge of the signal TTO is applied to the T terminal of the flip-flop 2740, this flip-flop is set to apply a more negative potential to one input of a gate 2752. The more positive potential at the output of the gate 2752 removes the continuous more negative potential previously supplied by the gate 2752 and thus changes the output of a gate 2720 from a continuous high level mark condition to a low level space condition. During the persistence of the signal TTO, both inputs to a gate 2748 are at a more positive potential, and the low output

of this gate sets a flip-flop 2754 so that its upper gate provides a more positive signal for partially enabling two gates 2618 and 2710 and for supplying a signal 1MK1. When the flip-flop 2740 is set, the more negative potential provided at its Q output also drives the output of the lower gate in the flip-flop 2754 to a more positive potential. When the signal TTO terminates, the gate 2748 is no longer fully enabled, and the signal from the Q terminal of the set flip-flop 2740 resets the flip-flop 2754 so that a more negative potential is provided at the output of the upper gate. This more negative potential holds the output of the gate 2720 at a high level or mark condition. Thus, the line to the printer 204 is supplied with a single space signal by the gate 2752 during the timing signal TTO and is thereafter returned to a mark condition through the timing interval defined by the signals TT1—TT10 (See FIG. 35).

At the leading edge of the next signal TT0, the flip-flop 2742 is set so that a more negative inhibiting signal is applied to one input of the gate 2748 and also to another input to the gate 2752. During the following output character timing interval, a gate 2750 is fully enabled by the signal TT4 in the fourth character position to apply a more negative signal to one input of the gate 2720. This, however, does not produce any change in the output inasmuch as the signal provided by the flip-flop 2754 maintains the line to the printer 204 in a continuous marking condition.

On the leading edge of the next following signal TT0, the flip-flop 2744 is set so that a more negative signal is supplied at its Q output terminal. This signal pulls the upper gate in the flip-flop 2754 to a condition in which a more positive signal is applied to the connected input of the gate 2720. The inputs to the gate are now all at a more positive potential, and the line to the printer 204 is in a continuous spacing condition. Thus, the application of any low level signal to the input of the gate 2720 results in the transmission of a mark signal to the printer 204. Further, the high level signal provided at the output of the flip-flop 2754 provides an enabling signal for the gates 2618 and 2710 to enable data to be transferred to the printer 204.

The signal COMP which completes the enabling of the gate 2616 to read one character from the drum 202 to the recorder 204 is developed by the circuit shown on FIG. 28 and is provided when the position in the block containing the message to be transmitted is reached at which is stored the next character to be printed. More specifically, a counter circuit 2800 is provided containing a series of flip-flops which are advanced in normal binary counting progression under the control of an inverted signal LD supplied from the flip-flop 2700. The counter 2800 is reset by an inverted signal RS. In its reset condition, the counter 2800 provides a pattern of input signals to a series of transfer gates, two of which 2204 and 2206 are illustrated, representing the binary complement of the character to be transferred. This binary complement is easily derived by taking the output signals from the Q terminals of the flip-flops. As an example and assuming that the counter 2800 has been primed to a reset position representing that the first character is to be printed out, all of the outputs from the counter 2800 are at a more positive potential.

The circuit 200 includes a second counter 2810 including a plurality of flip-flops connected for normal binary counting progression under the control of an input signal BLKEN·TO'. This signal appears in the interval following the block strobe signal at a drum character timing rate. Thus, the counter 2810 is advanced a step for each character on the drum. The counter 2810 is reset once during each block by the inverted signal BS. The input from the counter 2800 is conveniently applied to the prime terminals of the individual flip-flops in the counter 2810 so that a conductive pattern set in the counter 2810 by the counter 2800 is the complement of the value stored in the counter 2800.

The transfer of the counter from the counter 2800 into the counter 2810 is controlled by gates similar to the gates 2804 and 2806, one input of each of which is connected to the out-

put of an inverter 2802. The input to the inverter 2802 is supplied with an inverted signal STOP 1. This signal is developed on FIG. 29 of the drawings. More specifically, this signal is developed by a gate 2906, one input of which is enabled by the inverted signal PHASE B through an inverter 2908. Another input to the gate is enabled by the signal T7, and a third input to the gate 2906 is enabled during the first half of the drum track by the signal OP2CT which is inverted by the inverter 2912. The remaining input to the gate 2906 is enabled from the Q terminal of a flip-flop 2902 which is set by the signal BLK CT ADV through an inverter 2900 at the beginning of each block. Thus, the inverted signal STOP 1 is effective through an inverter 2802 to prime the binary complement of the desired character stored in the counter 2800 into the counter 2810.

In the illustrative example, all of the stages of the counter 2810 are primed on because the counter 2800 is in this normal condition representing the desire for a first character, and all of the inputs to the gate 2812 are thus enabled. The complete enabling of the gate 2812 is effective through an inverter 2814 to partially enable a gate 2816, the other input of which is enabled by the signal 1. Thus, the gate 2816 is fully enabled to provide a signal output which is effective through a gate 2818 to provide the compare signal COMP.

When the signal COMP is provided, the gate 2616 is fully enabled, and the flip-flop 2600 is reset in inhibit advance of the counter including the flip-flops 2604 and 2606. Further, the more negative output from the gate 2616 is effective through an inverter 2620 to apply a more positive signal to the input of the flip-flop 2700. The flip-flop 2700 is clocked through the gate 2618 by the signal TO·PHASE A. This signal is developed in FIG. 29 under the control of a flip-flop 2930 which is clocked by the inverted signal PHASE B when the signal T7 is applied to the D input of the flip-flop 2930. The Q terminal of the flip-flop 2930 provides a TO' output which is gated with the signal PHASE A in the gate 2932. The output of the gate 2932 provides an inverted signal TO·PHASE A. This signal also clears the flip-flop 2902 and thus removes the inverted signal STOP 1, as well as an inverted signal STOP 2 which is generated by a gate 2904 during the second half of the track.

When the flip-flop 2700 is clocked by the output of the gate 2618, the Q terminal supplies a more positive potential and the Q terminal provides the inverted signal LD which advances the counter 2800 a single step to indicate that the second character is the next character to be supplied to the printer 204. A more positive potential at the Q terminal of the flip-flop 2700 partially enables a gate 2706, the other input of which is supplied with a signal PHASE B. Thus, the gate 2706 is fully enabled and is effective through a gate 2708 to complete the enabling of the gate 2710 to supply negative-going clock pulse to the T terminal of the eight bit shift register 2712. The A input of the input gate to the register 2712 is enabled by the flip-flop 2700, and the B terminal of this gate is supplied with a signal DATA which is the data signal derived from the head of the drum. Thus, the first character stored in the selected block of the drum track is shifted into the shift register 2712 using the timing provided by the signal PHASE B.

At the end of the transmission of this single character, the counter 2810 is advanced by the signal BLKEN·TO', and the compare signal COMP is removed from the gate 2616. Thus, on the following signal TO·PHASE A, the flip-flop 2700 is clocked to terminate the inverted signal LD and to remove the enabling from the gate 2706 in the input to the shift register 2712. The more positive signal at the output of the gate 2616 also removes the resetting signal from the flip-flop 2600, but the character counter including the flip-flops 2604 and 2606 will not be advanced because of the long character time cycle for the output printer defined by the signals TT1—TT7 as compared with the time required for a three revolution cycle of the drum 202 (See FIG. 35).

To read the first character out of the shift register 2712 to the output recorder 204, the shift register 2712 is clocked by a

signal  $\overline{ATC+REV3}$ . This signal is generated on FIG. 29 by a gate 2926 supplied with the inverted signal REV3 and a signal ATC. Since the shift register 2712 is loaded during the third revolution of the drum 202 in a three revolution cycle, i.e., the inverted signal REV3 controls the enabling of the gate 2924 supplying the inverted signal CROP1, the output of the gate 2926 is held at a more positive potential during the third revolution. However, during the first and second revolutions of the drum, the signal ATC is applied to the gate 2926 at the clock rate of the output recorder timing signals TT1—TT7, and the gate 2926 provides the negative-going signal  $\overline{ATC+REV3}$ . This signal is forwarded through the gate 2708 to enable the gate 2710 at the output bit clock rate and clocks the bits stored in the register 2712 to one input of a gate 2718. On input to the gate 2718 is normally held at a more positive potential by a flip-flop 2715, and the third input to the gate 2718 is supplied with the inverted signal TT0. Thus, the gate 2714 provides a more positive output during the first bit interval defined by the signal TT0 which is effective through the gate 2720 to provide an initial space signal to the printer 204. During the next seven output character bit timing intervals defined by the signals TT1—TT7, the first seven bits of the character are shifted out of the register 2712 through the gates 2718 and 2720 to the output printer 204. This occurs during the first and second revolutions of the three revolution cycle of the drum 202. If the bit is a mark, the Q output terminal of the shift register 2712 provides a more positive signal that completes the enabling of the gate 2718 to apply a more negative input to the gate 2720. This results in a more positive output signal representing a mark on the signaling line to the printer 204. During the intervals defined by the timing signals TT8—TT10, the clock logic circuit develops an inverted signal TTMK which holds the output of the gate 2720 in a marking or high level condition. This provides the stop code during the intervals defined by the signals TT9 and TT10 and inserts an arbitrary parity bit in the interval defined by the signal TT8. Since, however, the output recorder 204 does not require a parity bit, the accuracy of the message transmission is not impaired.

This transfer of data to the output printer 204 takes place during the first and second revolutions of the drum in the three revolution cycle. At the beginning of the third revolution, the setting of the counter 2800 is again transferred to the counter 2810 which is advanced to the position occupied by the second character of the message. This second character is now read out of the drum 202 to the shift register 2712 using the drum timing provided by the signal PHASE B. During the following first and second revolutions of the drum 202, the second character is shifted out of the register 2712 to the output printer 204. This cycle is repeated to transfer all of the characters of the message from the drum to the recorder 204.

If, during the transfer of data from the drum 202 to the printer 204, a character supplied to the shift register 2712 does not satisfy an even bit parity check, a code representing a question mark is transmitted to the recorder 204 in place of the character in the shift register 2712. More specifically, the flip-flop 2715 provides a parity check. This flip-flop is cleared so that the  $\overline{Q}$  terminal provides a more positive output potential to enable the output gate 2718 by an inverted signal REV2 during each second revolution. The clock terminal T of the flip-flop 2715 is connected to the output of the gate 2704 and receives a positive-going clock pulse for each bit shifted into the register 2712 during a character. The gate 2704 is enabled by the flip-flop 2700 and an inverted signal DINH1 and is supplied with the incoming data signal DATA and the timing signal PHASE B.

If at the end of the reception of a character by the register 2712, an odd number of bits has been received, the Q terminal of the flip-flop 2714 provides a more positive output potential, and the  $\overline{Q}$  terminal of this flip-flop provides a more negative potential which inhibits the gate 2718 to prevent transmission of a character through the gate 2720 to the recorder 204. The other input to the partially enabled gate 2716 is supplied with

an inverted signal TT0+7 which controls the gate 2716 to insert the code for a question mark at this point in the message. More specifically, the gate 2716 is normally fully enabled to hold the line to the printer 204 at a high potential representing mark signals except during the timing intervals defined by the signals TT0 and TT7. During these intervals, the gate 2716 is inhibited so that the output line drops to a lower level representing spaces affording the start space and a space in the seventh bit position. The flip-flop 2715 is cleared by the inverted signal REV2.

The flip-flop 2714 provides a null detector which detects the end of the message by the absence of any bits of information in the incoming signal DATA during an interval in which the shift register 2712 has been enabled to receive intelligence. At the end of each block, the inverted signal BS resets a flip-flop 2702 so that a more positive signal is applied to the clear terminal of the flip-flop 2714. The D terminal of this flip-flop receives a more positive potential when the flip-flop 2700 is set to gate a character into the shift register 2712. If a mark bit is received in the incoming signal DATA, the gate 2704 is enabled as described above, and the flip-flop 2702 is set to hold a more negative potential on the C terminal of the flip-flop 2714. This prevents the generation of the reset signal RS. If, however, the flip-flop 2702 is not set during the interval in which it is enabled by the set flip-flop 2700, the next following signal TO-PHASE A is effective through the gate 2618 to clock the flip-flop 2714 to a condition in which a more positive potential is provided at the Q terminal developing the signal RS, which setting would not have been possible if the C terminal of the flip-flop 2714 is held negative by the flip-flop 2702. Generation of the reset signal RS clears the circuit 200 to indicate that the complete message has been transferred from the drum 202 to the output recorder 204.

More specifically, the signal RS enables one input to a gate 2502, the other input of which is enabled by the signal OP1BK1 derived from the output of the gate 2608 representing the current setting of the character counter. The fully enabled gate 2502 resets the flip-flop 2504 to terminate the signal IST1 and one enabling signal to the full gate 2506 and to also terminate the generation of the signal STAT1 is none of the flip-flops 2530, 2532, and 2534 is set at this time indicating other messages awaiting processing. The inverted signal RS also resets the counter 2800 to its initial setting to permit the selection of the first character in the next message to be processed. The inverted signal RS also resets the flip-flop 2600 so that the counter including the flip-flops 2604 and 2606 can be advanced to select the next block having a message stored therein.

To avoid maintaining the output recorder 204 in an operating condition during intervals in which output printing operations for not required, the circuit 200 includes a circuit for automatically transmitting a control H which shuts off the motor in the printer 204 when the last message in the four drum buffer areas or blocks has been transmitted. More specifically, when the last of the flip-flops 2504, 2430, 2532, and 2534 has been reset, the signal STAT1 is terminated, and a more negative potential is applied to the D terminal of the flip-flop 2740 by the gate 2730. During the next following signal TT0, the flip-flop 2740 is clocked so that a more positive potential appears at its  $\overline{Q}$  terminal and a more negative potential appears at its Q terminal. The positive potential at its  $\overline{Q}$  terminal partially enables a gate 2750 so that during the fourth character bit timing interval a signal TT4 completes the enabling of the gate 2750 to apply a more negative input to the gate 2720. This supplies a mark to the printer 204 and together with the preceding space signals and the following mark signals provided in the timing intervals TT8—TT10 provided by the inverted signal TTMK provides a complete control H character for stopping the motor in the printer 204.

On the leading edge of the next signal TT0, the flip-flop 2742 is reset so that both inputs to the gate 2752 are now at a more positive potential, and the low output of the gate 2752 holds the output of the gate 2720 at a high level marking con-

dition. The low output from the Q terminal of the reset flip-flop 2742 inhibits the gate 2750 to prevent further generation of mark signals by the signal TT4. On the next signal TT0, the flip-flop 2744 is reset.

The control circuit 200 also includes means by which input data derived from the central processing unit is supplied as the signal DATA for direct recording on the output recorder 204. When demand for this output condition arises, an inverted signal INQ1 is supplied which is effective through the gate 2730 to apply a more positive potential to the D terminal of the input flip-flop 2740. This signal also inhibits the gate 2732 to prevent the setting of the flip-flop 2738 to generate the inverted signal AOE.

The inverted signal INQ1 is effective through an inverter 2733 to partially enable a pair of gates 2734 and 2735. One or the other of these two gates is fully enabled in dependence on whether or not the output recorder 204 has messages waiting in the drum buffer storage track. More specifically, if no messages are awaiting transfer to the printer 204, the gate 2736 is enabled by the inverted signal STAT1 and the output timing signal TT10 to reset the flip-flop 2738 so that a more positive enabling potential is applied to one input of a gate 2746. Alternatively, if messages are stored in the drum buffer track associated with the output printer 204 when the inquiry is received, the gate 2734 is fully enabled whenever the reset signal RS appears at the termination of the output operation then in progress. The enabling of the gate 2734 also resets the flip-flop 2738 to partially enable the gate 2746.

The timing signals TT0 sequentially set the flip-flops 2740, 2742, and 2744 to produce the operations described above. When the flip-flop 2744 is set, the gate 2746 is fully enabled to provide a signal AOE which advises the central processor unit that it is now possible to supply output signals to the printer 204. This is supplied to an input signal DATAX to the gate 2720.

To provide means for detecting an abnormal overrun condition in the counter 2800, a gate 2801 is provided. This gate is fully enabled when the counter 2800 advances beyond the count normally used to select characters from the block on the buffer storage track of the drum 202. When the gate 2801 is fully enabled, the inverted signal DINH1 is generated. This signal is applied as an inhibit to one input of the gate 2704 and thus prevents the setting of the flip-flop 2702. If the flip-flop 2702 is not set, the flip-flop 2714 generates the reset signal RS because it appears that no data bits have been received in the signal DATA during a character readout. Generation of the reset signal RS restores the circuit 200 to a normal condition in the manner described above.

#### CASHIER'S OFFICE 103

The cashier's office 103 (FIGS. 30—32) in general does nothing more than add a receipt serial number and a dollars and cents amount to the message supplied by the card reader 102 associated with the cashier's office 103 whenever a control R&W second card is included as a part of the message.

The card information supplied from the reader 102 is normally supplied through a series of gates 3111—3118 and through additional gates 3132—3137 and related output inverters, such as the inverter 3142, to generate the bit signals D1—D8, respectively. These signals are supplies as inputs to the gates 720, 722 (FIG. 7) in the circuit 104 having access to the cashier's office 103. They are also applied to the inputs of the register 670 for control reasons, but the output of the register 670 need not be connected to the gates 720 and 727.

These signals D1—D8 are also returned to the input of a gate 3004 so that when the inverted signal LPR is received concurrently with the other input signals shown on the gate 3004 which represent a control W, the gate 3004 is fully enabled to set a flip-flop 3028. The setting of the flip-flop 3028 partially enables a gate 3026, the remaining inputs of which are enabled by the inverted signal LPR passed through an inverter 3001 and the signals JT4 and LP. When the gate 3026 is

enabled, a flip-flop 3024 is set so that the more positive signal from its Q output removes a clear signal from a conventional counter 3000 and a count signal from the input of a receipt numbering counter including three conventional binary coded decade counters 3100, 3102, and 3104 which are connected in series with the counter 3100 providing the input stage. The more positive output from the Q output of the flip-flop 3024 is effective through a gate 3030 and an inverter 3122 to inhibit the gates 3112—3118 and one AND input to the gate 3111. This prevents data transmission from the card 3600 to the delay line 110, but the card reader 102 continues to supply sprocket signals which clock the data input from the office 103 into the delay line 110. This signal partially enables a pair of gates 3120 and 3126. It also partially enables a gate 3002.

In the first setting of the counter 3000, the inverted signal 0 is effective through a gate 3124 to complete the enabling of the gate 3126 so that this gate applies an inhibit to the gate 3120 and is effective through the gates 3136 and 3137 to provide the output signals D6 and D8 representing a space code. This code is stored in the delay line 110 and results in the return of the inverted signal LPR when this code has been transferred to the delay line 110. The inverted signal LPR is effective through the inverter 3001 to enable the gate 3002 to advance the counter to its second setting. In the second, third, and fourth settings, the inverted signals 1, 2, and 3 are generated to supply space codes in these positions, and the counter 3000 is then advanced to its next setting supplying the signal 4. The signal 4 enables a group 3105 of gates to read out the value of the hundreds digit of the receipt number as a group of signals A1—A4. These signals are translated in a network 3210 to provide a marking condition representing the value of the hundreds digit of the receipt. The network 3210 includes a parity bit generator logic circuit 3212 which selectively supplies a parity bit where necessary. These signals are transferred to the delay line 110, and the counter is advanced to its next setting in which a signal 5 is generated. A signal 5 enables a group of gates 3103 to read out a group of signals B1—B4 to the network 3210 to supply the value of the tens digit of the receipt to the delay line 110. The counter 3000 is advanced to its next setting in which the signal 6 is developed to enable a group 3101 of gates to selectively supply a group of output signals C1—C4 representing the value of the units digit of the receipt number. This number is again translated in the network 3210 and supplied to the delay line 110. The counter 3000 is then advanced to its next position supplying an inverted signal 7 which controls the gates 3124 and 3126 to supply a space code for storage in the delay line 110. The storage of this character advances the counter 3000 to its next position in which a signal 8 is developed.

In this and following settings of the counter 3000, a dollar amount is transmitted for storage in the delay line 110. This dollar amount is provided by manually set switches at the cashier's office 103, and the setting of each of the switches which is decimal in nature is converted to binary code by diode translating networks similar to the one illustrated as 3240. Accordingly, when the signal 8 is generated, this signal is forwarded through the diode logic network 3240, and a group of pulse shaping networks indicated generally as 3235 enable one input of a group 3230 of gates. The other input to these gates is enabled by the flip-flop 3024 and the group 3230 of gates provides output signals E1—E4 in accordance with the binary coded value of the ten thousands digit represented by the switch input to a ten thousands dollar digit switch logic circuit 3200. This digit is stored in the delay line 110 in the manner described above, and the counter 3000 is advanced to its next setting in which the signal 9 is developed.

When a signal 9 reads out the value of the thousands digit of the amount, the counter 3000 is advanced to develop the signals 10—12 to read out the values of the hundreds, tens, and units dollars of the amount.

It should be noted that after the counter 3000 is advanced beyond the position at which the inverted signal 7 is developed, all of the inputs to the gate 3120 remain enabled

until the counter 3000 reaches the setting at which the inverted signal 13 is developed. Thus, the output of the gate 3120 continuously supplies signals D5 and D6 which are necessary for numerical information. In effect, data bits provided by the decoding network 3210 are in addition to those provided by the gate 3120.

When the counter 3000 advances to the setting supplying the inverted signal 13, a decimal point is generated for transmission to the delay line. The inverted signal 13 inhibits the gate 3120 so that this gate no longer supplies the signals D5 and D6. The inverted signal 13 generates the signals D2, D3, D4 and D6, which provide a code for a decimal point.

The inverted signal 13 also resets the flip-flop 3028. The resetting of the flip-flop 3028 applies an inhibit to the gate 3026 and partially enables the gate 3022.

When the next inverted signal LPR is received, the counter 3000 is advanced to its setting supplying a signal 14 which reads out the value of the tens cents digit in the delay line 110, after which the counter 3000 advances to its next setting to develop the signal 15. The signal 15 controls the reading of the units cents digit in the delay line 110.

When the inverted LPR signal is received following the storage of the units cents digit, the counter 3000 is advanced to its next setting which develops a signal for completing the enabling of the gate 3022. The gate 3022 is fully enabled, and the more negative signal applied to the C terminal of the flip-flop 3024 clears this flip-flop so that the higher potential at the Q terminal is effective through the gate 3030 to enable the gates 3111—3118 so that data can now be read from the card reader 102. This also inhibits the gates 3120 and 3126.

The more negative potential provided at the Q terminal of the flip-flop 3024 clocks the input counter 3100 to advance this counter a single number so that the receipt number provided during the next transaction is one greater in value. The more negative signal at the Q terminal of the flip-flop 3024 also inhibits the gate 3002 to prevent further advance of the counter on the inverted signals LPR and also clears the counter 3000 back to its initial setting in which the inverted signal 0 is generated.

The cashier's office 103 also includes auxiliary circuits used during the readout of information at its own recorder 204. More specifically, when an inverted signal STAT (CA) from the circuit 200 for its own recorder 204 is not present, an inverter 3008 sets a flip-flop 3010 to provide an enabling input to three gates 3012, 3018, 3020. These three gates receive the indicated signals from its own circuit 200 through three inverters 3006, 3014, and 3016 and return these signals to this circuit 200. However, when an inverted PCS signal is present, the flip-flop 3010 is reset, and the output recorder 204 for the office 103 is not available.

Although the present invention has been described with reference to a single illustrative embodiment thereof, numerous other modifications and embodiments can be devised by those skilled in the art that will fall within the spirit and scope of the principles of this invention.

What we claim and desire to be secured by Letters Patent of the United States is:

1. In a hospital data handling system for messages of different types at least one of which requires a charge to be made to a patient and in which each message includes a control data item,

a plurality of stations located at different places in the hospital, each of said stations including a data transmitter for transmitting messages and a data receiver for receiving messages,

a message storage means common to all of the stations,

a first control means coupled between the stations and the message storage means for storing messages received from the data transmitter,

a patient charge storage and collecting means,

and a second control means coupled to the message storage means and the patient charge storage means for selectively directing data from the messages stored in the message

storage means to the data receivers in the stations, said second control means including detecting means responsive to a control data item in a received message indicating that a patient charge is to be made for inhibiting transmission of the message from the message storage means to a data receiver and for retaining the message in the message storage unit for use by the patient charge storage and collecting means.

2. In a data handling system for a hospital including nursing stations and departmental stations,

a data transmitter and a data receiver at each of the stations, each of the receivers having an address and each of the transmitters transmitting a message including both the addresses of at least two data receivers and a control code, data storage means for storing a message received from a data transmitter,

output selector means controlled by the transmitted addresses for selecting the corresponding data receivers to receive the message stored in the data storage means, control means coupled to the data storage means for transferring the message from the data storage means to all of the data receivers selected by the output selector means, and control code detecting means connected to the data storage means for detecting the control codes included in the message and operative to inhibit the transmission of a message to a data receiver at a nursing station that has previously been selected by the output selector means when a predetermined control code is detected.

3. In a data handling system, a plurality of individually addressed data recorders, at least one data transmitter,

a first data storage means coupled to the data transmitter for receiving and storing data received from the data transmitter, said received data including message data and the individual addresses of two or more of said data recorders,

a second data storage means,

first control means for transferring at least part of the data stored in the first data storage means to the second data storage means and for transferring the data stored in the second data storage means to only the two or more data recorders identified by the received addresses,

and second control means connecting to the plurality of data recorders for checking the busy or idle status of the two or more data recorders identified by the received addresses and for inhibiting the transfer of data from the first data storage means to the second storage means if one of the addressed data recorders is busy.

4. In a data handling system,

a plurality of data receivers each having an identifying address,

a data transmitter,

a first data storage means for storing data received from the data transmitter including message data and the address of at least one of the data receivers,

a second data storage means for storing data received from the first data storage means,

first control means responsive to the address transferred to the second storage means for determining the busy/idle status of the data receivers identified by the transferred address,

second control means controlled by the first control means for transferring the data stored in the second storage means to the addressed data receivers and for clearing the first data storage means when the addressed data receivers are idle,

and third control means controlled by the first control means for inhibiting the clearing of the first data storage means when an addressed data receiver is busy and for enabling the storage of other data in the second data storage means.

5. In a data handling system using records having plural character messages including at least one control item,

a record reader for reading the record and supplying message signals in accordance with the message on the record,  
 data storage means coupled to the record reader and controlled by the message signals to store the message from the record, 5  
 a code detecting circuit for monitoring the message signals supplied by the record reader and for detecting the presence of a control item,  
 a first additional message signal source for supplying message signals to the data storage means, 10  
 and a control circuit controlled by the code detecting circuit in response to the detection of a control item for preventing the transmission of message signals from the record reader to the data storage means and for operating the additional message signal source to supply message signals to the data storage means in place of the message signals from the record reader. 15

6. The data handling system set forth in claim 5 in which the record includes different control items, and in which the system includes at least a second additional message signal source for supplying message signals to the data storage means, wherein the code detecting circuit, in addition to detecting the presence of a control item, generates a signal indicative of the particular control item detected, and wherein the control circuit responds to the signal supplied by the code detecting circuit and selects the message signal source corresponding to the particular control item detected as indicated by the signal. 20

7. In a data handling system for use with messages formed by data derived from a plurality of records each containing an identifying control data item, 25  
 a record reader for reading a group of records to provide a message containing the data derived from the group of records read in any random order, 30  
 a storage unit coupled to the record reader for storing the message,  
 a message receiver coupled to the storage unit for receiving a message from the storage unit,  
 a control data item detecting means supplied with the message from the record reader and operative to supply an error signal when the combination of control data items included in a message is not one of a given number of predetermined combinations, 35  
 and a control circuit controlled by the control data item detecting means for preventing the transfer of a message from the storage means to the message receiver in response to the receipt of an error signal. 40

8. In a data handling system using a message including at least two control data items, 45  
 a message signal source supplying a message,  
 a storage means (supplied with the message to store the message) into which the message signal source feeds the message for storage,  
 a message receiver coupled to the storage means to receive 50  
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a message from the storage means,  
 control data item detecting means supplied with the message from the signal source, said detecting means including first means for determining the presence of at least two control data items in a message and second means for determining whether the control data items provide any one of a number of known combinations, and means controlled by the detecting means when at least two control items are not present in a message or the control data items in the message do not provide one of the known combinations for arresting transfer of the message to the message receiver.  
 9. In a data handling system using a message formed of data derived from a plurality of different data records each having an identifying control data item, 15  
 a record reader supplied with a group of said records to transmit a message including the data derived from the group of records in random order,  
 a storage unit for storing the message supplied by the record reader,  
 a data utilization device for receiving a message from the storage unit,  
 a control data item detecting circuit supplied with the message from the record reader and operative to determine the combination of control data items included in the message, 20  
 and control means controlled by the detecting circuit and coupled to the storage unit for arranging the data derived from the records in a given order for use by the data utilization device in accordance with the detected control data items.  
 10. The data handling system set forth in claim 9 in which the storage unit includes both a number of addressable storage locations and addressing means for selecting the storage locations, 25  
 and the control means includes means coupled to the addressing means and controlled by the detecting means for controlling the addressing means to selected different storage locations in dependence on the detected control data item.  
 11. The data handling system set forth in claim 10 in which the control means includes means for controlling the addressing means to place the message data received from the record reader in the selected storage location.  
 12. The data handling system set forth in claim 11 in which the control means includes both means for storing the control data items and means controlled by the stored control data items for controlling the addressing means to select storage locations for transfer of message data to the data utilization device.  
 13. The data handling system set forth in claim 10 in which the control means includes means for controlling the addressing means to remove message data from the selected storage locations. 30  
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