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— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

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16 July 2015

(54) **Title**: METHODS AND APPARATUS FOR PARALLEL PROCESSING

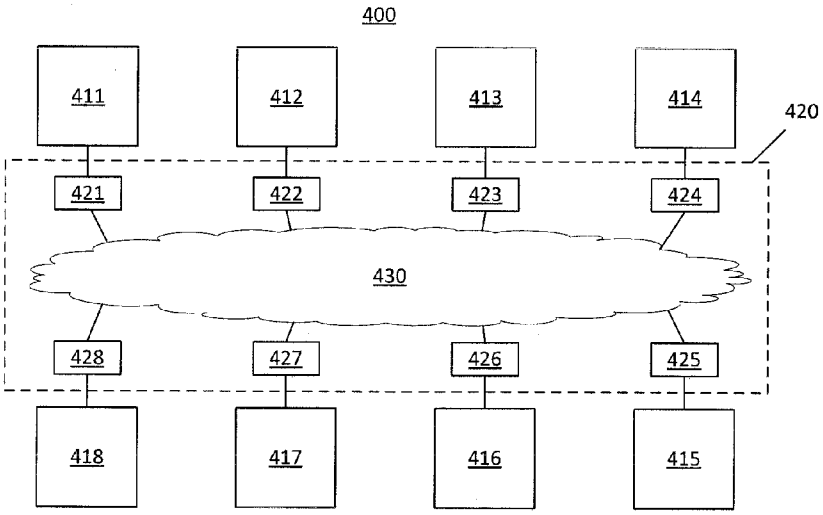

FIGURE 4

(57) **Abstract**: Methods and apparatus for parallel processing are provided. A multicore processor is described. The multicore processor may include a distributed memory unit with memory nodes coupled to the processor's cores. The cores may be configured to execute parallel threads, and at least one of the threads may be data-dependent on at least one of the other threads. The distributed memory unit may be configured to proactively send shared memory data from a thread that produces the shared memory data to one or more of the threads.

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A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - G06F 7/00 (2015.01); G06F 9/38 (2015.01)
CPC - G06F9/3885
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC: 707/764; IPC(8): G06F 7/00 (2015.01); G06F 9/38 (2015.01); CPC: G06F9/3885

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC: 718/102; 370/235, 370/230, 370/389, 370/412, 370/413, 370/392; 712/16, 712/203, 712/11; 707/764; 709/223; CPC: G06F17/30445, G06F17/30545, G06F17/30595, G06F17/30486, G06F17/30539, G06F9/3885; IPC(8): G06F 7/00 (2015.01); G06F 9/38

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PatBase, Google Patents, IEEE; Search Terms: multi-core processor; multi-threaded code; ring network; distributed memory node; cache memory hierarchy; serial parallel code conversion; loop iteration processing; shared data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X ------- Y	US 2004/0193841 A1 (Nakanishi) 20 September 2004 (20.09.2004), entire document especially Figure 2A, Figure 2B, elements 11-1, 11-n, 12-1, 12-m, 13-1,13-m; paras [0025], [0026], [0055], [0056], [0057], [0060], [0062], [0066], [0117]-[0118], [0123], [0125]	1-7, 10-14, 18, 21-26, 28-31, 34 and 36 ---------- 8, 9, 15-17, 19, 20, 27, 32, 33 and 35
Y	US 2009/0240869 A1 (O'Krafka et al.) 24 September 2009 (24.09.2009), entire document, especially paras [0106], [0107], [0109], [0112]	15-17, 32 and 33
Y	US 2010/0306733 A1 (Bordelon et al.) 02 December 2010 (02.12.2010), entire document especially Abstract, paras [0014], [0015], [0017], [0018]	8, 9, 19, 20, 27 and 35
A	US 2005/0044319 A1 (Olukotun) 24 February 2005 (24.02.2005), entire document	1 - 36
A	US 5,394,555 A (Hunter et al.) 29 February 1995 (28.02.1995), entire document	1 - 36
A	US 2012/0124344 A1 (Jarvis) 17 May 2012 (17.05.2012), entire document	1 - 36
A	US 2011/0265068 A1 (Elnozahy et al.) 27 October 2011 (27.10.2011), entire document	1 - 36

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 April 2015 (16.04.2015)	18 MAY 2015
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

International application No.
PCT/US 14/42402

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

--- see extra sheet ---

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1 - 36

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

International application No.
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Continuation of Box No. III, Observations wher unity of invention is lacking:

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1.

Group I: Claims 1-36, directed towards a multi-core multi-threaded processor that executes a first and second thread in parallel with the input of a consumer instruction (shared data).

Group II: Claims 37-52, directed towards a system and method of evaluating program code and selecting and further generating additional multi-threaded code for execution on a multi-core multi-threaded processor based on the evaluation.

Group III: Claims 53-59, directed towards a system and method that identifies loops in a program, generating multi-threaded code for those loop sections, performs a simulation of said code, evaluates the timings from the simulation and generates the complied code for the program.

The groups of inventions listed above do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons:

The special technical feature of the Group I invention is a multi-core processor having a set of cores including first and second cores; and a distributed memory unit including a set of memory nodes including a first memory node coupled to the first core and a second memory node coupled to the second core; wherein the first core is configured to process one or more producer instructions of a first thread, including storing, in the first memory node, data shared by the first thread and a second thread; the second core is configured to process one or more first instructions of the second thread in parallel with the first core processing the one or more instructions of the first thread, wherein the distributed memory unit is configured to send the shared data to the second memory node in response to the first core storing the shared data in the first memory node, and wherein the second core is configured to process one or more second instructions of the second thread after the second memory node stores the shared data sent by the distributed memory unit... (See Figure 6).

The special technical feature of the Group II invention is a method/system that includes determining a value corresponding to parallel execution of multi-threaded code on a multicore processor configured to send shared data from a first thread to a second thread in response to the first thread producing the shared data, wherein the multi-threaded code implements a sequential portion of a program; selecting the sequential portion of the program for parallelization based, at least in part, on the determined value; and generating compiled code for the program, the compiled code including the multi-threaded code corresponding to the sequential portion of the program...(See Figure 7).

The special technical feature of the Group III invention is a method/system that includes identifying sequential loops in a program; generating portions of multi-threaded code implementing the respective sequential loops; simulating execution of the portions of multi-threaded code on a multi-core processor by determining simulated durations of execution of the portions of multi-threaded code on the multi-core processor; selecting one or more of the sequential loops for parallelization based, at least in part, on the simulated durations of execution of the portions of multi-threaded code corresponding to the sequential loops; and generating compiled code for the program, the compiled code including the multithreaded code cooresponding to the selected sequential loops... (See Figure 8).

Groups I, II and III share the technical features of, in various combination, the execution of multi-core multi-threaded code on a multi-core multi-threaded processor. However, these shared technical features fail to represent a contribution over the prior art of US 2005/0044319 A1 which discloses the execution of multi-core multi-threaded code on a multi-core multi-threaded processor (Abstract; Figure 1 and 2).

Thus, the inventions listed as Groups I, II and III lack unity of invention because they do not share a same or corresponding special technical feature providing a contribution over the prior art.