

- [54] **SYSTEM FOR FREQUENCY MODIFICATION OF SPEECH AND OTHER AUDIO SIGNALS**
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- [58] Field of Search. **340/172.5**, 347 AD; 179/15 AC, 15.55, 1 SA 179/15 AV, 1 SA, 15.55

[56] **References Cited**

UNITED STATES PATENTS

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|-----------|--------|----------------------|-----------|
| 3,394,228 | 7/1968 | Flanagan et al. | 179/1 SA |
| 3,431,356 | 3/1969 | Copel. | 179/1 SA |
| 3,571,515 | 3/1971 | Buron | 179/1 SA |
| 3,584,158 | 6/1971 | Jefferies. | 179/1 SA |
| 3,500,441 | 3/1970 | Brolin | 179/15 AV |

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|-----------|--------|-----------------|-------------|
| 3,594,509 | 7/1971 | Shimamura. | 179/15 AV |
| 3,555,522 | 1/1971 | Martin. | 340/172.5 X |

OTHER PUBLICATIONS

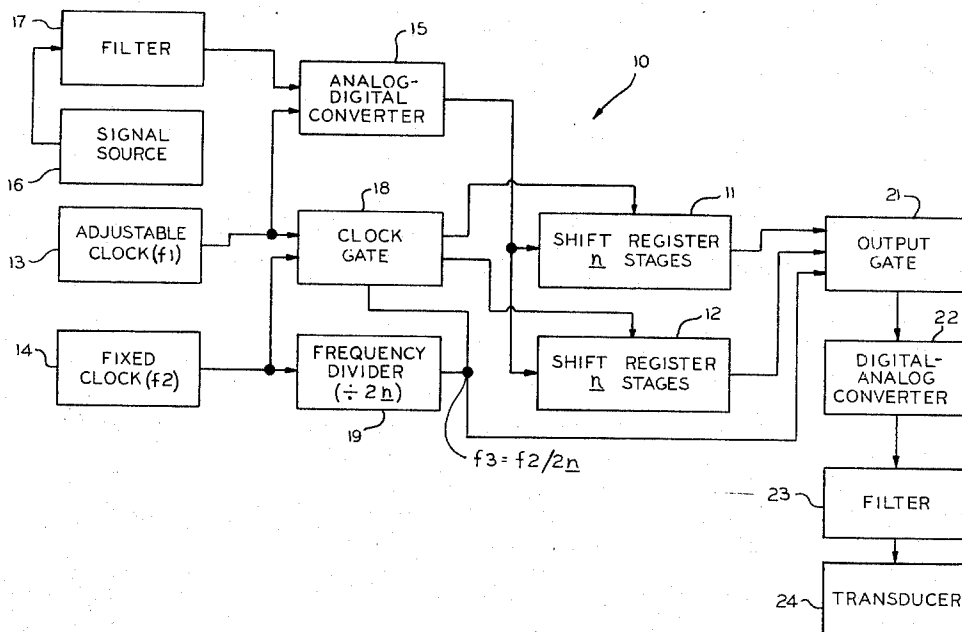
"Unscrambler Improves Communications in Helium-Oxygen Atmosphere," Westinghouse Engineer, Jan. 1969, Vol. 29/No. 1.

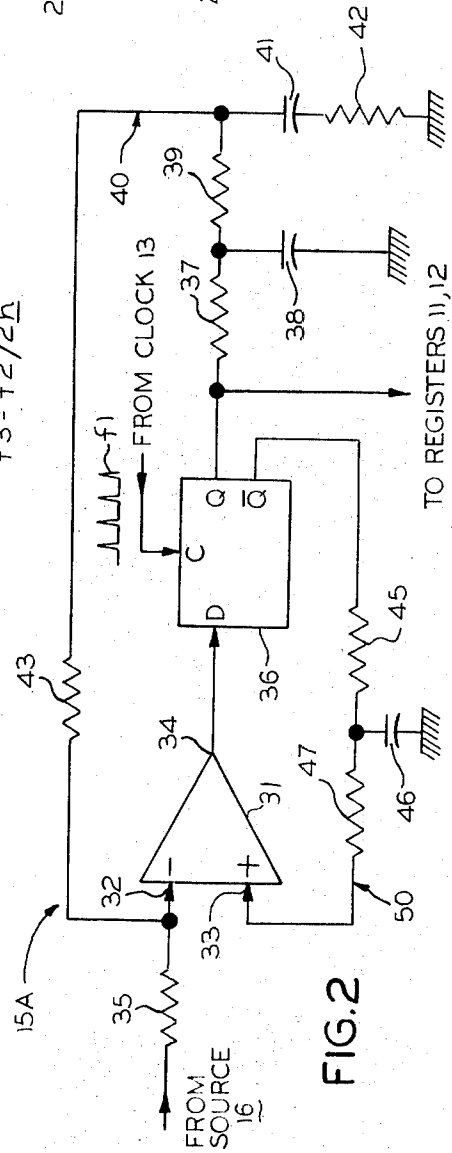
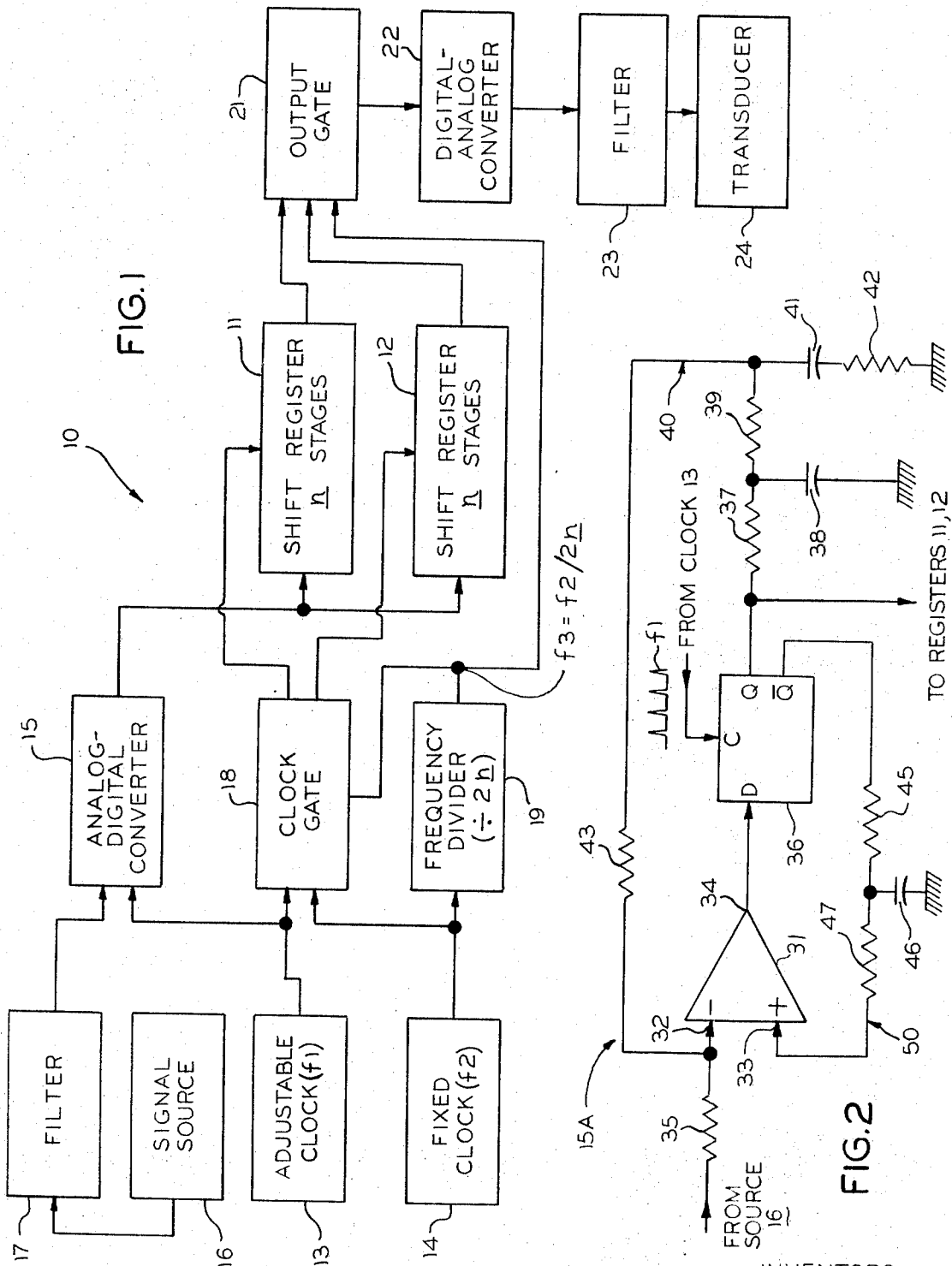
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[57] **ABSTRACT**

A system for multiplying the frequencies of a speech signal, or other audio signal, by a given multiplication factor, comprising an analog-digital converter for converting an audio signal to a digital signal having a bit rate f_1 and means for temporarily storing that digital signal. The system further comprises apparatus for reading out the stored digital signal, in groups of n digits, at a bit rate f_2 , with means for synchronizing the readout apparatus to connect the groups of n digits in sequence. A digital-analog converter uses the digital readout to develop a speech signal modified in frequency in accordance with the rate f_1/f_2 but having the same time span as the original speech signal.

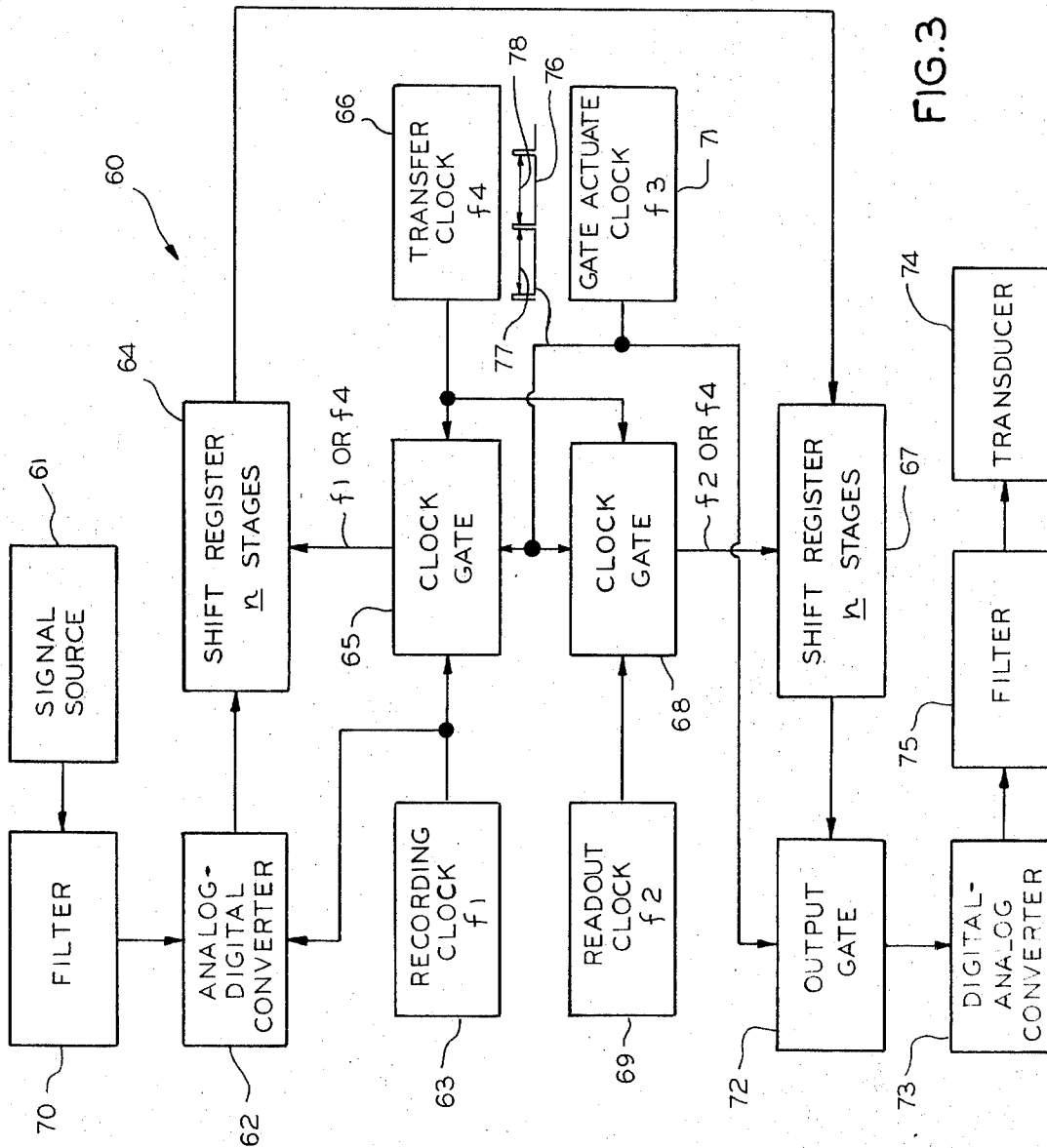
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SYSTEM FOR FREQUENCY MODIFICATION OF SPEECH AND OTHER AUDIO SIGNALS

BACKGROUND OF THE INVENTION

There are a number of applications in which it is necessary or desirable to reproduce speech or other audio signals with either an effective increase or decrease in frequency. One example is in the presentation of recorded material to blind persons. It is recognized that a person can assimilate spoken material at rates considerably higher than normal speaking rates. Consequently, if a recorded passage can be reproduced at a higher speed than the original recording, but maintained within the familiar portion of the frequency spectrum instead of being raised in pitch because of the accelerated reproduction, the high speed audio presentation of information can be greatly facilitated.

The use of helium instead of nitrogen atmospheres in high pressure diving has created a special and critical audio communication difficulty. The substitution of helium for nitrogen changes the resonant frequencies of the throat, mouth, and nose cavities used for speech, due to the fact that the velocity of sound in helium is greater than in nitrogen. The result is a multiplication of speech frequencies by a factor that may be as great as 2.8, depending upon the atmospheric pressure and concentration of helium. As a consequence, in order to maintain intelligible communications with a diver working under high pressures in a helium atmosphere, an effective frequency modification system is needed for the diver's speech.

Another application for frequency multiplication processing of speech signals or other audio signals entails an inverted time situation, in which the speed of presentation of the audio signal is reduced and "naturalness" is restored by raising the frequency range of the reproduced signal. Thus, on poorly recorded audio messages, a substantial slowdown in reproduction, while maintaining the reproduction within the normal audio frequency range, may contribute substantially to effective and accurate interpretation. A related learning situation, for certain types of handicapped persons, can benefit from the same technique, reducing the rate of presentation but maintaining the reproduced sound in the natural portion of the frequency spectrum. Similar systems can be useful to some persons having hearing losses; a frequency reduction can materially increase intelligibility. In the compression of information for storage, as in a "talking book" program, storage space can be reduced substantially by recording at normal speeds in a frequency increase mode with playback at a reduced speed.

A number of different audio signal processing systems have been proposed, directed to the several applications set forth above. In many of the suggested systems, the processing consists essentially of playback of the original audio signal, from a recording, at a different rate from the original recording rate. One example is a tape deck having multiple heads for scanning a moving magnetic tape at a rate such that the heads move relative to the tape. An example of a system of this kind is Fairbanks et al, U.S. Pat. No. 2,886,650.

Another and more complex approach has been described in Flanagan U.S. Pat. No. 3,394,228, which is specifically directed to the conversion of helium-atmosphere speech to more intelligible form. In the

Flanagan apparatus, there is a breakdown of the helium-distorted speech into a plurality of "formant patterns", followed by non-linear modulations of the various "formants" in accordance with various functions representative of the characteristics of the environment in which the speech is produced.

In another approach, described in a report entitled "The Development of a Digital Helium Speech Processor" No. 4007-F-2, Office of Naval Research, May 1968, the correction of helium-distorted speech signals is accomplished by an apparatus that treats voiced sounds differently from unvoiced sounds. For sounds in which the system cannot detect "pitch" in the speech waveform, the system decides that the signal is "unvoiced" and does not require temporal modification. When the system does detect pitch in the input signal, it treats the signal as encompassing a "voiced" sound. The voiced portion of the signal is converted to digital form and stored alternately in two storage registers. The digital voiced sound signals are read out alternately from these registers, at a lower rate than the recording rate, and are then re-converted to analog form and are recombined with the unmodified unvoiced sounds.

SUMMARY OF THE INVENTION

It is a principal object of the present invention, therefore, to provide a new and improved system for frequency modification of a speech signal or other audio signal, while retaining the same time of presentation as the input signal, which does not require splitting the speech signal on the basis of the pitch, formants, or any other functional characteristic.

A further object of the invention is to provide a new and improved system for frequency modification of a speech signal or other audio signal that affords optimum intelligibility and quality in its output while treating all parts of the speech signal the same.

A specific object of the invention is to provide a new and improved digital processing system for frequency modification of a speech signal or other audio signal that is simple and compact and can be used virtually anywhere, being suitable for carrying by an individual under virtually any circumstances.

Another object of the invention is to provide a new and improved frequency multiplication system for audio signals that is readily and effectively applicable to the various fields referred to above, and others, such as correction of helium-distorted speech, aid to the deaf, audio bandwidth compression, and special entertainment effects.

A particular object of the invention is to provide a new and improved frequency-multiplication system for audio signals that is entirely non-mechanical in nature and requires little or no continuing maintenance.

A processing system for frequency modification of a speech signal or other audio signal, constructed in accordance with the invention, comprises analog-digital converter means for converting a complete speech signal to a digital data signal. Two temporary serial storage means, which may be connected in parallel or in series, are provided for recording the digital data signal at a primary bit rate f_1 ; readout means are provided for reading out the recorded digital data signal, in groups of digits, and at a secondary bit rate f_2 substantially different from f_1 , to develop an output signal. The

system includes synchronizing means for actuating the readout means at time intervals recurring at a frequency f_3 that is very much lower than both f_1 and f_2 and is preferably a subharmonic of f_2 . Output means, comprising a digital-analog converter, are provided for utilizing the digital data to develop a processed speech signal with a frequency modification of f_1/f_2 but within the same time span as the original speech or other audio signal.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of an audio signal processing system constructed in accordance with one embodiment of the invention;

FIG. 2 is a schematic diagram of an analog/digital converter used in the system of FIG. 1; and

FIG. 3 is a block diagram of another embodiment of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 illustrates a processing system 10, constructed in accordance with the invention, for frequency modification of a speech signal in which the output signal has the same time span as the original signal. System 10 comprises a first temporary serial storage means 11 for storing a digital data signal. The storage means 11 has a total capacity of n digits, where n is a positive integer which is at least 32 as a practical lower limit. The temporary serial storage means 11 may be constructed as a shift register of n stages; it would constitute a delay line or other storage device having a total capacity of n digits when supplied with a digital input signal of an appropriate frequency. System 10 further includes a second shift register or other temporary serial storage means 12 that also has a capacity of n digits and that is preferably essentially identical in construction to the first storage means 11.

System 10 comprises a first clock signal source 13 and a second clock signal source 14. The first clock signal source 13 is preferably an adjustable-frequency multivibrator or other oscillator, and is utilized to develop a first clock signal having a primary frequency f_1 that may be adjusted to meet the frequency multiplication and division requirements imposed upon the system. The second clock signal source 14 may be a fixed-frequency oscillator or similar device and develops a second clock signal having a frequency f_2 . In those instances in which a frequency downshift of an initial speech or other audio signal is required, frequency f_2 should be substantially lower than frequency f_1 . This would be the situation for the correction of helium-distorted speech. In those instances in which a frequency upshift is required, the fixed frequency f_2 is substantially higher than the adjustable clock frequency f_1 .

The system 10 of FIG. 1 further comprises an analog-to-digital converter circuit 15 having two inputs, one for an audio signal and the other for a synchronizing clock signal. The audio signal input of the analog-digital converter 15 is coupled to a speech or other audio signal source 16. The signal source 16 may be a reproducing device, if the signals to be processed have previously been recorded. On the other hand, the signal source may be a live source, such as the communica-

tion line, amplifiers, and microphone of a telephone link to a diver. In either event, it may be assumed that source 16 includes appropriate spectrum shaping circuits to accommodate and compensate for general spectrum deficiencies in the initial signal due to microphone characteristics, etc. A low-pass filter 17 is preferably interposed between source 16 and converter 15 to minimize high-frequency overload noise in operation of the converter. The clock input of converter 15 is connected to the output of adjustable clock source 13, so that the output signal from converter 15 is a digital data signal having a bit rate f_1 .

There are several different forms of analog-to-digital converter that can be used for converter 15 in signal processing system 10. However, a particularly effective and useful circuit for this purpose is the type known as a delta modulator. A delta modulator is a single digit feedback encoding device, operated at a rather high sampling frequency (preferably 20 KHz or more), based upon comparison of an integrated output signal with the input signal. A "one" shows an input amplitude greater than the integrated output, a "zero" reflects the opposite situation. Construction and operation of a delta modulator are more fully described hereinafter in conjunction with FIG. 2. The output of converter 15, the digital data signal referred to above, is supplied to the data inputs of the two temporary storage means 11 and 12.

The clock signals f_1 and f_2 from sources 13 and 14 are also supplied to the two inputs of a clock gate 18. Functionally, clock gate 18 is the equivalent of a double-pole double-throw switch having its output terminals connected together in pairs. In one operating condition, clock gate 18 applies clock signal f_1 to shift register 11 and applies clock signal f_2 to shift register 12. In its other operating condition, clock gate 18 supplies signal f_1 to shift register 12 and signal f_2 to shift register 11. It is thus seen that, at any given time, data is being stored in, advance through and read out of one of the shift registers at the bit rate f_1 while the same operations go forward in the other shift register at the different bit rate f_2 .

To control the operation of clock gate 18, the signal processing system 10 includes a frequency divider 19 having a division ratio of $1/2n$. The input to frequency divider 19 is taken from the fixed clock source 14 and constitutes clock signal f_2 . Consequently, it is seen that the output of frequency divider 19 is an actuating signal having a frequency f_3 such that $f_3 = f_2/2n$. This signal is supplied to clock gate 18 to change the operating condition of the clock gate each time n data bits have been read out of either of the two temporary storage devices 11 at rate f_2 .

An output gate 21 is included in signal processing system 10. Functionally, output gate 21 is equivalent to a single-pole double-throw switch. It has two data signal inputs, each connected to the output stage of one of the two temporary storage means 11 and 12. Actuation of gate 21 is effected at the cyclic rate $f_2/2n$ by means of an actuating signal supplied to the gate from frequency divider 19. The output of gate 21 is thus alternately connected to storage means 11 and 12 respectively when data is being advanced through and read out of each one at bit rate f_2 . By this means a stream of data at bit rate f_2 is gated to a digital-to-

analog converter 22 that re-generates an analog audio signal from the digital input signal. Basically, converter 22 may constitute an integrator, integrating the digital data signal over short time intervals. The output of converter 22 may be supplied, through an appropriate filter or spectrum shaping circuit 23, to a transducer 24 or other utilization circuit. For example, transducer 24 may be a speaker, where a telephone system is involved, as in the correction of helium-distorted speech. On the other hand, transducer 24 may be a recorder in systems in which the frequency modification of the original signal from the source 16 is being effected to achieve particular recording characteristics.

The capacity n for the two shift registers 11 and 12 is preferably selected as a number that is an exponential power of two. By way of example, for each of the registers, the total number of stages n may be 1024, the tenth power of two; for greater accuracy and fidelity, the eleventh power of two (2048) may be selected. This capacity selection simplifies the construction of frequency divider 19; division by a factor of two is simple and is easy to control accurately. The output signal of frequency divider 19, at frequency f_3 , must be maintained within a relatively restricted range. It should be less than one hundred hertz in order to prevent the switching operations which occur at frequency f_3 from interfering with intelligibility in the reproduced speech. Thus, measurements have shown that interruptions of speech with a relatively low duty cycle, such as a duty cycle of 50 percent, have reasonably high intelligibility as long as the interruption rate is substantially less than one hundred hertz and is greater than ten hertz. Apparently, physiological or psychological persistence, and signal redundancy, bridge the gaps. At interruption rates lower than 10 hz, substantial amounts of the audio signal are "lost" to the listener, and intelligibility decreases rapidly. At interruption rates above 100 hz, side band frequencies are produced in the speech band, causing substantial deterioration in intelligibility.

Another factor to be considered in connection with the audio system is the overall length, on a time basis, of the signal that is stored at any given time in either of the temporary storage means 11 and 12. The ability of a human being to determine the frequency or pitch of an acoustic signal is essentially constant and is good for signal durations of fifteen milliseconds or longer when the frequency is 1,000 hz or greater. Below 1000 hz the ability to determine pitch requires a signal duration that is inversely proportional to the period of the basic frequency of the audio signal. By limiting the output sampling time of the system to about fifteen milliseconds, good discrimination of voice components in the high frequency range, as is necessary for good articulation, is obtained. The storage capacity n , and the sampling frequency f_3 , which is $f_2/2n$, together determine the fixed clock frequency f_2 ; in the typical system under consideration, f_2 is about 67 KHz when n is 1024.

When the processing system 10 first starts in operation, it may be assumed that both of the temporary storage means 11 and 12 are empty. Furthermore, it may be assumed that clock gate 18 is initially conditioned, by the actuating signal from frequency divider 19, to apply the adjustable clock signal f_1 from source 13 to shift register 11 and to apply the fixed clock signal f_2 from source 14 to shift register 12. Ac-

cordingly, the digital data signal from converter 15 is initially stored in temporary storage means 11 at a bit rate f_1 . The same data from converter 15 may be stored in shift register 12 at a rate f_2 , but the parallel arrangement of registers 11 and 12 makes this recording superfluous, as will be apparent from the description of the output circuitry for the system. During this initial time interval, in which the first segment or sample of the digital data signal is stored in shift register 11, there is no effective output signal from gate 18 to converter 19 because there has been no information previously stored in either of the temporary storage registers.

After a sampling time interval of $f_3/2$, in this instance about 15 milliseconds, one-half cycle of the output from frequency divider 19, clock gate 18 is actuated by the actuating signal from frequency divider 19. Gate 18 now changes the shift signal inputs to storage means 11 and 12, supplying clock signal f_1 to shift register 12 and supplying clock signal f_2 to register 11.

The actuating signal from frequency divider 19 also actuates output gate 21 to connect the output stage of the first shift register 11 to the digital-analog converter 22. Shift register 11 has been filled with information during the first sampling time interval. Consequently, during the next sample interval, the data previously stored in shift register 11 is read out at the rate f_2 , through gate 21, to converter 22. Converter 22, which may be a relatively simple integrator, regenerates the speech or other audio signal with a frequency change ratio of f_1/f_2 but with the same time span as the original speech signal. During this same time interval, the original speech signal from source 16 continues to be stored, in digital form, at the rate f_1 in the second temporary storage means 12.

Operation proceeds for a second sampling time interval of approximately 15 milliseconds, at which point the actuating signal from frequency divider 19 again actuates both of the gates 18 and 21, reverting to the original operating conditions with clock signal f_1 supplied to shift register 11 and clock signal f_2 supplied to shift register 12. Output gate 21 now connects the output stage of shift register 12 to converter 22. During the succeeding sampling time interval of 15 milliseconds, therefore, the incoming signal from source 16 is recorded, in digital form, at rate f_1 , in shift register 11. The information previously recorded in shift register 12 is read out to converter 22, at rate f_2 , and it utilized to reproduce the desired frequency-shifted audio signal.

If the ratio of frequency f_1 to frequency f_2 is of the order of 2:1, it can be seen that information is recorded in the temporary storage means 11 and 12 at twice the rate that is read out of those same storage means. In essence, this means that one-half of the digital data signal from converter 15 never reaches the digital-analog converter 22. Nevertheless, in the case of helium-distorted speech, there is a marked improvement in intelligibility in the output signal as reproduced by transducer 24, compared with previously known systems. Speech signals are often generated under noisy conditions, and hence include noise that interferes with the detection of voiced and unvoiced sounds. Because system 10 does not separate the speech signal into voiced and unvoiced segments, it does not encounter the noise problem and other difficulties prevalent in systems that split and then recombine the

speech signals. In particular, avoiding any necessity for detection of voiced and unvoiced sounds permits use of system 10 for a variety of different audio signals, including completely non-vocal signals such as music. The system is highly adaptable to integrated circuit construction and can be incorporated in a single hand-portable device for battery or A.C. power.

Speech processing system 10 can be used for a frequency upshift as well as for a frequency downshift. To this end, the operating frequency of the adjustable clock 13 may be established at some value substantially less than the frequency f_2 of the fixed clock 14. With this change in relationships, it will be apparent that information is read out of shift registers 11 and 12 at a greater rate than employed for storing data in the registers. A series of blanks are incorporated in the output signal as supplied to transducer 24.

FIG. 2 illustrates an analog-digital converter circuit 15A that is a delta modulator and that constitutes the preferred form of circuit for use as the converter 15 in system 10. Converter 15A comprises a comparator amplifier 31 having an inverting input 32, a non-inverting input 33, and an output 34. The inverting input 32 is connected to a signal source (e.g., source 16 in FIG. 1) by a series resistor 35. The amplifier output 34 is connected to the D input of a type D sampling flip-flop circuit 36. The clock input C of flip-flop 36 is connected to the clock source 13 (FIG. 1).

Flip-flop circuit 36 has a main output Q and a complementary output $\bar{Q}$. The output Q is the output terminal for converter 15A, and is connected to shift registers 11 and 12. Terminal Q is also connected to a dual integrator circuit comprising a series resistor 37, a shunt capacitor 38, a second series resistor 39, and a second shunt capacitor 41, a resistor 42 being connected in series with capacitor 41. The common terminal of resistor 39 and capacitor 41, in the second integrator stage, is connected back to the inverting input 32 of comparator amplifier 31 through a feedback resistor 43.

Converter 15A (FIG. 2) includes a second feedback loop for comparison amplifier 31. This secondary loop originates at the $\bar{Q}$ output of flip-flop 36 and includes an integrator or low-pass filter comprising a series resistor 45 and a shunt capacitor 46. The loop is complete by a resistor 47 that connects the common terminal of resistor 45 and capacitor 46 back to the non-inverting input 33 of amplifier 31.

In operation, a positive-going signal supplied from source 16 to input 32 of amplifier and, in coincidence with a pulse of the f_1 clock signal, produces a negative-going pulse at the Q output of flip-flop 13. The pulse signal from terminal Q is averaged in the integrating circuit 40 and applied to terminal 32 as a negative feedback. If the positive-going input from source 16 exceeds the negative-going feedback at the time of the next f_1 pulse, another negative-going pulse is produced at the circuit output, and the integrated negative feedback signal increases in amplitude. When the negative feedback signal exceeds the input signal in amplitude, no additional pulses are developed at the Q output of flip-flop 36. Thus, whenever the input signal amplitude exceeds signal amplitude in negative feedback circuit 40, a series of pulses representative of one binary value are produced at terminal Q; when the reverse am-

plitude relation obtains, "blank" spaces representative of the other binary value occur in the Q terminal output.

The second feedback loop 50, connected from the $\bar{Q}$ output of flip-flop 36 back to the non-inverting input 33 of comparator amplifier 31, provides a self-bias or self-generated reference for the comparator. This preferred circuit, in effect, gives a self-compensating threshold and more uniform "white noise" characteristic for delta modulator 15A, when idling, then in a conventional circuit using a fixed reference. In loop 50, the low-pass filter formed by resistor 45 and capacitor 46 maintains a D.C. voltage on amplifier input 33 that bucks the D.C. voltage of loop 40 as applied to input 32. Any D.C. component of the signal from source 16 or D.C. offsets within amplifier 31 are effectively eliminated, avoiding the single-frequency "warbling" that may be produced by a fixed-level delta modulator signal when re-converted to analog form. Moreover, the effect of low-level signals, just breaking the threshold of the modulator idling pattern, is more gradual and subjectively more tolerable.

FIG. 3 illustrates a processing system 60 for frequency modification of a speech signal that constitutes another embodiment of the present invention. In system 60, a signal source 61 is connected through an appropriate filter 70 to an analog-digital converter 62 which may constitute a delta modulator. The timing input to converter 62 comprises a clock signal at frequency f_1 derived from a first clock signal source 63. The output of converter 62 is supplied to the input stage of a shift register or other temporary serial storage means 64. Shift register 64 has a second or timing input taken from a clock gate 65. Clock gate 65 has two inputs; one is taken from clock source 63 and constitutes the recording clock signal f_1 . The other input to clock gate 65 is taken from a transfer clock signal source 66 and constitutes a transfer clock signal of frequency f_4 . The transfer clock frequency f_4 is very much higher than the recording clock frequency f_1 and, in fact, should be more than 10 times f_1 .

The output of the temporary storage register 64 is connected to the input of a second essentially similar temporary storage means 67. The shift or other control circuits for the temporary storage means 67 are actuated by input signals from a second clock gate 68. Clock gate 68 has two inputs; one is connected to the output of a readout clock source 69 that develops a readout clock signal of frequency f_2 which is substantially different from frequency f_1 but is of the same order of magnitude. The other input to the clock gate 68 is taken from the transfer clock source 66 and constitutes the transfer clock signal f_4 which is at least an order of magnitude higher in frequency than the readout clock signal f_2 .

The two clock gates 65 and 68 are a part of a clock input gate means. The actuation means for the two clock gates comprises a gate actuation clock 71 that develops a gate actuation signal 76 of a quite low frequency f_3 that also has a very low duty cycle. The output of the gate actuation clock 71 is supplied to both of the clock gates 65 and 68. The gate actuation signal 76 is also applied to an output gate 72 that couples the output stage of the second temporary storage means 67 to an analog-digital converter 73. The output

of converter 73 is connected to a transducer 74 by a suitable output filter 75.

In considering the operation of signal processing system 60, FIG. 3, it may first be assumed that clock gate 65 is conditioned to supply the recording clock signal f_1 from clock source 63 to the first temporary storage means 64. This is the normal operating condition for system 60 for most of the time, and corresponds to the condition occurring during the long intervals 77 in the gate actuation signal 76. Under these conditions, a speech signal or other audio signal from source 61 is converted to digital form in converter 62 and is stored in the temporary storage means 64 at frequency f_1 .

The foregoing operational conditions are maintained for a time interval sufficient to fill, or nearly fill, the shift register 64. This time interval corresponds to the time 77 between pulses in the gate actuation signal 76. When one of the short pulses 78 occurs in the gate actuation signal, clock gate 65 is actuated to its alternate operating condition and supplies the high frequency transfer clock signal f_4 to the temporary storage means 64 and 67. For a brief period of time, therefore, the previously recorded data is advanced at a very high speed through shift register 64 and is transferred to the second temporary storage register 67. At the end of each short pulse 78, the clock gate 65 reverts to its original operating condition and again supplies a recording clock signal f_1 to temporary storage means 64 to control the recording of further information in the storage means 64.

During the long time intervals 77 in the gate actuation control signal 76, clock gate 68 is conditioned to supply the readout clock signal f_2 from source 69 to temporary storage means 67. As a consequence, any information that has been transferred from shift register 64 to register 67 is read out of register 67, at rate f_2 . When one of the short pulses 78 occurs in the gate actuation clock signal 76, however, gate 68 is actuated to its alternate condition and supplies the high frequency clock signal f_4 to shift register 67. This enables the shift register 67 to receive data from shift register 64 in a rapid transfer operation and to clear previously recorded data when this is necessary. The gate actuation signal from clock 71 is also supplied to output gate 72 and closes the output gate during each of the brief transfer pulses 78. This is done to prevent high-frequency signals from being forwarded from shift register 67 to converter 73 during those time intervals in which data is being transferred from shift register 64 to shift register 67. In some instances the output gate 72 can be omitted.

The illustrated wave form for the gate actuation signal 76 is not essential; the same effect can be realized using signals of other wave forms and different duty cycles. However, the duty cycle for the gate means in system 60 must be quite high, in terms of time for record-readout operations compared to time for transfer operations.

For effective operation, the ratio between frequencies f_1 and f_2 should be kept within reasonable limits. For downshift operation, f_1/f_2 should be greater than one but preferably not greater than three. For an upshift in frequency, the ratio f_2/f_1 should be at least unity and preferably smaller than three. The frequency

f_3 is preferably in the range of 10–100 hz as described above for the interruption of sampling frequency for the embodiment of FIG. 1. The transfer clock f_4 should operate at an extremely high frequency in comparison to the other operating frequencies in the system. For example, in a frequency downshift operation with a desired ratio of two to one, the recording clock frequency f_1 may be established at 100 khz with the readout clock frequency f_2 being 50 khz. Under these circumstances, the operating frequency for the transfer clock f_3 , should be of the order of 1 to 10 megahertz or even higher.

The series construction for the shift registers that is used in system 60 entails a slight signal interruption compared to the parallel arrangement of system 10, but the overall effect on performance is not appreciable. As before, f_3 may be made a subharmonic of f_2 , with the gate actuation clock 71 controlled by a frequency divider driven by signal f_2 .

We claim:

1. A processing system for frequency modification of a speech or other original audio signal, which retains the time span of the original signal, comprising:

analog-digital converter means for converting an original audio signal to a digital data signal;

two temporary serial storage means, each having a capacity of n digits, where n is a positive integer greater than or equal to 32;

recording means for alternately recording said digital data signal in said two storage means at a primary bit rate f_1 ;

readout means for reading out said digital data signal from said storage means, in groups of digits taken alternately from said two storage means, at a secondary bit rate f_2 substantially different from f_1 , to develop an output signal;

synchronizing means for actuating said recording means and said readout means at time intervals recurring at a frequency f_3 , where f_3 is approximately equal to $f_2/2n$ in the range of 10 to 100 hz; and

output means, comprising a digital-analog converter, for utilizing said output signal to develop a processed audio signal with a frequency modification of f_1/f_2 but having the same time span as the original audio signal.

2. A processing system for frequency modification of a speech or other original audio signal which retains the time span of the original signal, comprising:

first temporary serial storage means, having a capacity of n digits, where n is a positive integer greater than or equal to 32;

second temporary serial storage means also having a capacity of n digits;

a first clock signal source for developing a first clock signal of frequency f_1 ;

a second clock signal source for developing a second clock signal of frequency f_2 , f_2 being substantially different from frequency f_1 ;

an analog-digital converter;

means for applying an original audio signal to said converter to develop a digital data signal;

means for supplying the digital data signal to the inputs of both of said temporary storage means;

clock gate means for applying said first and second clock signals to said temporary storage means, in alternation, to store said digital data signal therein at rate f_1 and to read out said digital data signal therefrom at rate f_2 ;

output gate means for alternately coupling the outputs of said temporary stores to a single output circuit;

gate actuation means, comprising a frequency divider with a division ratio of approximately $1/2n$, having an input coupled to said second clock signal source and having an output coupled to both said gate means, for developing and supplying to both said gate means an actuating having a frequency f_3 , where f_3 is approximately equal to $f_2/2n$, so that said output circuit always receives said digital data read out at rate f_2 ;

and a digital-analog converter, connected to the output gate means, for developing a regenerated speech signal with a frequency change ratio of f_1/f_2 but within the same time span as the original audio signal.

3. An audio signal processing system according to claim 2 in which said actuating signal frequency f_3 is in the range of 10 to 100 hz.

4. An audio signal processing system according to claim 2 in which said a actuating signal frequency f_3 is approximately 33 hz.

5. An audio signal processing system according to claim 4 in which the value of n is greater than 500.

6. An audio signal processing system according to claim 4 in which the value of n is a power of two.

7. An audio signal processing system according to claim 4 in which the value of n is a power of two exceeding 2^9 .

8. An audio signal processing system according to claim 2 in which said analog-digital converter is a delta modulator driven by the first clock signal f_1 .

9. A processing system for frequency modification of an audio-frequency analog signal which retains the same time span as the original signal, comprising:

a first temporary serial storage means, having a capacity of n digits, where n is a positive integer greater than or equal to 32;

a second temporary serial storage means, also having a capacity of n digits and having its input stage connected to the output stage of said first temporary storage means;

a recording clock signal source for developing a recording clock signal of frequency f_1 ;

a readout clock signal source for developing a readout clock signal of frequency f_2 , f_2 being substantially different from frequency f_1 ;

a transfer clock signal source for developing a transfer clock signal of frequency f_4 such that f_4 is very much greater than f_1 and f_4 is very much greater than f_2 ;

an analog to digital converter;

means for applying an original audio-frequency analog signal to said converter to develop a digital data signal;

means for supplying the digital data signal to the input of said first temporary storage means;

clock input gate means for alternately applying said

recording and transfer clock signals to said first temporary storage means, and for alternatively applying said readout and transfer clock signals to said second temporary storage means;

a digital-analog converter;

output gate means for coupling the output of said second temporary storage means to said digital analog converter; and

gate actuation means for developing a gate actuation signal of a frequency f_3 , where f_3 is approximately equal to $f_2/2n$ and is lower than f_1 , and for applying said gate actuation signal to actuate both said gate means, applying said transfer clock signal to both said storage means and cutting off the input to said digital-analog converter periodically at frequency f_3 to enable said digital-analog converter to develop a regenerated speech signal with a frequency change ratio of f_1/f_2 but within the same time span as the original audio signal.

10. A processing system for frequency modification of an audio signal, according to Claim 9, in which the time during which said transfer clock signal is applied to said storage means, in each cycle of said gate actuation signal, is much smaller than the time during which said recording and readout clock signals are supplied thereto.

11. A processing system system for frequency modification of an audio signal, according to Claim 9, in which f_3 is in the range of 10-100 hz.

12. A processing system for frequency modification of a speech or other original audio signal, which retains the time span of the original signal, comprising:

analog-digital converter means for converting an original audio signal to a digital data signal;

first temporary serial storage means, having a capacity of n digits, where n is a positive integer greater than or equal to 32;

recording means for recording said digital data signal in said first temporary serial storage means at a primary bit rate f_1 ;

second temporary serial storage means also having a capacity of n digits, and, having an input connected to the output of said first temporary serial storage means;

transfer means for transferring said digital data signal from said first storage means to said second storage means, at a transfer rate f_4 very much higher than rate f_1 ;

readout means for reading out said digital data signal from said second storage means at a secondary bit rate f_2 substantially different from f_1 and very much lower than f_4 , to develop an output signal;

synchronizing means for actuating said transfer means and for interrupting said recording means and said readout means, at time intervals recurring at a frequency f_3 , where f_3 is approximately equal to $f_2/2n$ in the range of 10 to 100 hz, said time intervals being very much smaller than $1/f_3$; and

output means, comprising a digital-analog converter, for utilizing said output signal to develop a processed audio signal with a frequency modification of f_1/f_2 but having the same time span as the original audio signal.

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