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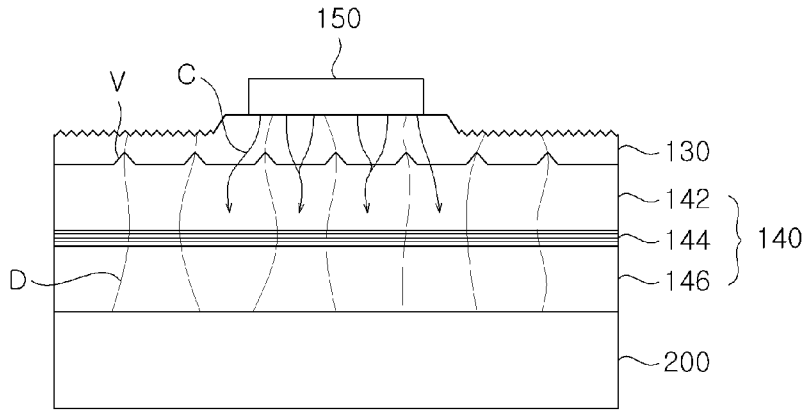
(54) Title: VERTICAL LIGHT EMITTING DIODE WITH V-PIT CURRENT SPREADING MEMBER AND MANUFACTURING METHOD OF THE SAME



(57) Abstract: Disclosed are a vertical type light emitting diode and a method of fabricating the same. The vertical type light emitting diode includes: a support substrate; a p-type electrode formed on the support substrate; a p-type semiconductor layer formed on the p-type electrode; an active layer formed on the p-type semiconductor layer; an n-type semiconductor layer formed on the active layer; a nitride semiconductor layer formed on the n-type semiconductor layer and having V-pits filled with the nitride semiconductor layer; and an n-type electrode formed on the nitride semiconductor layer, wherein a plurality of protrusions formed on a growth substrate for growing the nitride semiconductor layer causes the V-pits to be formed in alignment with the plurality of protrusions, and V-pit regions have higher resistance than surrounding regions.

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Description

Title of Invention: VERTICAL LIGHT EMITTING DIODE WITH V-PIT CURRENT SPREADING MEMBER AND MANUFACTURING METHOD OF THE SAME

Technical Field

[1] Exemplary embodiments relates to a vertical type light emitting diode and a method of fabricating the same, and more particularly, to a vertical type light emitting diode which includes high-resistance V-pits formed in electric current leakage region to improve withstand voltage characteristics.

Background Art

[2] Generally, a light emitting diode directly converts electric current into light using a principle that electrons supplied from an n-type semiconductor layer are recombined with holes supplied from a p-type semiconductor layer to emit light upon application of voltage to semiconductor layers composed of the p-type semiconductor layer, an active layer, and the n-type semiconductor layer. Such a light emitting diode has good energy conversion efficiency, long lifespan, and excellent light directivity, and can be driven at low voltage. In addition, since light emitting diodes do not require preheating time and a complex drive circuit and can withstand impact and vibration, the light emitting diodes are regarded as a next-generation light source to replace existing light sources such as incandescent lamps, fluorescent lamps, and mercury lamps.

[3] Although luminous efficacy of the light emitting diode generally depends upon internal quantum efficiency and extraction efficiency, it is more important to allow voltage to be normally applied to the light emitting diode than other factors.

[4] Particularly, unlike a lateral type light emitting diode, a vertical type light emitting diode is fabricated by a process of growing epitaxial layers on a sapphire substrate 11, as shown in Figure 1, followed by removing the sapphire substrate. In addition, an n-electrode is formed to face a p-electrode. Further, since threading dislocation of a nitride semiconductor layer 13 grown on the sapphire substrate 11 due to a difference in lattice parameter between the nitride semiconductor layer and the sapphire substrate coincides with the direction in which electric current flows upon operation of the light emitting diode, current leakage is more likely to increase. Such threading dislocation reduces a probability of recombination between electrons and holes, thereby causing reduction in electrical properties of the light emitting diode and thus deterioration in luminous efficacy.

[5] **Prior Literature

[6] *Patent Document

[7] Korean Patent Publication No. 10-2014-0049273 A (Publication Date: April 25, 2014)

Disclosure of Invention

Technical Problem

[8] Exemplary embodiments provide a vertical type light emitting diode which can minimize deterioration in electrical characteristics caused by defects due to a difference in lattice parameter between a sapphire substrate and semiconductor layers, and a method of fabricating the same.

[9] Exemplary embodiments provide a vertical type light emitting diode which exhibits substantially enhanced light extraction efficiency by removing a substrate having unevenness such that the unevenness is transferred to a surface of an n-type semiconductor layer.

Solution to Problem

[10] In accordance with one aspect of the present disclosure, a vertical type light emitting diode includes: a support substrate; a p-type electrode formed on the support substrate; a p-type semiconductor layer formed on the p-type electrode; an active layer formed on the p-type semiconductor layer; an n-type semiconductor layer formed on the active layer; a nitride semiconductor layer formed on the n-type semiconductor layer and having V-pits filled with the nitride semiconductor layer; and an n-type electrode formed on the nitride semiconductor layer, wherein a plurality of protrusions formed on a growth substrate for growing the nitride semiconductor layer causes the V-pits to be formed in alignment with the plurality of protrusions, and V-pit regions have higher resistance than surrounding regions.

[11] The nitride semiconductor layer may be further formed with a plurality of convex/concave portions by etching, and the V-pits may be formed between a lower surface of the n-type electrode and the active layer. In addition, the n-type electrode may be formed on a region of the n-type semiconductor layer remaining after partial removal of the n-type semiconductor layer including the V-pits.

[12] In accordance with another aspect of the present disclosure, a method of fabricating a vertical type light emitting diode includes: forming a first nitride semiconductor layer on a growth substrate having a plurality of protrusions formed on a surface thereof such that the plurality of protrusions are exposed; forming a second nitride semiconductor layer on the first nitride semiconductor layer such that the second nitride semiconductor layer covers upper portions of the plurality of protrusions and the first nitride semiconductor layer so as to be formed with V-pits; forming an n-type semiconductor layer on the second nitride semiconductor layer such that the V-pits are filled with the n-type semiconductor layer; forming an active layer on the n-type semi-

conductor layer; and forming a p-type semiconductor layer on the active layer, wherein the V-pits may be formed above the plurality of protrusions, respectively.

[13] The method may further include: removing the growth substrate and the first nitride semiconductor layer; and forming an electrode on the exposed second nitride semiconductor layer.

[14] The method may further include: performing dry or wet etching such that a plurality of convex/concave portions are formed on the exposed second nitride semiconductor layer, wherein the electrode may be formed on the second nitride semiconductor layer having the plurality of convex/concave portions formed thereon.

[15] The second nitride semiconductor layer may be etched to allow the V-pits to remain only in a partial region thereof, and the electrode is formed on the second nitride semiconductor layer having the remaining V-pits.

[16] V-pit regions having the V-pits formed therein may have higher resistance than surrounding regions; the first nitride semiconductor layer may be a low-concentration doped layer; and the second nitride semiconductor layer may be a high-concentration doped layer.

Advantageous Effects of Invention

[17] According to exemplary embodiments, a substrate having a plurality of protrusions is removed such that the protrusions of the substrate are transferred to an n-type semiconductor layer, thereby substantially improving light extraction efficiency of a light emitting diode.

[18] In a vertical type light emitting diode in the related art, dislocations are concentrated at tips of the plurality of protrusions, thereby causing increase in current leakage, and electrodes are disposed to face each other, thereby causing increase in current leakage. However, in a vertical type light emitting diode according to the exemplary embodiments, V-pits aligned with the plurality of protrusions are formed above the plurality of protrusions of a sapphire substrate, which is a growth substrate, whereby current paths can be formed between V-pit regions having higher resistance than surrounding regions to allows electric current to intensively flow through the current paths, thereby improving leakage characteristics of the vertical type light emitting diode while increasing VR.

Brief Description of Drawings

[19] Figure 1 is a view of a typical vertical type light emitting diode.

[20] Figure 2 is a view of a vertical type light emitting diode according to one exemplary embodiment of the present disclosure.

[21] Figure 3 is a view of a V-pit of the vertical type light emitting diode according to the exemplary embodiment of the present disclosure, showing a thickness of an inclined

surface of the V-pit when the V-pit is completely filled with an n-type semiconductor layer.

[22] Figures 4 to 7 are views illustrating a method of fabricating a vertical type light emitting diode according to one exemplary embodiment of the present disclosure.

[23] Figure 8 is a view of a vertical type light emitting diode according to another exemplary embodiment of the present disclosure.

[24] Figure 9 is a graph depicting VR characteristics of a vertical type light emitting diode according to one exemplary embodiment of the present disclosure.

Mode for the Invention

[25] Hereinafter, exemplary embodiments of the present disclosure will be described in detail with reference to the accompanying drawings.

[26] Figure 2 is a view of a vertical type light emitting diode according to one exemplary embodiment of the present disclosure.

[27] A vertical type light emitting diode 100 according to this embodiment includes a support substrate 200, a p-type semiconductor layer146, an active layer 144, an n-type semiconductor layer 142, and a second nitride semiconductor layer 130.

[28] The support substrate 200 may be an insulating substrate, a conductive substrate, or a circuit board. For example, the support substrate 200 may be a sapphire substrate, a gallium nitride substrate, a glass substrate, a silicon carbide substrate, a silicon substrate, a metal substrate, or a ceramic substrate. In addition, the support substrate 200 may be bonded to the p-type semiconductor layer 146. In this structure, a bonding layer (not shown) may be disposed between the support substrate 200 and the p-type semiconductor layer 146 to bond the support substrate to the p-type semiconductor layer.

[29] Here, the bonding layer may include a metallic material. Further, a reflective layer (not shown) may be formed between the support substrate 200 and the p-type semiconductor layer 146. The reflective layer may include a reflective metal layer and a barrier metal layer, wherein the reflective metal layer may be covered with the barrier metal layer. In addition, a transparent electrode may be formed between the support substrate 200 and the p-type semiconductor layer 146.

[30] The p-type semiconductor layer 146 may be a semiconductor layer doped with p-type dopants such as Mg. The p-type semiconductor layer 146 may be formed on the support substrate 200, have a monolayer or multilayer structure, and include a p-type clad layer and a p-type contact layer. In addition, a transparent electrode such as ITO may be disposed on the p-type nitride semiconductor layer.

[31] The active layer 144 emits light having a certain energy level through recombination of electrons and holes and is disposed on the p-type semiconductor layer 146. The

active layer 144 may have a single-quantum well structure or a multi-quantum well (MQW) structure in which quantum barrier layers and quantum well layers are alternately stacked one above another. The quantum barrier layer may be a semiconductor layer formed of a nitride such as GaN, InGaN, AlGaN or AlInGaN and having a wider bandgap than the quantum well layer. In one exemplary embodiment, the quantum barrier layer may be formed of AlInGaN to enhance recombination efficiency of carriers.

[32] The quantum well layer may be a nitride semiconductor layer having a narrower bandgap than the quantum barrier layer. For example, the quantum well layer may be a gallium nitride-based semiconductor layer formed of, for example, InGaN. A composition ratio for adjustment of bandgap may depend upon desired light wavelength.

[33] The n-type semiconductor layer 142 is a nitride-based semiconductor layer doped with n-type dopants and may be, for example, a Si-doped nitride semiconductor layer. The n-type semiconductor layer 142 may be doped with Si in a concentration of 5E17/cm3 to 5E19/cm3. The n-type semiconductor layer 142 may be formed by MOCVD, for example, by supplying a metal source gas to a chamber, followed by growth at 100°C to 1200°C (for example, at 1050°C to 1100°C) at a growth pressure of 150 Torr to 200 Torr.

[34] The second nitride semiconductor layer 130 is disposed on the n-type semiconductor layer 142 and may be doped with n-type dopants in a higher concentration than the n-type semiconductor layer 142. Since the nitride semiconductor layer 130 is grown on a growth substrate 110 with a plurality of protrusions 112 exposed thereon, V-pits V aligned with the plurality of protrusions 112 of the growth substrate 110 are formed at an interface between the second nitride semiconductor layer 130 and the n-type semiconductor layer 142. Formation of the V-pits V in the second nitride semiconductor layer 130 will be described below. V-pit regions having the V-pits formed therein are more difficult to dope with Si than the surrounding regions and thus have higher resistance than surrounding regions. Specifically, this is because an inclined surface of the V-pit V is semi-polar and thus makes it more difficult for Si to penetrate crystals than a horizontal surface having polarity.

[35] In addition, as shown in Figure 3, when a surface of the second nitride semiconductor layer having the V-pits V is subjected to doping, since a thickness t3 of the inclined surface of the V-pit V in a direction perpendicular to the inclined surface is smaller than a thickness t1 of the horizontal surface thereof, the V-pit regions are doped at a relatively low level and thus exhibit increased resistance. Here, although the thickness t1 of the horizontal surface is the same as or similar to the thickness t2 of the inclined surface in the vertical direction, the thickness t3 of the inclined surface is smaller than the thickness t1 of the horizontal surface.

[36] Further, a plurality of jagged cones is formed on an upper surface of the second nitride semiconductor layer 130 by etching. An n-type electrode 150 may be formed on the etched second nitride semiconductor layer 130. Further, the plurality of jagged cones may be formed around the n-type electrode 150 rather than being formed at a portion at which the n-type electrode 150 is to be formed. Here, the plurality of cones is different from unevenness resulting from removal of the growth substrate. The plurality of cones and the unevenness may overlap each other, and the plurality of cones may be smaller in unit size than the unevenness.

[37] As described above, since the V-pit regions formed in the second nitride semiconductor layer have higher resistance than the surrounding regions, current paths C can be formed between the adjacent V-pits V to allow electric current to intensively flow therethrough upon application of electric current through the n-type electrode 150. As a result, reverse voltage VR can be increased, thereby reducing current leakage while improving withstand voltage characteristics.

[38] Figures 4 to 7 are views illustrating a method of fabricating a vertical type light emitting diode 100 according to one exemplary embodiment of the present disclosure.

[39] A method of fabricating a vertical type light emitting diode according to one exemplary embodiment will be described with reference to Figures 4 to 7, and Figure 2 will also be referred to, as needed.

[40] Referring to Figure 4, a first nitride semiconductor layer 120 is grown on a growth substrate 110. The growth substrate 110 is not particularly limited so long as the substrate allows a luminous structure 140 to grow thereon. For example, the growth substrate may be a sapphire substrate, a silicon carbide substrate, a silicon substrate, a gallium nitride substrate, or an aluminum nitride substrate. In this exemplary embodiment, the growth substrate 110 is a patterned sapphire substrate (PSS). The sapphire substrate is patterned to have a plurality of protrusions 112. Although the plurality of protrusions 112 is shown as having a hemispherical shape, the plurality of protrusions may be formed in various shapes, as needed.

[41] As described above, the first nitride semiconductor layer 120 is grown on the growth substrate 110 with the plurality of protrusions 112 formed thereon. Here, the first nitride semiconductor layer 120 is grown only between the plurality of protrusions 112 rather than being grown over the entirety of the growth substrate 110. In other words, the first nitride semiconductor layer 120 is grown three-dimensionally such that upper sides of the plurality of protrusions 112 are exposed. Here, the first nitride semiconductor layer 120 may include GaN. When the growth substrate 110 is a sapphire substrate, the first nitride semiconductor layer 120 may serve as both a nucleation layer allowing growth of other semiconductor layers and a buffer layer relieving stress due to a difference in lattice parameter between the sapphire substrate and other semi-

conductor layers.

[42] Referring to Figure 5, a second nitride semiconductor layer 130 is grown on the first nitride semiconductor layer 120. As described above, the second nitride semiconductor layer 130 includes silicon. The second nitride semiconductor layer 130 is grown two-dimensionally to cover the first nitride semiconductor layer 120 and the growth substrate 110. Here, the plurality of protrusions 112 of the growth substrate 110 causes V-pits V to be formed above the plurality of protrusions. This is because the plurality of protrusions 112 allows threading dislocations to be generated above the plurality of protrusions, thereby making it difficult to achieve silicon doping in regions above the plurality of protrusions.

[43] N-type dopants doped in a high concentration can cause deterioration in crystal quality. Thus, the underlying first nitride semiconductor layer 120 may be doped with the n-type dopants in a lower concentration than the second nitride semiconductor layer 130. On the other hand, the second nitride semiconductor layer 130 has the V-pits V causing difference in resistance and thus may be doped with the n-type dopants in a higher concentration than upper and lower layers adjacent thereto.

[44] The V-pits V may be formed above the plurality of protrusions formed on the growth substrate 110 to be aligned with the plurality of protrusions 112, respectively.

[45] Referring to Figure 6, a luminous structure 140 is grown on the second nitride semiconductor layer 130 having the V-pits V to fill the V-pits V. Here, the V-pits V formed in the second metal compound are filled with the n-type semiconductor layer 142.

[46] Referring to Figure 7, after completion of growth of the luminous structure 140, the growth substrate 110 is separated and removed together with the first nitride semiconductor layer 120. In one exemplary embodiment, the growth substrate may be separated and removed from the luminous structure 140 by laser lift-off, chemical lift-off, stress lift-off, thermal lift-off, lapping, or the like. Here, Figure 7 shows a stack structure rotated 180 degrees after removing the growth substrate 110 and the first nitride semiconductor layer 120 shown in Figure 6.

[47] After the growth substrate 110 is separated and removed as shown in Figure 7, a plurality of cones may be formed by etching an upper surface of the first nitride semiconductor layer 120. Here, the plurality of cones formed by etching the first nitride semiconductor layer 120 may be formed over the entire surface of a first metal compound or may be formed only at a portion other than a region in which the n-type electrode 150 is to be formed, as shown in Figure 2.

[48] Figure 8 is a view of a vertical type light emitting diode according to another exemplary embodiment of the present disclosure.

[49] A vertical type light emitting diode 100 according to this exemplary embodiment includes a support substrate 200, a p-type semiconductor layer 146, an active layer

144, an n-type semiconductor layer 142, and a second nitride semiconductor layer 130. In description of the vertical type light emitting diode 100 according to this embodiment, descriptions of the same components as those of the above embodiment will be omitted.

[50] The vertical type light emitting diode 100 according to this exemplary embodiment is fabricated by processes as shown in Figs 4 to 7, as in the vertical type light emitting diode 100 according to the above embodiment. However, etching of the second nitride semiconductor layer 130 is performed until the second nitride semiconductor layer 130 is entirely removed excluding a region in which an n-type electrode 150 is to be formed, and the n-type semiconductor layer 142 is partially exposed. As a result, a plurality of cones may be formed on an upper surface of the exposed n-type semiconductor layer 142. The n-type electrode 150 is formed on the second nitride semiconductor layer 130 having no cone formed thereon.

[51] Since the n-type electrode 150 is formed as above, the second nitride semiconductor layer 130 is present only under the n-type electrode 150, with the V-pits V remaining in the second nitride semiconductor layer 130. Thus, when electric current applied through the n-type electrode 150 flows through the second nitride semiconductor layer 130, current paths C are formed between V-pit regions, whereby the electric current can be applied to a luminous structure 140 through the current paths C.

[52] As such, the V-pits V are disposed on a region under the n-type electrode 150, i.e. a region where leakage is most likely to occur, thereby providing intensive leakage protection. On the other hand, in other regions, the thickness of the n-type semiconductor layer 142 may be decreased to reduce the length of an optical path, thereby improving light extraction efficiency.

[53] Figure 9 is a graph depicting VR characteristics of a vertical type light emitting diode according to one exemplary embodiment of the present disclosure.

[54] In order to identify VR characteristics of a vertical type light emitting diode 100 according to one exemplary embodiment of the present disclosure, a 2" MP chip and a 4" RD chip were used. The 2" MP chip had a power output of 598 mW, a Vf of 2.99V, and a VR of 21.08, and the 4" RD chip (PSS Sub.) had a power output of 614 mW, a Vf of 2.99V, and a VR of 28.08.

[55] [Table 1]

4" M+S PSS Sub. Data						
Lot ID	W/F No.	Yield	VF	WD	PO	VR
V14K017A	R141017059B04	86.50%	2.91	454.99	625.19	27.65
	V14K017AR141017059B05	86.80%	2.92	454.07	619.8	28.28
	V14K017AR141017059B07	89.40%	2.91	454.53	619.61	27.97
	V14K017AR141017059B10	76.50%	2.93	454.66	615.33	28.3
	V14K017AR141017059B11	80.50%	2.91	452.81	616.32	27.43
	V14K017AR141017059B14	68.10%	2.9	452.77	624.92	28.65
V14K018A	R141017059C03	91.30%	2.88	453.28	626.67	28.81
	V14K018AR141017059C04	80.50%	2.88	453.7	624.24	28.16
	V14K018AR141017059C06	82.60%	2.9	452.82	623.96	28.09
	V14K018AR141017059C07	90.40%	2.87	454.37	620.75	28.15
	V14K018AR141017059C12	75.00%	2.88	454.14	612.82	27.87
	V14K018AR141017059C13	65.70%	2.87	453.53	616.33	28.47

V14K019A	R141018059A04	61.70%	2.88	453.72	626.59	28.22
	V14K019AR141018059A07	92.30%	2.89	453.49	624.35	28.35
	V14K019AR141018059A08	96.20%	2.88	454.98	620.01	27.76
	V14K019AR141018059A10	90.60%	2.87	454.95	622.68	28.76
	V14K019AR141018059A11	90.20%	2.89	454.99	615.13	27.16
	V14K019AR141018059A14	65.90%	2.89	454.63	617.63	27.45
	Total Average	81.70%	2.89	454.02	620.69	28.08

[56] From test results, it was confirmed that the 4" RD chip using a patterned sapphire substrate (PSS) had a VR of 28.08 V and was thus enhanced in VR by 30% as compared with the 2" MP chip which had a VR of 21.08V. Here, the 2" MP chip was fabricated using a non-patterned flat sapphire substrate, and the 4"RD chip was fabricated using a patterned sapphire substrate. In total, eighteen 2" MP chips and eighteen 4" RD chips were used in the test.

[57] Although some embodiments and features of the present disclosure have been described above, it should be understood that these embodiments and features are given for illustration only and are not to be construed in any way as limiting the present disclosure. Therefore, the scope and sprit of the present disclosure should be defined only by the accompanying claims and equivalents thereof.

[58] <List of Reference Numerals>

[59] 100: Vertical type light emitting diode

[60] 110: Growth substrate 112: Protrusion

[61] 120: First nitride semiconductor layer

[62] 130: Second nitride semiconductor layer

[63] 140: Luminous structure 142: N-type semiconductor layer

[64] 144: Active layer 146: P-type semiconductor layer

[65] 150: Electrode 200: Support substrate

[66] V: V-pit D: Threading dislocation

[67] C: Current path

Claims

[Claim 1] A vertical type light emitting diode comprising:
a support substrate;
a p-type electrode formed on the support substrate;
a p-type semiconductor layer formed on the p-type electrode;
an active layer formed on the p-type semiconductor layer;
an n-type semiconductor layer formed on the active layer;
a nitride semiconductor layer formed on the n-type semiconductor layer and having V-pits filled with the nitride semiconductor layer; and
an n-type electrode formed on the nitride semiconductor layer,
wherein a plurality of protrusions formed on a growth substrate for growing the nitride semiconductor layer causes the V-pits to be formed in alignment with the plurality of protrusions, and
V-pit regions having the V-pits formed therein have higher resistance than surrounding regions.

[Claim 2] The vertical type light emitting diode according to claim 1, wherein the nitride semiconductor layer is further formed with a plurality of convex/concave portions by etching.

[Claim 3] The vertical type light emitting diode according to claim 1, wherein the V-pits are formed between a low surface of the n-type electrode and the active layer.

[Claim 4] The vertical type light emitting diode according to claim 1, wherein the n-type electrode is formed on a region of the n-type semiconductor layer remaining after partial removal of the n-type semiconductor layer including the V-pits.

[Claim 5] A method of fabricating a vertical type light emitting diode, comprising:
forming a first nitride semiconductor layer on a growth substrate having a plurality of protrusions formed on a surface thereof such that the plurality of protrusions are exposed;
forming a second nitride semiconductor layer on the first nitride semiconductor layer such that the second nitride semiconductor layer covers upper portions of the plurality of protrusions and the first nitride semiconductor layer so as to be formed with V-pits;
forming an n-type semiconductor layer on the second nitride semiconductor layer such that the V-pits are filled with the n-type semiconductor layer;

forming an active layer on the n-type semiconductor layer; and
forming a p-type semiconductor layer on the active layer,
wherein the V-pits are formed above the plurality of protrusions, respectively.

[Claim 6] The method of fabricating a vertical type light emitting diode according to claim 5, further comprising:
removing the growth substrate and the first nitride semiconductor layer; and
forming an electrode on the exposed second nitride semiconductor layer.

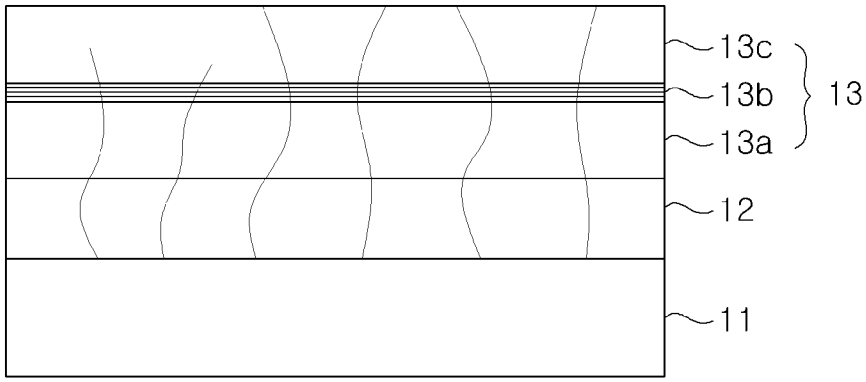
[Claim 7] The method of fabricating a vertical type light emitting diode according to claim 6, further comprising:
performing dry or wet etching such that a plurality of convex/concave portions are formed on the exposed second nitride semiconductor layer,
wherein the electrode are formed on the second nitride semiconductor layer having the plurality of convex/concave portions formed thereon.

[Claim 8] The method of fabricating a vertical type light emitting diode according to claim 7, wherein the second nitride semiconductor layer is etched to allow the V-pits to remain only in a partial region thereof, and the electrode is formed on the second nitride semiconductor layer having the remaining V-pits.

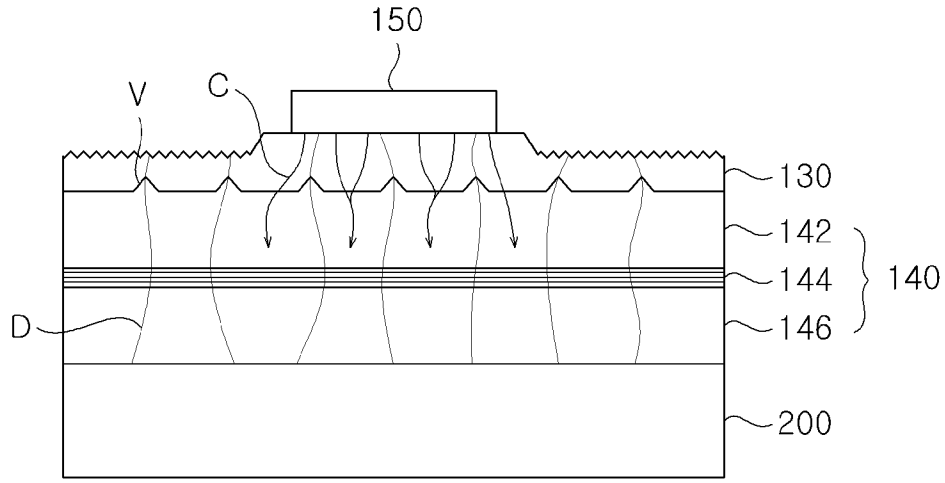
[Claim 9] The method of fabricating a vertical type light emitting diode according to claim 5, wherein V-pit regions having the V-pits formed therein have higher resistance than surrounding regions.

[Claim 10] The method of fabricating a vertical type light emitting diode according to claim 5, wherein the first nitride semiconductor layer is a low-concentration doped layer and the second nitride semiconductor layer is a high-concentration doped layer.

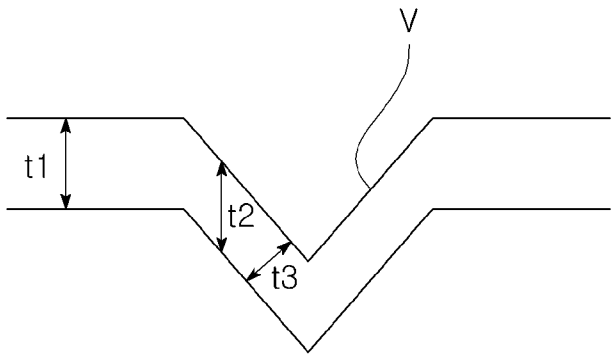
[Fig. 1]



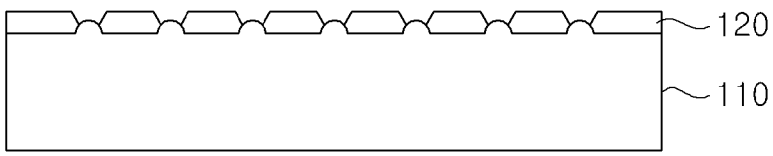
[Fig. 2]



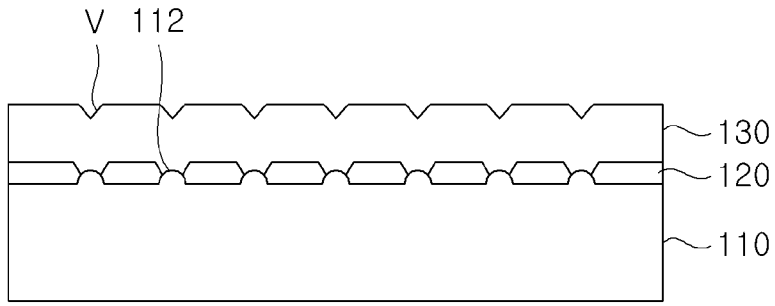
[Fig. 3]



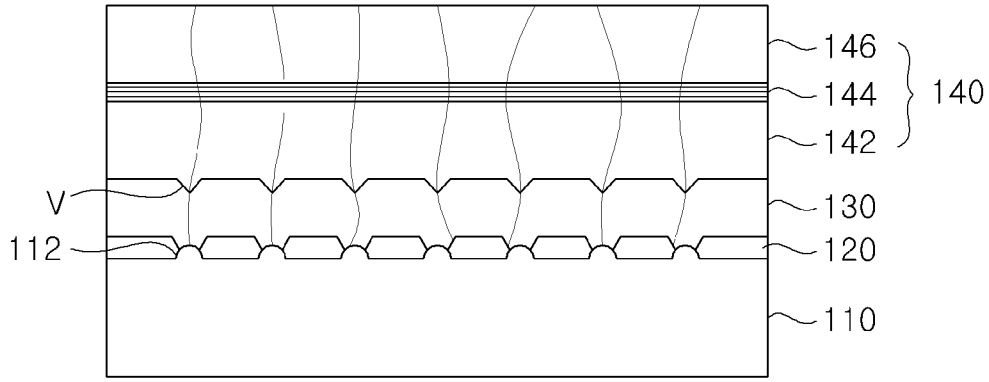
[Fig. 4]



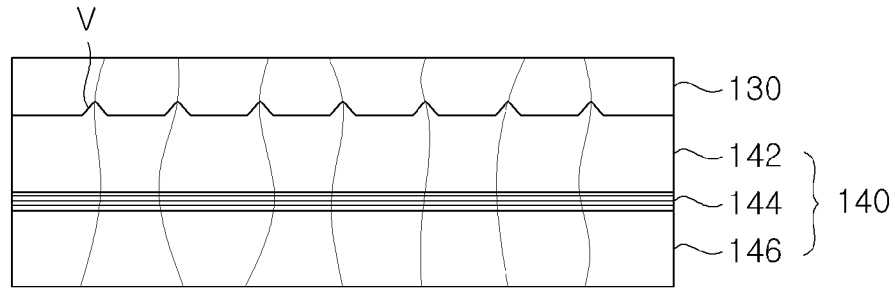
[Fig. 5]



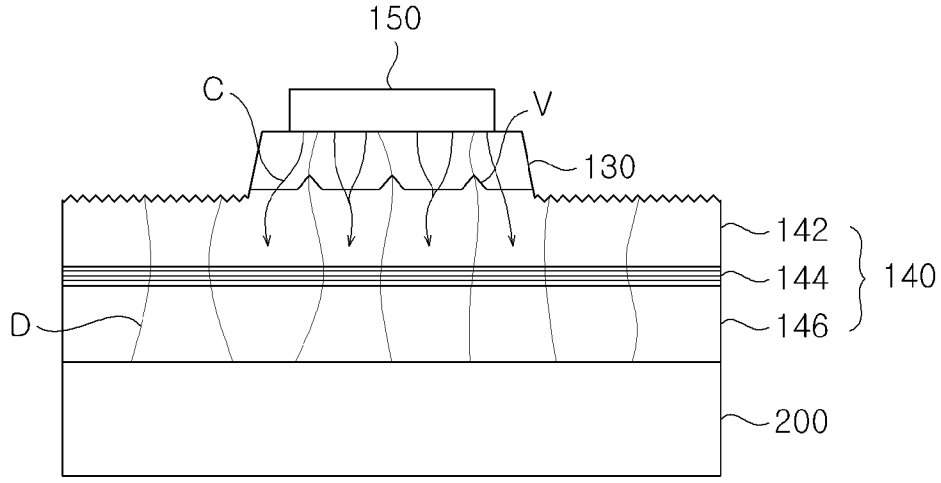
[Fig. 6]



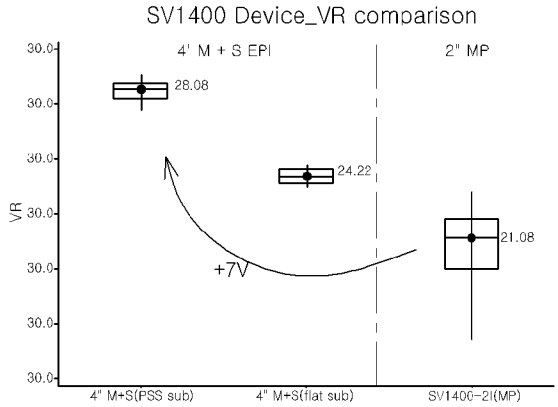
[Fig. 7]



[Fig. 8]



[Fig. 9]


SV1400 Device_VR comparison
4' M + S EPI
2" MP
28.08
24.22
21.08
+7V
VR
30.0
4" M+S(PSS sub)
4" M+S(flat sub)
SV1406-2I(MP)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2015/012104

A. CLASSIFICATION OF SUBJECT MATTER

H01L 33/22(2010.01)i, H01L 33/36(2010.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 33/22; H01L 33/20; H01L 21/205; H01L 33/00; H01L 21/461; H01L 33/36

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: LED, protrusion, V-pits, current path, resistance

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	KR 10-2011-0041683 A (SAMSUNG LED CO., LTD.) 22 April 2011 See abstract, paragraphs 46-50 and figures 7-10.	1-10
A	KR 10-2005-0097075 A (SAMSUNG ELECTRO-MECHANICS CO., LTD.) 07 October 2005 See abstract, paragraphs 32-33, 38-40, claims 1-6 and figure 2.	1-10
A	JP 2007-266472 A (STANLEY ELECTRIC CO., LTD.) 11 October 2007 See paragraphs 22-48, claims 1-7 and figures 3-4.	1-10
A	JP 2012-064902 A (SHARP CORP.) 29 March 2012 See paragraphs 72-82 and figures 3, 6.	1-10
A	US 2010-0308359 A1 (RAJIV K. SINGH et al.) 09 December 2010 See abstract, paragraphs 80-90 and figures 9A-13.	1-10

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 February 2016 (25.02.2016)	**25 February 2016 (25.02.2016)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/KR2015/012104

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