United States Patent [19]

Tumbush

[11] **3,825,827**

[45] **July 23, 1974**

[54] **COLUMNAR DISPLAY FOR ELECTRICAL SIGNALS WITH DIGITAL SIGNAL LIMIT SET**

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[73] Assignee: **The Bendix Corporation,** Southfield, Mich.

[22] Filed: **Apr. 13, 1972**

[21] Appl. No.: **243,649**

[52] **U.S. Cl.** ..... **324/103 P,** 324/96, 324/122

[51] **Int. Cl.** **G01r 19/16,** G01r 13/02

[58] **Field of Search** ..... 324/103 P, 103 R, 122, 324/99 R, 157, 99 D, 96

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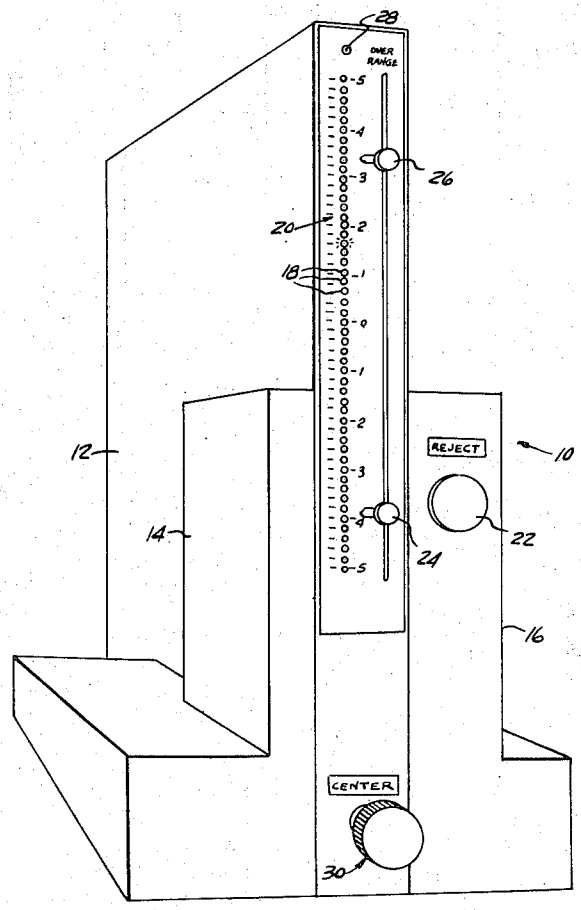
Assistant Examiner—Ernest F. Karlsen
Attorney, Agent, or Firm—John R. Benefiel

[57] **ABSTRACT**

A system for displaying the level of a variable electrical signal is disclosed, in which the variable electrical signals are converted into digital form, which are in turn decoded and arranged to consecutively activate a vertical series of indicator elements up and down the series in response to increases and decreases respectively in the digital signal, and with any preceding activated element being deactivated so that only a single individual indicator element corresponding to each digital signal is activated. Accordingly, the rise and fall of the position of the activated indicator element indicates the level of the electrical signal. An arrangement is also disclosed for providing signal limit indication comprising means for comparing the digital signal corresponding to the variable electrical signal with preset digital limit signals which means drives a limit indicator element whenever the generated digital signal is outside the preset values.

9 Claims, 8 Drawing Figures



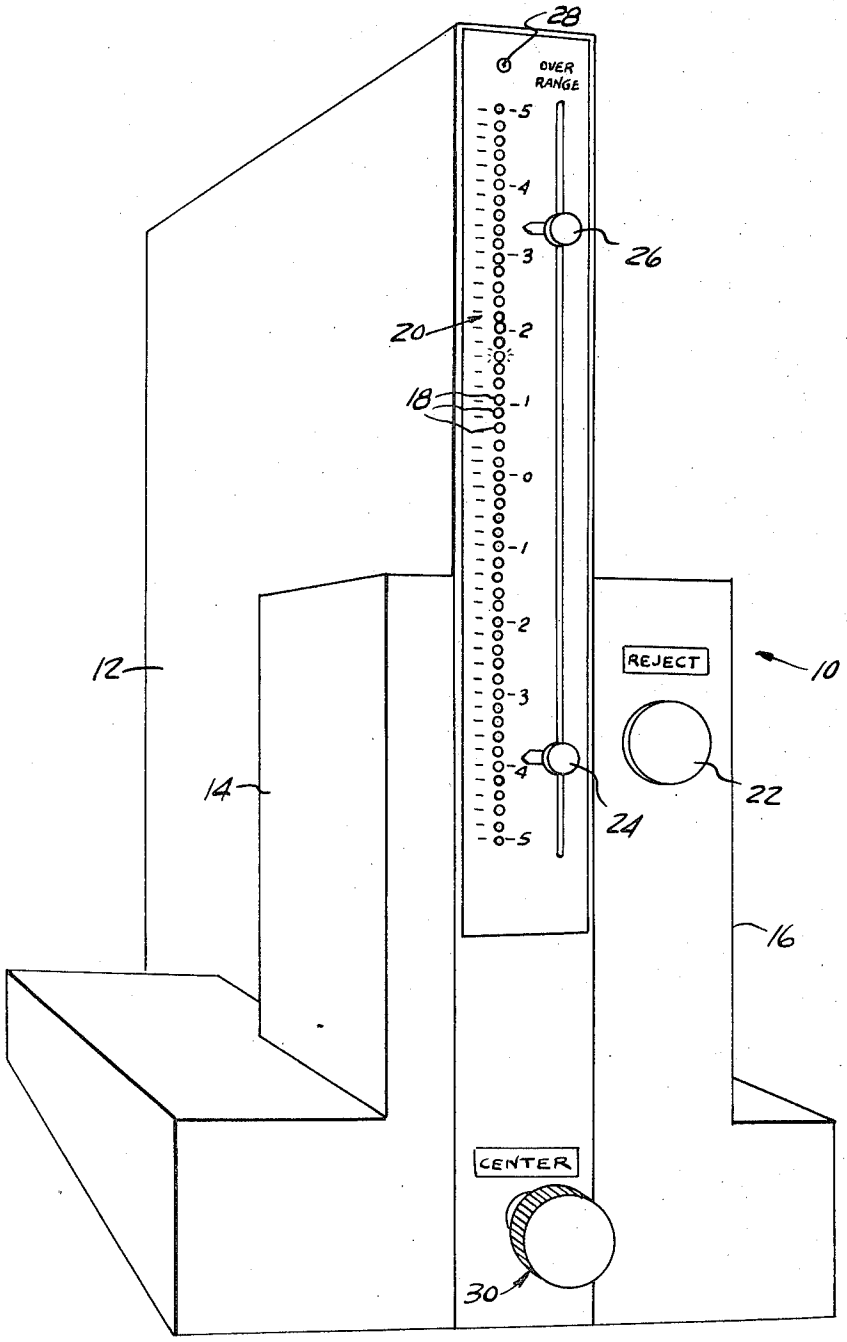
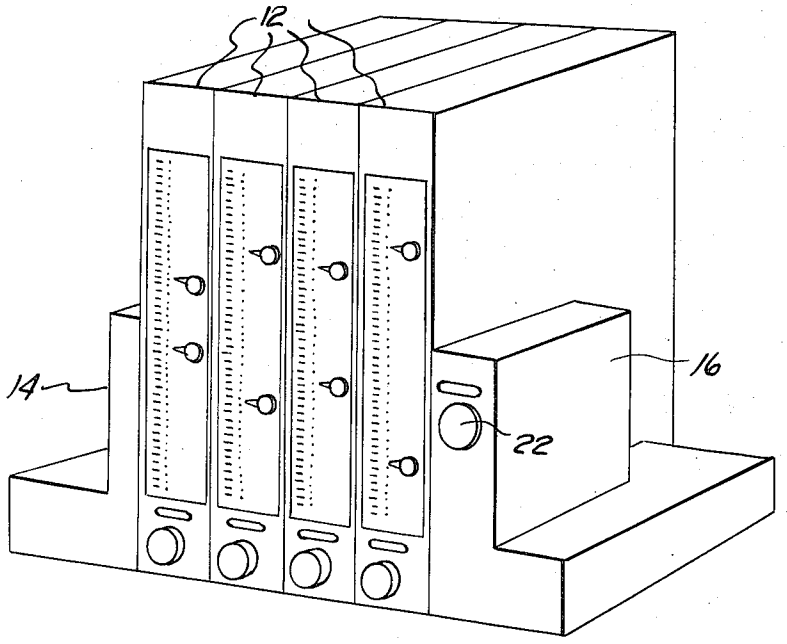

28
OVER RANGE
-5
-4
-3
-2
-1
0
-1
-2
-3
-4
-5
26
20
18
12
14
10
REJECT
22
24
16
CENTER
30

FIG. 1

FIG. 2


12
14
16
22

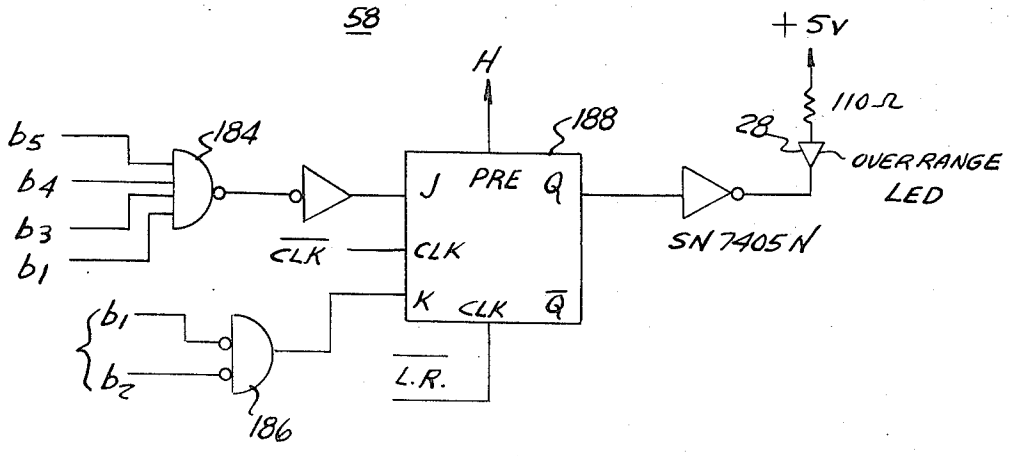

58
H
+5V
110Ω
28
OVER RANGE LED
188
184
b5
b4
b3
b1
J PRE Q
CLK
K CLK Q
SN 7405 N
b1
b2
186
L.R.

FIG. 8

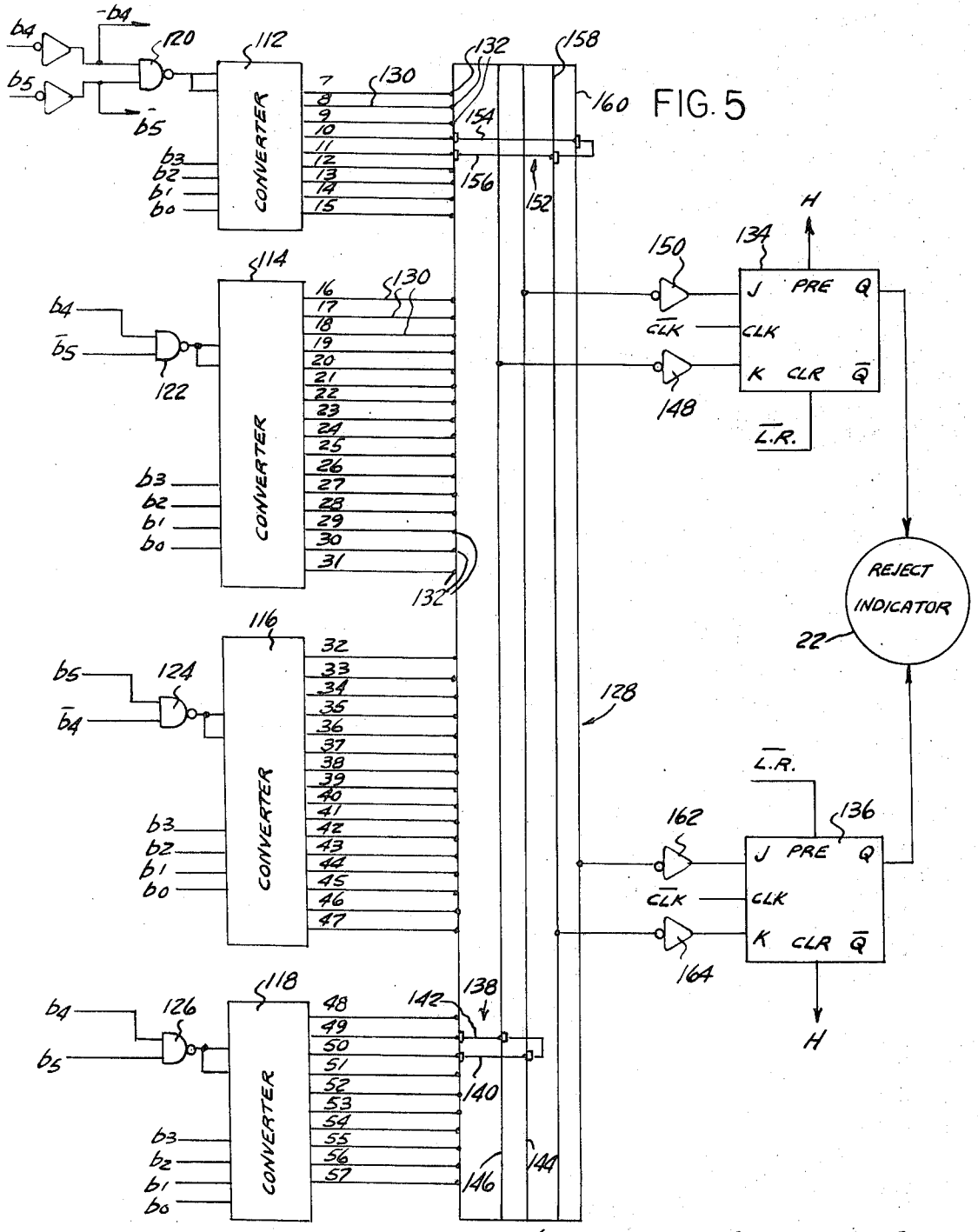

b4
b5
120
112
CONVERTER
130
132
158
160
154
156
152
b3
b2
b1
b0
114
122
116
124
118
126
134
136
150
148
162
164
J PRE Q
CLK
K CLR Q
H
L.R.
REJECT INDICATOR
22
128
138
140
142
144
146

FIG. 5

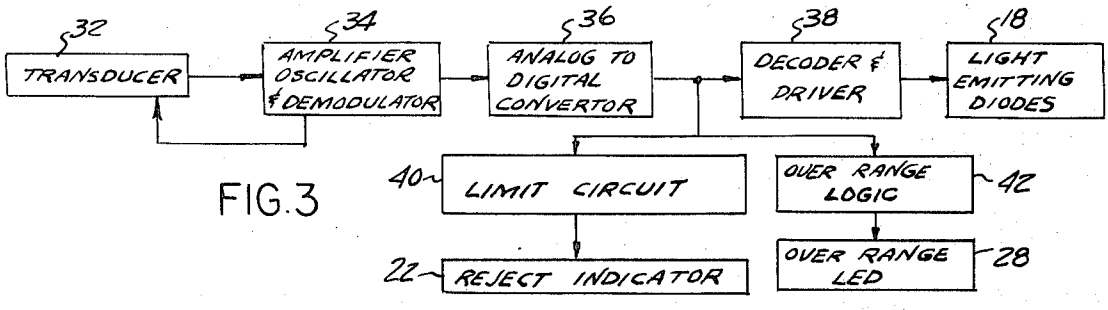

32
TRANSDUCER
34
AMPLIFIER OSCILLATOR & DEMODULATOR
36
ANALOG TO DIGITAL CONVERTOR
38
DECODER & DRIVER
18
LIGHT EMITTING DIODES
40
LIMIT CIRCUIT
42
OVER RANGE LOGIC
22
REJECT INDICATOR
28
OVER RANGE LED

FIG. 3

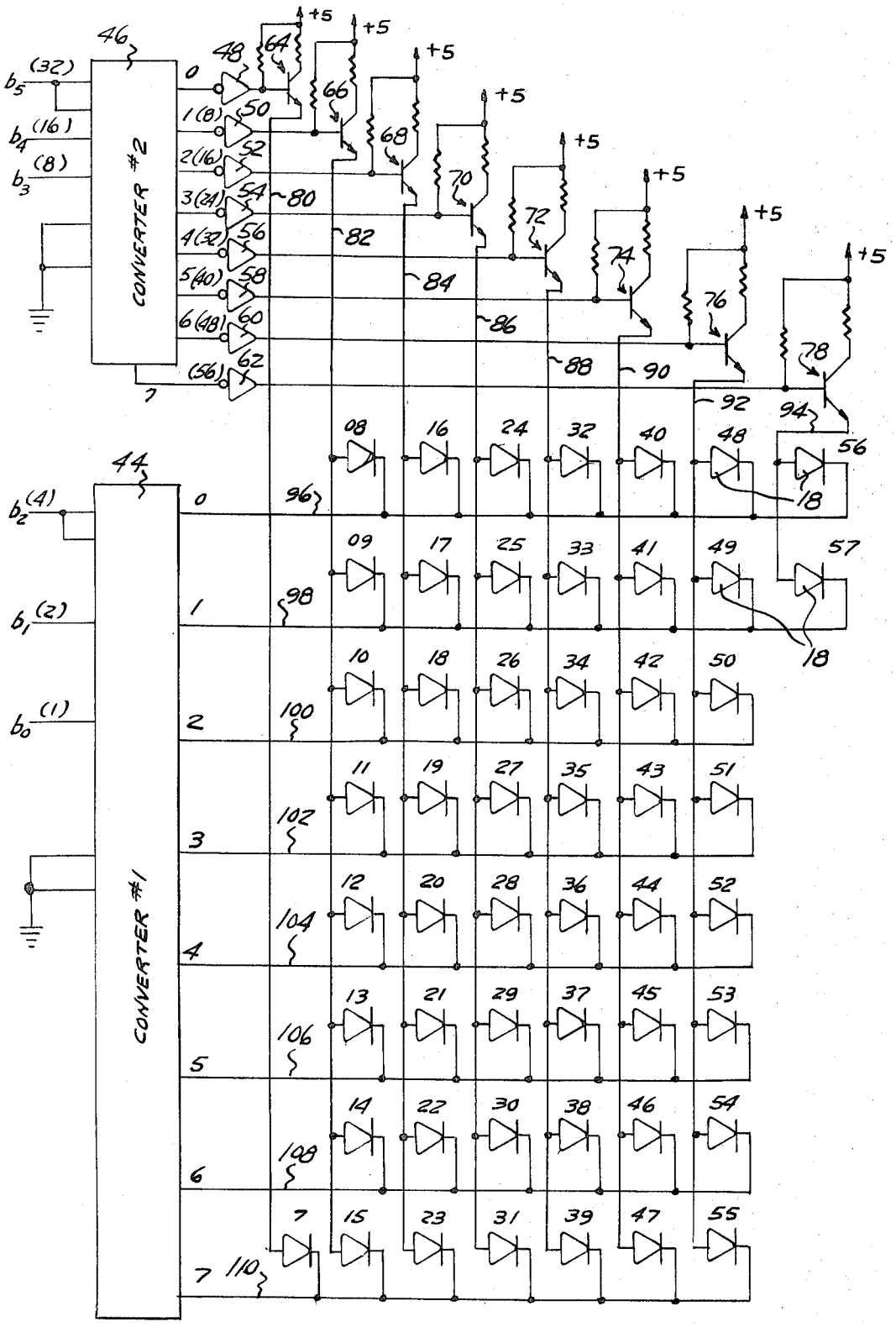


FIG.4

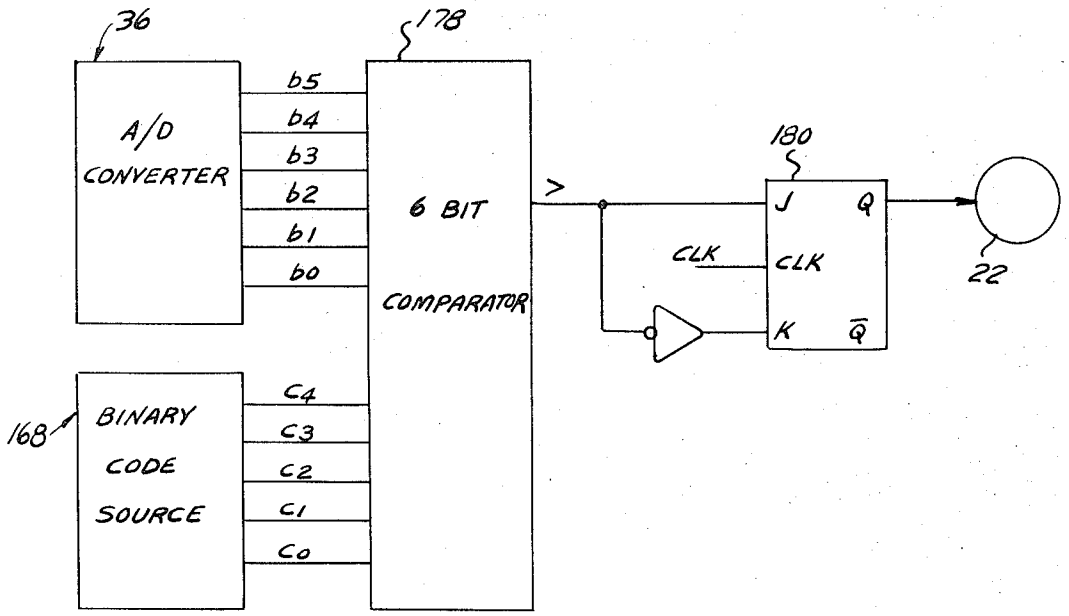

36
178
A/D CONVERTER
b5
b4
b3
b2
b1
b0
6 BIT COMPARATOR
>
180
J
Q
CLK
CLK
K
Q
22
168
BINARY CODE SOURCE
C4
C3
C2
C1
C0

FIG. 7

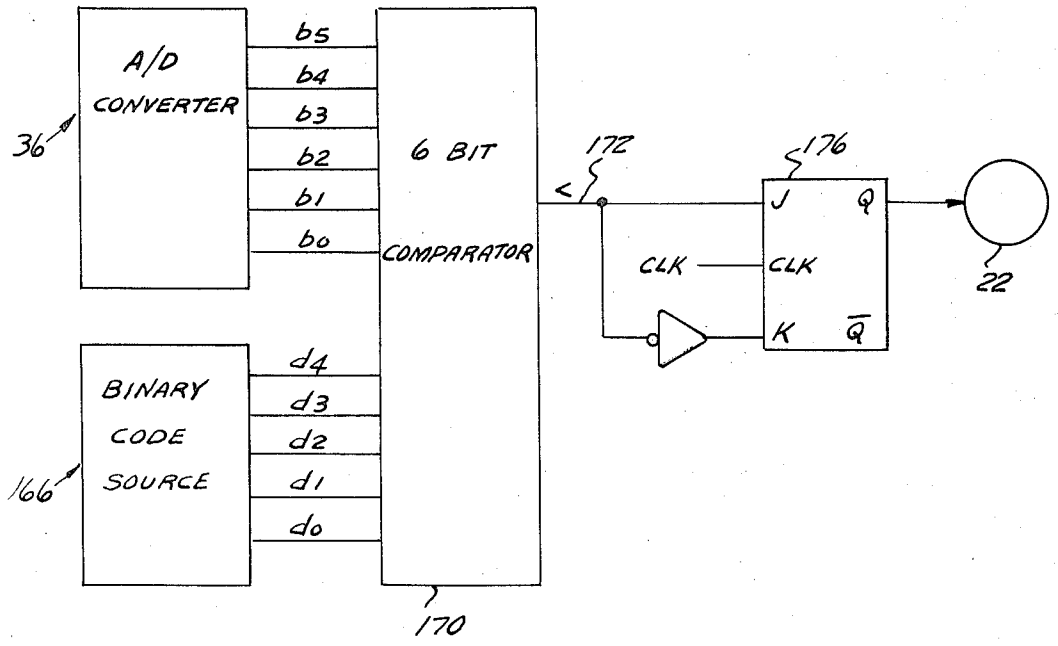

A/D CONVERTER
36
b5
b4
b3
b2
b1
b0
6 BIT COMPARATOR
172
<
176
J
Q
CLK
CLK
K
Q
22
BINARY CODE SOURCE
166
d4
d3
d2
d1
d0
170

FIG. 6

COLUMNAR DISPLAY FOR ELECTRICAL SIGNALS WITH DIGITAL SIGNAL LIMIT SET

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention covers signal readout devices and more particularly concerns devices for displaying the level of variable electrical signals in a columnar form.

2. Description of the Prior Art

In arrangements for inspecting workpieces on a production basis in which various parameters such as dimensional values are to be compared with upper and lower limits, it has been found to be advantageous to display the signals generated by the measuring transducer in columnar form; i.e., as the signal value increases and decreases, a corresponding indicator rises and falls relative to a vertical scale. This is because of the relative ease and accuracy of reading such displays as compared with ordinary meter type instruments. Furthermore, often there are a number of parameters measured simultaneously and such column type instruments are then ganged with each instrument measuring a separate parameter, and in this situation, the columnar display allows rapid scanning of the value of each of these parameter values to determine which of these if any are outside the preset value limit.

Heretofore, this type of signal display has been limited to air gauge type instrumentation, since only in air-flow type gauges in which a float element rises and falls in a vertical transparent tube has such a display been attainable at reasonable cost. Various attempts at such a display for electrical signals have involved relatively bulky, complex, and unreliable apparatus which has also been excessively costly, so that wide commercial acceptance thereof has not occurred.

In addition, the widespread use of such air-flow gages has led to a preference among users for the "float" type indication, and heretofore such electrical apparatus have not produced a read-out which is similar in appearance to an air-flow gage float.

Since in many situations electrical sensing of these parameters is preferable to air gauging it would be advantageous if such a display could be provided at a reasonable cost if it was not unduly cumbersome and/or unreliable, and it would be preferable if the indication produced the same visual effect as an air gage float.

In most such sensing arrangements, the variable electrical signals are produced in analog form; i.e., the magnitude and/or phase of the voltage or current produced by the transducer corresponds to the parameter value. In a visual display system such as that according to the present invention, these signals are converted to digital form for further processing.

If a limit system is utilized, that is, an indication is provided whenever the parameter value reaches a preset value, and if the analog signal is compared to a preset analog value, "drift" or shifts in the correspondence between the digital signals and the analog signals sometimes occurs, leading to change in the digital value triggering the indicator. This may lead the operator to believe there is a malfunction in the limit set circuit, even though the drift is within the operating tolerance of the instrument.

Therefore, it is an object of the present invention to provide a column display of the level of variable electrical signals without the use of complex, unreliable or excessively costly apparatus, and which produces a visual effect similar to an air gage float.

It is another object of the present invention to provide a limit set circuit which avoids the effects of drift in the analog-digital converter on the digital value corresponding to the limit set.

SUMMARY OF THE INVENTION

These and other objects which will become apparent upon a reading of the following specification and claims is accomplished by means for converting the variable level electrical signals into digital form, which digital signals in turn are decoded and arranged to consecutively activate a vertical series of indicator elements up and down the series in response to increases and decreases in the digital signal respectively and to deactivate the preceding activated indicator element so that a single individual indicator element is activated, corresponding to each digital signal, the relative position of this single indicator element thus indicating the level of the variable electrical signal. An arrangement is also disclosed for providing signal limit indication comprising means for comparing the digital signal generated by the A/D converter with a preset digital limit signal which means drives a limit indicator element whenever the generated digital signal is outside the preset value.

DESCRIPTION OF THE DRAWINGS

FIG. **1** is a perspective view of an instrument utilizing the columnar display according to the present invention.

FIG. **2** is a perspective view of a group of instruments of the type shown in FIG. **1** as ganged together.

FIG. **3** is a block diagram of the signal processing system according to the present invention.

FIG. **4** is a schematic diagram of the decoding and driving circuit together with the light emitting diodes shown in block form in FIG. **3.**

FIG. **5** is a schematic diagram of a first embodiment of a limit circuit shown in block form in FIG. **3.**

FIG. **6** is a schematic diagram of a portion of a second embodiment of the limit circuit shown in block form in FIG. **3.**

FIg. **7** is a schematic diagram of a portion of a second embodiment of the limit circuit shown in block form in FIG. **3.**

FIG. **8** is a schematic diagram of the over-range logic circuit.

DETAILED DESCRIPTION

In the following detailed description certain specific terminology will be utilized for the sake of clarity and a specific embodiment will be described in order to provide a complete understanding of the invention, but it is to be understood that the invention is not so limited and may be practiced in a variety of forms and embodiments.

Referring to the drawings, and particularly FIGS. **1** and **2,** a column type display unit **10** is depicted. This unit includes an instrument housing unit **12** containing the instrument electronics, with the housing unit **12** being supported vertically by a pair of support blocks **14** and **16.**

The visual display is comprised of a vertical series of indicator elements comprising light emitting diodes

(LED's) **18** arranged adjacent a vertical scale **20,** with increments thereof opposite respective LED's **18.** The LED's are driven to emit for respective digital values corresponding to an incremental value of an input variable level electrical signal by means of circuitry to be herein described so that as the level of the signal increases and decreases the LED's experience changes of state such that they are activated consecutively up and down the column and the preceding activated LED **18** is deactivated so that a single individual LED is activated for each incremental value of the analog signal thus, the position of the activated LED provides an indication of the level of the electrical signal and gives the same general appearance as the float element used in conventional air-flow gauging.

In order to provide an indication of the occurrence of signals either above or below the preselected values, limit circuitry to be herein described is utilized to drive a reject indicator light **22.** In addition adjustable mechanical indicators **24** and **26** are provided to set the preselected limit values and to provide an indication directly at the scale **20** of the preselected limit values.

Whenever the signal value goes beyond the range of the instrument regardless of the limit values, an over-range LED **28** is provided driven by a logic circuit to be described infra to indicate such a reading.

Also included is a centering control including control knob **30** used to apply a bias signal to shift the correspondence between a given analog signal with a given LED for purposes well-known in the art.

As mentioned above, provision is made for ganging several instruments as shown in FIG. **2,** in which several instrument housing units **12** are joined together between common support blocks **14** and **16** for simultaneous reading of several parameters. In this arrangement a common reject indicator light **22** which is lit if any of the parameter values go beyond the preset limits. In this event the operator can conveniently scan each of the housing units **12** to determine the out-of-tolerance parameter or parameters.

Thus the advantages of the conventional air-flow column instruments is obtained with the use of electronics. Additionally, the essentially incremental or digital display eliminates any mistakes arising from the necessity for interpolation present in conventional air-flow column instruments.

Referring to FIG. **3,** a block diagram of the system electronics accomplishing the above function is shown.

A source of an analog of a variable level electrical signal is shown as a displacement transducer **32.** This displacement transducer **32** could for many purposes suited to the present invention be of the differential transformer type, which as is well-known in the art has very linear characteristics and other useful attributes in this context.

In this case, the signal generated is in AC form with the variations in amplitude and phase thereof providing the displacement indication, which necessitates the inclusion of an oscillator and demodulator circuit together with the usual amplifier in the signal processing stage **34.** The nature of this circuitry and the design requirements thereof are very well-known in the art and hence a detailed description of a representative circuit is not here included.

This signal processing circuitry **34** provides a DC output voltage which is an analog of the displacement sensed by the displacement transducer **32.**

According to the present invention, this analog signal is then converted into digital form by converter means including analog-to-digital converter **36,** such devices also being well-known in the art and which function to generate corresponding digital signals from the analog signal generated by the transducer **32.** For the specific logic and decoding circuits herein described this output comprises a six-bit binary word. One common and suitable approach to the analog digital conversion is to provide means for controlling the counting of clock pulses into a binary register by a comparator circuit which matches the analog signal value against a control signal value which increases incrementally with the counting of each pulse to an extent depending on the amplification built into the converter **36.** When these match, pulse counting into the register stops and the count is read into a storage register for use in the decoding and limit logic circuitry described herein.

The decoding and driver circuit **38** reads and deocdes the binary number corresponding to a given analog signal and causes a single respective LED **18** to emit, with increasing and decreasing binary values causing higher and lower LED's **18** in the column to be activated to produce the effect described above in which the relative position of the single activated LED provides an indication of the level of the variable electrical signal.

The system is provided with limit indicator means including the limit circuit **40** which compares the binary number with preset digital values for upper and lower limits and triggers the reject indicator **22** in response to generation of digital signal values above or below respectively these preset digital values. It can be seen that since the signal value compared with the limit values is in digital (binary) form, drift occurring in the A/D converter cannot cause a variation in the particular binary number triggering the rejection indicator **22.**

The over-range logic **42** also reads the binary number, and provides emitting by the over-range LED **28** whenever it exceeds the binary number corresponding to the maximum range of the instrument.

FIG. **4** depicts the decoder and driver circuit **38** in schematic form which is arranged to read and decode the six-bit binary word contained in the storage register of the A/D converter and drive a respective LED **18.**

At the outset, it is noted that a six-bit binard word is capable of representing 0–63 increments corresponding to values of the analog signal. However, for most purposes, a scale comprised of 51 increments is adequate, allowing for a −25 to +25 increment range. Thus, the decoding and driver circuit **38** is arranged to drive a respective LED **18** for binary numbers 07 through 57. This is accomplished by setting the amplification in the A/D converter **36** such that the analog signal corresponding to −25 units produces a binary signal from the converter equal to 07.

The decoder and driver circuit **38** includes octal coverters **44** and **46** which have inputs connected to the output of the A/D converter such that the lowest three digits of the binary number b_0, b_1, and b_2 are connected to octal converter **44** and the highest three digits b_3, b_4, and b_5 are connected to octal converter **46.** Octal converter **46** is conventional in the sense that for various

binary number 0–7 represented at the inputs, a respective output 0–7 goes to the low state. Octal converter **44** on the other hand is internally connected so that for each binary number 0–7 represented at the input terminals a respective output 0–7 is connected to ground.

Each of the outputs 0–7 of octal converter **46** is connected to inverters **48–62** and junction transistors **64–78** so that if a respective output 0–7 is "low" the corresponding junction transistor **64–78** is turned on to apply a potential to the respective emitter line **80–94.**

The emitter lines **80–94** are connected to the anodes of groupings of the LED's **18** as shown, the emitter line **80** corresponding to the 0 output connected to the 07 LED (corresponding to −25 on the scale), the emitter line **82** connected to LED's **08–15,** (corresponding to −24 to −17 on the scale) emitter line **84** connected to LED **16–23** (corresponding to −16 to −9 on the scale) and so on as shown.

Each of the outputs **0–7** of octal converter **44** on the other hand is connected to lines **96–110** respectively which connect the cathodes of LED's **18** in the different grouping shown in FIG. **4.**

These connections cause a respective LED **18** designated by decimal 07–57 to emit when the equivalent binary number $b_0 - b_5$ is read at the octal converter **44** and **46** inputs. For example, if binary 000111 equal to decimal 7 is read out of the A/D converter b_3, b_4, and b_5 are at zero, while b_0, b_1, and b_2 are at 1. Thus all of the outputs of the octal converter **46** are "high" or at a logic one except the zero output which causes a potential to be applied to emitter line **80** which is connected to the 07 LED.

Since b_0, b_1, and b_2 are all high for binary 000111, line **110** only is connected to ground, to thus cause the 07 LED to emit since this completes the circuit thereto. While line **110** also connects the 15, 23, 31, 39, 47, and 55 LED's to ground, these do not have a potential applied to the anode, hence none of these emit, so that for binary 000111 only the 07 LED emits. Taking a second example, binary 00100 equal to decimal 8, since b_3 is equal to 1 and b_4 and b_5 are equal to zero, only the 1 output is low, causing the line **82** alone to be energized, applying a potential to 08–15 LED's. However, for binary number 001000, b_0, b_1, and b_2 are all zero so that only line **96** is connected to ground. Thus, only the 08 LED is activated because the circuit is complete only for this LED.

The net result is that for each binary number 07–57 read at the inputs of octal converters **44–46,** a single respective LED **07–57** as indicated has potential applied to its anode and its cathode to ground to cause it to emit.

As noted, these LED's are arranged physically on the instrument in vertical sequence with the 07 LED being lowest and the 57 LED being highest.

It can be appreciated that this matrix of connections with the two octal converters (**44** and **46**) in effect provide a conversion means for converting a six-bit binary number into an output pattern of "states" at points in the matrix unique to each binary number, these "states" comprising completed circuits at each point to thus provide a decoding of the binary number and driving of each corresponding LED **18.**

Thus, as the level of the variable electrical signal increases the LED's **18** are consecutively activated upwardly at incremental values thereof, and similarly as the signal level decreases the LED's **18** are consecutively activated downwardly. It will of course be understood that if the signal level varies rapidly by several increments a subsequent LED **18** in one direction or the other (i.e., upwardly or downwardly) will be activated rather than a strictly consecutive activation. Since the decoder and driver circuit **38,** provides for only a single activated LED **18,** any preceding activated LED is deactivated as the individual LED **18** corresponding to the analog signal level is activated, so that only a single LED **18** is activated for a given level of the analog signal.

Referring to FIG. **5,** a first embodiment of a limit circuitry **40** is depicted in schematic form. This circuit includes a series of converters **112, 114, 116,** and **118** which combined with a series of AND gates **120, 122, 124,** and **126** serve to decode the six-bit binary word $b_0 - b_5$ read out of the A/D converter **36.** The most significant bits b_4 and b_5 are read by the AND gates **120, 122 124,** and **126,** while th least significant bits b_0, b_1, b_2, and b_3 are read by the converters **112, 114, 116,** and **118.** Each of the converters **112, 114, 116,** and **118** is of the type which function to convert a four-bit binary word to low outputs at one of 16 outputs, each corresponding to a binary number in the series capable of being represented by a four-bit word. In the present embodiment, however, the lower seven outputs of converter **112** and the upper six outputs of converter **118** are not utilized since only 51 increments, are used in the column.

The output of the AND gates **120, 122, 124,** and **126** serves to inhibit any output from each of the converters **112–118** which associated therewith if the output is "high" and will enable converters **112–118** if the output is low. The b_4 and b_5 inputs are read in combinations inverted and not inverted such that if b_4 and b_5 are zero, converter **112** is allowed to produce outputs **07–15,** if b_4 is "one" and b_5 is zero, converter **114** is allowed to produce outputs **16–31,** if b_4 is "one " and b_5 is "one", converter **116** is allowed to produce outputs **32–47,** and if both b_4 and b_5 are "one" converter **118** is allowed to produce its outputs **48–57.** This it can be seen that this arrangement in effect produces a six-bit conversion of the binary number into 51 respective low states at the outputs of the converters **112–118.** These outputs are used to set the upper and lower limits by means of a slide wire system **128** which functions to allow selective connection of the converter **112–118** outputs which are connected to series of slide wire contacts **130** via line **132** to a pair of flip-flops **134** and **136.**

Flip-flop **134** functions to trigger the reject indicator **22** whenever the binary signal increases to the value corresponding to that of the high value of these two contacts **132** engaged by a slidable contact **138.** The slidable contact **138** includes a pair of contact elements **140** and **142** structurally joined to move together but electrically insulated and which serve to connect a respective contact **132** to conductive strips **144** and **146** respectively in turn respectively connected to the J and K inputs of the flip-flop **134** via inverters **148** and **150.** When the binary signal reaches the value corresponding to that connected to contact **144,** flip-flop **134** is to trigger the reject indicator **22.** When the signal declines to the level corresponding to that connected by contact **142,** the flip-flop **134** is reset to discontinue the reject indication.

Similary, flip-flop **136** functions to trigger the reject indicator **22** whenever the binary signal declines to the value corresponding to that of the lower value of these two contacts **132** engaged by a slidable contact **152.** Slidable contact **152** includes a pair of contact elements **154** and **156** structurally joined to move together but electrically insulated from each other and which serve to connect a respective contact **132** to conductive strips **160** and **158** respectively in turn respectively connected to the J and K inputs of the flip-flop **136** via inverters **162** and **164.** When the binary signal declines to the value corresponding to that connected by contact **154** flip-flop **136** is set to trigger the reject indicator **22.** When the signal increases to the value corresponding to that connected by contact **156** the flip-flop **136** is reset to discontinue the reject indication.

In order to insure proper start-up operation with a zero signal level, a reset logic signal LR is applied upon turning on the power so that the upper limit flip-flop **134** is reset and the lower limit flip-flop **136** is set as indicated.

Referring to FIGS. **6** and **7,** an alternate arrangement for providing the digital limit circuitry is shown, which involves simpler electronics than the version shown in FIG. **5.**

This system depends on the operational restriction that the upper limits must always be set above scale 0 (the binary signal corresponding to decimal number 32) and the lower limits below scale 0, the disadvantage of which limitation is offset to a great extent by the center adjust capability of the instrument. Since this restriction applies, five-bit binary code sources **166** and **168** (FIGS. **6** and **7**) for the lower and upper limit respectively can be utilized for comparison purposes, since for all binary signals above decimal 32 (scale 0), the sixth bit b_5 will be one, for all binary signals below decimal 32, this bit will be zero. This one fewer bit allows for one fewer connecting conductor from the binary code sources **166** and **168** to the rest of the circuitry. Thus, for the lower limit, the binary code source **166** is set at a particular desired limit $d_0 - d_4$ and this value is compared in a comparator **170** with the six bits $b_0 - b_5$ of the binary signal read from the A/D converter **36.** The comparator **170** functions such that it will produce an output high state on line **172** whenever the binary signal is less than the value selectively set in the binary code source **166.** This signal is used to set a flip-flop **176** whenever the binary signal is less than that set in the binary code source **166** to trigger the reject indicator **22** under these conditions.

Similarly, as shown in FIG. **7,** a five-bit selectively set binary code $C_0 - C_4$ is compared with the six bits of the binary signal contained in the A/D converter **36** $b_0 - b_5$ in comparator **178** which produces an output whenever the $b_0 - b_5$ signal is greater than the $C_0 - C_4$ value. This output is used to set a flip-flop **180** whenever an output is received from comparator **178** to thus trigger the reject indicator **22** whenever these conditions exist.

The binary code sources **166** and **168** could comprise a slidable bus bar grounding a binary pattern of conductive strips to form a binary code source, or any other such suitable arrangement, as is well-known in the art.

FIG. **8** shows a logic circuit for triggering the over-range LED **28.** This includes a combination of the b_1, b_3, b_4, and b_5 bits in AND gate **184,** and the inverted b_1 and b_2 bits in AND gate **186,** the outputs of which are connected to the reset and set inputs of a flip-flop **188** as shown having its Q output inverted and connected to LED **28** so that whenever the flip-flop **188** is set the over-range LED **28** is caused to emit. The flip-flop **188** is set when the bits b_1, b_3, b_4, and b_5 go to one (indicating a binary signal 111010 corresponding to decimal 58) or greater and reset as soon as the bits b_1 and b_2 return to zero (indicating binary signal 111001, equivalent to decimal 57) or less.

From the above description, it can be appreciated that a column display of the level of variable electrical signals has been provided which does not involve complex moving parts, or unduly complex electronic circuitry, and which is of a nature lending itself to low-cost volume manufacturing techniques. Also, the appearance of the relative change in position of the single individual indicator element also resembles closely the appearance of a float in a column type air gage to minimize transitions of user reading facility.

Furthermore, the digital form of the limit comparison described herein eliminates the disadvantage of drifting digital reject triggering values described above.

It should also be appreciated that a great number of variations from these described embodiments are possible within the spirit of the invention, which is to be limited only by the scope of the following claims.

Therefore, what is claimed is:

1. A display arrangement for providing a visual display of the level of variable electrical analog signals comprising:

converter means generating corresponding digital signals from said analog signals;

display means responsive to said digital signals to provide a visual display corresponding to said generated digital signal values;

limit indicator means including an indicator and also including means responsive to the generation of a preset digital signal value to activate said indicator, including a digital signal source and comparator means comparing said digital signals to a preset value of said digital signal source whereby said indicator is activated in response to the generation of the same preset digital signal value notwithstanding drift in said converter means.

2. The display arrangement of claim **1** wherein said limit indicator means includes means for varying the preset digital signal value causing activation of said indicator.

3. The display arrangement of claim **1** wherein said display means includes:

a series of indicator elements;

means for consecutively changing states of individual indicator elements in said series in response to generation of each of said digital signals, whereby a visual display of the digital signal value is provided.

4. The system of claim **3** wherein said means consecutively changing states of individual indicator elements includes means activating individual indicator elements and means deactivating any preceding activated elements so that only a single indicator element in said series is activated for each digital signal whereby the relative position of the single activated individual indicator element in said series provides a visual display of the digital signal.

5. The system of claim **4** wherein said series of indicator elements is arranged vertically and wherein said

means activating said indicator elements activates indicator elements consecutively upward in said vertical series in response to increasing digital signal levels and activates an indicator element consecutively downward in response to decreases in said digital signal levels, whereby the rise and fall of the relative position of said single activated indication element in said vertical series thereof provides a visual display of said digital signal levels.

6. The system of claim **3** wherein said indicator elements comprise light emitting diodes.

7. The system of claim **3** further including displacement transducer means generating said variable electrical analog signal as an indication of a displacement whereby said activated indicator element in said series of indicator elements provides a display of displacements indicated by said variable electrical analog signal.

8. The display arrangement of claim **1** wherein said limit indicator means responsive to the generation of preset digital values above or below preset digital values to define upper and lower limit indications.

9. The display arrangement of claim **3** further including at least one adjustable limit indicator providing an indication along the series of indicator elements of the preselected limit set by said limit indicator means.

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