

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
18 November 2004 (18.11.2004)

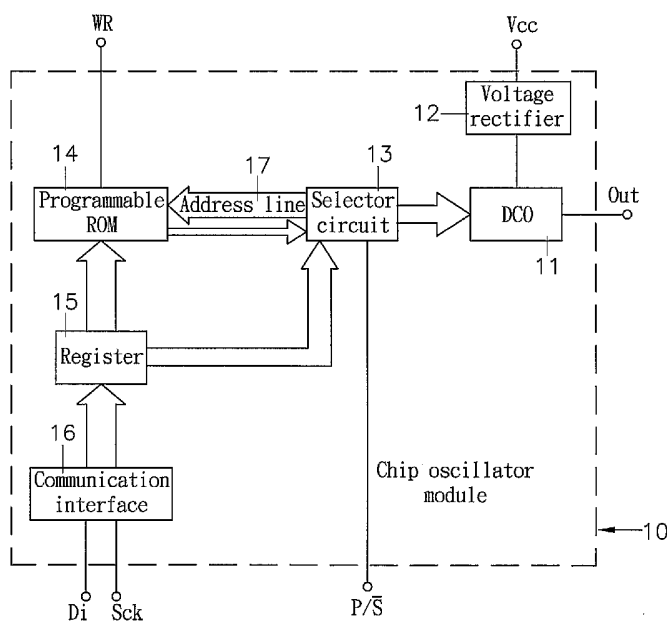
PCT

(10) International Publication Number
WO 2004/100378 A1

- (51) International Patent Classification⁷: H03L 7/06, H03B 5/12
 - (21) International Application Number: PCT/US2003/010758
 - (22) International Filing Date: 10 April 2003 (10.04.2003)
 - (25) Filing Language: English
 - (26) Publication Language: English
 - (71) Applicants (for all designated States except US): ZEROPUS TECHNOLOGY CO., LTD. [—/—]; 5F-9, No. 2, Chien-Pa Road, Chungho City, Taipei Hsien (TW). CHEN, Chung-Chin [US/US]; 4th Floor, 625 Slaters Lanes, Alexandria, VA 22314 (US).
 - (72) Inventors; and
 - (75) Inventors/Applicants (for US only): CHENG, Chiu-Hao [—/—]; No. 44 Chung-Cheng Road, Yuan-Li Town, Miaoli Hsien (TW). CHENG, Ming-Gwo [—/—]; No. 16-3 Hsin-Yi Road, Ta-Chia Town, Taichung Hsien (TW).
 - (74) Agents: FICHTER, Richard, E. et al.; Bacon & Thomas, PLLC, 4th Floor, 625 Slaters Lane, Alexandria, VA 22314 (US).
 - (81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
 - (84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).
- Published:
— with international search report

[Continued on next page]

(54) Title: CHIP OSCILLATOR MODULE AND ITS VERIFICATION METHOD



(57) Abstract: A chip oscillator module (10) and its verification method in which the chip oscillator module is formed of a DCO (digital controlled oscillator) (11), a selector circuit (13), a programmable ROM (read only memory) (14), a register (15), and a communication interface (16); inputted frequency set value is stored in the register through the communication interface for transferring the DCO (11); when output frequency judged to be incorrect, a frequency set value verification procedure is proceeded; when output frequency judged to be correct, the frequency set value is programmed into the programmable ROM, for enabling the frequency set value to be transferred to the DCO.

WO 2004/100378 A1



For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

CHIP OSCILLATOR MODULE AND ITS VERIFICATION

METHOD

BACKGROUND OF THE INVENTION

1. Field of the Invention:

5 The present invention relates to a chip oscillator module and its verification method and, more particularly to such a chip oscillator module, in which inputted frequency set value is stored in a register through a communication interface for transferring to a digital controlled oscillator; when output frequency judged to be
10 incorrect, a frequency set value verification procedure is proceeded; when output frequency judged to be correct, the frequency set value is programmed into a programmable ROM, for enabling the frequency set value to be transferred to the digital controlled oscillator.

15 2. Description of the Related Art:

 Regular oscillators used in electronic circuits include two types, namely, the RC (resistance-capacitance) oscillator and the transistor oscillator. The manufacturing cost of a RC oscillator is much cheaper than a transistor oscillator, however its precision is
20 much lower than a transistor oscillator. Therefore, conventional RC oscillators are commonly used in circuits that are not critical in frequency precision. Transistor oscillators are important base components in 3C (consumer electronics, computer,

communication) industries, and commonly used in motherboards, instrument circuit boards, digital counters, mobile communication devices.

FIG. 1 is a circuit diagram of the variable resistor control logic of a conventional RC oscillator module. The circuit comprises a base resistor **R_b**, a series of resistors **R**, **2R**, **4R**, **8R**, **16R** and **32R**, fuses **F0**, **F1**, **F2**, **F3**, **F4** and **F5** respectively connected in parallel to the resistors **R**, **2R**, **4R**, **8R**, **16R** and **32R**, selector switches **S2**, **S4** and **S6**, and control switches **S1**, **S3**, **S5** and **S7**. Electric current is connected to at least one of the fuses **F0**, **F1**, **F2**, **F3**, **F4** and **F5** to break the assigned fuse(s), so as to regulate the resistance value. As indicated, the resistance value is adjusted by employing an electric current to break at least one of the fuses. However, if one fuse is broken erroneously, the circuit cannot be reset. Any error causes a big loss. The error of a RC oscillator is resulted from the tolerance of the resistors and the capacitors. Because every resistor and every capacitor built in an integrated circuit have a different tolerance, there are differences among RC oscillator modules of same specification after setting (fuse breaking procedure). Minimizing such differences depend on component manufacturers' techniques.

Therefore, it is desirable to provide a chip oscillator module, which eliminates the aforesaid drawbacks.

SUMMARY OF THE INVENTION

The present invention has been accomplished under the circumstances in view. It is therefore the main object of the present invention to provide a chip oscillator module and its verification
5 method, which eliminates the aforesaid drawbacks.

According to one aspect of the present invention, the chip oscillator module is comprised of a DCO (digital controlled oscillator), a selector circuit, a programmable ROM (read only memory), a register, and a communication interface. The inputted
10 frequency set value is stored in the register through the communication interface for transferring to the DCO. When output frequency was judged to be incorrect, a frequency set value verification procedure is preceded. When output frequency was judged to be correct, the frequency set value is programmed into
15 the programmable ROM, for enabling the frequency set value to be transferred to the DCO. According to one embodiment of the present invention, the digital controlled oscillator is comprised of a RC oscillator, a digital rough adjustment variable resistor, and a digital fine adjustment variable resistor. According to another
20 embodiment of the present invention, the digital controlled oscillator is comprised of a voltage controlled oscillator and a digital-analog converter.

According to another aspect of the present invention, an

addition address line is set up when two or more correct frequency set values are stored in the programmable ROM. Through the communication interface, the user can set the address line and select the desired correct frequency set value from the
5 programmable ROM.

According to still another aspect of the present invention, the chip oscillator module verification method includes the steps of (a) enabling the user to set the MSB (most significant bit) of the verification frequency set value to be 1, and the other bits to be 0;
10 (b) inputting the verification frequency set value through the communication interface to the register; (c) enabling the user to connect the source pin of the selector circuit to the ground terminal for letting the verification frequency set value to be transferred from the register to the digital controlled oscillator; (d) measuring
15 the output frequency of the frequency output pin and judging whether it is correct or not, and then proceeding to following step (i) if positive, or to following step (e) if negative; (e) judging the output frequency of the frequency output pin to be greater or smaller than the set frequency value, and then proceeding to
20 following step (f) if greater, or to following step (g) if smaller; (f) setting the bit in the verification frequency set value to be 0 and the next bit to be 1, and then proceeding to following step (h); (g) keeping the bit in the verification frequency set value to be 1 and

then setting the next bit to be 1 too, and then proceeding to following step (h); (h) judging whether verification frequency set value has been verified to LSB (least significant bit) or not, and then proceeding to following step (i) if positive, or returning to
5 step (b) if negative; (i) enabling the user to enable the write/read enable pin of the programmable read only memory, and to record the verification frequency set value from the register into the programmable read only memory; and (j) enabling the user to open
10 the circuit of the source pin of the selector circuit, for letting the correct frequency set value be transferred from the programmable read only memory to the digital controlled oscillator so as to complete the verification flow.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit diagram of the variable resistor
15 controlled logic circuit of a RC oscillator module according to the prior art.

FIG 2 is a circuit block diagram of a chip oscillator module according to the present invention.

FIG. 3 is a chip oscillator module verification flow
20 according to the present invention.

FIG. 4 is a circuit block diagram of a chip oscillator module made subject to a resistance-capacitance oscillator circuit design according to the present invention.

FIG. 5 is a circuit block diagram of a chip oscillator module made subject to a voltage-controlled oscillator circuit design according to the present invention.

FIG. 6A is a first type chips test curve obtained according to the present invention.

FIG. 6B is a second type chips test curve obtained according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to FIG. 2, a chip oscillator module **10** is shown comprising a DCO (digital controlled oscillator) **11**, a selector circuit **13**, a programmable ROM (read only memory) **14**, a register **15**, and a communication interface **16**. The DCO **11** is adapted to produce an oscillation frequency. The selector circuit **13** is controlled by the user to select the source for frequency set value. The programmable ROM **14** is adapted to store the correct frequency set value. The register **15** is adapted to store the verified frequency set value temporarily. The communication interface **16** is adapted to let a frequency set value be passed to the register **15**.

Referring to FIG. 3, the frequency verification method of the present invention is to be used to verify the aforesaid chip oscillator module **10**, comprising the steps as follows:

600 Start;

610 The user sets the MSB (most significant bit) of the

- verification frequency set value to be 1, and the other bits to be 0;
- 620 Transfer the verification frequency set value through the communication interface 16 to the register 15;
- 5 630 The user connects the source pin P/\bar{S} of the selector circuit 13 to the ground terminal for enabling the verification frequency set value to be transferred from the register 15 to the DCO 11;
- 640 Measure the output frequency of the frequency output pin 10 Out and judge whether it is correct or not? And then proceed to step 690 if positive, or to step 650 if negative;
- 650 Judge the output frequency of the frequency output pin to be greater or smaller than the set frequency value? And then proceed to step 660 if greater, or to step 670 if 15 smaller;
- 660 Set the bit in the verification frequency set value to be 0 and the next bit to be 1, and then proceed to step 680;
- 670 Keep the bit in the verification frequency set value to be 1 and then set the next bit to be 1 too, and then proceed to 20 step 680;
- 680 Judge whether verification frequency set value has been verified to LSB (least significant bit) or not? And then proceed to step 690 if positive, or return to step 620 if

negative;

690 The user enables the write/read enable pin **WR** of the programmable ROM **14**, and records the verification frequency set value from the register **15** into the programmable ROM **14**;

700 The user opens the circuit of the source pin P/\bar{S} of the selector circuit **13**, for enabling the correct frequency set value to be transferred from the programmable ROM **14** to the DCO **11**;

10 710 End.

FIG. 4 is a circuit block diagram of the chip oscillator module **10** made subject to a resistance-capacitance oscillator circuit design, and comprised of a DCO (digital controlled oscillator) **11**, a voltage rectifier circuit **12**, a selector circuit **13**, a programmable ROM **14**, a register **15**, and a communication interface **16**. The DCO **11** comprises a RC (resistance-capacitance) oscillator **111**, a digital rough adjustment variable resistor **112**, and a digital fine adjustment variable resistor **113**. The RC oscillator **111** is adapted to generate an oscillation frequency subject to capacitance charging discharging characteristics. The digital rough adjustment variable resistor **112** is adapted to adjust the output frequency of the RC oscillator **111** roughly. The digital fine adjustment variable resistor **113** is adapted to adjust the output

frequency of the RC oscillator **11** on a fine scale. The selector circuit **13** is controlled by the user to select the source for frequency set value. The programmable ROM **14** is adapted to store the correct frequency set value. The register **15** is adapted to store
5 verified frequency set value temporarily. The communication interface **16** is adapted to let frequency set value be passed to the register **15**.

FIG. 5 is a circuit block diagram of the chip oscillator module **10** made subject to a voltage controlled oscillator circuit
10 design, and comprised of a DCO (digital controlled oscillator) **11**, a voltage rectifier circuit **12**, a selector circuit **13**, a programmable ROM **14**, a register **15**, and a communication interface **16**. The DCO **11** comprises a VCO (voltage controlled oscillator) **115**, and a digital-analog converter **116**. The VCO **115** controls the oscillator's
15 output frequency subject to the nature of the variation of a varactor with the intensity of reverse voltage. The selector circuit **13** is controlled by the user to select the source for frequency set value. The programmable ROM **14** is adapted to store the correct frequency set value. The register **15** is adapted to store verified
20 frequency set value temporarily. The communication interface **16** is adapted to let frequency set value be passed to the register **15**.

FIGS. 6A and 6B are first type IC chips test curve and second type IC chips test curve obtained according to the present

invention. The test curve of the first type IC chips was obtained by using same oscillation frequency to measure the variation of resistance value. The test curve of the second type IC chips was obtained by using same resistance value to measure the oscillated
5 frequency variation. As illustrates, the frequency difference between IC chips of the same type is insignificant.

Referring to FIGS. 4 and 6A again, the resistance value of the digital rough adjustment variable resistor **112** and the resistance value and precision of oscillation frequency of the digital fine
10 adjustment variable resistor **113** are explained by means of the example of the first type of IC chips. When the oscillation frequency desired to be 4MHz and the range of oscillation frequency assumed to be 2MHz, the set frequency value will be 4MHz±1MHz, i.e., the maximum value will be 5MHz and the
15 minimum value will be 3MHz. The resistance values required of 5MHz and 3MHz are 15KΩ and 24.25KΩ respectively. 24.25KΩ (the resistance value of 3MHz)-15KΩ(the resistance value of 5MHz)=9.25KΩ, which is the resistance value of the digital rough adjustment variable resistor **112**. 15KΩ(the resistance value of
20 5MHz)-9.25KΩ(the resistance value of the digital rough adjustment variable resistor **112**)=5.75KΩ, which is the resistance value of the digital fine adjustment variable resistor **113**. The precision of oscillated frequency depends upon the number of bits of the digital

fine adjustment variable resistor **113**. For example, if the digital fine adjustment variable resistor **113** is of 10 bits, the precision will be $2000000/2^{10}$ ($\cong 1953.125$); if of 20 bits, the precision will be $2000000/2^{20}$ ($\cong 1.907$). Therefore, the higher the number of bits
5 of the digital fine adjustment variable resistor **113** is, the better the precision of the oscillated frequency will be.

Referring to FIGS. 2, 4 and 5 again, a voltage rectifier circuit **12** and a temperature compensation circuit **114** may be added to the chip oscillator module **10**. The voltage rectifier circuit
10 **12** provides the chip oscillator module **10** with the necessary working voltage. The temperature compensation circuit **114** improves the stability and accuracy of the output of oscillation frequency of the oscillator.

In each of the aforesaid embodiments, the chip oscillator
15 module **10** can be made in the form of an independent electronic component, or built in an integrated circuit.

Referring to FIGS. 4 and 5 again, the programmable ROM
14 can be any of a variety of programmable read only memories that are capable of maintaining memorized value intact upon power
20 failure. The programmable ROM **14** can be used to store one or a number of correct frequency set values. When the programmable ROM **14** used to store a number of correct frequency set values, an additional address line **17** is necessary. Through the communication

interface 16, the user can set the address line 17 and select the desired correct frequency set value from the programmable ROM 14.

A prototype of chip oscillator module and its verification method has been constructed with the features of the annexed drawings of FIGS. 1~6. The chip oscillator module and its verification method functions smoothly to provide all of the features discussed earlier.

Although particular embodiments of the invention have been described in detail for purposes of illustration, various modifications and enhancements may be made without departing from the spirit and scope of the invention. Accordingly, the invention is not to be limited except as by the appended claims.

What the invention claimed is:

1. A chip oscillator module comprised of a digital controlled oscillator, a selector circuit, a programmable read only memory, a register, and a communication interface, wherein:

5 said communication interface is adapted to let the user input a frequency set value into said register;

 said register is adapted to temporarily store the verified frequency set value been transmitted through said communication interface, and to transfer the verified frequency set value to said
10 digital controlled oscillator through said selector circuit or to program the verified frequency set value into said programmable read only memory;

 said programmable read only memory is adapted to store the correct frequency set value, or to transfer the correct frequency set value to said digital controlled oscillator through said selector
15 circuit;

 said selector circuit is controlled by the user to select the source for frequency set value, for enabling the correct frequency set value to be transferred from said programmable read only
20 memory to said digital controlled oscillator or the verified frequency set value to be transferred from said register to said digital controlled oscillator;

 said digital controlled oscillator is adapted to receive the

verified frequency set value from said register or the correct frequency set value from said programmable read only memory, and then to output a correct oscillation frequency.

2. The chip oscillator module as claimed in claim 1,
5 wherein said digital controlled oscillator is comprised of a resistance-capacitance oscillator, a digital rough adjustment variable resistor, and a digital fine adjustment variable resistor, said resistance-capacitance oscillator comprising at least one capacitor and one resistor and adapted to generate an oscillation
10 signal subject to discharging and discharging operation of the at least one capacitor thereof.

3. The chip oscillator module as claimed in claim 1, wherein said digital controlled oscillator is comprised of a voltage controlled oscillator and a digital-analog converter, said digital
15 controlled oscillator controlling an output frequency thereof subject to the nature of the variation of a varactor with the intensity of reverse voltage.

4. The chip oscillator module as claimed in claim 1, further comprising a voltage rectifier adapted to provide said digital
20 controlled oscillator with stabilized power source.

5. The chip oscillator module as claimed in claim 2, wherein said digital controlled oscillator further comprises a temperature compensation circuit adapted to control the

temperature of said digital controlled oscillator within a predetermined range.

6. The chip oscillator module as claimed in claim 3, wherein said digital controlled oscillator further comprises a temperature compensation circuit adapted to control the temperature of said digital controlled oscillator within a predetermined range.

7. The chip oscillator module as claimed in claim 1, which is made in the form of an independent electronic component.

8. The chip oscillator module as claimed in claim 1, which is built in an integrated circuit.

9. The chip oscillator module as claimed in claim 1, wherein said programmable read only memory is capable of maintaining memorized value intact upon power failure.

10. The chip oscillator module as claimed in claim 1, wherein said programmable read only memory is capable of storing at least one correct frequency set value.

11. The chip oscillator module as claimed in claim 1, further comprising an address line set by the user through said communication interface for selecting the desired correct frequency set value from said programmable read only memory.

12. A chip oscillator module verification method used to verify the chip oscillator module as claimed in claim 1, comprising

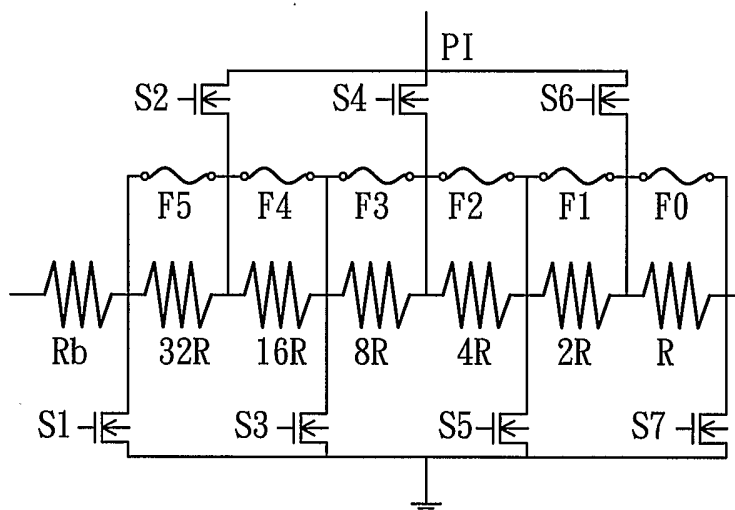
the steps of:

- (a) enabling the user to set the MSB (most significant bit) of the verification frequency set value to be 1, and the other bits to be 0;
- 5 (b) inputting the verification frequency set value through the communication interface to the register;
- (c) enabling the user to connect the source pin of the selector circuit to the ground terminal for letting the verification frequency set value to be transferred from the register to the digital
- 10 controlled oscillator;
- (d) measuring the output frequency of the frequency output pin and judging whether it is correct or not, and then proceeding to following step (i) if positive, or to following step (e) if negative;
- (e) judging the output frequency of the frequency output
- 15 pin to be greater or smaller than the set frequency value, and then proceeding to following step (f) if greater, or to following step (g) if smaller;
- (f) setting the bit in the verification frequency set value to be 0 and the next bit to be 1, and then proceeding to following step
- 20 (h);
- (g) keeping the bit in the verification frequency set value to be 1 and then setting the next bit to be 1 too, and then proceeding to following step (h);

(h) judging whether verification frequency set value has been verified to LSB (least significant bit) or not, and then proceeding to following step (i) if positive, or returning to step (b) if negative;

5 (i) enabling the user to enable the write/read enable pin of the programmable read only memory, and to record the verification frequency set value from the register into the programmable read only memory; and

(j) enabling the user to open the circuit of the source pin of
10 the selector circuit, for letting the correct frequency set value be transferred from the programmable read only memory to the digital controlled oscillator so as to complete the verification flow.



PRIOR ART
FIG. 1

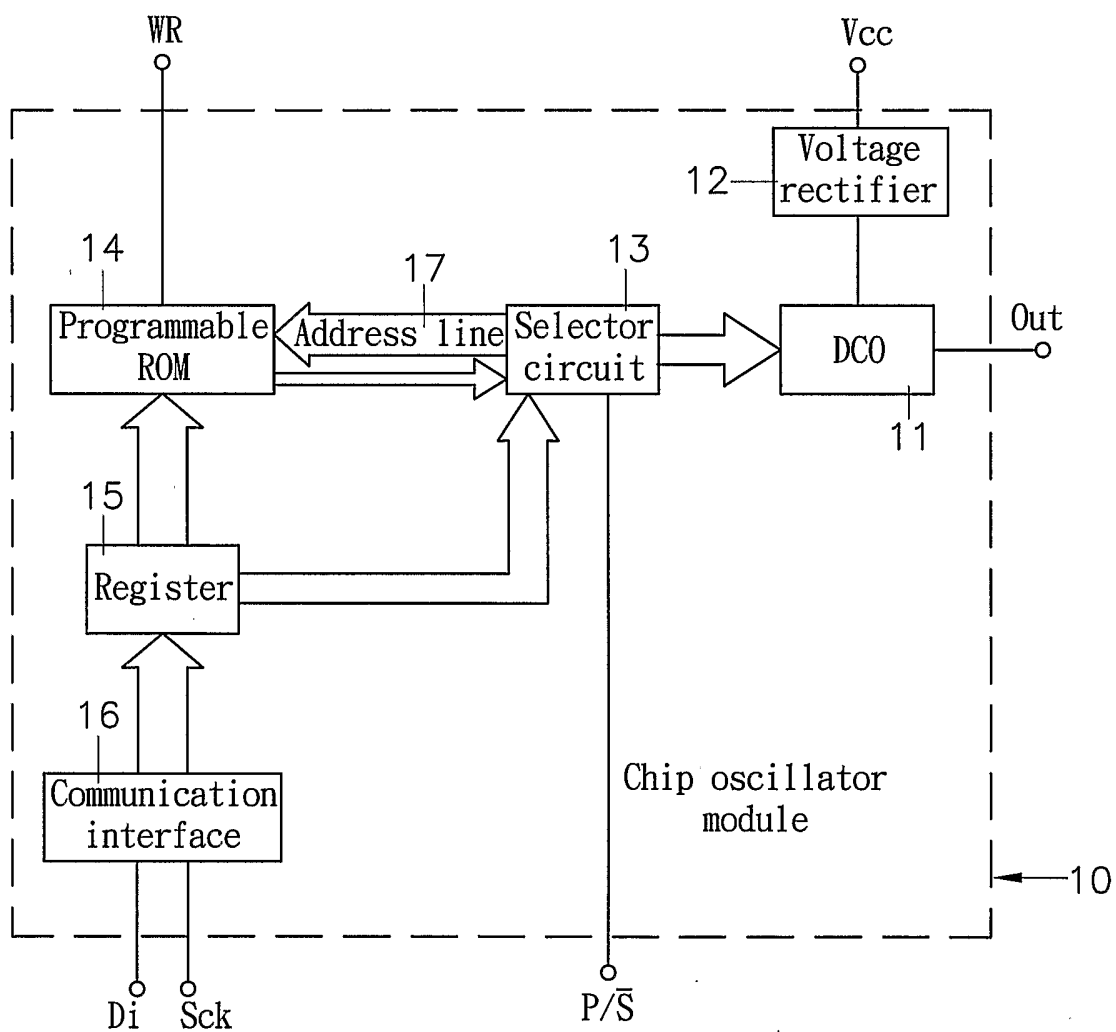


FIG. 2

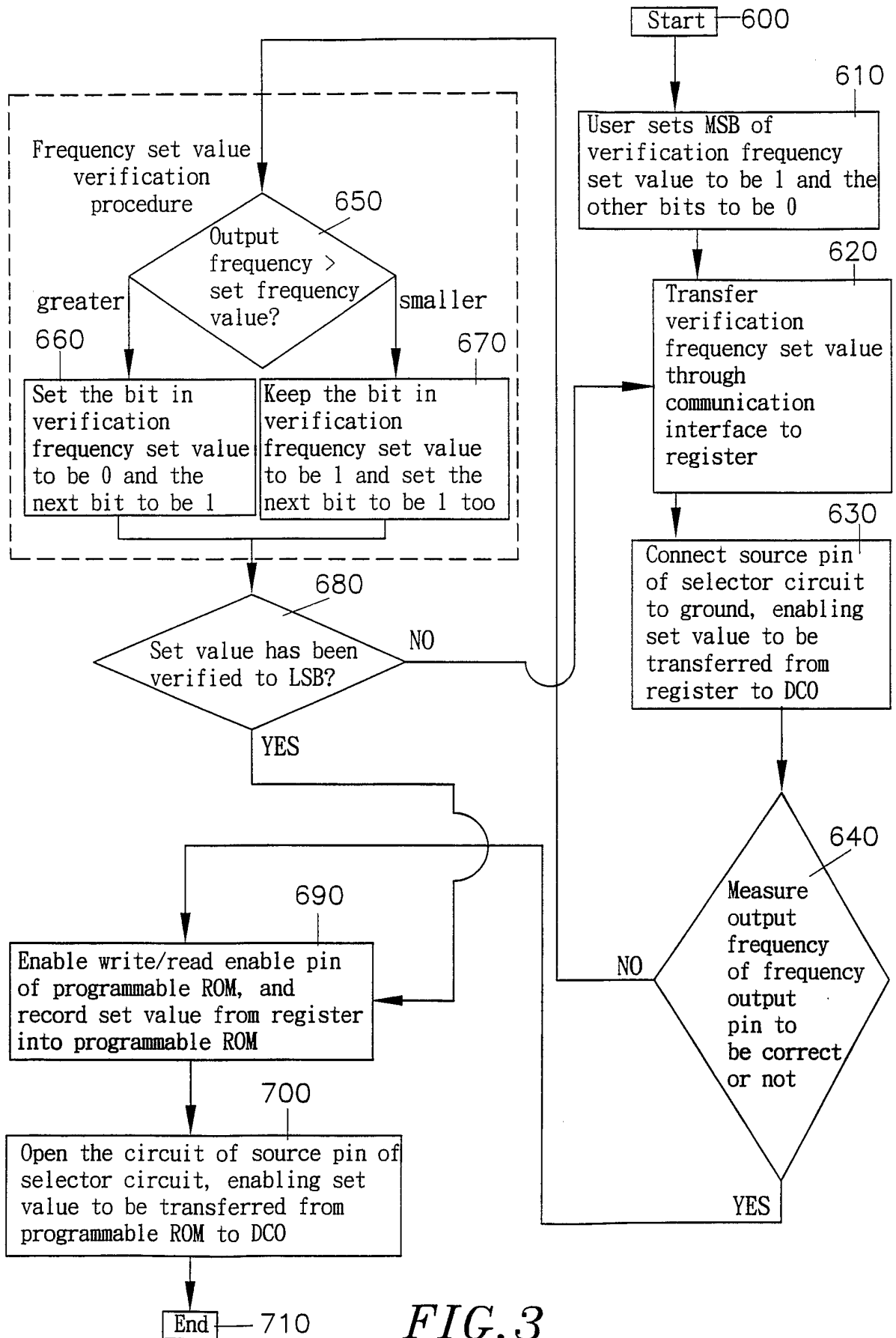


FIG. 3

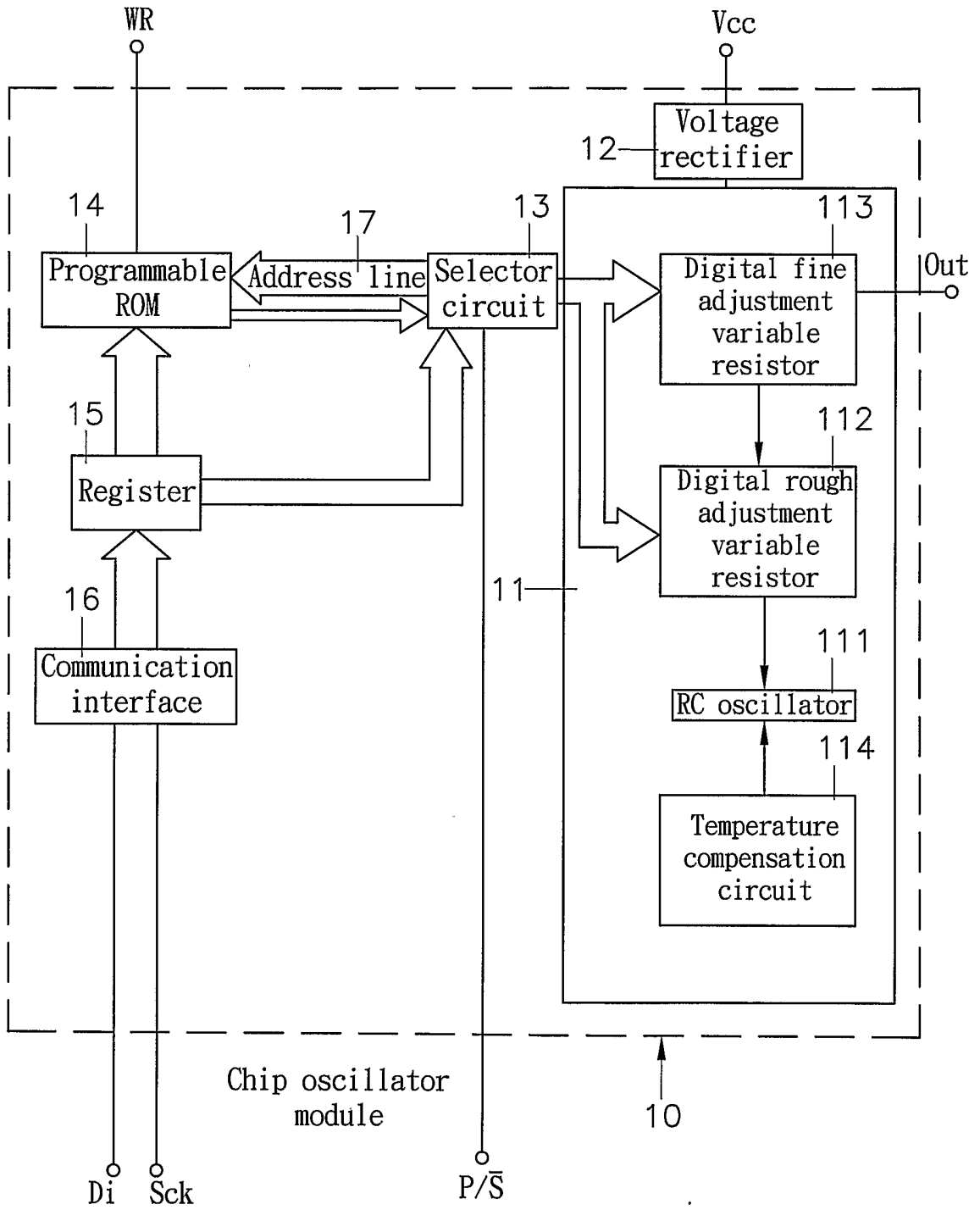


FIG. 4

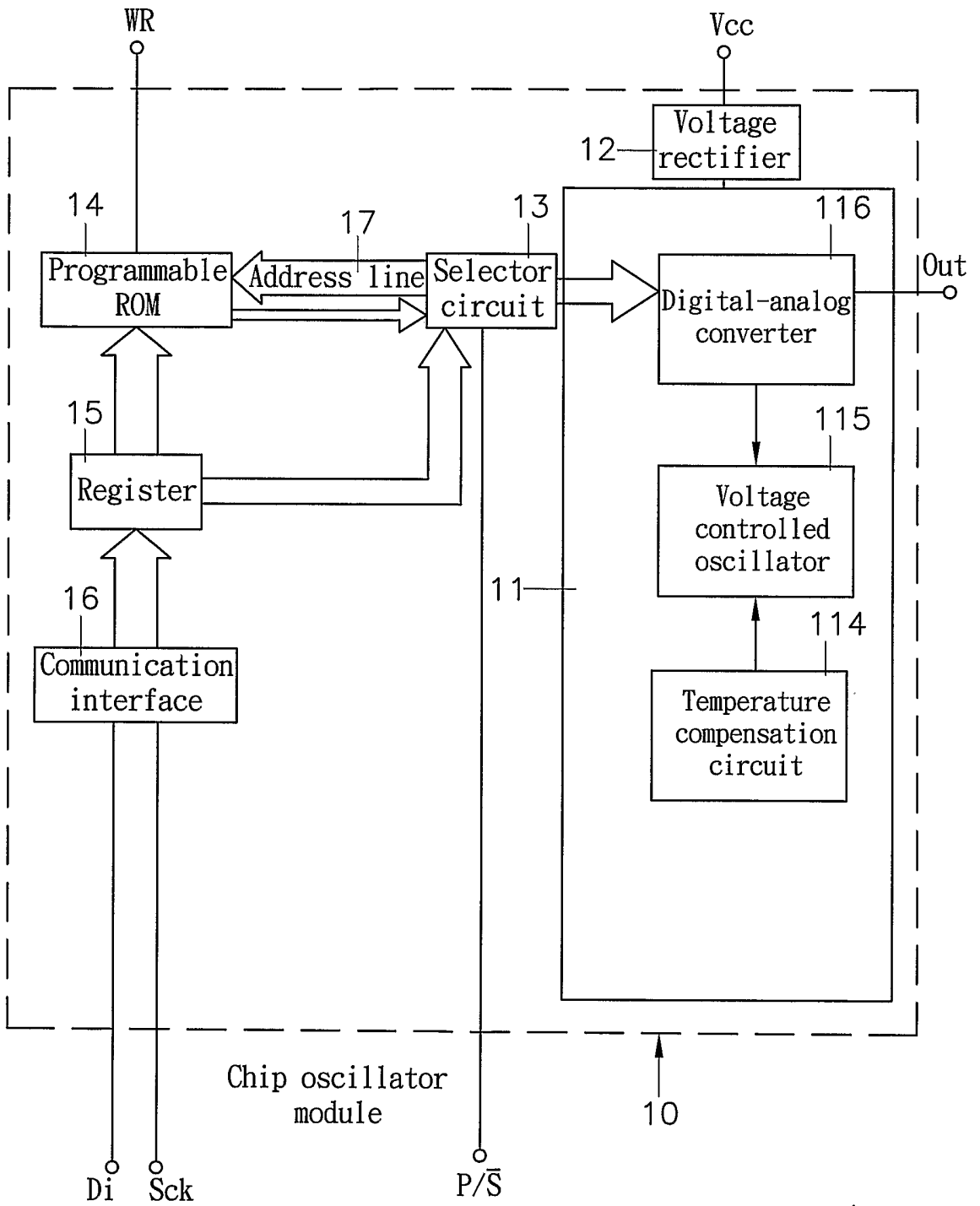


FIG. 5

First IC
Second IC

Frequency (MHz)	1	2	3	4	5	6	7	8	9	10
Resistance value(K Ω)	56.50	31.50	23.50	17.70	15.50	10.80	10.30	9.00	8.00	7.70
Resistance value (K Ω)	58.50	32.50	25.00	20.00	14.50	13.30	9.30	8.50	8.20	8.00
Mean value	57.50	32.00	24.25	18.50	15.00	12.05	9.80	8.75	8.10	7.85

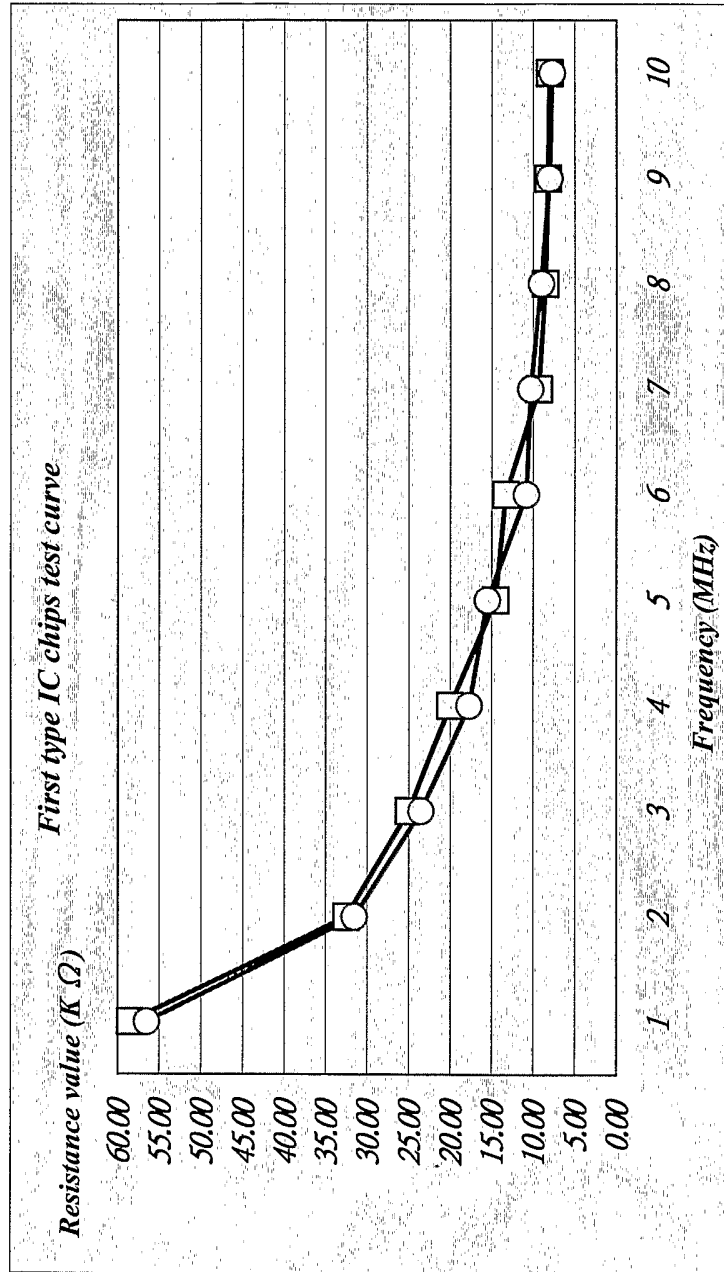


FIG. 6A

● ■

First IC
Second IC

Resistance value (K Ω)	0.68	0.79	1	1.19	1.68	2.17	2.97	4	6.85	13.3
Frequency (MHz)	10.01	9.14	8.26	7.08	5.99	5.04	3.94	3.02	2.02	1.07
Frequency (MHz)	9.83	9.04	8.15	6.97	6.00	4.70	3.91	3.10	2.04	1.08
Mean value	9.92	9.09	8.21	7.03	6.00	4.87	3.93	3.06	2.03	1.08

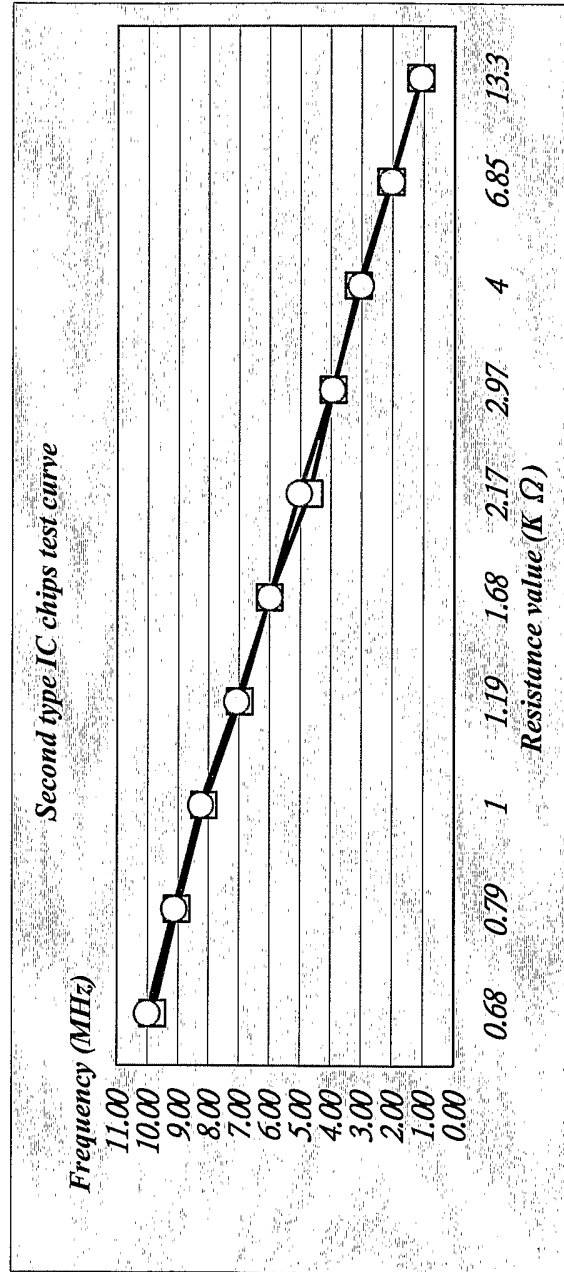


FIG. 6B

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US03/10758

A. CLASSIFICATION OF SUBJECT MATTER		
IPC(7) : H03L 7/06; H03B 5/12		
US CL : 331/158, 176, 177V		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols) U.S. : 331/158, 176, 177V		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) EAST text searches. search terms: dco, digital, oscillator, rom		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6,404,246 B1 (Estakhri et al) 11 June 2002 (11.06.2002), entire document.	1-3, 8, 9-11
A	US 5,418,751 A (Kaiser) 23 May 1995 (23.05.1995), entire document.	1-12
A	US 5,235,293 A (Mendolia) 10 August 1993 (10.08.1993), entire document.	1, 3, 8-11
<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.		
* Special categories of cited documents:		
"A"	document defining the general state of the art which is not considered to be of particular relevance	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"E"	earlier application or patent published on or after the international filing date	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O"	document referring to an oral disclosure, use, exhibition or other means	"&" document member of the same patent family
"P"	document published prior to the international filing date but later than the priority date claimed	
Date of the actual completion of the international search	Date of mailing of the international search report	
22 May 2003 (22.05.2003)	15 SEP 2003	
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (703)305-3230	Authorized officer Joseph Chang <i>Diana Smith</i> Telephone No. (703) 308-0956	