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(54) IMPROVEMENTS IN OR RELATIN G TO FIELD-EFFECTS TRANSISTORS

(71) We, SIEMENS AKTIENGESELLSCHAFT, a German Company of Berlin and Munich, German Federal Republic, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to field-effect transistors having an MIS gate arrangement.

The prior art already includes a large number of publications relating to field-effect transistors having MIS gate arrangements. The source zone and the drain zone of the transistor are spaced from one another in a semiconductor body; the spatial arrangement of these two zones relative to one another may vary, but arrangements in which they are located laterally next to one another on or in a selected surface of a semiconductor body are preferred.

In order to achieve as high a switching rate as possible with field-effect transistors of this type, the channel length between the source and the drain zones, i.e. that region of the semiconductor body in which the actual control effect of the gate arrangement takes place, should be short in the direction of the current path. One way of achieving this is by means of the so-called double diffusion process which is described, for example, in "Solid State Electronics" Pergamon Press 1968, Vol. 11, pp. 411—418. In this process, in a first step, a doping by diffusion is carried out with a dopant which produces a first conductivity type in a semiconductor body. The diffusion is carried out from the exterior through a window in a mask, the dopant also diffusing laterally into the semiconductor body beyond the boundary of the mask window. In a second diffusion step, a dopant which produces the opposite conductivity type is diffused through the same mask window. In this second process step, the final lateral diffusion beyond the edge of the window is less than has already been obtained with the dopant of the first process step. Charge carriers which drift laterally out of the diffusion zone of the opposite type produced by the second process step towards a drain zone, meet with a spatially short channel zone in which the doping is of the one conductivity type produced by the first diffusion step.

Quite separate from the above-described double-diffusion process, so-called buried layers and buffer layers have also already been described. As described, for example, in "Electronics", Vol. 42 (21st July 1969), pp. 74—80, these layers are used in bipolar transistors to electrically screen regions of a semiconductor body close to the surface from underlying regions thereof. In a screened region of this type lying close to the surface, a bipolar semiconductor component, e.g. a bipolar transistor, is produced. The buried layer extends completely across the entire region occupied by the semiconductor component. This buried layer does not have any function which directly interacts with the action of the semiconductor component.

Another type of field-effect transistor which has a short channel length is the so-called VMOS transistor which is described in "Electronic Design", Vol. 23, No. 21, 1975, Circle No. 304.

Another case of a layer which is arranged inside a semiconductor body and which is somewhat comparable with a buried layer is described in our co-pending Application No. 8396/75 (Serial No. 1,507,081). In this, a field-effect transistor arrangement is described in which a p-n junction lying within a semiconductor body produces a space charge zone beneath an overlying field-effect transistor which screens the field-effect transistor from underlying regions both electrically and, in particular, functionally.

It is an object of the present invention to provide an MIS field-effect transistor which has a short channel length and thus has the electrical advantages associated with a short channel length, and in particular a small space requirement, which is of special advantage in the integrated circuit technique.

According to the invention, there is provided a field-effect transistor having a source zone and a drain zone in a semiconductor body and an MIS gate arrangement comprising a gate insulation layer and a gate electrode located on a surface of said body, wherein a further zone of conductivity type opposite to that of said source zone is located in said body below said source zone considered in the direction away from said surface, the conductivity of said further zone being opposite in type to and/or greater than the conductivity of that part of said body surrounding said further zone, wherein said further zone lies at a distance *a* from said gate insulation layer equal to 1 to 5 times the thickness *d* of said gate insulation layer, wherein below said gate arrangement, said further zone has an edge projecting laterally beyond the corresponding edge of said source zone by a distance *b* equal to 1 to 10 times the thickness *d* of said gate insulation layer, wherein the ratio of the distances $b:a$ is in the range of 1:1 to 10:1; and wherein the doping of said further zone is such that when the maximum permissible operating voltage is applied between said gate electrode and said source zone, the majority charge carriers are not discharged from said further zone.

The invention will now be further described with reference to the drawings, in which:—

Figure 1 is a schematic side-sectional view of a first embodiment of the invention; the arrangement illustrated may be either a rotationally-symmetrical arrangement or a strip-shaped arrangement, as will be hereinafter explained;

Figures 2 and 3 are schematic side-sectional views of part of a semiconductor crystal to illustrate two process steps in a process for the production of one form of transistor in accordance with the invention;

Figure 4 is a schematic side-sectional view of part of a semiconductor crystal to illustrate the production of another form of transistor according to the invention;

Figure 5 is a schematic side-sectional view of a further form of transistor in accordance with the invention; and

Figure 6 is a schematic side-sectional view of a modified form of the transistor of Figure 1.

As previously mentioned, the transistor illustrated in Figure 1, may have either a rotationally-symmetrical arrangement, or a parallel-strip arrangement of the appropriate zones, the particular geometric shape which will be preferred in any given situation depending, for example, on the other components with which the field-effect transistor is to be integrated and their geometric shapes.

Referring to Figure 1, a semiconductor body which preferably has a relatively high resistivity and is therefore only weakly doped to be either N- or P-conducting, is preferably made of silicon. In the exemplary embodiment which will be described, it will be assumed that the semiconductor body 1 is N-conductive. A gate insulation layer 2, which can, for example, consist of silicon dioxide or silicon nitride, is arranged on a surface of the body 1. On this insulation layer 2, a gate electrode 3 is arranged, which may, for example, be a vapour-deposited aluminium electrode layer, or an electrode layer made of polysilicon. Regions 4 and 14 having a degenerate N^+-doping are located on the surface of the body 1. In the case where the transistor possesses rotational symmetry, the regions 4 and 14 will, in fact, constitute a single annular zone, whilst in the case of a strip-shaped arrangement they will form two strips which are electrically connected to one another, and will thus effectively form a single zone. The regions 4 and 14 are provided with contact terminals 5 and 15 respectively which are electrically connected to the zones at least basically in a non-blocking manner. For example, for a rotationally-symmetrical arrangement, the contact terminals 5 and 15 can be in the form of a continuous electrode coating. The body 1 is provided at its opposite face to that on which the regions 4 and 14 are formed with an N^+-doped zone 6, serving as the drain zone of the transistor and provided with a metallic contact terminal 7.

The arrangement described above can be used as field-effect transistor, the N^+-regions 4 and 14 being used as the source zone and the N^+-zone 6 being used as the drain zone, in which case, if the semiconductor body 1 is N-conducting, a normally-on field-effect transistor, i.e. a field-effect transistor of the depletion type, is produced for an N-doping above $5 \times 10^{15} cm^{-3}$.

With an MIS gate arrangement comprising the insulation layer 2 and the gate electrode 3, when a voltage is connected between the gate electrode 3 and the contact terminals 5 and 15, to the source zone, it is possible to achieve a voltage-dependent control of the charge carrier current flowing between the source zone 4, 14 and the drain zone 6, as a result of the field-effect of the gate arrangement. A charge carrier current of this type is indicated by the arrows 8 in Figure 1.

For such control of the transistor arrangement schematically shown in Figure 1 to be technically practical, a further feature is required, namely the provision of appropriately doped zones 9 and 19. In the same way as the regions 4 and 14, in the case of a rotationally-symmetrical arrangement, the zones 9 and 19 will constitute a single annular zone, whilst in the case of a strip-shaped

arrangement of the regions 4 and 14, the zones 9 and 19 will correspondingly be strip-shaped. These zones 9 and 19 are doped to have the opposite conductivity type to that of the source formed by the regions 4 and 14. In the embodiment of the invention, where the regions 4 and 14 have the same conductivity type as the body 1 (i.e. a depletion type transistor) the zones 9 and 19 will have a conductivity type which is opposite to that of the semiconductor body 1. Preferably, the zones 9 and 19 are highly doped relative to the degree of doping of the semiconductor body 1. However, the zones 9 and 19 may have to have the same conductivity type as the surrounding semiconductor material of the semiconductor body 1 (i.e. when the regions 4 and 14 are oppositely doped to the body 1), in which case, however, it is necessary for the zones 9 and 19 to have a higher degree of doping than that of the semiconductor body 1. For example, where in a weakly N-conducting semiconductor body 1, the source zone formed by the regions 4 and 14 and the drain zone 6 are P^+-doped, the zones 9 and 19 will be N-doped (preferably N^+-doped). In all the embodiments of the invention, it is essential that the zones 9 and 19 should be of the opposite conductivity type to the source zone 4, 14, so that a p-n junction is always present between the zones 9 and 19 on the one hand, and the source zone 4, 14 on the other hand. In the region of the field-effect exerted by the gate electrode, the zones 9 and 19 always lie at a distance *a* from the surface of the semiconductor body 1. (It should be mentioned that the lines shown in the Figure as delimiting the regions 4 and 14 and the zones 9 and 19 are only approximate boundaries for these zones).

Particularly when the zones 9 and 19 are of the same conductivity type as the semiconductor body 1, it should be noted that the doping of these zones 9 and 19 should be higher than that of the body 1, so that on the occurrence of the potentials and potential differences which arise during operation, in particular that of the gate, the majority charge carriers of the zones 9 and 19 are not discharged, i.e. are not forced out of the zones 9 and 19 as a result of field effects. When the zones 9 and 19 are of the opposite conductivity type to that of the semiconductor body, in order to enable the zones 9 and 19 to be electrically connected, the zones 9 and 19 are led out to the surface of the body in a way which will depend upon the particular circumstances. These zones are then electrically connected to the source zone formed on the regions 4 and 14.

With the zones 9 and 19 which may form one annular zone, it is possible to achieve a constriction of the charge carrier drift path 8 between the source and drain of the transistor. This very decisively improves the sensitivity of the control of the field-effect transistor in accordance with the invention, effected by the gate material. However, certain particular dimensions are also of significance in this respect, as will be explained hereinafter, namely the distances indicated at *a* and *b* in Figure 1.

As in all field-effect transistors, the source zone 4, 14 of the field-effect transistor of the invention extend to beneath the outer edge of the gate electrode 3, so that as regards the charge carrier drift path 8 between the source and the drain, a field influence of the charge carrier current by the gate potential (especially for the "normally-off" enhancement transistor type) can be achieved directly from the edge of the source which injects charge carriers. To ensure that the field-dependent control exerted by the gate potential is particularly efficient, it is provided that the zone or zones 9 and 19 in each case be arranged to project beyond the source zone 4, 14, i.e. into the channel zone, by a distance *b* in Figure 1. Thus, in the embodiment of Figure 1, a constriction *c* of the charge carrier drift path 8 is produced, which constriction is an essential feature of the invention. The distance *a* approximates to the thickness *d* of the insulation layer 2, the value of *a* having a value of from 1 to 5 times that of *d*. Also the value of *b* is 1 to 10 times the value of the thickness d. As a secondary condition, the ratio of $b:a$ is in the range of 1:1 to 10:1.

The following numerical examples give dimensions and doping values for embodiments of the invention.

The semiconductor body 1, which may consist, for example, of silicon, is provided with an N-doping which exceeds the intrinsic value where there is basically no excess doping, by up to $10^{15}cm^{-3}$. The doping of the N-conducting source zone has a degree of doping in the range $10^{18}cm^{-3}$ to $10^{20}cm^{-3}$. Such doping is preferably produced by the implantation of phosphorus atoms, e.g. at a dosage of 1 to $10\times10^{15}cm^{-2}$ with an implantation energy of 50 to 100 keV, when the semiconductor body 1 is made of silicon. The thickness of the regions 4 and 14 forming the source zone is preferably about 0.01 μm, the average distance of these regions from the surface of the semiconductor body thus being 0.005 μm. Boron is particularly suitable for the doping of the zones 9 and 19 which are P-doped (thus having the opposite conductivity type to that of the source zone 4, 14). With a dosage of 3 to $10\times10^{12}cm^{-2}$ and an ion energy of 50 to 200 keV, a doping of 1×10^{16} to $10\times10^{16}cm^{-3}$ is achieved, which latter value should preferably be adhered to as a maximum value. This produces in the semicon-

ductor body 1, zones 9 and 19 which are at an average distance of 0.05 to 0.5 μm from the surface of the semiconductor body 1, and have a thickness of 0.05 to 0.1 μm.

Such dopings can be effected by ion implantation using suitable masks to achieve the required area 1 and spatial delimination of the implantation zones produced; preferably, a mask is used which is in the form of a layer applied to the surface of the semiconductor body 1 and which screens the semiconductor body from the implantation ions. This covering layer is provided with the necessary implantation windows. With the embodiment illustrated in Figure 1, the gate insulation layer 2 which may consist, for example, of silicon dioxide and has a thickness of 0.02 to 0.1 μm can, for example, be used as a mask, in which case the left-hand and right-hand edges of the layer 2 act as lateral implantation boundaries for the regions 4 and 14 and the zones 9 and 19 respectively. Because of the greater implantation depth of the zones 9 and 19, owing to the lateral expansion of the implantation zone (this lateral expansion of the implantation zone is described, for example, in "Jap. Journ. Appl. Phys.", Vol. 11, p. 134 (1972)) the edges of the zones 9 and 19, which in accordance with the invention, project beyond the lateral edges of the regions 4 and 14 by a distance b, can be produced in a simple manner using the same implantation mask. When the above-described measures are carried out, a suitable value for the distance b of 0.05 to 0.5 μm can be obtained. The value of the thickness of the zones 9 and 19 is in the range of 0.05 to 0.1 μm.

Values of 1 to 5 μm are most advantageous for the dimension c.

The doping of the zones 9 and 19 relative to that of the semiconductor body 1 given above, is sufficiently high to ensure that when voltages in the range of 20—60 V are applied between the gate electrode and the zones 9 and 19 and the regions 4 and 14, no discharge of the majority carriers occurs from the zones 9 and 19, in particular in that part of the edge zones which projects by a distance b beyond the regions 4 and 14. This means that, even at the maximum voltage given above, these edge zones possess an electrical conductivity which is still considerably higher than their surroundings and that the p-n junctions with the source zones 4 and 14 are maintained.

The distance b of the projecting edge is arranged to be such that, at the maximum gate voltage (i.e. between the gate electrode 3 and the source zone 4, 14) an effective constriction of the charge carrier drift path 8, i.e. of the actual channel of the field-effect transistor, is achieved.

A field-effect transistor in accordance with the invention as illustrated in Figure 1 and produced having parameters in accordance with the values given above, may be operated with a source-drain voltage of up to 100 Volts and a gate-source voltage of up to 10 Volts.

Referring now to Figure 2, a preferred process for the production of a field-effect transistor in accordance with the invention as illustrated, for example, in Figure 1, will be described. A weakly N-conductive silicon layer 1 is applied (preferably epitaxially) to a semiconductor substrate body consisting e.g. of N^+-silicon, which latter then forms the drain zone 6 of the transistor. Over a given limited area of the surface of the layer 1, a gate insulation layer 2 is then produced by vapour deposition or by thermal oxidation of the silicon surface. An aluminium layer 3 is then applied to the layer 2. On the layer 3, pyrolitically deposited silicon dioxide is then applied, and then by means of a photolithographic process using a photo-lacquer layer 21, this silicon dioxide is chemically etched using a liquid etchant to form a structure 22 as shown in Figure 2, having lateral boundaries to serve as a mask for subsequent ion implantation. The pyrolitic silicon dioxide layer 22 has a thickness of about 0.5 μm. The aluminium layer 3 has a thickness of about 0.1 μm, and the gate insulation layer 2 has a thickness of 0.06 μm. Using the photo-lacquer layer 21 and the structure 22 as a mask, the aluminium layer 3 is removed by ion beam etching except for that part required to serve as the gate electrode, thus producing the arrangement shown in Figure 2. The photo-lacquer layer 21 is then removed.

Figure 3 illustrates the steps of carrying out ion implantation with phosphorus and boron, in which the aluminium layer 3 and the pyrolitically produced silicon dioxide layer 22 exert a masking effect. The shading from right to left indicates the implantation zones including the regions 4 and 14, produced by the implantation of phosphorus P, whilst the zones shaded from left to right including the zones 9 and 19 indicate the implantation zones produced by the implantation of boron B. In this process, the edges of the zones 9 and 19 which project outwards by a distance b and form an essential feature of the invention, can be produced even without a lateral widening of the implantation zone, since, in particular with the above-mentioned implantation conditions, because of its small thickness, the aluminium layer 3 has no appreciable screening effect against the boron implantation which extends to a considerably greater depth than does the phosphorus implantation. It will be seen from Figure 3 that this produces a structure for the field-effect tran-

sistor which is identical to that of Figure 1. To complete the component, it is basically only necessary to remove the pyrolitic silicon dioxide layer 22. The other measures required for completion, such as, for example, the application of contacts to the individual semiconductor zones are carried out conventionally.

Another advantageous production process is illustrated in Figure 4, in which elements which are the same as in Figures 1 to 3 have been given the same reference numerals. An auxiliary aluminium layer 31 is produced on the insulation layer from an initially continuous layer of aluminium for example, by etching, the required lateral delimitation being produced by masking. Using ion implantation with phosphorus and boron, as described above, the implantation zones shown by shading in Figure 3 can be produced as a result of the covering effect of the auxiliary aluminium layer 31. In this case, the previously-mentioned lateral widening of the deeper implantation zone has been employed to produce the projecting edges having the width *b*. The horizontal width of the aluminium auxiliary layer 31 is arranged to be such that the end result is a non-implanted zone having the dimension *c* as shown in Figure 1. On completion of the implantation steps, the auxiliary layer 31 is removed and replaced by the gate electrode 3 of Figure 1. The terminals 5, 15 and 7 are then applied in known manner.

Preferably, an annealing carried out at about 900° C is effected after completion of the implantation processes, in order to activate the implanted material.

A transistor in accordance with the invention can be produced with a gate electrode width of 2 μm without difficulties. In the integrated circuit technique, it is possible to reduce to a value of 4 μm the distance between adjacent gate electrodes 3 of adjacent separate transistors. It is thus possible to achieve a high packing density of 25 μm^2 per transistor.

Figure 5 is a schematic side-sectional view of a field-effect transistor in which, in contrast to the embodiment of Figure 1, the drain zone 62 which can only be functionally compared with the drain zone 6 of Figure 1, is arranged on the same surface of the semiconductor body 61 as the source. The embodiment of Figure 5 is of particular interest for applications in which it is important that the source and drain zones with a drain terminal 63 should be accessible from a single side of the body. The charge carrier drift path which occurs in the embodiment of Figure 5 and which is comparable with the drift path 8 in Figure 1 is indicated by the arrow 81. With this embodiment it is again an essential feature of the invention that the dimensions *a* and *b*, i.e. the width of the projecting edge *b* and the distance *a* of the latter from the semiconductor surface, i.e. from the boundary surface between the semiconductor body 61 and the insulation layer 2, should, as before, obey the conditions that the value of *a* is 1 to 5 times the thickness *d* of the insulation layer 2 and the value of *b* is 1 to 10 times the thickness *d*, whilst the ratio of *b*:*a* is in the range 1:1 to 10:1.

The production of the transistor of Figure 5 can be carried out fundamentally in the same way as described above for the embodiment of Figure 1, an here too the preferred dimensions given above apply.

Figure 6 shows another embodiment of the invention, which is particularly suitable for those electronic circuits in which the gate electrode and the source zone of the field-effect transistor are electrically connected to one another. Such electronic circuits include, for example, inverters and flip-flop circuits in which a field-effect transistor is used as the load resistor.

Elements of the embodiment of Figure 6 which are identical to those of Figure 1 have been given the same reference numerals. The source zone 71 of the embodiment of Figure 6 is comparable with the source zone 4, 14 of Figure 1. This source zone 71 can, for examuple, have a rotationally symmetrical shape, or alternatively can have the form of a strip. A zone 79 is provided below the source zone 71 which is comparable with the zone 9, 19 of Figure 1. In this embodiment also, the or each edge of the zone 79 projects beyond the corresponding edge of the source zone 71 by a distance *b*. This projecting edge *b* lies at a distance *a* from the surface of the semiconductor body 1, which distance again conforms, in accordance with the invention, with the distance *a* in the embodiment of Figure 1. The drift path of the charge carriers between the source zone 71 and the drain zone 6 is indicated by the arrows 82.

The embodiment of Figure 6 again provides the short channel which can be achieved by means of the invention, by suitable dimensioning of the distance *a* and *b* as explained in detail above. For this purpose, the gate electrode 3 projects laterally beyond the side edge of the source zone 71, so that control actually occurs in the area marked by the arrows *a* in Figure 6.

An electrical contact 103 is provided between the gate electrode 3 and the source zone 71. At a suitable point on the semiconductor body 1, the zone 79 is led to the surface of the body so that this zone can be electrically or electronically connected, which is of significance, for example, when the transistor in accordance with the invention is to be used as a load resistor as described above.

WHAT WE CLAIM IS:—

1. A field-effect transistor having a source zone and a drain zone in a semiconductor body and an MIS gate arrangement comprising a gate insulation layer and a gate electrode located on a surface of said body, wherein a further zone of conductivity type opposite to that of said source zone is located in said body below said source zone considered in the direction away from said surface, the conductivity of said further zone being opposite in type to and/or greater than the conductivity of that part of said body surrounding said further zone, wherein said further zone lies at a distance *a* from said gate insulation layer equal to 1 to 5 times the thickness *d* of said gate insulation layer, wherein below said gate arrangement, said further zone has an edge projecting laterally beyond the corresponding edge of said source zone by a distance *b* equal to 1 to 10 times the thickness *d* of said gate insulation layer, wherein the ratio of the distances $b:a$ is in the range of 1:1 to 10:1; and wherein the doping of said further zone is such that when the maximum permissible operating voltage is applied between said gate electrode and said source zone, the majority charge carriers are not discharged from said further zone.

2. A transistor as claimed in Claim 1, wherein said drain zone lies below said further zone in the direction away from said surface.

3. A transistor as claimed in Claim 2, wherein said source zone and said further zone are in the form of concentric annular zones, the inner periphery of said further zone extending inwardly beyond the inner periphery of said source zone by the distance *b*.

4. A transistor as claimed in Claim 2, wherein said source zone and said further zone are each composite zones formed by two parallel and electrically interconnected strips spaced apart, said gate arrangement being located between the strips forming said source zone.

5. A transistor as claimed in Claim 1, wherein the source and drain zones lie adjacent to one another on said surface.

6. A transistor as claimed in Claim 2, wherein said source zone and said further zone are in the form of concentric circular zones lying below said gate insulation layer, the outer periphery of said further zone projecting outwardly beyond the outer periphery of said source zone by the distance *b*.

7. A field-effect transistor substantially as hereinbefore described with reference to and as shown in Figure 1, or Figure 5, or Figure 6, of the drawings.

8. A field-effect transistor produced substantially as hereinbefore described with reference to Figures 2 and 3, or Figure 4, of the drawings.

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Sheet 1

Fig. 1

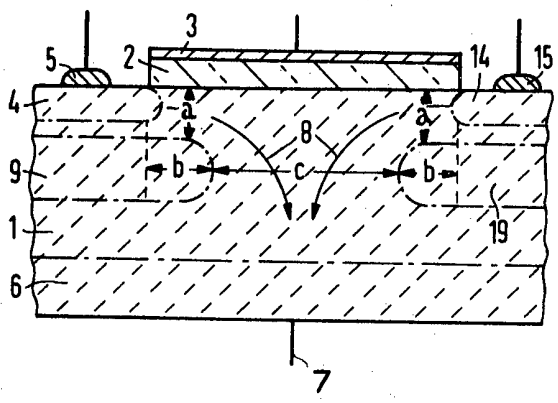

Fig. 2

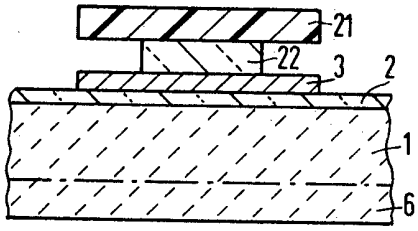

Fig. 3

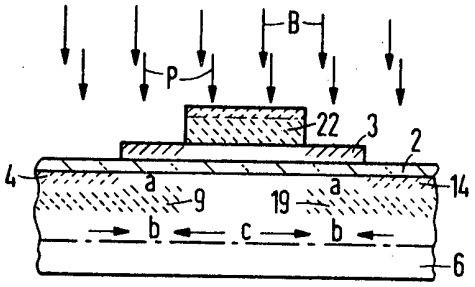

Fig. 4

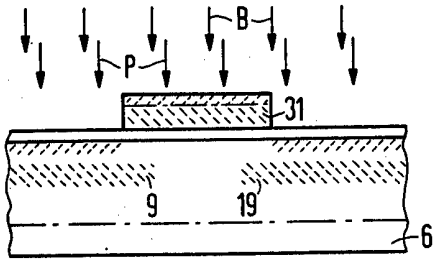

Fig. 5

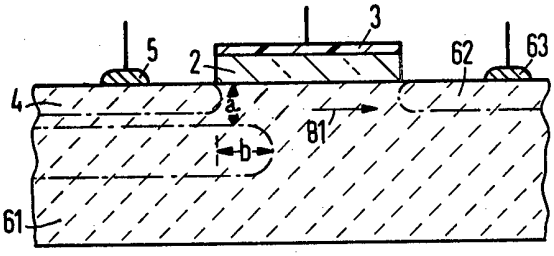

Fig. 6