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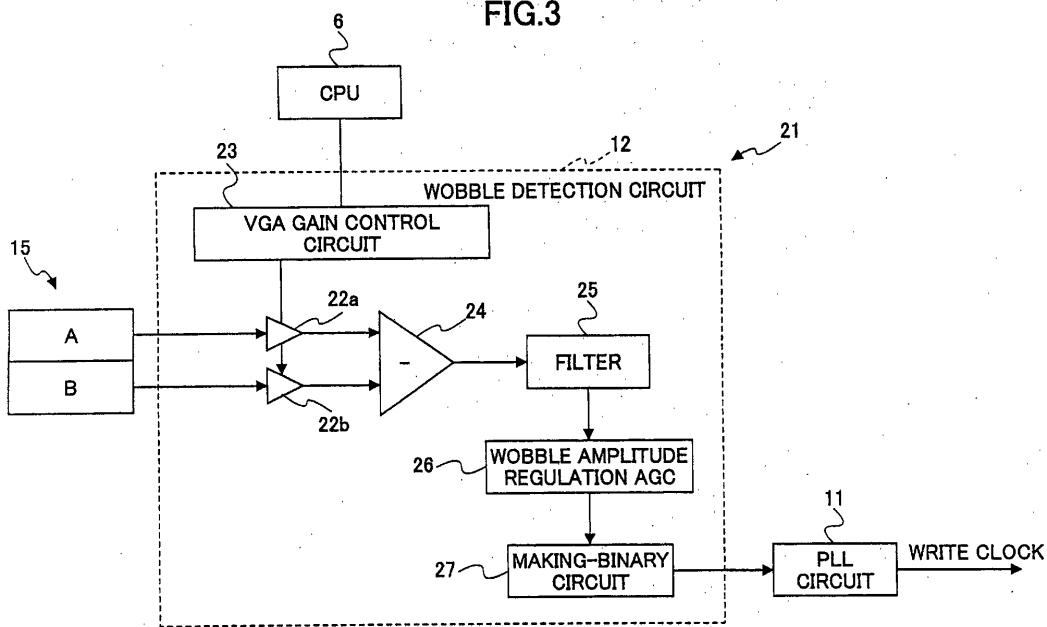
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**(54) LIGHT CLOCK GENERATING CIRCUIT AND OPTICAL DISK UNIT**

(57) A write clock generation circuit is provided that can detect wobble signal in high accuracy and can appropriately generate write clock with only small jitter even when the operation is switched from reproduction to recording. The wobble signal is obtained by changing stepwise the gain of a variable gain amp in the rear stage of a divided photo detector using a gain control circuit in a predetermined time period just after the beginning

of recording. The write clock signal is generated using the above wobble signal. According to this arrangements, the change in wobble signal just before and after the beginning of recording can be reduced, and the gain change of a wobble signal amplitude regulation AGC is made slow. As a result, high frequency deviation of the wobble signal can be reduced even when the operation is switched from reproduction to recording, and the write clock with only small jitter can be generated.

**FIG.3**



**Description****TECHNICAL FIELD**

**[0001]** The present invention relates to a write clock generation circuit that generates write clock based on wobble signal acquired from wobbling track on a recording medium. The present invention further relates to an optical disk apparatus provided with the write clock generation circuit.

**BACKGROUND ART**

**[0002]** Information storage apparatuses (optical disk apparatuses) are practically used that write information on an optical disk, or read information written on an optical disk using a laser beam output from an optical pick-up.

**[0003]** As the performance of personal computers (PC) is being improved, the personal computers become more capable of handling even audio-visual information such as music and video. Audio-visual information is usually very large in memory size. Optical disks have drawn attention as recording media for storing audio-visual information. Because the cost of optical disks is being reduced, as well as their high memory capacity, optical disk apparatuses have became the popular peripherals of personal computers.

**[0004]** Typically, a rewritable recording medium such as a CD-R/RW disk (Compact Disk-Recordable/Rewritable), a DVD-R/RW disk (Digital Versatile Disk), and a DVD+R/RW disk, is formatted so that, when rotated in a constant linear velocity mode, wobble signal detected from wobbling tracks formed on the recording medium becomes constant in order to accurately detect the linear velocity at each radial position.

**[0005]** Wobble signal always needs to be detected, regardless of reading or writing. However, data written on the recording medium and/or modulated laser beam for writing data become the source of noise, and may degrade the quality of wobble signal. That is, wobble signal is included in reflective light from a track, but the reflective light complicatedly includes components that becomes noise to the wobble signal due to data written on the optical disk and/or the power modulation of laser beam for writing data on the optical disk.

**[0006]** Wobble signal is generally extracted in the following manner. The reflective light from a track is received by a photo detector divided into two parts with respect to tangential direction to the track. Noise component included in the reflective light is removed by subtracting output signal from one part of the divided photo detector from output signal from the other part.

**[0007]** Before an optical disk apparatus is shipped from a manufacturing plant, the divided photo detector is aligned so that the reflective light from a track hits the center of the photo detecting surface of the divided photo detector. However, the reflective light may deviate

from the center of the photo detecting surface due to temperature change during operation and/or change over time due to vibration. In such a case, because the output signal from each part of the divided photo detector

5 includes different noise component, the noise components may remain un-canceled even if output signal of one part is subtracted from output signal of the other.

**[0008]** To solve such a problem, Japanese Laid-Open Patent Application No. 8-194969, for example, discloses a method of detecting wobble signal in which data signal component can be clearly removed by normalizing (so-called amplitude regulation automatic gain control (AGC)) the amplitude of output signals from a photo detector divided in the tangential direction of a track and

10 by generating the wobble signal based on the difference between the output signals. This application further discloses an embodiment in which, when an optical disk on which data has not yet been written is read, amplitude regulation AGC is not used since the data signal component

15 does not need to be removed. A determination is made of whether the amplitude regulation AGC circuit is used based on a determination of whether data has been written on the optical disk.

**[0009]** This application No. 8-194969 provides a 20 method of detecting wobble signal in which wobble signal of high quality can be obtained during reproduction of signal from an optical disk. However, the method disclosed in this application is not applicable to wobble signal detection while data is being written.

**[0010]** Particularly, the above method does not take 25 into account the switching of operation from data-reading to data-writing, and fails to obtain good wobble signal during time period in which reproduction is ended and recording is started. As a result, accurate write clock

30 cannot be generated based on such a wobble signal of low quality. That is to say, laser power for data-reading is different from laser power for data-writing, and as a result, the levels of detected wobble components are different. As will be appreciated, when operation is

35 switched from data-reading to data-writing, if the operation is not adequately controlled, the slice voltage of made-binary wobble signal may be deviated (hysteresis, for example). The deviation may cause jitter (deviation over time), which may result in that PLL circuit fails

40 to lock in write clock and operates unstably.

**DISCLOSURE OF THE INVENTION**

**[0011]** It is an object of the present invention to provide 50 a write clock generation circuit that can detect wobble signal at high accuracy even in time in which operation is switched from data-reading to data-writing, and generate suitable write clock containing only a little jitter. Another object of the present invention is to provide an

55 optical disk apparatus that is provided with such a write clock generation circuit.

**[0012]** At the same time, according to the present invention, a write clock generation circuit of which circuit

scale can be made more compact can be provided.

[0013] According to the present invention, a write clock generation circuit that can generate accurate write clock regardless of whether data has been written on the recording medium or not.

[0014] According to the present invention, a write clock generation circuit that ensures to prevent PLL circuit from being out of lock, and can generate write clock with only a little jitter.

[0015] According to an aspect of the present invention, a write clock generation circuit for generating write clock from wobble signal based on a wobbling track formed on a recording medium includes: two variable gain amps that amplify respective signals from a photo detector divided into two portions with a dividing line in a tangential direction of the track at a determined gain; a gain control circuit that determines the gain of the variable gain amps in a particular period immediately after data-writing has been started by varying the gain of the variable gain amps stepwise; a subtractor that produces wobble signal by subtracting outputs from the respective variable gain amps; a wobble amplitude regulation AGC circuit that automatically controls gain thereof so as to regulate amplitude of the wobble signal output therefrom; a making-binary circuit that digitizes signals output from the wobble amplitude regulation AGC circuit into made-binary wobble signal; and a PLL circuit that generates write clock using the made-binary wobble signal as a reference.

[0016] The write clock is generated based on a wobble signal obtained by changing stepwise the gain of the variable gain amps at the rear stage of the divided photo detectors by the gain control circuit in a predetermined time period just after the beginning of recording. According to this arrangement, the change in the wobble signal can be reduced just before and after the beginning of recording, and the change in the gain of wobble signal amplitude regulation AGC circuit can be made slow. Accordingly, the high frequency deviation of the wobble frequency can be reduced even when the operation is switched between reproduction and recording, which results in the generation of write clock with only small jitter. Once the gain of the variable gain amps is changed stepwise for the last time, appropriate signal level can be sustained, which results in the generation of steady write clock.

[0017] According to another aspect of the present invention, a write clock generation circuit for generating write clock from wobble signal based on a wobbling track formed on a recording medium includes: a subtractor that produces wobble signal by subtracting respective signals from a photo detector divided into at least two portions with a dividing line in a tangential direction of the track; a variable gain amp that amplifies the wobble signal output from the subtractor at a determined gain; a gain control circuit that determines the gain of the variable gain amps in a particular period immediately after data-writing has been started by varying

the gain of the variable gain amps stepwise; a wobble amplitude regulation AGC circuit that automatically controls gain thereof so as to regulate amplitude of the wobble signal output from the variable gain amp; a making-binary circuit that digitizes signals output from the wobble amplitude regulation AGC circuit into made-binary wobble signal; and a PLL circuit that generates write clock using the made-binary wobble signal as a reference.

[0018] The write clock is generated based on a wobble signal obtained by changing stepwise the gain of the variable gain amps at the rear stage of the divided photo detectors by the gain control circuit in a predetermined time period just after the beginning of recording. According to this arrangement, although the write clock generation circuit becomes compact, the same function and effect can be achieved.

[0019] According to yet another aspect of the present invention, either one of the above write clock generation circuits may be characterized in that the gain control circuit once reduces the gain of the variable gain amps to a level lower than a gain level of data-reading in the particular period immediately after data-writing has been started, and increases stepwise the gain of the variable gain amps to a gain level of data-reading.

[0020] The wobble signal input to the variable gain amp is great just after the beginning of recording. If the gain is set is lower than the gain of reproduction operation, the wobble signal that is not different from the wobble signal in the reproduction operation can be obtained. On the other hand, since noise is great in the recording operation after the steady state, the gain of the variable gain amp is preferable to be great. Thus, the wobble signal can be surely obtained, and as a result, the write clock can be generated appropriately by increasing the gain stepwise up to the gain level of reproduction operation.

[0021] According to yet another aspect of the present invention, either one of the above write clock generation circuits may be further characterized in that the gain control circuit (23) varies gain steps and time intervals of the variable gain amps to an extent in which the wobble amplitude regulation AGC circuit can follow in the particular period immediately after data-writing has been started.

[0022] According to the above arrangement, the wobble amplitude regulation AGC circuit can surely follow the stepwise change in the gain of the variable gain amp. The write clock can be generated appropriately.

[0023] According to yet another aspect of the present invention, either one of the above write clock generation circuits may be characterized in that the gain control circuit switches the gain of the variable gain amps before data-writing is begun in accordance with whether a preceding region to data-writing starting position is data-written or data-not-yet-written, so that amplitude of the wobble signal immediately before the data-writing starts and amplitude of the wobble signal immediately after the

data-writing starts become substantially equal.

**[0024]** The gain of the variable gain amp before the beginning of recording is switched in accordance with whether the region immediately preceding to the data-writing starting position is data-not-yet-written or data-written, and the amplitudes just before and after the beginning of recording (data-writing) are at the same level. According to the above arrangement, regardless of the recording state of the recording medium (data-not-yet-written or data-written), the change in the wobble signal just before and after the beginning of recording (data-writing) can be reduced, and the gain change of the wobble amplitude regulation AGC circuit can be made slow. As a result, the high frequency deviation of the wobble frequency can be reduced, which results in the generation of write clock with only small jitter.

**[0025]** According to yet another aspect of the present invention, either one of the above write clock generation circuits may further include a PLL gain control circuit that determines loop gain of the PLL circuit so as to increase the loop gain in a predetermined time period immediately after the beginning of data-writing.

**[0026]** The loop gain of the PLL circuit is increased during a predetermined time period just after the beginning of recording. According to the above arrangement, the drawing-in capability of the PLL circuit is increased during the time period in which the change in wobble signal is expected to be great so as to prevent the PLL circuit from being disengaged from the locked state, and once the wobble signal becomes steady, a write clock with only a small jitter can be generated.

**[0027]** According to yet another aspect of the present invention, either one of the above write clock generation circuit may be characterized in that the PLL gain control circuit sets the loop gain of the PLL circuit at a high level in a predetermined time period just after the beginning of data-writing and then, sets the loop gain at a low level.

**[0028]** The loop gain of the PLL circuit is increased to a high level just after the beginning of recording. According to the above arrangement, even if high frequency deviation is caused in the binary wobble signal caused by the change in quality and amplitude of the wobble signal, the wobble signal can be prevented from being disengaged from the locked state. In addition, once the wobble signal becomes steady, the write clock with only small jitter can be generated by lowering the gain.

**[0029]** According to yet another aspect of the present invention, either one of the above write clock generation circuits may be characterized in that the PLL gain control circuit can change the loop gain of the PLL circuit stepwise from the high level to the low level.

**[0030]** The loop gain of the PLL circuit is set at a high level just after the beginning of recording. According to this arrangement, even if the quality and amplitude of the wobble signal changes when the operation is switched from reproduction to recording and consequently, high frequency deviation occurs in the made-binary wobble signal, the wobble signal can be surely

prevented from being disengaged from the locked state. Additionally, the preferable write clock with only small jitter can be generated by lowering the loop gain stepwise to the step in which the wobble signal becomes steady.

**[0031]** According to an aspect of the present invention, an optical disk apparatus includes: a rotation mechanism that rotates a recording medium, wherein a wobbling track is formed on a recording surface of the recording medium; an optical pickup comprising a photo detector divided into at least two portions by a dividing line in a tangential direction of the track, and a laser light source that emits a laser beam to the recording medium; a light source driving circuit that controls the light emission of the light source; and the write clock generation circuit as claimed in claim 1 that receives signals output by the divided photo detector, and outputs write clock to the light source driving circuit.

**[0032]** Because the above write clock generation circuit is used, recording may not fail due to the disengagement of the PLL circuit from the locked state. Additionally, the recording quality when the recording is begun can be retained at a high level.

## 25 BRIEF DESCRIPTION OF THE DRAWINGS

### **[0033]**

**30** FIG. 1 is a block diagram illustrating the structure of an optical disk apparatus according to a first embodiment of the present invention;

**35** FIG. 2 includes schematic diagrams for explaining a recording medium and a divided photo detector according to an embodiment;

**40** FIG. 3 is a block diagram illustrating a write clock generation circuit according to an embodiment;

**45** FIG. 4 illustrates waveforms showing signals in a steady state according to an embodiment;

**50** FIG. 5 illustrates waveforms showing signals in which VGA gain is fixed according to an embodiment;

**55** FIG. 6 illustrates waveforms showing signals in which VGA gain is changed stepwise according to an embodiment;

**45** FIG. 7 is a block diagram illustrating a write clock generation circuit according to a second embodiment of the present invention;

**50** FIG. 8 illustrates waveforms showing signals in respective data-writing states according to a third embodiment; and

**55** FIG. 9 is a block diagram illustrating PLL circuit according to a fourth embodiment.

## BEST MODE FOR CARRYING OUT THE INVENTION

**[0034]** A first embodiment of the present invention is described with reference to FIGs. 1-6. The structure and function of an optical disk apparatus to which the

present invention is applicable is described with reference to FIG. 1.

**[0035]** The optical disk drive is provided with a spindle motor 2 that mainly constitutes a rotation mechanism that rotates a rewritable recording medium 1 such as a CD-R/RW and a DVD±R/RW. The optical disk drive is further provided with an optical pickup 3 that applies a beam spot of a laser beam emitted by a laser light source (not shown) to the rotated recording medium 1, and detects reflective light from the recording medium 1 using a divided photo detector (to be described below).

**[0036]** The following are connected to the optical pickup 3 in that order: a reproduction circuit 4 that filters a detected reproduced signal and makes it into digital signal, and a decoder 5 that converts the data format of user data component generated by the reproduction circuit 4. The data-format-converted user data component can be transferred to an external host computer (not shown) via a CPU 6.

**[0037]** On the other hand, information to be recorded is transferred from the external host to an encoder 7 via the CPU 6. The encoder 7 converts the data format of the information, and a laser control circuit 8, that is, a light source drive circuit controls the light emission of the laser light source in the optical pickup 3 in accordance with information bits thereby to writes the information on the recording medium 1.

**[0038]** The optical disk drive is further provided with an operation circuit 9 that generates servo signal based on output signal obtained from the divided photo detector in the optical pickup 3. The optical disk drive is configured to control the position of an optical lens (not shown) in the optical pickup 3 by outputting the servo signal to a servo circuit 10. This servo circuit 10 controls the rotation of the spindle motor 2 based on write clock signal obtained from PLL circuit 11.

**[0039]** The optical disk drive is also provided with a wobble detection circuit 12 to which the output signal from the divided photo detector is fed after the operation by the operation circuit 9. The wobble detection circuit 12 extracts the wobble signal. The wobble signal output from the wobble detection circuit 12 is fed to the PLL circuit 11, which generates the write clock signal based on the wobble signal. According to the above arrangements, an accurate write clock in synchronization with the rotation of the recording medium 1 can be generated. The PLL circuit 11 and the wobble detection circuit 12 constitutes a write clock generation circuit according to the present invention.

**[0040]** Since the wobble signal contains physical address information, the wobble signal is transferred to an address detection circuit 13 and converted into address information by an address decoder 14 thereby to reproduce address information of current accessing position.

**[0041]** An exemplary recording medium 1 and an exemplary divided photo detector that are used for the present embodiment are described with reference to FIG. 2. As shown in FIG. 2 (a), a wobbling spiral track

or wobbling concentric tracks is formed on the recording medium 1. As shown in FIG. 2 (b), the divided photo detector 15 receives a reflective signal from the spot S on the recording medium 1, and is provided with two

5 photo detection regions A and B divided by a division line 16 corresponding to the tangential direction of the track. As shown in FIG. 2 (c), one of the simplest operations for obtaining the wobble signal is to produce the difference (A-B) between photo detection amounts of 10 the photo detection regions A and B of the divided photo detector. Of course, the photo detector of the optical pickup 3 may be divided into 4 or more photo detection regions, instead of two. In such a case, the 4 or more photo detection regions may be grouped for the similar 15 operation in accordance with the two photo detection regions divided by the division line 16.

**[0042]** Based on the above presumed configuration of the optical disk drive, the write clock generation circuit 21 according to the present embodiment is structured 20 as shown in FIG. 3. As described above, the write clock generation circuit 21 includes the wobble detection circuit 12 and the PLL circuit 11. The wobble detection circuit 12 is provided with two variable gain amps VGA 22a and 22b to which output signals from the photo detection 25 regions A and B of the divided photo detector 15 of the optical pickup 3 via the operation circuit 9. The variable gain amps VGA 22a and 22b amplify or attenuate the output signals from the photo detection regions A and B in accordance with a desired gain. The wobble detection circuit 12 is further provided with a VGA gain control circuit 23 that controls the gain of the variable gain amps 30 VGA 22a and 22b. The VGA gain control circuit 23 may automatically control the gain of the variable gain amps VGA 22a and 22b in accordance with the operational state (writing or reading, for example) of the optical disk drive. In this embodiment, the VGA gain control circuit 23 is configured to control the gain of the variable gain amps VGA 22a and 22b based on an instruction from the CPU 6.

**[0043]** A subtractor 24 is connected to the outputs from the variable gain amps VGA 22a and 22b. The subtractor 24 outputs the wobble signal by producing difference between the output signals from the variable gain amps VGA 22a and 22b. A filter circuit 25 is connected 45 to the rear stage of the subtractor 24. The wobble signal output by the subtractor 24 contains noise component other than a real wobble signal caused by, for example, the leakage of data signal written on the recording medium and the DC offset due to positional deviation of the 50 optical pickup 3. The filter circuit 25 extracts only needed frequency component. Particularly, the filter circuit 25 may be a combination of a low-pass filter LPF and a high-pass filter HPF, or a band-pass filter BPF. After frequency separation by the filter circuit 25, the wobble signal is fed to a wobble amplitude regulation AGC (automatic gain control) circuit 26 that regulates the wobble signal amplitude that is high enough to make the wobble signal binary. A making-binary circuit 27 that makes the 55

wobble signal into binary data is connected to the rear stage of the wobble amplitude regulation AGC 26. The PLL circuit 11 generates the write clock based on the binary wobble signal output from the making-binary circuit 27. The filter circuit 25 may be provided after the wobble amplitude regulation AGC circuit 26.

**[0044]** Based on the above configuration, signal waveforms in a steady state (not immediately after the switching between reproduction and recording, but a predetermined time period after the switching in which the wobble signal remains steady) are described with reference to FIG. 4. As shown in FIG. 4(a), in a steady state in which signal being reproduced from a recording medium on which data has not yet been written (data-not-yet-written medium), the DC level of the output signal from the divided photo detector 15 is low because the laser power is low. At the output of the filter circuit 25 after the subtraction by the subtractor 24, the DC component of the output signal from the divided photo detector 15 has been removed, and only the wobble component is extracted. The wobble signal is amplified by the wobble amplitude regulation AGC circuit 26 (amplified from the dotted line to the block line) so that the amplitude of the wobble signal is increased to a level great enough to make the wobble signal binary or to detect address information (the wobble signal of some format may contain address information superposed thereon). At this time, the AGC gain is great.

**[0045]** On the other hand, as shown in FIG. 4 (b), in a steady state in which data are being written to the recording medium, the light emitting component of the laser light source is superposed on the output signal from the divided photo detector 15. Since the laser power is great, the wobble component is also great. If the light emitting component and the DC component are removed by the subtractor 24 and the filter circuit 25, a greater wobble signal can be obtained compared with the state in which signal being reproduced from a data-not-yet-written medium. Accordingly, the wobble amplitude regulation AGC circuit 26 amplifies the wobble signal at a lower gain from the dotted line to the block line.

**[0046]** Referring to FIG. 5, a description is given about the waveforms in the case in which, while the gain of the variable gain amps VGA 22a and 22b is fixed, the operation is switched from reproduction to recording. The waveforms in this case are similar to those of the steady state in which signal being reproduced from a data-not-yet-written medium (not-written reproduction steady state) and those of the steady state in which data are being written to the recording medium (recording steady state) combined together. If the AGC is sustained at a high level of the not-written reproduction steady state, a wobble signal of great amplitude is input. The amplitude of output from the wobble amplitude regulation AGC circuit 26 becomes very great immediately after the beginning of data-writing. As a result, jitter (deviation over time) may be caused due to deviation (hysteresis, for example) in slice voltage of the binary wobble signal

in the rear stage. The jitter may disengage locked write clock, and makes the write clock unstable.

**[0047]** Taking the above problems into account, according to the present embodiment, when the operation 5 is switched from reproduction to recording, the VGA gain control circuit 23 changes stepwise the gain of the variable gain amps VGA 22a and 22b in a predetermined time period immediately after the beginning of data-writing. FIG. 6 shows an exemplary operation in 10 which the gain of the gain amp VGA 22a and 22b is changed stepwise immediately after the beginning of data-writing.

**[0048]** That is to say, since the wobble signal input to the wobble amplitude regulation AGC circuit 26 is great 15 immediately after the beginning of data-writing, the gain of the gain amps VGA 22a and 22b are set at a low level for the meantime. According to this arrangement, wobble signal that is at the same level as that during reproduction can be obtained. However, since noise component 20 due to the modulation of laser emission is great during recording, the gain of the gain amp VGA 22a and 22b is preferably great when the operation change to the recording steady state. Thus, the gain of the gain amps VGA 22a and 22b is increased stepwise. The step 25 for which the gain is increased and time for which the gain is kept constant may be determined so that the wobble amplitude regulation AGC circuit 26 in the rear stage can easily follow change in the gain, and the output of the wobble amplitude regulation AGC circuit 26 30 does not change too much.

**[0049]** As described above, according to the present embodiment, the gain of the VGA gain control circuit 23 is changed stepwise thereby to obtain the wobble signal in a predetermined time period immediately after the beginning of recording. The write clock is generated based 35 on the above wobble signal. According to this arrangement, the change in wobble signal before and after the beginning of recording can be reduced, and the change in gain of the wobble amplitude regulation AGC circuit 40 26 can be made small and smooth. Therefore, even when reproduction and recording are switched, the high frequency deviation of the wobble frequency can be reduced, which results in the generation of write clock with only small jitter. After the gain of the variable gain amps 45 VGA 22a and 22b is finally changed stepwise, the signal level can be kept at preferable level in the recording. Accordingly, steady write clock can be generated. In addition, the wobble amplitude regulation AGC circuit 26 can surely follow the stepwise change of the gain of the 50 variable gain amps VGA 22a and 22b. As a result, the write clock can be appropriately generated. Furthermore, even if the wobble amplitude regulation AGC circuit 26 needs to be fine tuned, no special switching feature, for example, is required, and no special external 55 component is required. The write clock generation circuit can be embedded in a LSI.

**[0050]** A second embodiment of the present invention is described below with reference to FIG. 7. Portions

identical to those of the first embodiment are referred to by the same reference symbols, and their description is omitted. The order of the variable gain amps and the subtractor is opposite in the present embodiment. The difference between the output signals from the divided photo detector 15 is generated by the subtractor 24 into the wobble signal. The wobble signal is fed to the variable gain amp VGA 22, and is amplified or attenuated in accordance with the gain.

**[0051]** The operation of the write clock generation circuit according to the second embodiment is similar to that of the write clock generation circuit according to the first embodiment. According to the present embodiment, since only one variable gain amp VGA is required, the write clock generation circuit becomes smaller in circuit scale than the write clock generation circuit according to the first embodiment, but is the same in effects.

**[0052]** A third embodiment of the present invention is described below with reference to FIG. 8. In the present embodiment, the gain of the variable gain amps VGA 22a and 22b (or 22) before the beginning of recording is switched in accordance with whether the region preceding to the position at which recording is begun is a data-not-yet-written region or a data-written region. According to the above arrangement, the amplitude of wobble signal immediately before and after the beginning of recording can be substantially the same level.

**[0053]** A detailed description is given with reference to FIG. 8. FIG. 8 (a) shows waveforms in a steady state in which signal being reproduced from the data-not-yet-written medium (a recording medium on which data has not yet been written), and FIG. 8 (b) shows waveforms in a steady state in which signal being reproduced from the data-written medium (a recording medium on which data has been written). When signal is reproduced from a data-written region, data signal component is superposed on the output signal from the divided photo detector 15, and thus the average signal level of the data-written region becomes smaller than that of the data-not-yet-written region. Thus, the wobble signal becomes small. In order to make the amplitude of the wobble signal immediately after the beginning of recording equal to that of the wobble signal just before the beginning of recording, the gain of the variable gain amps VGA 22a and 22b (or 22) needs to be changed in accordance with whether the region preceding to the data-writing starting position is data-not-yet-written or data-written. Typically, information about the region of the recording medium 1 in which data has been written (data-written) is available. The setting of the VGA gain control circuit 23 may be adjusted by the CPU 6, for example, in accordance with the information.

**[0054]** According to the above arrangement, according to the present embodiment, the change in the wobble signal before and after the beginning of recording can be reduced regardless of the recording state (data-not-yet-written / data-written) of the recording medium 1, and the change in gain of the wobble amplitude reg-

ulation AGC circuit 26 can be small and smooth. Accordingly, the high frequency deviation of the wobble frequency can be reduced, which results in the generation of write clock with only small jitter.

5 **[0055]** A fourth embodiment of the present invention is described below with reference to FIG. 9. This embodiment relates to the structure of the PLL circuit 11 provided in the write clock generation circuit 21. As known, the PLL circuit 11 is basically a loop circuit provided with PD (phase comparator) 31, filter 32, VCO (voltage controlled oscillator) 33, 1/n divider 34. The PLL circuit 11 according to the present embodiment is provided with two or more filters 32a and 32b of which properties are different. PLL gain control circuit 35 can switch 15 the gain of the PLL circuit 11.

**[0056]** Generally, the PLL circuit only needs to follow low frequency change in frequency caused by the rotation of the recording medium 1. The loop gain is designed to be relatively low in order to reduce the jitter of 20 the write clock. However, the quality and amplitude of the wobble signal changes before and after the beginning of reproduction and recording as described above. As a result, high frequency deviation may be caused in the binary wobble signal obtained from the make-binary 25 circuit 27. If the loop gain is unchanged, the PLL circuit 11 may easily be disengaged from locked state. In the present embodiment, as described above, the loop gain can be switched by the PLL gain control circuit 35.

**[0057]** The output signal of VCO (voltage controlled oscillator) 33 is the write clock. The phase of 1/n-divided write clock (n: division ratio that makes 1/n-divided write clock is equal in frequency as wobble signal) output from the 1/n-divider 34 is compared with the phase of the binary wobble signal output from the making-binary circuit 35 27 by the PD (phase comparator) 31. The result of the comparison is provided to one of the multiple filters 32a and 32b of which properties are different, and the output signal from the one of the filters is fed to the VCO 33 so as to determine the oscillation frequency of the VCO 33. 30 The multiple filters 32a and 32b are switched, or are turned on/off, by the PLL gain control circuit 35 so as to change the loop gain of the PLL circuit 11. Particularly, the loop gain is increased just after the beginning of recording (data-writing), and when the wobble signal becomes steady, the loop gain is decreased. If multiple 35 PLL gains are available, the loop gain may be reduced stepwise after the beginning of recording in the same manner as the variable gain amps VGA 22a and 22b.

**[0058]** As described above, according to the present embodiment, the loop gain of the PLL circuit 11 is increased in a predetermined time period just after the beginning of recording. According to this arrangement, the PLL circuit 11 can be prevented from being disengaged from the locked state by increasing the drawing-in capability only during a time period in which the wobble signal is expected to be great. At the same time, once the wobble signal becomes steady, a preferable write clock signal having only small jitter can be generated.

### INDUSTRIAL APPLICABILITY

**[0059]** According to an aspect of the present invention, the write clock is generated based on a wobble signal obtained by changing stepwise the gain of the variable gain amps at the rear stage of the divided photo detectors by the gain control circuit in a predetermined time period just after the beginning of recording. According to this arrangement, the change in the wobble signal can be reduced just before and after the beginning of recording, and the change in the gain of wobble signal amplitude regulation AGC circuit can be made slow. Accordingly, the high frequency deviation of the wobble frequency can be reduced even when the operation is switched between reproduction and recording, which results in the generation of write clock with only small jitter. Once the gain of the variable gain amps is changed stepwise for the last time, appropriate signal level can be sustained, which results in the generation of steady write clock.

**[0060]** According to another aspect of the present invention, the write clock is generated based on a wobble signal obtained by changing stepwise the gain of the variable gain amps at the rear stage of the divided photo detectors by the gain control circuit in a predetermined time period just after the beginning of recording. According to this arrangement, although the write clock generation circuit becomes compact, the same function and effect can be achieved.

**[0061]** According to yet another aspect of the present invention, because the above write clock generation circuit is used, recording may not fail due to the disengagement of the PLL circuit from the locked state. Additionally, the recording quality when the recording is begun can be retained at a high level.

### **Claims**

1. A write clock generation circuit for generating write clock from wobble signal based on a wobbling track formed on a recording medium, comprising:

two variable gain amps that amplify respective signals from a photo detector divided into two portions by a dividing line in a tangential direction of the track at a determined gain; a gain control circuit that determines the gain of said variable gain amps in a particular period immediately after the beginning of data-writing by varying the gain of said variable gain amps stepwise; a subtractor that produces wobble signal by subtracting outputs from said respective variable gain amps; a wobble amplitude regulation AGC circuit that automatically controls gain thereof so as to regulate amplitude of the wobble signal output

therefrom;

a making-binary circuit that digitizes signals output from said wobble amplitude regulation AGC circuit into made-binary wobble signal; and a PLL circuit that generates write clock using the made-binary wobble signal as a reference.

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2. The write clock generation circuit as claimed in claim 1, wherein said gain control circuit once reduces the gain of said variable gain amps to a level lower than a gain level of data-reading in the particular period immediately after the beginning of data-writing, and increases stepwise the gain of said variable gain amps to a gain level of data-reading.

3. The write clock generation circuit as claimed in claim 1, wherein said gain control circuit varies gain steps and time intervals of said variable gain amps to an extent in which said wobble amplitude regulation AGC circuit can follow in the particular period immediately after data-writing has been started.

4. The write clock generation circuit as claimed in claim 1, wherein said gain control circuit switches the gain of said variable gain amps before data-writing is begun in accordance with whether a preceding region to data-writing starting position is data-written or data-not-yet-written, so that amplitude of the wobble signal immediately before the data-writing starts and amplitude of the wobble signal immediately after the data-writing starts become substantially equal.

5. The write clock generation circuit as claimed in claim 1, further comprising a PLL gain control circuit that determines loop gain of said PLL circuit so as to increase the loop gain in a predetermined time period immediately after the beginning of data-writing.

6. The write clock generation circuit as claimed in claim 5, wherein said PLL gain control circuit sets the loop gain of said PLL circuit at a high level in a predetermined time period just after the beginning of data-writing and then, sets the loop gain at a low level.

7. The write clock generation circuit as claimed in claim 6, wherein said PLL gain control circuit can change the loop gain of said PLL circuit stepwise from the high level to the low level.

8. A write clock generation circuit for generating write clock from wobble signal based on a wobbling track formed on a recording medium, comprising:

a subtractor that produces wobble signal by

subtracting respective signals from a photo detector divided into at least two portions with a dividing line in a tangential direction of the track;

a variable gain amp that amplifies the wobble signal output from said subtractor at a determined gain;

a gain control circuit that determines the gain of said variable gain amps in a particular period immediately after data-writing has been started by varying the gain of said variable gain amps stepwise;

a wobble amplitude regulation AGC circuit that automatically controls gain thereof so as to regulate amplitude of the wobble signal output from said variable gain amp;

a making-binary circuit that digitizes signals output from said wobble amplitude regulation AGC circuit into made-binary wobble signal; and

a PLL circuit that generates write clock using the made-binary wobble signal as a reference.

9. The write clock generation circuit as claimed in claim 8, wherein said gain control circuit once reduces the gain of said variable gain amp to a level lower than a gain level of data-reading in the particular period immediately after data-writing has been started, and increases stepwise the gain of said variable gain amp to a gain level of data-reading.

10. The write clock generation circuit as claimed in claim 8, wherein said gain control circuit varies gain steps and time intervals of said variable gain amp to an extent in which said wobble amplitude regulation AGC circuit can follow in the particular period immediately after data-writing has been started.

11. The write clock generation circuit as claimed in claim 8, wherein said gain control circuit switches the gain of said variable gain amp before data-writing is begun in accordance with whether a preceding region to data-writing starting position is data-written or data-not-yet-written, so that amplitude of the wobble signal immediately before the data-writing starts and amplitude of the wobble signal immediately after the data-writing starts become substantially equal.

12. The write clock generation circuit as claimed in claim 8, further comprising a PLL gain control circuit that determines loop gain of said PLL circuit so as to increase the loop gain in a predetermined time period immediately after the beginning of data-writing.

13. The write clock generation circuit as claimed in claim 12, wherein said PLL gain control circuit sets

the loop gain of said PLL circuit at a high level in a predetermined time period just after the beginning of data-writing and then, sets the loop gain at a low level.

5 14. The write clock generation circuit as claimed in claim 13, wherein said PLL gain control circuit can change the loop gain of said PLL circuit stepwise from the high level to the low level.

10 15. An optical disk apparatus, comprising:

15 a rotation mechanism that rotates a recording medium, wherein a wobbling track is formed on a recording surface of the recording medium; an optical pickup comprising a photo detector divided into at least two portions by a dividing line in a tangential direction of the track, and a laser light source that emits a laser beam to the recording medium; a light source driving circuit that controls the light emission of the light source; and the write clock generation circuit as claimed in claim 1 that receives signals output by the divided photo detector, and outputs write clock to said light source driving circuit.

20 16. An optical disk apparatus, comprising:

25 a rotation mechanism that rotates a recording medium, wherein a wobbling track is formed on a recording surface of the recording medium; an optical pickup comprising a photo detector divided into at least two portions by a dividing line in a tangential direction of the track, and a laser light source that emits a laser beam to the recording medium; a light source driving circuit that controls the light emission of the light source; and the write clock generation circuit as claimed in claim 2 that receives signals output by the divided photo detector, and outputs write clock to said light source driving circuit.

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FIG.1

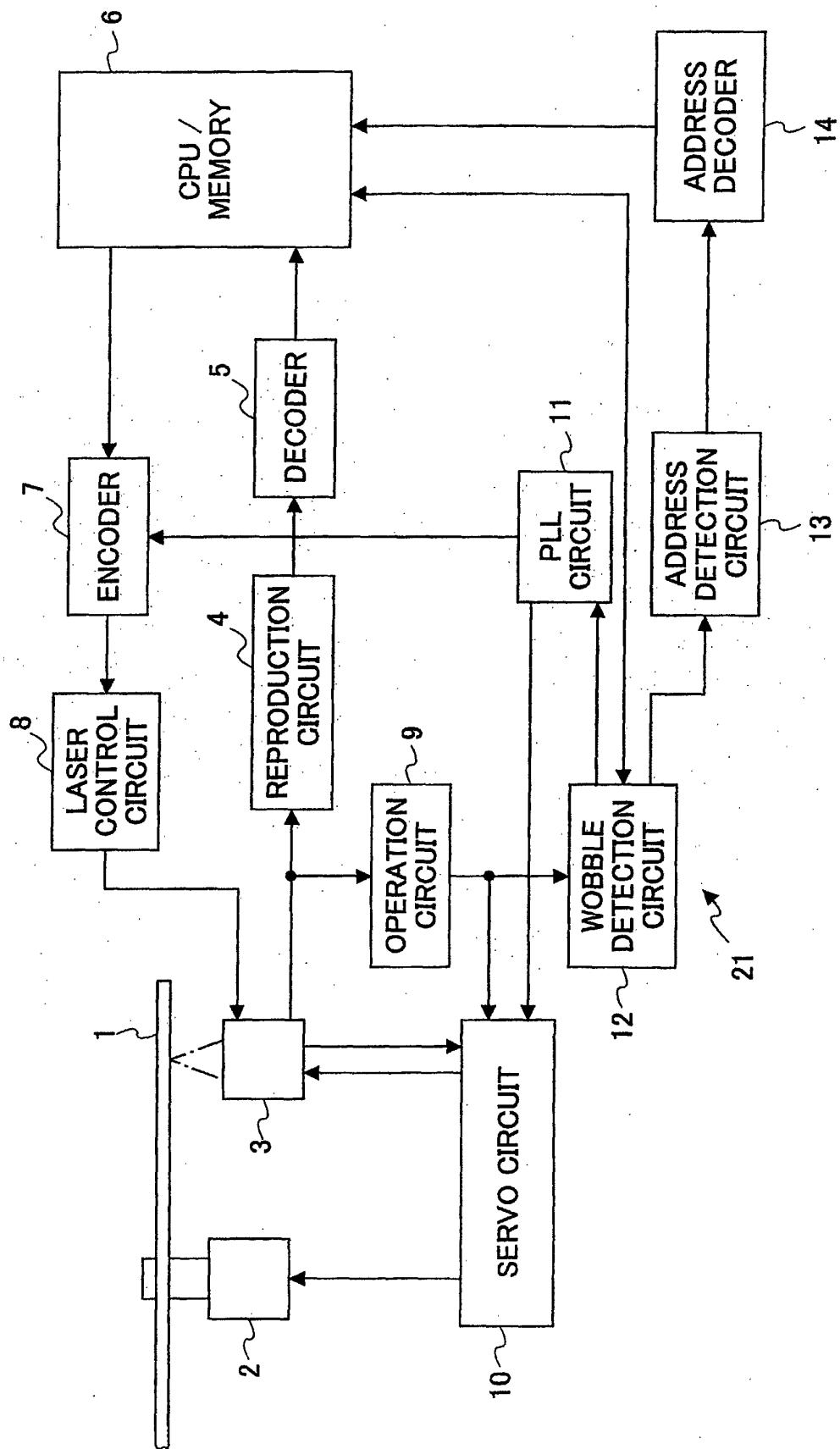


FIG.2

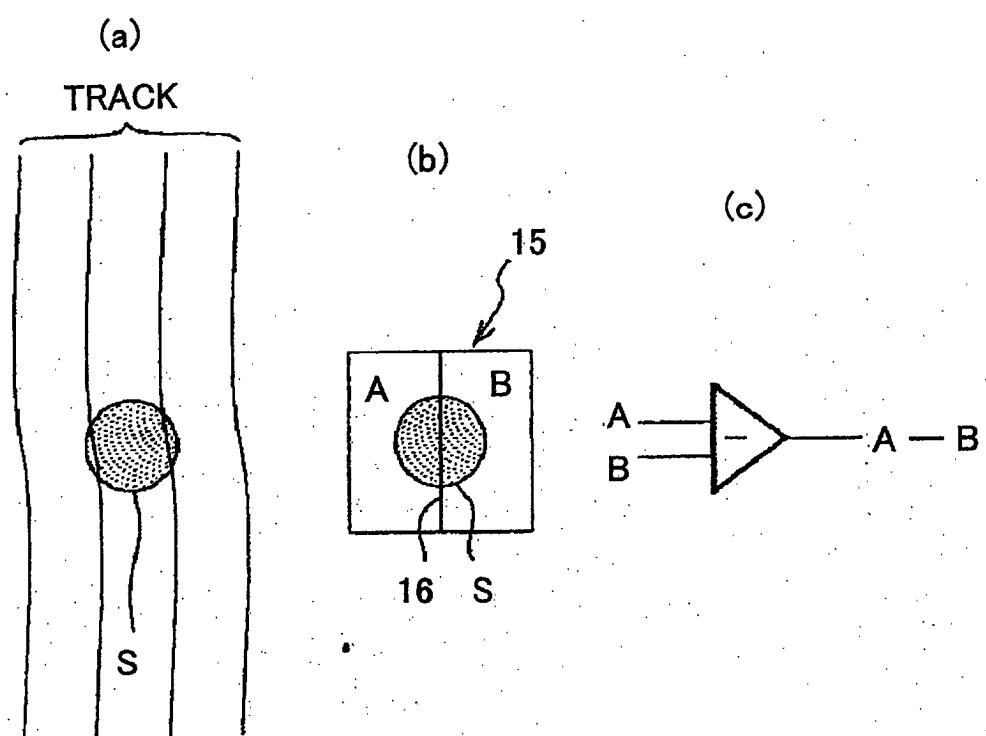


FIG.3

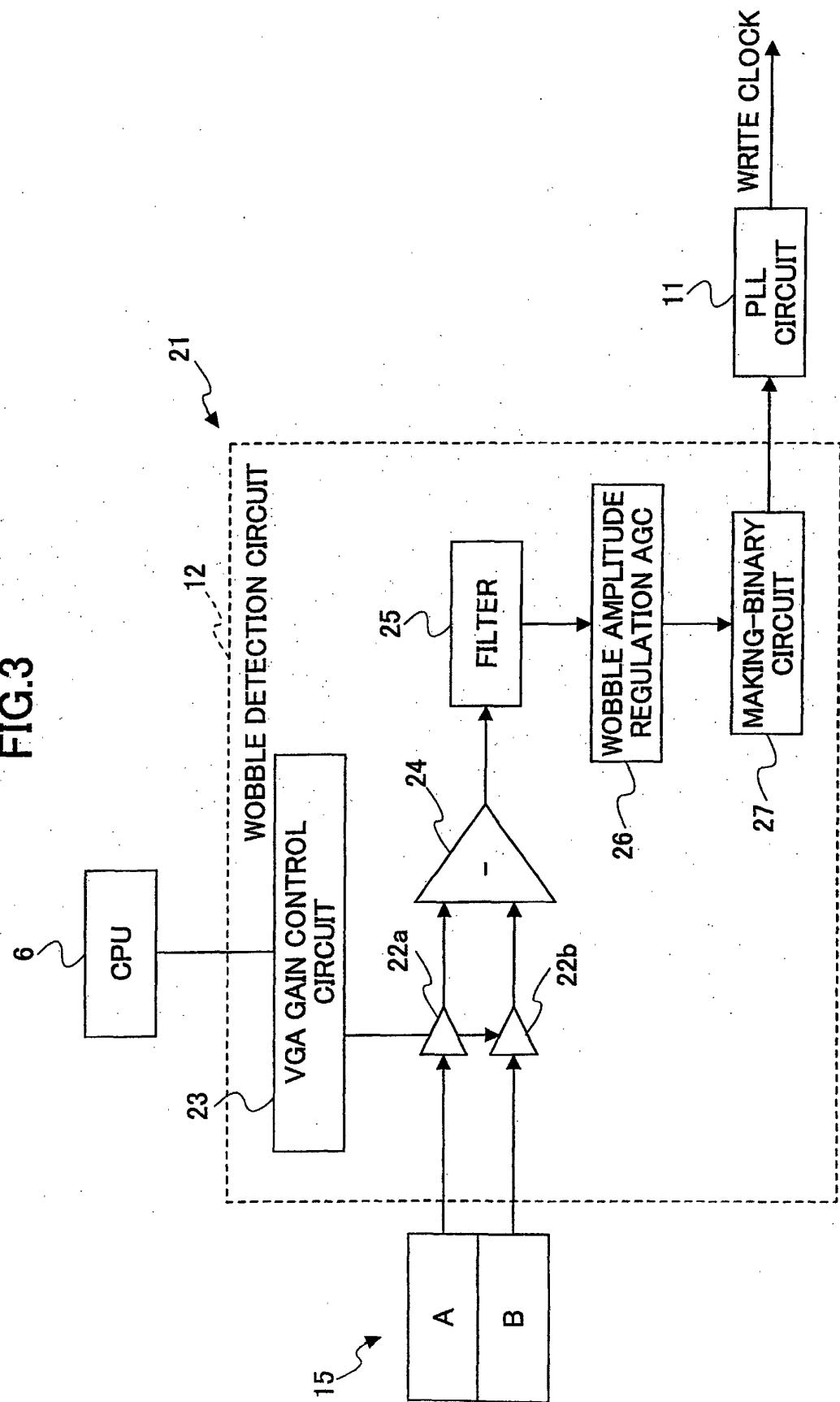
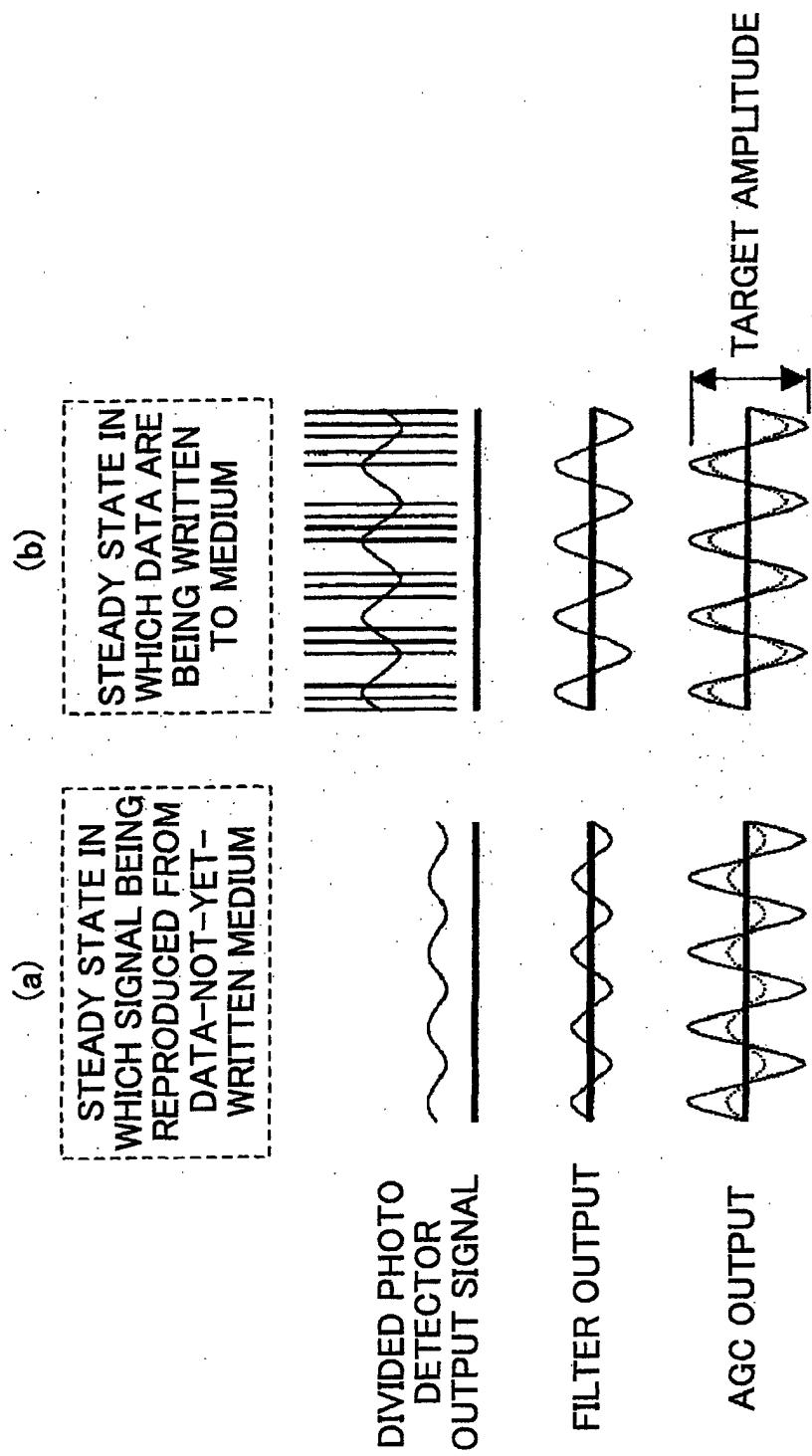
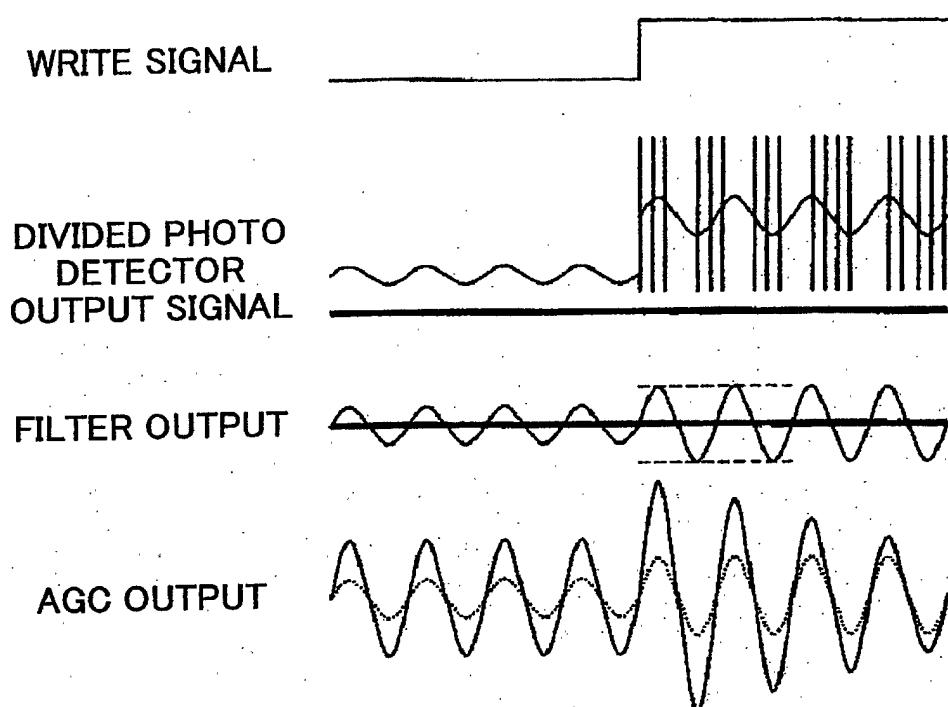


FIG.4



**FIG.5**



**FIG.6**

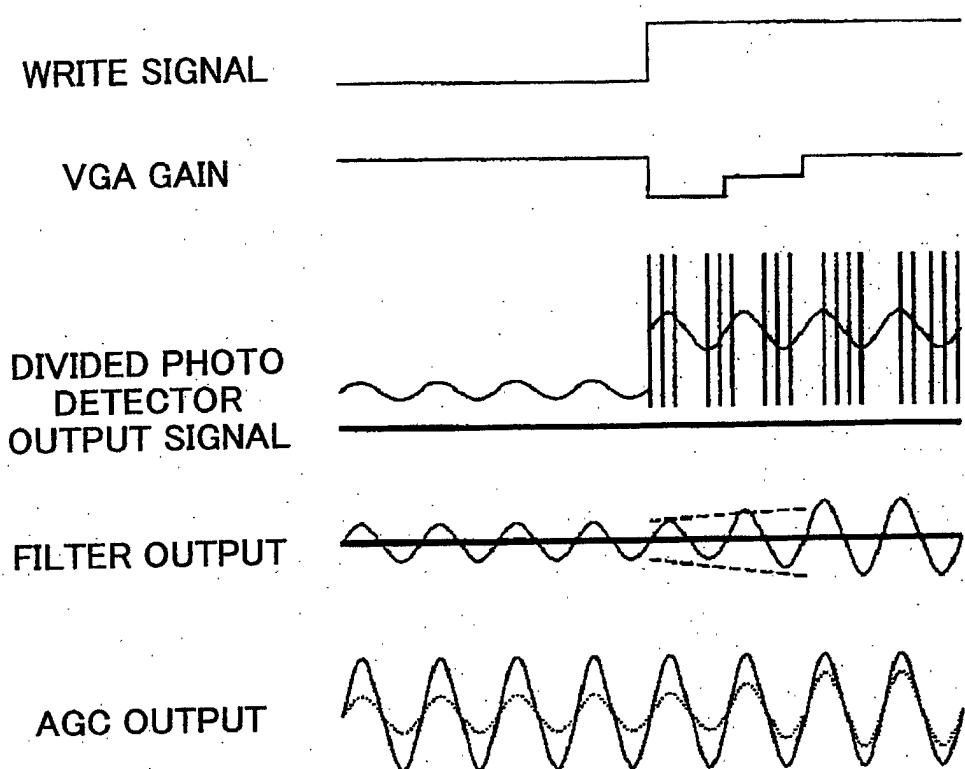


FIG.7

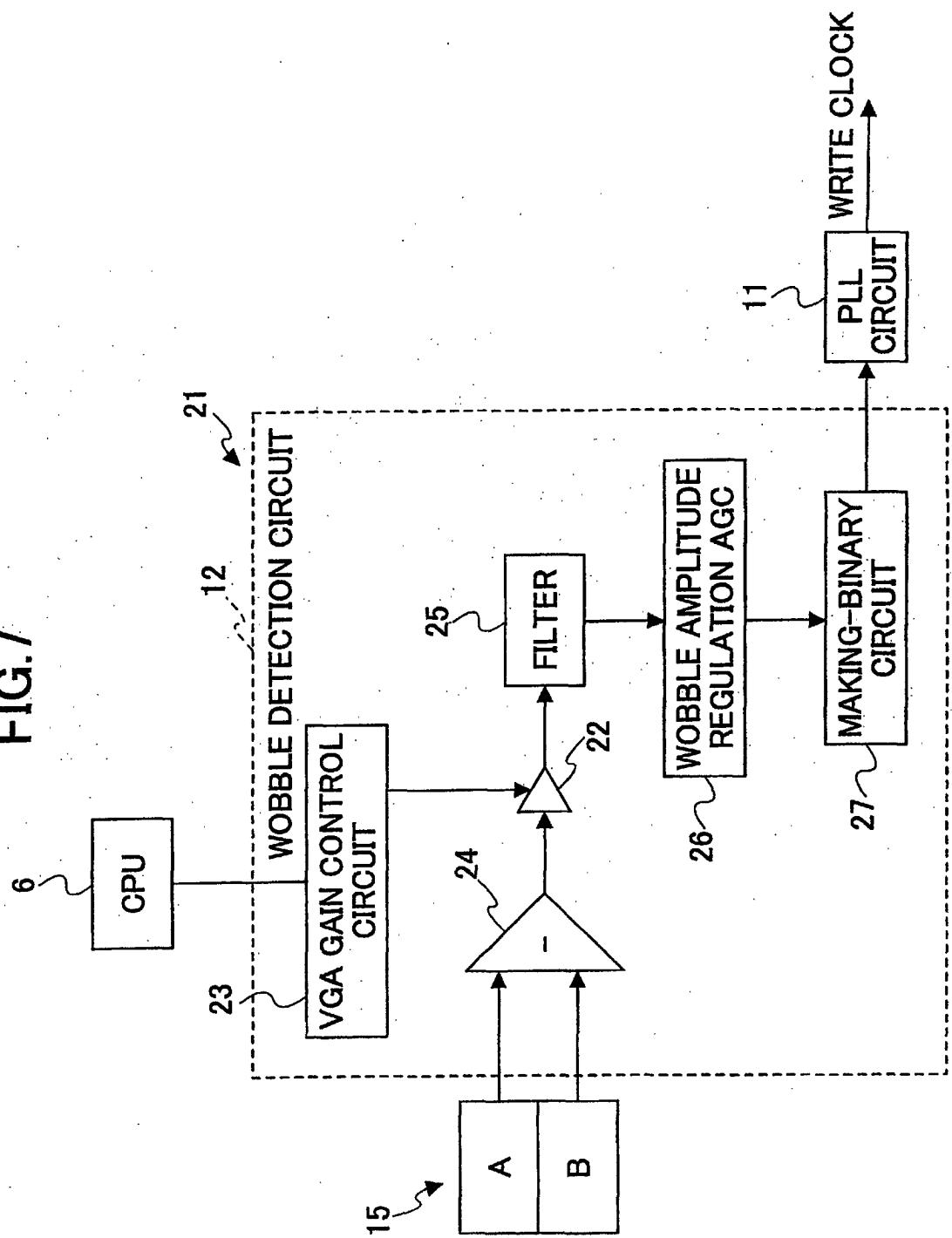


FIG.8

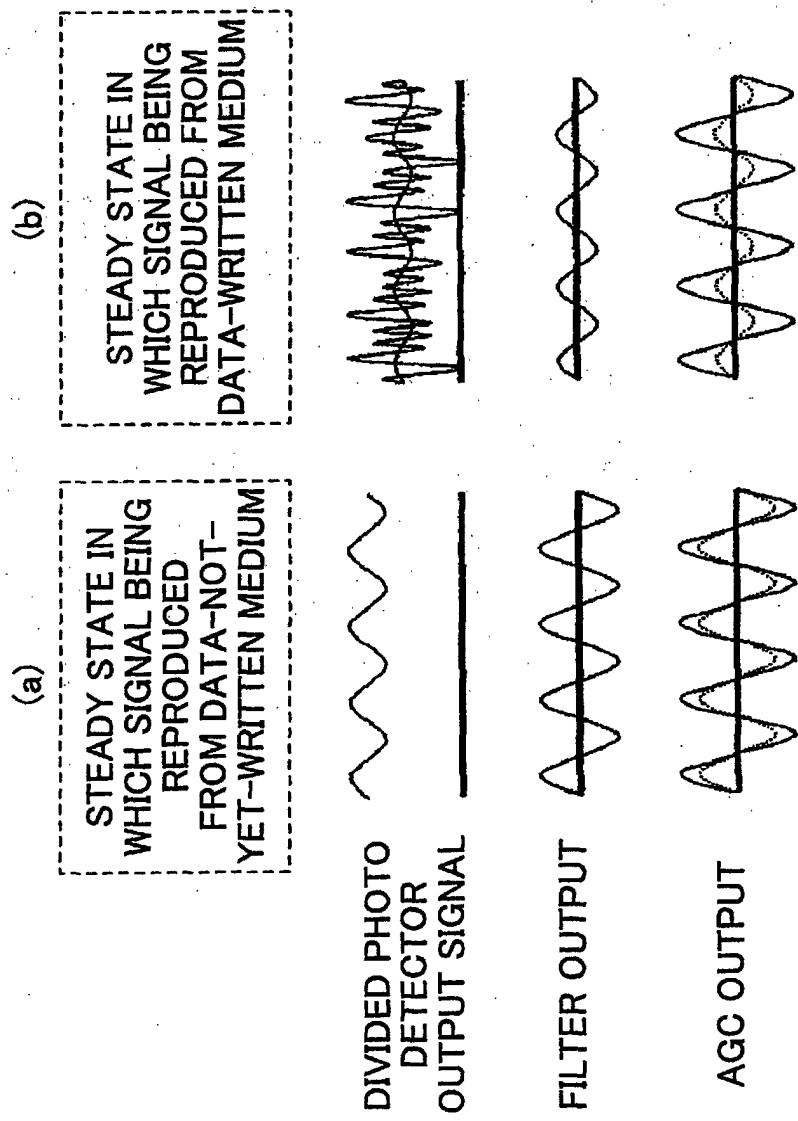
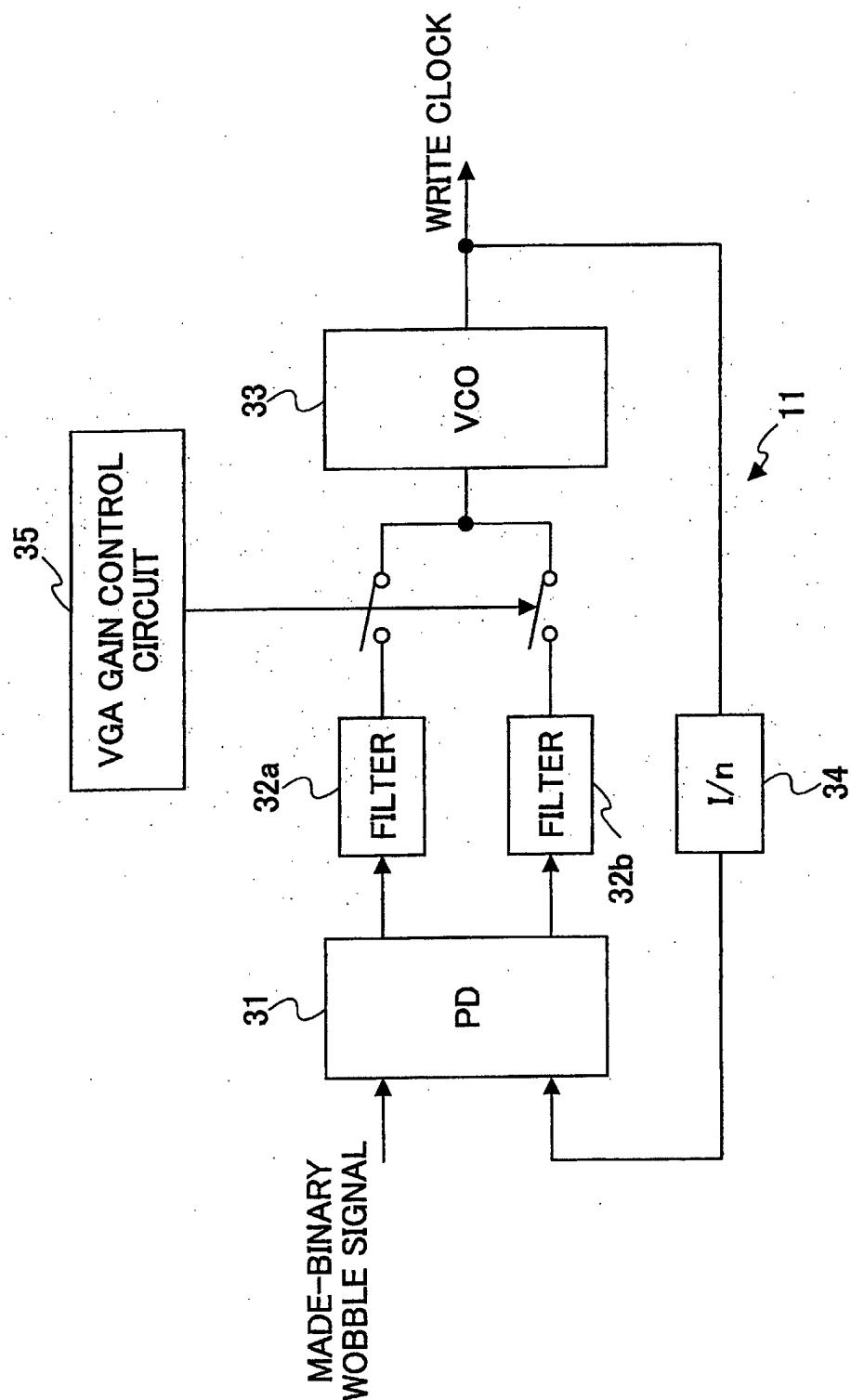


FIG.9



## INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP03/02585

## A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl<sup>7</sup> G11B7/005, G11B7/0045, G11B20/10

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl<sup>7</sup> G11B7/005, G11B7/0045, G11B20/10, G11B7/007, G11B7/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho 1926-1996 Jitsuyo Shinan Toroku Koho 1996-2003  
Kokai Jitsuyo Shinan Koho 1971-2003 Toroku Jitsuyo Shinan Koho 1994-2003

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2001/0026512 A1 (NISHIMURA et al.), 04 October, 2001 (04.10.01), Full text & JP 2001-266486 A & CN 1316729 A	1-16
A	US 6081490 A (KURODA et al.), 27 June, 2000 (27.06.00), Full text & US 6215742 B1 & US 6310843 B1 & US 2002/0018415 A1 & JP 10-293926 A	1-16
A	JP 2000-67434 A (Pioneer Electronic Corp.), 03 March, 2000 (03.03.00), Full text (Family: none)	1-16

 Further documents are listed in the continuation of Box C. See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means	"&" document member of the same patent family
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search 04 June, 2003 (04.06.03)	Date of mailing of the international search report 17 June, 2003 (17.06.03)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

Form PCT/ISA/210 (second sheet) (July 1998)

## INTERNATIONAL SEARCH REPORT

International application No.  
PCT/JP03/02585

## C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 8-194969 A (Sony Corp.), 30 July, 1996 (30.07.96), Full text (Family: none)	1-16

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