

[54] **VARIABLE TIME RATIO CONTROL HAVING POWER SWITCH WHICH DOES NOT REQUIRE CURRENT EQUALIZING MEANS**

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[57] **ABSTRACT**

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A pulse width modulation control having a power switch arrangement which does not require external current equalization means has a plurality of paralleled power transistors whose forward current transfer ratio decreases abruptly with increase in collector current and whose base drive is supplied by a constant current switching regulator having a plurality of paralleled clamping transistors in shunt to the regulator output terminals which are turned on by variable width pulses to shunt current away from the power transistors and thereby turn the power switch off and on. The regulator output is coupled to the base of each power transistor by a diode whose forward drop promotes base current sharing and which prevents multiple transistor failure.

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[52] U.S. Cl. .... **318/341, 307/297**

[51] Int. Cl. .... **H02p 5/40**

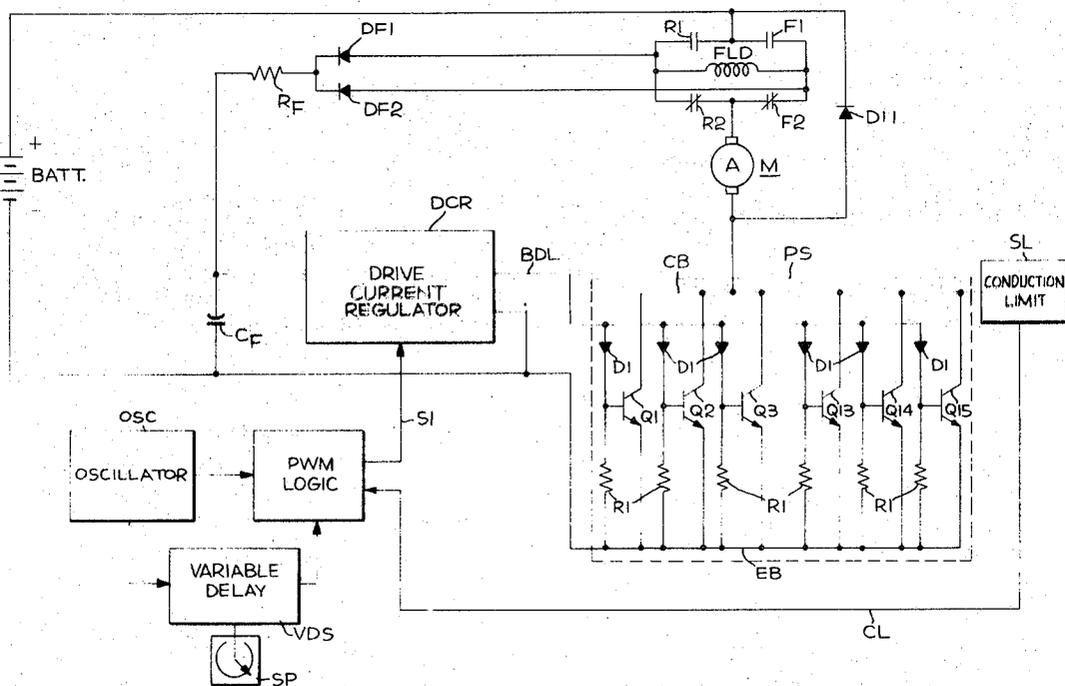
[58] Field of Search..... **318/341; 307/297**

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**21 Claims, 10 Drawing Figures**



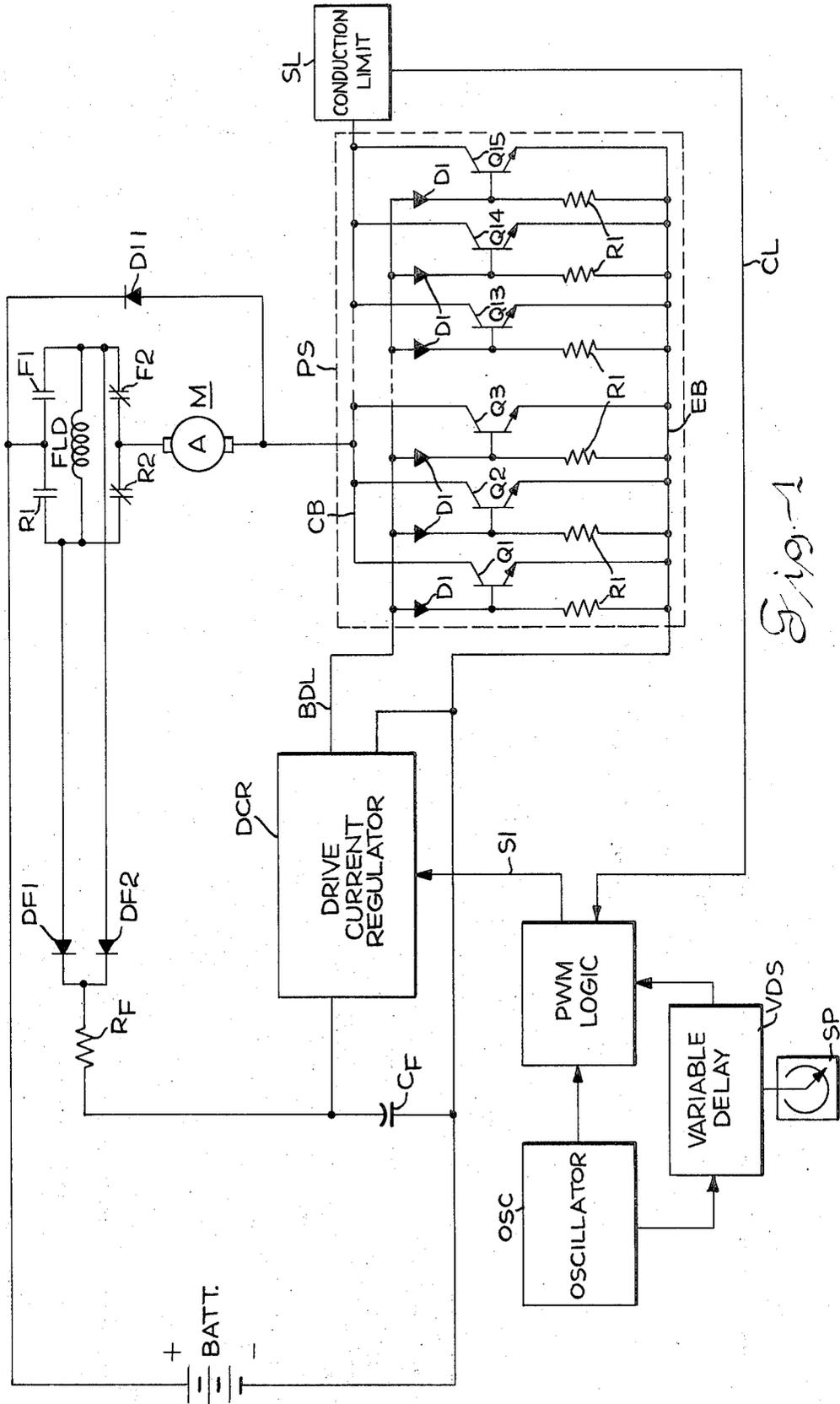


Fig. 1

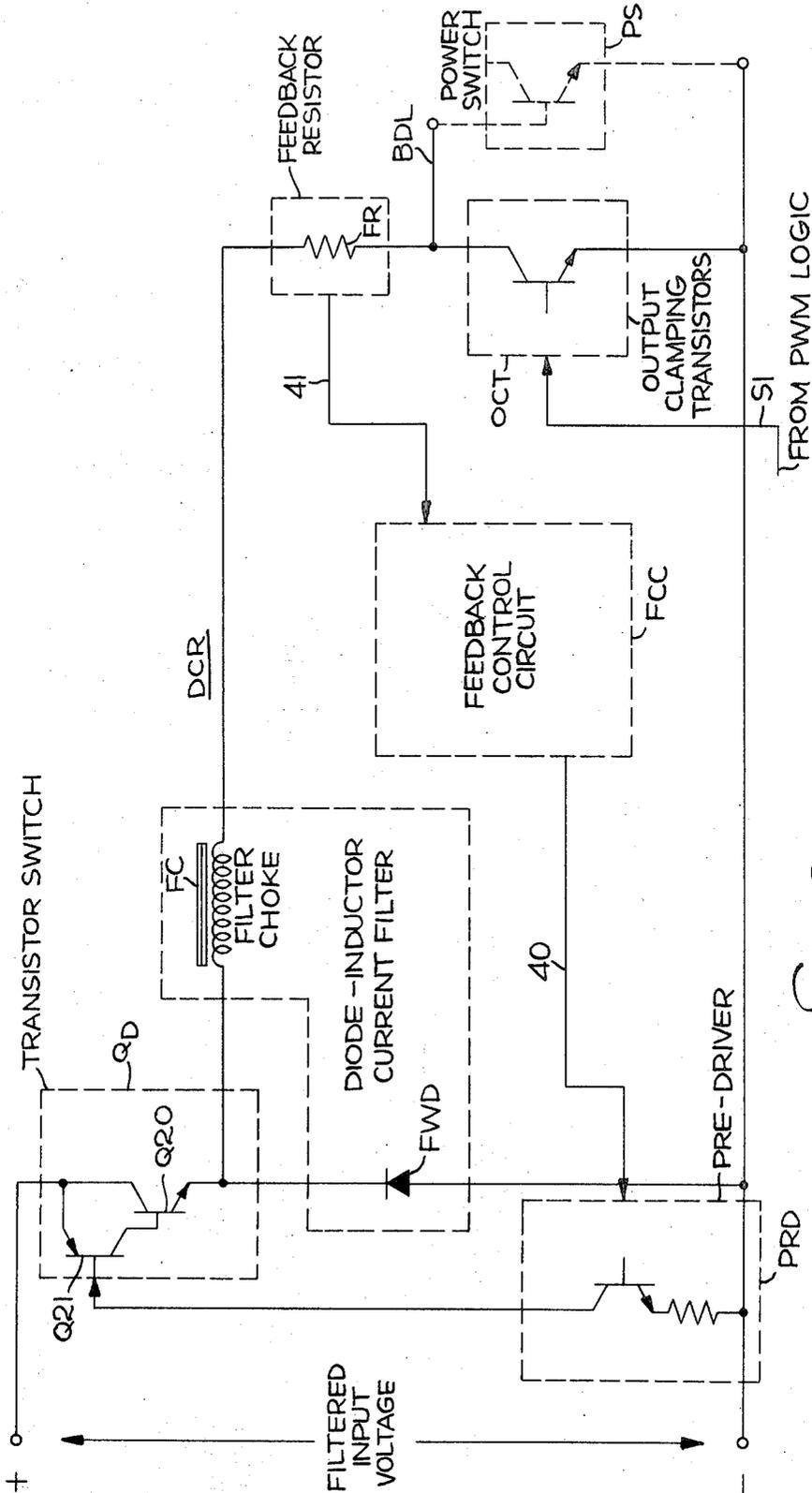


Fig. 2

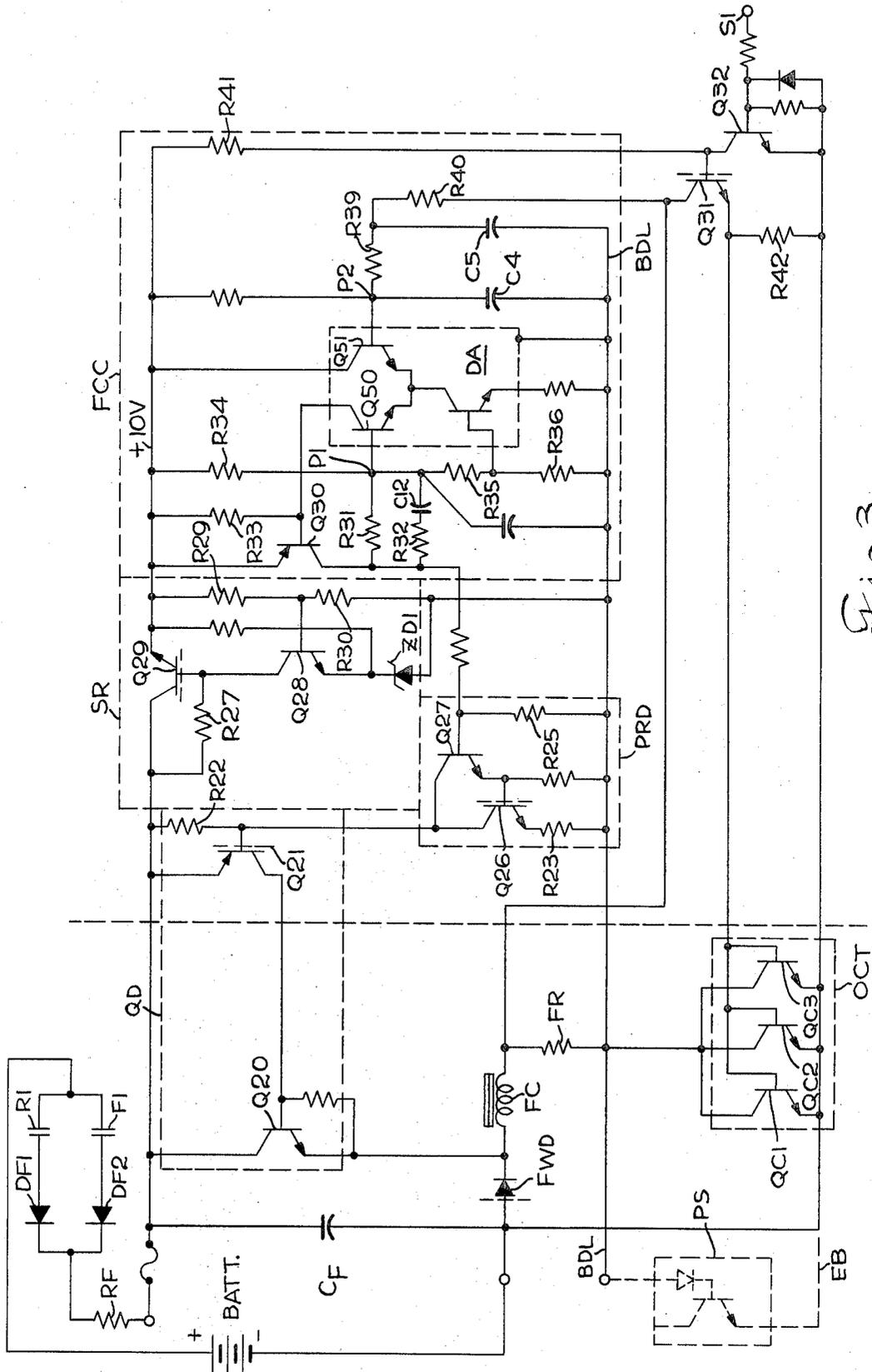


Fig. 3

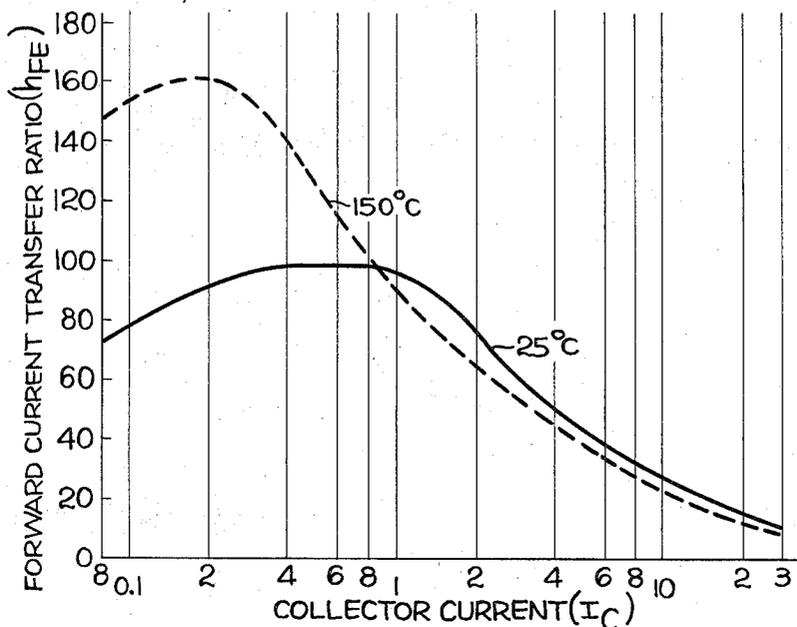


Fig. 4

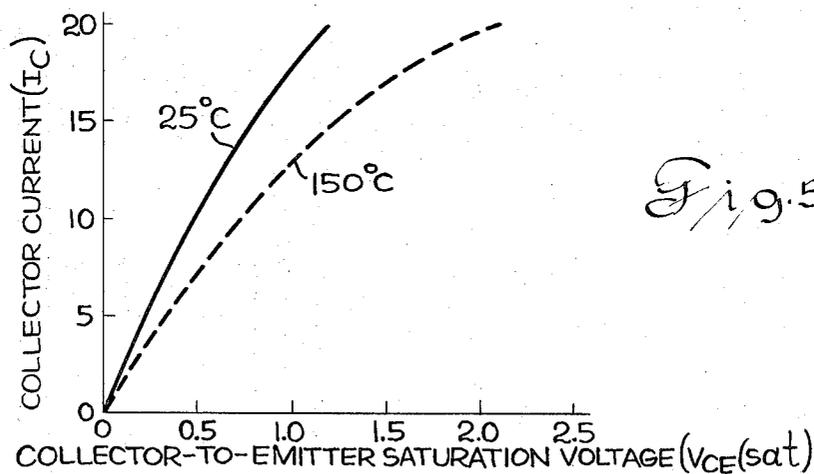


Fig. 5

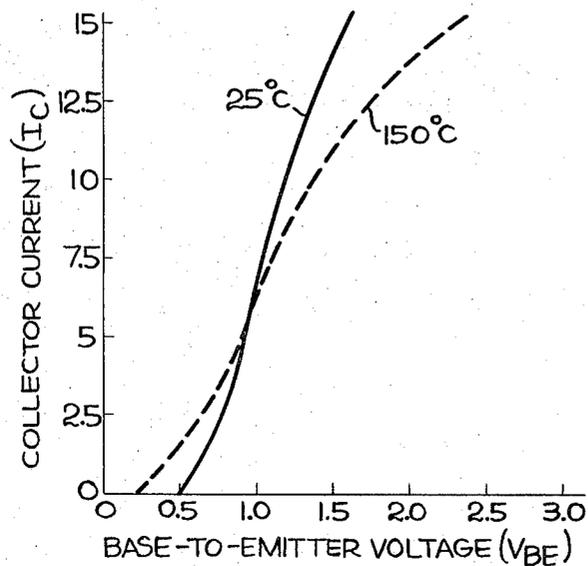


Fig. 6

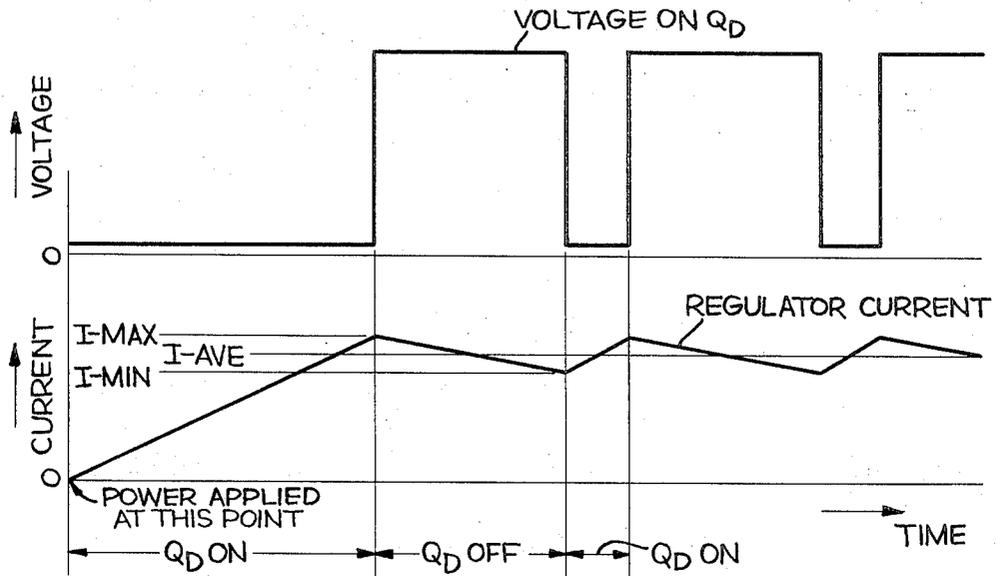


Fig. 7

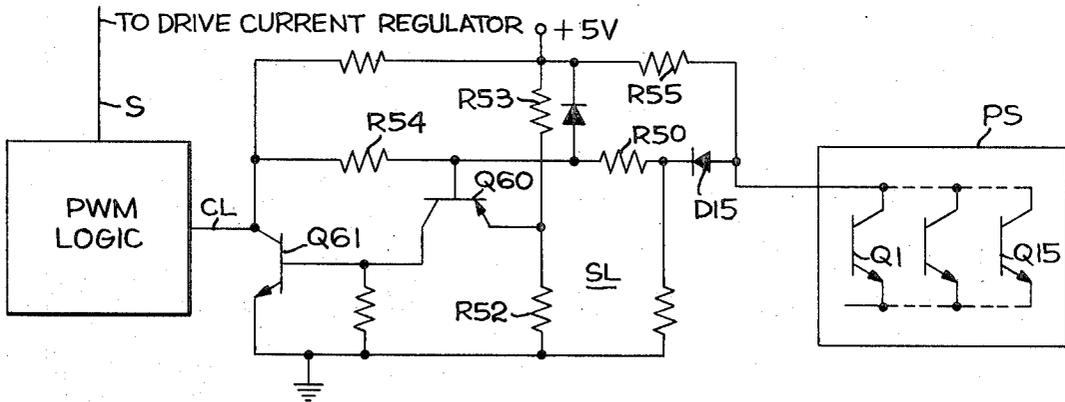


Fig. 8

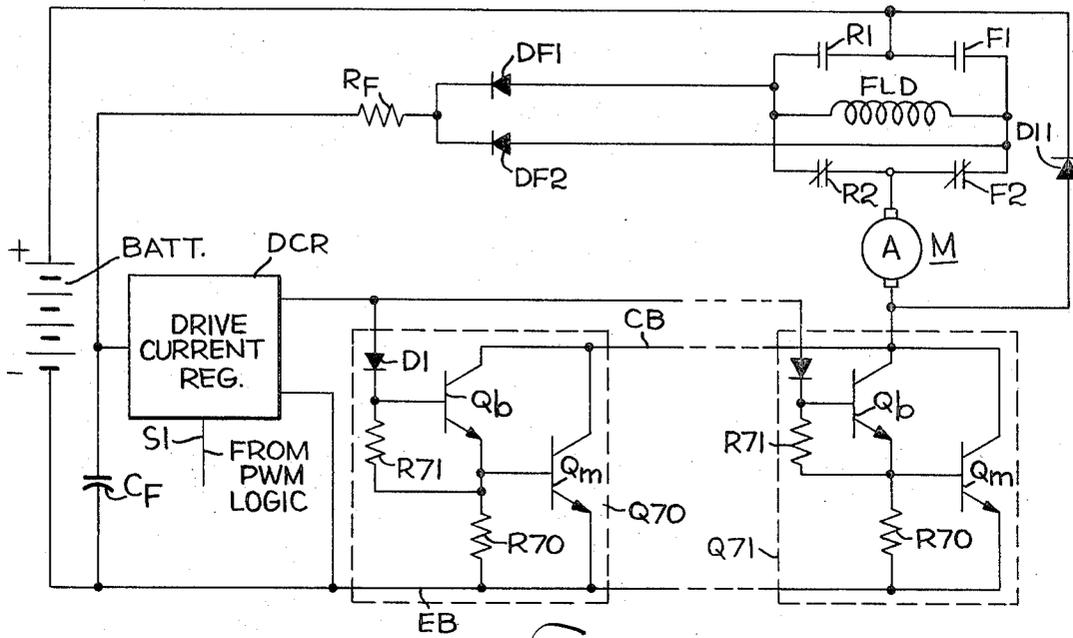


Fig. 9

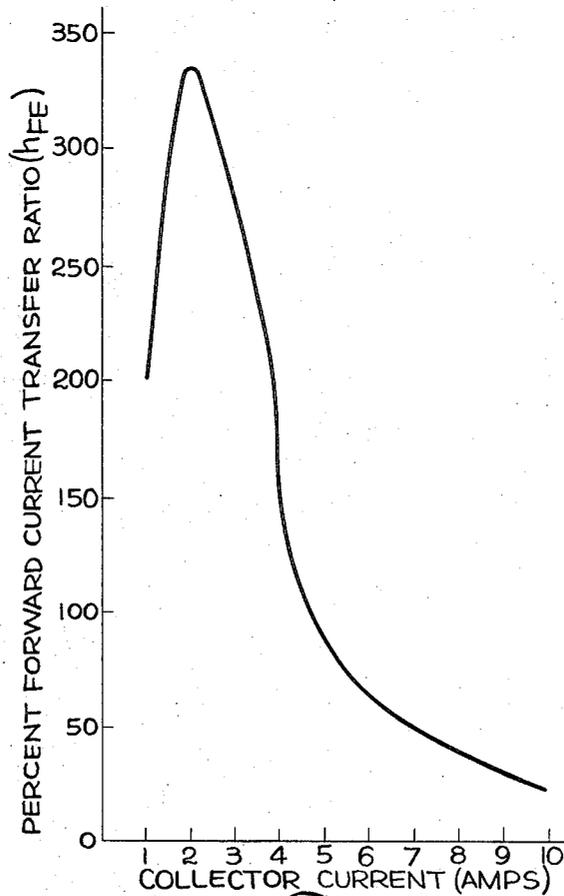


Fig. 10

## VARIABLE TIME RATIO CONTROL HAVING POWER SWITCH WHICH DOES NOT REQUIRE CURRENT EQUALIZING MEANS

This invention relates to variable time ratio controls and in particular to a power switch arrangement for a variable time ratio control such as a pulse width modulation control system for a D.C. traction motor used to propel a fork lift truck.

### BACKGROUND OF THE INVENTION

Pulse width modulation (PWM) controls for D.C. traction motors energized from a battery are known wherein a power switch of the germanium transistor type provides variable width pulses to the motor to vary the average voltage applied to the motor terminals. The torque demands of such a traction motor require switching of very high currents which makes it necessary to parallel power transistors to meet the required current level. Because of variation of the base-to-emitter voltage  $V_{BE}$  from transistor to transistor, the collector currents of the individual transistors of the paralleled combination can be quite different, and it has heretofore been necessary to match the transistors or use feedback resistors to compensate for variation between transistors. Emitter resistors are generally used for current equalization because they also provide thermal stability, and current equalization can be obtained with a base resistor having a value equal to that of the emitter resistor times the forward current gain  $h_{FE}$ .

Germanium transistors switch relatively slowly and suffer switching losses when rapidly switched which heat the transistors, and such switching losses in germanium power transistors have heretofore limited the frequency of switching in PWM motor control systems. Such relatively low switching frequency, necessitated because of switching losses in germanium power transistors, also limits the average current that can be supplied by the paralleled transistors to the motor. Failure of one transistor of a prior art paralleled transistor power switch often resulted in multiple transistor failure or necessitated turning off the power switch. When the base-emitter junction of one power transistor of a prior art power switch burned open, its base assumed the potential of the collector supply with the result that current could feedback through the shorted junction and burn out the remaining transistors.

### OBJECTS OF THE INVENTION

Accordingly, it is an object of the invention to avoid the above disadvantages of the prior art and provide a variable time ratio control having an improved power switch arrangement of paralleled transistors wherein external current equalizing means are not required to accomplish balanced collector currents in all of the transistors.

It is a further object of the invention to provide a variable time control having an improved paralleled transistor power switch arrangement wherein switching losses are low and which can be rapidly switched to increase the average current supplied to the load without increased heating of the transistors.

A still further object of the invention is to provide such a variable time ratio control having an improved paralleled transistor power switch arrangement wherein the burning out of a single transistor will not

cause multiple transistor failure or necessitate turning off the power switch.

### SUMMARY OF THE INVENTION

A variable time ratio control in accordance with the invention has a power switch comprising a plurality of paralleled power transistors whose forward current transfer ratio  $h_{FE}$  decreases abruptly with increase of collector current and whose base drive is supplied by a constant current switching regulator so that increase in collector current of one transistor decreases its gain to thereby promote current sharing between paralleled transistors. The constant current switching regulator is preferably coupled to the base of each power transistor by a diode whose forward drop increases with increase in base drive current to thereby promote base current sharing, and the diode blocks feedback of collector voltage in the event one transistor fails and thus prevents multiple transistor failure. The output of the switching regulator is across a plurality of output clamping transistors, and variable width pulses are coupled to the bases of the clamping transistors to shunt current away from the power transistors and thus turn the power switch off and on. In one embodiment the power transistors are of the single-diffused silicon type whose collector-to-emitter saturation voltage  $V_{CE}(\text{sat})$  and base-to-emitter voltage  $V_{BE}$  increase with increase in collector current to thereby further promote current equalization. In another embodiment each of the paralleled power transistors is in a Darlington circuit with a base driver transistor so that the forward current transfer ratio decreases much more steeply with increase of collector current to thereby further promote current sharing.

### DESCRIPTION OF THE DRAWINGS

These and other objects and advantages of the invention will be more readily apparent from the following detailed description when considered in conjunction with the accompanying drawings wherein:

FIG. 1 is a schematic diagram representing in block form a D.C. traction motor PWM control system incorporating a preferred embodiment of the invention;

FIG. 2 is a schematic diagram representing in block form the drive current regulator shown in FIG. 1;

FIG. 3 is a circuit diagram of the drive current regulator shown in FIGS. 1 and 2;

FIGS. 4, 5 and 6 are graphs showing characteristics of the single-diffused silicon power transistors of the embodiment of FIG. 1;

FIG. 7 represents the output current waveform from the drive current regulator and the voltage across the Darlington transistor switch;

FIG. 8 is a circuit diagram of the saturation voltage limit circuit which is shown in block form as in FIG. 1; and

FIG. 9 is a schematic diagram of a control incorporating an alternative embodiment of power switch having paralleled Darlington arrangements of power transistors and wherein current gain is not only an inverse function of collector current but also the current gain decreases much more steeply with increase of collector current than in the FIG. 1 embodiment.

### DETAILED DESCRIPTION

A preferred embodiment of the invention is represented in FIG. 1 which illustrates in block form a pulse

width modulation control for a D.C. series traction motor M having an armature A and a field winding FLD for driving the wheels of a fork lift truck (not shown). Armature A may be connected in series with field winding FLD and a power switch PS across the terminals of a battery BATT either through the contacts F1 of a forward contactor and R2 of a reverse contactor to drive the motor M in one direction to propel the fork lift truck forward or through the contacts R1 of the reverse contactor and F2 of the forward contactor to reverse the motor M and propel the fork lift truck to the rear. A diode D11 in parallel with the inductive motor path provides a circuit for the inductive motor current when power switch PS is turned off.

Motor M is energized by unidirectional pulses of current from battery BATT conducted by power switch PS, and the speed of motor M is regulated by a pulse width modulation system which controls the variable width pulses of voltage applied to motor M to proportionally vary the average voltage applied to motor M and includes an oscillator OSC shown in block form which produces a train of pulses that establish the frequency of the PWM system.

As disclosed in copending application Ser. No. 317,596 in the name of F. A. Stich filed Dec. 22, 1972 and having the same assignee as the invention each pulse from oscillator OSC may be coupled to a PWM LOGIC circuit shown in block form and set a bistable element (not shown) therein which provides an output pulse over a lead S1 to the drive current regulator DCR shown in block form to turn on power switch PS and thus initiate a variable width voltage pulse applied to motor M. Each pulse from oscillator OSC is also coupled to a variable delay circuit VDS shown in block form which is reset by the oscillator output pulse and subsequently produces an output pulse to PWM LOGIC circuit after a selectively variable time delay determined by the setting of a speed potentiometer SP whose wiper is controlled by a manually operated foot pedal (not shown) on the fork lift truck. The output pulse from variable delay circuit VDS resets the bistable element in the PWM LOGIC circuit which terminates the pulse to the drive current regulator DCR to turn off power switch PS. The "on-time" and the power duty cycle of power switch PS is thus controlled by the time delay of the variable delay circuit VDS and is a function of the position of the speed potentiometer SP.

### POWER SWITCH

Drive current regulator DCR is a constant current switching regulator that supplies constant base drive to power switch PS which comprises a plurality (preferably 15 for a 225 ampere power switch) of transistors Q1, Q2, Q3...Q15 of the single-diffused NPN silicon type such as are commercially available from RCA Corporation under the type designation 2N3771. Each transistor Q1-Q15 has its collector connected directly to a common collector bus CB that is coupled to one side of motor armature A and its emitter connected directly to an emitter bus EB which is coupled to one output terminal from drive current regulator DCR and to the negative terminal of battery BATT. The other output terminal from the drive current regulator is connected to a base drive lead BDL which is coupled through individual diodes D1 to the base of each power transistor Q1-Q15, and the base of each power transis-

tor Q1-Q15 is also coupled through a resistance R1 to the emitter bus EB.

The collector current levels of paralleled power transistors Q1-Q15 are substantially equal without the presence of current-sharing emitter resistors or other external current equalizing means utilized in prior art paralleled-transistor power switches. The amount of current each transistor will conduct is dependent upon its forward current transfer ratio, or current gain  $h_{FE}$ , its saturated collector-to-emitter drop  $V_{CE(sat)}$  and its base-to-emitter voltage drop  $V_{BE}$ . The current gain  $h_{FE}$  of a single-diffused silicon power transistors is a strong inverse function of collector current  $I_c$  and falls off very rapidly as collector current increases as shown in the representative  $I_c$  vs.  $h_{FE}$  curves illustrated in FIG. 4 and also falls off rapidly as junction temperature increases. Since the base drive supplied by drive current regulator DCR is constant, the collector current  $I_c$  becomes directly proportional to current gain  $h_{FE}$ . With  $h_{FE}$  decreasing as  $I_c$  increases, the point is rapidly reached where current gain is so small that collector current  $I_c$  cannot increase beyond a safe level. Because power transistors Q1-Q15 operate at high current densities, the current gains of these transistors are approximately inversely proportional to collector current, and this means that a spread between the forward current transfer ratios of  $n$ -to-1 would contribute a current spread of only approximately  $\sqrt{n}$ -to-1.

The base-to-emitter voltage drop  $V_{BE}$  and the collector-to-emitter saturated voltage drop  $V_{CE(sat)}$  of a single-diffused silicon transistor are both strong functions of collector current as illustrated in the representative  $I_c$  vs.  $V_{CE(sat)}$  curves of FIGS. 5 and 6 respectively. Thus, if one of the paralleled transistors Q1-Q15 has a higher gain than the others or is driven harder than the others due to base current unbalance, its  $V_{CE(sat)}$  and  $V_{BE}$  voltage drops will increase with collector current until a stable current balance is achieved among the plurality of paralleled transistors within the current handling capability of each transistor. Also the base-to-emitter voltage drops of such a single-diffused silicon transistor also increase as temperature increases, thereby further promoting stable operation and balanced collector currents in all of the paralleled transistors Q1-Q15.

The base drive to each transistor Q1-Q15 is through a diode D1 which further promotes base current sharing between paralleled transistors Q1-Q15 because of its current-voltage dependency, and diode D1 also prevents multiple transistor failure. The voltage drop across the internal impedance of each diode D1 increases in proportion to the base current flowing through it to the associated transistor, and since the base drive supplied by drive current regulator DCR is constant, the increase in voltage drop across each diode D1 with base current is in a direction to decrease the base current to the corresponding transistor and thus tend to equalize the base current levels of all the paralleled transistors Q1-Q15.

Each diode D1 isolates the associated transistor from the others so that if the transistor fails, the diode blocks the collector to base voltage  $V_{CB}$  from feeding back and burning out the other transistors as frequently occurred in prior art paralleled-transistor power switches. If a transistor burns out, its collector-to-base junction may short so that the base assumes the collector potential, but diode D1 prevents the collector voltage of such a failed transistor from feeding back and turning on (or

from burning out) the remaining paralleled transistors. Each diode D1 also provides an additional 0.60 volts of off-state voltage immunity so that power transistors Q1-Q15 will not be affected by the output voltage drop of drive current regulator DCR during the off-time of the power switch.

The resistors R1 are connected between base and emitter of each power transistor Q1-Q15 and provide bias for the power transistors in their off state.

A conduction limit, or saturation voltage limit circuit SL shown in block form in FIG. 1 senses the voltage drop across power switch PS and provides a signal over a lead CL to the PWM LOGIC circuit when power transistors Q1-Q15 began to pull out of saturation which terminates the pulse over lead S1 to drive current regulator DCR and turns power switch PS off. Since power switch PS pulls out of saturation at a magnitude of current below the maximum current carrying capabilities of transistors Q1-Q15, saturation limit circuit SL prevents excessive peak currents in the PWM control.

FIG. 9 schematically illustrates a variable time ratio control incorporating an alternative embodiment of power switch PS' wherein the forward current transfer ratio decreases much more steeply with increase of collector current than in the FIG. 1 embodiment. Power switch PS' has a plurality of paralleled Darlington arrangements of power transistors, only two Darlington circuits Q70 and Q71 being shown in FIG. 9. Each Darlington circuit Q70, Q71 includes a main power transistor  $Q_m$  having its emitter and collector connected respectively to emitter bus EB and the collector bus CB and a base drive power transistor  $Q_b$  whose emitter is connected to the base of main transistor  $Q_m$  and whose collector is connected to the collector bus CB. The emitter of each driver transistor  $Q_b$  is connected through a resistance R70 to emitter bus EB and its base is coupled through a resistance R71 to its emitter. FIG. 9 illustrates that drive current regulator DCR supplies constant base drive to the base of each drive transistor  $Q_b$  through a diode D1 which promotes base current sharing as described hereinbefore. Each Darlington circuit Q70, Q71 may be a NPN, triple-diffused Darlington power transistor unitary device of the type commercially available from the Delco Division of General Motors Corporation under the designation DTS-0730 wherein base drive transistor  $Q_b$  and main transistor  $Q_m$  are integral and in a unitary package with the base-emitter resistors. Alternatively each Darlington circuit Q70, Q71 may be a six-device Darlington unitary device of the type commercially available from RCA Corporation under the designation TA 8624-V2 or separate power transistors may be used for  $Q_m$  and  $Q_b$ .

Base drive source DCR provides substantially constant base drive current to the base of drive transistors  $Q_b$  so that the Darlington devices Q70, Q71 operate on the very steep portion of the  $h_{FE}$  vs.  $I_c$  characteristic shown in FIG. 10 wherein current gain decreases very steeply with increase of collector current. Because two amplifier stages are cascaded in a Darlington circuit, the forward current transfer ratios are approximately inversely proportioned to  $I_c^2$ , and this means that a spread of  $n$ -to-1 between forward current transfer ratios would contribute a collector current spread of approximately  $\sqrt{n}$ -to-1. The collector-to-emitter saturation voltage and the base-to-emitter voltage of the paralleled Darlington devices Q70, Q71 increase with in-

crease in collector current and are in a direction to promote current equalization between the paralleled power transistors of power switch PS'.

## DRIVE CURRENT REGULATOR

### General Description

Drive current regulator DCR supplies constant base drive to the paralleled power transistors Q1-Q15 of the FIG. 1 embodiment. A capacitor-resistor-diode filter, comprising a capacitor  $C_F$  in series with a resistor  $R_F$  and also with the parallel arrangement of two steering diodes DF1 and DF2, is coupled across the - and + terminals of battery BATT as shown in FIG. 1 and filters the battery voltage to remove ripples caused by switching of power switch PS and also provides a steering network so that the forward contactor when operated can energize regulator DCR through diode DF2 and the reverse contactor when operated can energize regulator DCR through diode DF1. Thus drive current regulator DCR is only connected to battery BATT when the forward or reverse contactor is operated, and consequently average power dissipation in the PWM control is reduced. The filter also reduces high frequency current flowing of the wiring of the fork lift truck.

Drive current regulator DCR is schematically represented in block form in FIG. 2 and includes a transistor switch  $Q_D$  comprising two transistors Q20 and Q21 connected in a complementary Darlington arrangement and in series with a free-wheeling diode FWD across the + and - terminals of battery BATT. A path in shunt to free-wheeling diode FWD includes the series arrangement of a filter choke, or inductor FG, a current feedback resistor RF, and a plurality of output clamping transistors OCT shown in block form in FIG. 2. The clamping transistors OCT are connected across the output terminals of drive current regulator DCR, and thus across base drive lead BDL to power switch PS and the negative terminal of battery BATT. Each time oscillator OSC generates an output pulse, the PWM LOGIC circuit supplies a signal over lead S1 to drive current regulator DCR which results in turning off the output clamping transistors OCT and turning on power transistors Q1-Q15 to initiate a variable width voltage pulse to motor M. When clamping transistors OCT are turned on, base current drive is shunted away from power switch PS. When the clamping transistors OCT are turned off, base current flows over lead BDL to the power transistors Q1-Q15 of power switch PS and turns them on.

Complementary Darlington transistor switch  $Q_D$  provides the high current switching for regulator DCR, and when it is turned on current flows from the + terminal of battery BATT through filter choke FC and the current feedback resistor FR to the - terminal of battery BATT through either conducting clamping transistors OCT or through power switch PS. When the Darlington transistor switch  $Q_D$  turns off, filter choke FC causes current to continue to flow through feedback resistor FR, clamping transistors OCT or power switch PS, and free-wheeling diode FWD in series.

A constant current pre-driver stage PRD shown in block form in FIG. 2 supplies base drive to the Darlington switch  $Q_D$  so that the drive current will not vary with changes in battery voltage, and the pre-driver stage PRD is controlled by signals over a lead 40 from a feedback control circuit FCC shown in block form in FIG. 2. Feedback control circuit FCC detects the mag-

nitude of output current from drive current regulator DCR by sensing the voltage developed across feedback resistor FR and provides the proper switching and duty cycle signals over lead 40 to the pre-driven stage PRD to regulate output current from regulator DCR at a constant value.

#### Operation

Closed loop feedback control of the magnitude of output current from drive current regulator DCR is accomplished by controlling the ratio of the on-time to the off-time of Darlington transistor switch  $Q_D$ . When a forward contactor or a reverse contactor is initially operated, no output current from the regulator is flowing through feedback resistor FR, and feedback control circuit FCC supplies signals over lead 40 to turn on pre-driver stage PRD and thus turn on Darlington transistor switch  $Q_D$ . Conduction by switch  $Q_D$  applies battery voltage across filter choke FC so that current begins to build up in filter choke FC until it reaches the upper current level  $I_{max}$  shown in FIG. 7 preset in feedback control circuit FCC. At this point, feedback control circuit FCC senses that regulator output current flowing through feedback resistor FR has reached the upper level  $I_{max}$  and applies a signal over lead 40 which turns off the pre-driver stage PRD and thus turns off Darlington switch  $Q_D$ . Filter choke FC tends to keep current flowing in the path through free-wheeling diode FWD, which decays in magnitude when transistor switch  $Q_D$  is off until the feedback control FCC senses that this regulator output current through feedback resistor FR has reached lower current level  $I_{min}$  shown in FIG. 7, and feedback control circuit FCC then supplies a signal over lead 40 to turn on pre-driver stage PRD and thus turn on Darlington switch  $Q_D$ . Turning on Darlington transistor switch  $Q_D$  causes regulator output current to build up again to the upper current level  $I_{max}$  at which time feedback control circuit FCC supplies a signal over lead 40 that shuts off pre-driver stage PRD and Darlington switch  $Q_D$ . This cycle continues, and feedback control FCC continuously monitors regulator output current flowing through feedback resistor FR and varies the switching frequency and duty cycle of transistor switch  $Q_D$  to maintain constant output current from drive current regulator DCR. The difference in upper and lower current levels  $I_{max}$  and  $I_{min}$  is known as hysteresis and is reflected as a ripple in the output current waveform shown in FIG. 7.

The 300 Hz frequency output from drive current regulator DCR which cyclically turns power switch PS on and off is considerably higher than that of prior art PWM motor control systems, and such higher frequency results in a substantial increase in average current delivered to motor M for the reason that the current does not decay during off time to as low a magnitude  $I_{min}$  as occurred in prior art lower frequency PWM systems. Further, the power loss in switching transistors Q1-Q15 turning on and off at the higher frequency of 300 cycles per second is not increased materially in comparison to prior art PWM motor controls because of the faster switching characteristics of silicon transistors in comparison to the germanium transistors used in known PWM controls.

#### Detailed Description

Referring to FIG. 3, the complementary Darlington transistor switch  $Q_D$  comprises a NPN main current switching transistor Q20 whose base is coupled to the collector of a PNP driver transistor Q21 which provides

base drive current to main transistor Q20. The collector of main current switching transistor Q20 is coupled to the + terminal of battery BATT through the capacitor-resistor-diode filter CF, RF, DF1-DF2 and the emitter of main transistor Q20 is coupled through free-wheeling diode FWD to the - terminal of battery BATT and is also coupled to one side of filter choke FC. The other side of filter choke FC is connected through current feedback resistor FR to the commoned collectors of output clamping transistors OCT (shown with a dotted line rectangle as including three NPN transistors, QC1, QC2 and QC3) and is also connected to base drive lead BDL to power switch PS. The emitters of the three paralleled output clamping transistors QC1, QC2 and QC3 are commoned and coupled to the - terminal of the battery BATT. Each clamping transistor QC1, QC2 and QC3 carries only relatively low current so that its  $V_{CE(sat)}$  voltage drop is very low, and this keeps the power switch transistors Q1-Q15 well into the cutoff region during off-time of the power switch.

Feedback resistor FR develops a voltage signal on lead 41 proportional to the magnitude of regulator output current flowing therethrough, and this signal is an input over lead 41 to feedback control circuit FCC as described hereinafter. A normally conducting transistor Q31 has its emitter connected to the commoned bases of output clamping transistors QC1, QC2 and QC3 and provides base drive thereto. Feedback resistor FR acts as a collector resistor in a saturated Darlington arrangement for the output clamping transistors QC1, QC2 and QC3. Feedback resistor FR permits the output clamping transistor OCT to operate in saturation and the regulator output voltage to be very low since it is developed across the parallel collector-emitter circuits of three saturated transistors. Base drive to normally conducting transistor Q31 is provided through a resistance R41 which is connected to a regulated +10 volt source described hereinafter so that the base drive for Q31 is independent of changes in battery voltage.

Output clamping transistors QC1, QC2 and QC3 are switched on and off at the 300 Hz output frequency of oscillator OSC and control switching by power transistors Q1-Q15. When power switch PS is to be turned on, a pulse over lead S1 from PWM LOGIC circuit turns on a transistor Q32 which clamps the base of NPN drive transistor Q31 to the - terminal of battery BATT to turn off drive transistor Q31. Turning off transistor Q31 diminishes flow of current through emitter resistance R42 and thus decreases the potential at the commoned bases of clamping transistors QC1, QC2 and QC3 to turn them off and thereby permit base drive current to flow over lead BDL to power switch PS and turn it on. Since power switch PS is only turned on when a pulse is received over lead S1 to turn off drive transistor Q31, it will be appreciated that if lead S1 is accidentally opened or grounded, transistor Q31 will conduct and thereby forward bias clamping transistors QC1, QC2 and QC3 and thus turn off power switch PS.

A series feedback regulator SR shown within a dotted line rectangle in FIG. 3 maintains a constant potential of 10 volts between a lead designated +10V and lead BDL and includes a series transistor Q29 which absorbs battery voltage changes having its collector connected to the + terminal of battery BATT, a reference Zener

diode ZD1, a control resistor R27, a voltage divider comprising two resistances R29 and R30 connected in series across the output of the regulator, and a control transistor Q28 which compares the reference voltage across Zener diode ZD1 with a portion of the regulator output voltage across resistance R30 and varies the control current through control resistor R27 and the base drive to series transistor Q29 in a direction to maintain regulator output voltage constant.

The negative side of the regulated voltage supply SR on lead BDL is connected through clamping transistors OCT to the - terminal of battery BATT so that it shifts in potential relative to the - terminal of battery BATT (while the 10 volt supply is kept constant) depending upon whether the clamping transistors QC1, QC2 and QC3 are on or off.

Constant drive current for transistor switch  $Q_D$  regardless of the voltage level of battery BATT is provided by a pre-drive stage PRD including the Darlington arrangement of a main transistor Q26 and a driver transistor Q27 for Q26. The collector of main transistor Q26 is connected to the base of drive transistor Q21 of transistor switch  $Q_D$  and also to the + terminal of battery BATT through a collector resistor R22, and the emitter of transistor Q26 is connected to the - terminal of battery BATT through the series arrangement of an emitter resistor R23, feedback resistor FR, filter choke FC and free-wheeling diode FWD. The base of pre-driver main transistor Q26 is connected to the emitter of driver transistor Q27 whose base is set at a 5 volt level. Four resistors R25, R26, R31 and R34 are connected in series across the output terminals of the regulated 10 volt supply POW to form a voltage divider, and the base of driver transistor Q27 is connected to the junction of resistors R25 and R26 which is set at 5 volts. The magnitude of current flowing through the emitter-collector circuit of pre-driver main transistor Q26 is thus determined by the value of emitter resistance R23. Once the current in main transistor Q26 builds up to the point where the voltage drop across resistance R23 plus the serial base-emitter drops of transistors Q26 and Q27 equal the 5 volt signal applied to the base of transistor Q27, main transistor Q26 will limit current by pulling out of saturation, thereby assuring relatively constant base drive to complementary Darlington transistor switch  $Q_D$  regardless of changes in battery voltage.

Feedback control circuit FCC shown within a dotted line rectangle in FIG. 3 includes a differential amplifier DA which on one input P1 receives a reference potential of 5 volts set on a voltage divider comprising resistance R34 in series with two resistances R35 and R36 across the regulated 10 volt supply. The other input P2 to differential amplifier DA is a signal proportional to regulator output current flowing through feedback resistor FR and appearing on lead 41. The voltage signal proportional to regulator current appearing on lead 41 increases in a positive direction relative to the negative side of regulated supply SR (at lead BOL) and is coupled to differential amplifier input P2 through a resistance R40 and a high frequency, noise-removing pi filter comprising two capacitors C4 and C5 and a resistance R39.

When the current feedback voltage signal on lead 41 applied to input P2 is lower than the 5 volt reference signal applied to input P1, a transistor Q50 of differential amplifier DA conducts, and the resulting voltage

drop across its collector resistance R33 is coupled to the base of an PNP output transistor Q30 and turns it on. Conduction by transistor Q30 clamps the junction between resistances R26 and R31 to the +10V lead to thereby raise the potential on lead 40 at the base of pre-driver stage NPN transistor Q27, thereby turning on the pre-drive stage PRD and thus turning on Darlington transistor switch  $Q_D$  to start the flow of regulator current. As regulator current increases, the voltage drop across feedback resistor FR appearing on lead 41 increases until the upper current level  $I_{max}$  is reached when the input voltage at differential amplifier input P2 equals the reference voltage on input P1. At this point transistor Q50 is turned off and transistor Q51 of differential amplifier DA is turned on with the result that output transistor Q30 becomes reverse biased and turns off, thereby turning off pre-driver stage PRD and transistor switch  $Q_D$ . Regulator current and the voltage drop across feedback resistor FR then decay until the power level  $I_{min}$  shown in FIG. 7 is reached when the voltage on differential amplifier input P2 is again sufficiently low to reverse bias transistor Q51 and to turn on transistor Q50, thereby turning on output transistor Q30, pre-driver stage PRD, and transistor switch  $Q_D$ .

Resistor R31 connected between differential amplifier input P1 and the collector of output transistor Q30 provides hysteresis. Conduction by transistor Q30 clamps one side of resistance R31 to the +10V lead and results in current flow through resistance R31 which forces the voltage at input P1 to become slightly more positive, thereby introducing positive feedback and causing feedback control circuit FCC to switch very rapidly. Further, the series arrangement of a resistance R32 and a capacitor C12 connected between input P1 and the collector of transistor Q30 applies a transient spike to input P1 when transistor Q30 conducts which forces the voltage at input P1 in a direction to momentarily further forward bias the base of Q30 and thereby assure rapid switching. When output transistor Q30 turns off, its collector is coupled through relatively low resistances R25 and R26 to the negative side of the regulated supply with the result that input P1 is forced to a voltage slightly below the 5 volt D.C. reference level and thereby causes transistor Q30 to switch off rapidly.

Such change of voltage caused by current flow through resistance R31 produces a square wave at input P1 superimposed upon the D.C. reference level and results in hysteresis and ripple current in the regulator output current waveform. Capacitor C12 and resistance R2 also result in a transient spike overshoot at input P1 when transistor Q30 turns off which is in the direction to further reverse bias the base of transistor Q30 and thus cause it to turn off rapidly.

#### Saturation Voltage Limit Circuit

The saturation voltage limit circuit SL shown in block form in FIG. 1 and in detail in FIG. 8 monitors the voltage drop across transistor Q1-Q15 of power switch PS and provides a logic 1 voltage signal at all times over lead CL to the PWM LOGIC circuit except when power switch PS is saturated, at which time it provides logic 0 voltage on lead CL to the PWM LOGIC circuit which terminates the pulse over lead S1 to drive current regulator DCR and turn off power switch PS.

When transistors Q1-Q15 of power switch PS are saturated, their collector voltage is low and is coupled

through a diode D15 and a resistance R50 to the base of a PNP transistor Q60 which is forward biased and remains conducting to hold a transistor Q61 on and provide logic 0 on lead C6 to the PWM LOGIC circuit. The emitter of transistor Q61 is connected to ground and its collector is connected to lead CL so that lead CL is at logic 0 voltage when transistor Q61 conducts. The emitter of transistor Q60 is coupled to the junction of two resistances R52 and R53 which are connected in series between a +5 volt source and ground so that the emitter of Q60 is biased between +5V and ground. When the power switch transistors Q1-Q15 pull out of saturation to the point where their collector voltage minus the forward drop of diode D15 equals the voltage on the emitter of transistor Q60 minus its base-emitter drop, transistor Q60 becomes reverse biased and turns off, thereby turning transistor Q61 off so that its collector voltage increases to provide logic 1 on lead CL to PWM LOGIC circuit which turns off power switch PS. Positive feedback from the collector of transistor Q61 through a resistance R54 to the base of transistor Q60 is provided to assure quick switching.

When power switch PS is turned off, the positive +5V source is coupled through a resistance R55, diode D15, and resistor R50 to reverse bias transistor Q60 and thus hold transistors Q60 and Q61 off and maintain logic 1 on lead CL. Further, if the connection from power switch PS to saturation voltage limit circuit SL is accidentally opened, the base of transistor Q60 is reversed biased from the +5V source through R55, D15 and R50 to maintain transistor Q60 and Q61 off and logic 1 on lead CL so power switch transistors Q1-Q15 remain off.

When only two embodiments of our invention have been illustrated and described, it should be understood that we do not intend to be limited to these embodiments for many modifications and variations thereof will be obvious to those skilled in the art.

The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows:

1. A control for supplying variable time ratio pulses from an electrical source to a load including, in combination,

a power switch between said source and said load having a plurality of paralleled power transistors with commoned collectors and commoned emitters, each said power transistor having a forward current transfer ratio characteristic with a portion wherein said ratio decreases abruptly with increase in collector current,

a substantially constant current base drive source for said power switch coupled to the base of each of said power transistors and providing substantially constant current output sufficient to cause each of said power transistors to operate on said portion of said characteristic wherein said forward current transfer ratio decreases abruptly with increase in collector current, and

means for periodically removing said base drive source to selectively vary the time ratio of pulses from said electrical source supplies by said power switch to said load,

whereby external current equalization means are not required to balance the collector current levels in said plurality of paralleled power transistors.

2. A control in accordance with claim 1 wherein each of said power transistors is in a Darlington circuit with a base drive transistor and said base drive source is coupled to the base of said base drive transistor.

3. A control in accordance with claim 1 and including a plurality of diodes each of which couples said base drive source to the base of one of said power transistors.

4. A control in accordance with claim 1 wherein each of said power transistors is of the single-diffused silicon type.

5. A control in accordance with claim 1 wherein each of said power transistors has a characteristic wherein collector-to-emitter saturation voltage increases with increase in collector current.

6. A control in accordance with claim 1 wherein each of said power transistors has a characteristic wherein base-to-emitter voltage increases with increase in collector current.

7. A control in accordance with claim 3 wherein each of said power transistors has a characteristic wherein collector-to-emitter saturation voltage increases with increase in collector current and also has a characteristic wherein base-to-emitter voltage increases with increase in collector current.

8. A control in accordance with claim 1 wherein the emitter-collector circuit of a clamping transistor is in shunt to the output of said base drive source, and said means for periodically removing said base drive source includes means for applying variable time ratio pulses to the base of said clamping transistor to shunt current away from said power transistors and thereby turn them off.

9. A control in accordance with claim 8 wherein said base drive source includes a plurality of clamping transistors having commoned emitters, commoned bases and commoned collectors connected in shunt to the output of said drive source, said means for applying variable time ratio pulses is coupled to the commoned bases of said plurality of clamping transistors, and said base drive source also includes a transistor switch, a filter choke in a series circuit with said transistor switch and also with said plurality of clamping transistors, means for detecting the magnitude of current flowing in said series circuit, and duty cycle varying means responsive to said current detecting means for controlling said transistor switch to maintain the magnitude of current flowing in said series circuit substantially constant.

10. A control in accordance with claim 2 wherein each said power transistor is a unitary Darlington device having said base drive transistor integral therewith.

11. A control in accordance with claim 10 wherein each power transistor is a triple-diffused silicon Darlington power transistor.

12. A control in accordance with claim 2 wherein each said power transistor has a collector-to-emitter saturation voltage characteristic which increases with increase in collector current and also has a base-to-emitter voltage characteristic which increases with increase in collector current.

13. A control in accordance with claim 12 and including a plurality of diodes each of which couples said base drive source to the base of one of said base drive transistors.

14. A control for supplying variable time ratio pulses from an electrical source to a load including, in combination,

a power switch between said source and said load having a plurality of paralleled power transistors with commoned collectors and commoned emitters, each said power transistor having a forward current ratio characteristic with a portion wherein said ratio decreases abruptly with increase in collector current,

a switching current regulator coupled to the base of each of said power transistors and including a transistor switch, output transistor clamping means, an inductor in a series circuit with said transistor switch and said output transistor clamping means, means for varying the duty cycle of said transistor switch to maintain substantially constant current output from said regulator sufficient to cause each of said power transistors to operate on said portion of said characteristic wherein said ratio decreases abruptly with increase in collector current, and means for periodically applying variable time ratio pulses to the base of said output transistor clamping means to shunt current away from said power switch and thereby turn it off.

15. A control in accordance with claim 14 wherein each of said power transistors is in a Darlington circuit with a base drive transistor and said switching current regulator is coupled to the base of said base drive transistor.

16. A control in accordance with claim 15 wherein each said power transistor is a unitary Darlington device having said base driver transistor integral therewith.

17. A control in accordance with claim 14 and in-

cluding a plurality of diodes each of which is connected between said switching current regulator and the base of one of said power transistors.

18. A control in accordance with claim 14 wherein each of said power transistors is of the single-diffused silicon type which has a collector-to-emitter saturated voltage characteristic that increases with increase in collector current and also has a base-to-emitter voltage characteristic which increases with increase in collector current.

19. A control in accordance with claim 14 wherein each of said power transistors has a collector-to-emitter saturated voltage characteristic which increases with increase in collector current.

20. A control in accordance with claim 14 wherein said transistor switch is of the complementary Darlington configuration including a main transistor and a driver transistor and said switching regulator also includes a constant current pre-driver stage coupled to the base of said driver transistor.

21. A control in accordance with claim 20 wherein said output transistor clamping means includes a plurality of paralleled clamping transistors having commoned bases, commoned collectors and commoned emitters, and wherein said means for varying the duty cycle of said transistor switch includes feedback impedance means in said series circuit for deriving a feedback signal which is a function of the magnitude of current flowing in said series circuit, means for deriving a reference voltage signal, and differential amplifier means responsive to said feedback and reference signals for controlling said pre-driver stage to maintain the magnitude of current flowing in said series circuit substantially constant.

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UNITED STATES PATENT OFFICE  
CERTIFICATE OF CORRECTION

Patent No. 3,803,471 Dated April 9, 1974

Inventor(s) Raymond G. Price, Frederick A. Stich, and David L. Moore

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 11, line 62, "supplies" should read --- supplied ---.

Signed and sealed this 10th day of September 1974.

(SEAL)  
Attest:

MCCOY M. GIBSON, JR.  
Attesting Officer

C. MARSHALL DANN  
Commissioner of Patents

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