United States Patent [19]

Apitz

[11] **3,710,081**

[45] **Jan. 9, 1973**

[54] SYSTEM FOR COMPUTING THE AVERAGE OF SUCCESSIVE TRAFFIC MEASUREMENTS

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[22] Filed: **June 14, 1971**

[21] Appl. No.: **152,789**

[52] **U.S. Cl.**.....**235/150.24**, 235/92 TC, 340/31 A, 340/38 R, 343/112 TC

[51] **Int. Cl.**.....**G06f 15/48**

[58] **Field of Search**.....235/150.2, 150.24, 92 TC; 340/31 R, 31 A, 38 R, 39; 343/8, 112 TC; 307/220, 226

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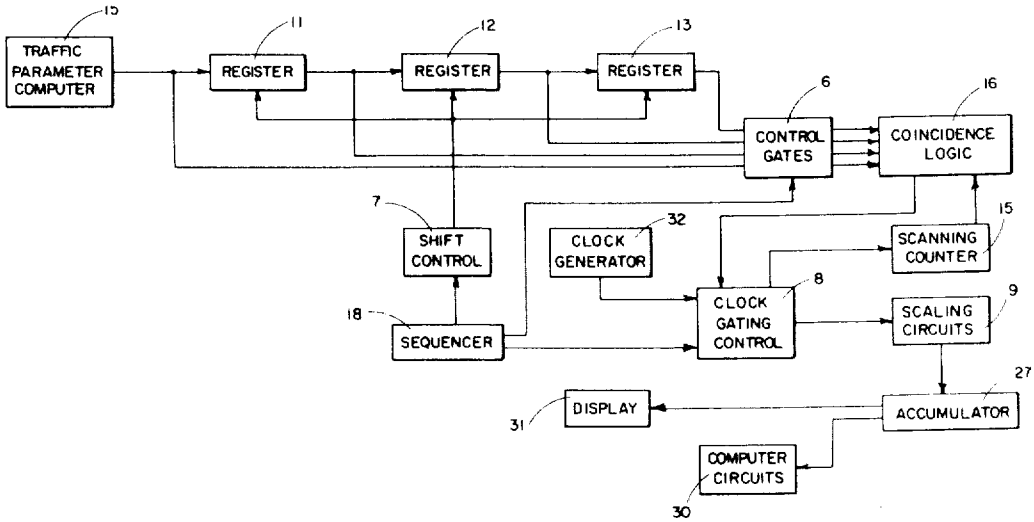
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[57] **ABSTRACT**

Successive samplings of digital signals representing traffic measurements are fed to a first digital register, the signals in this first register being shifted into second and third registers as each successive sampling is received. The input signals as they appear and the signals in each register are sequentially scanned with a scanning counter to produce a pulse output in accordance with the numerical value of the signal at the input and that of each of the registers. These signals are appropriately scaled by a factor in accordance with the number of samplings taken to produce a signal in accordance with an average of these samplings, this pulse count being accumulated in an accumulator. The signal in the accumulator, which represents the average of each last group of successive samplings evaluated, is continually updated to include each newly arriving input sampling, with the oldest sampling being dropped from the computation. The signal in the accumulator is fed to computer circuits or to a display for appropriate utilization.

9 Claims, 4 Drawing Figures



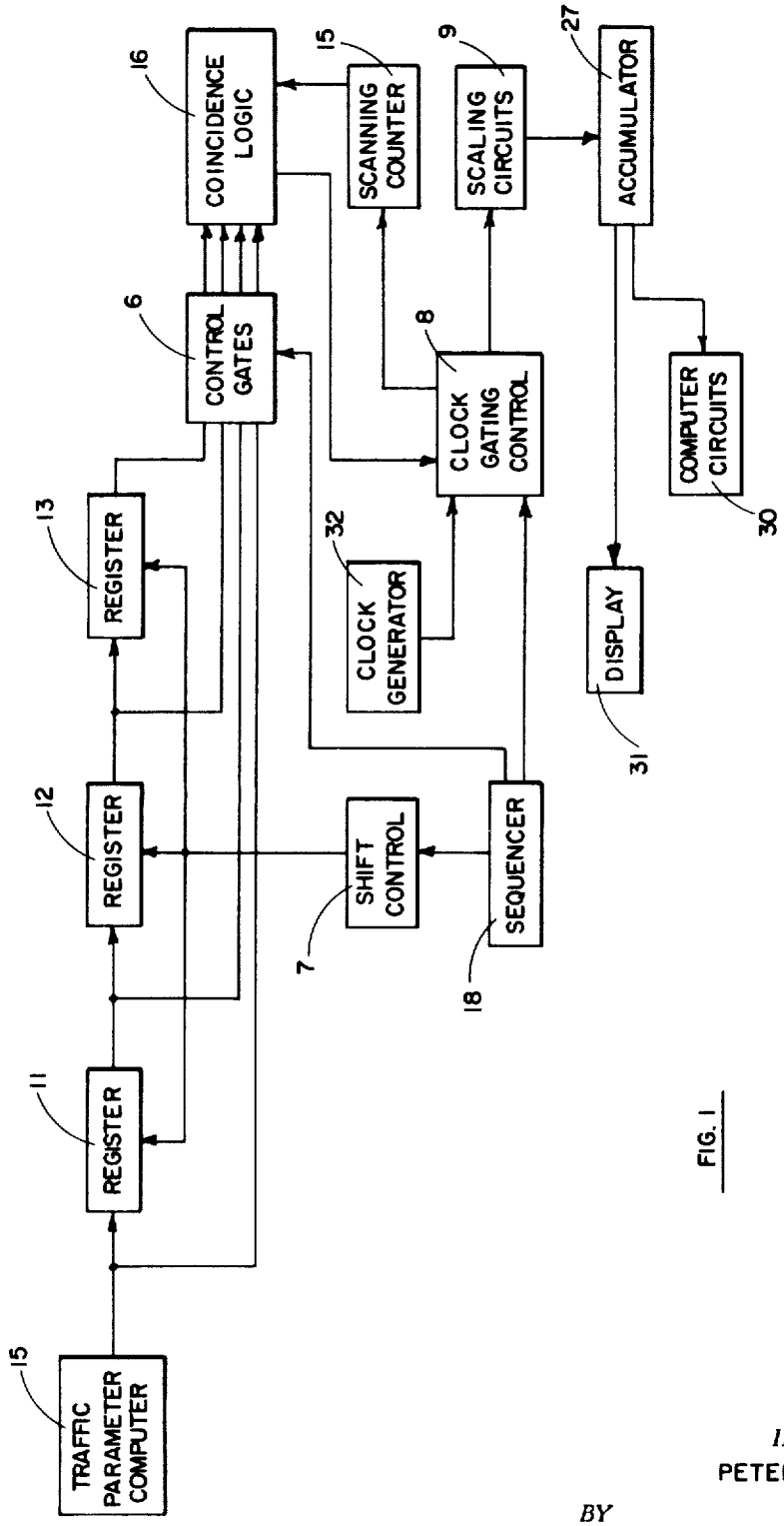


FIG. 1

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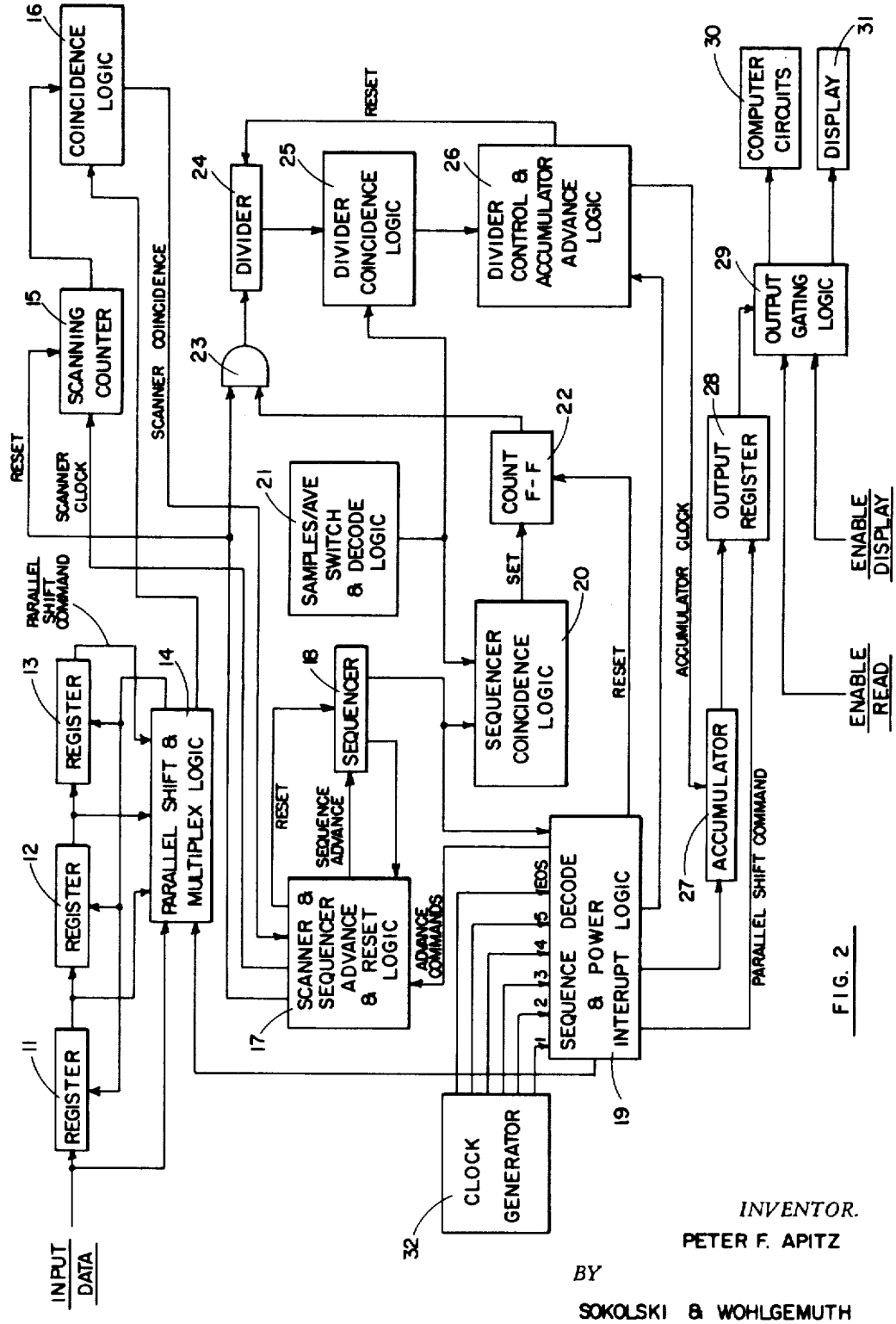


FIG. 2

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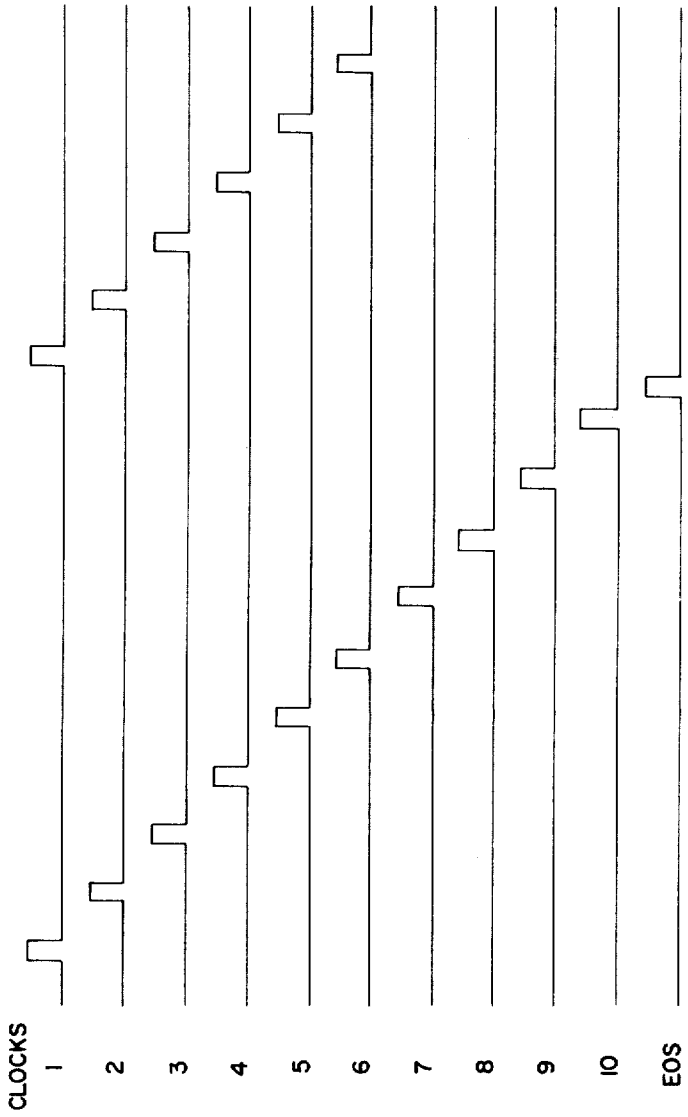


FIG.3

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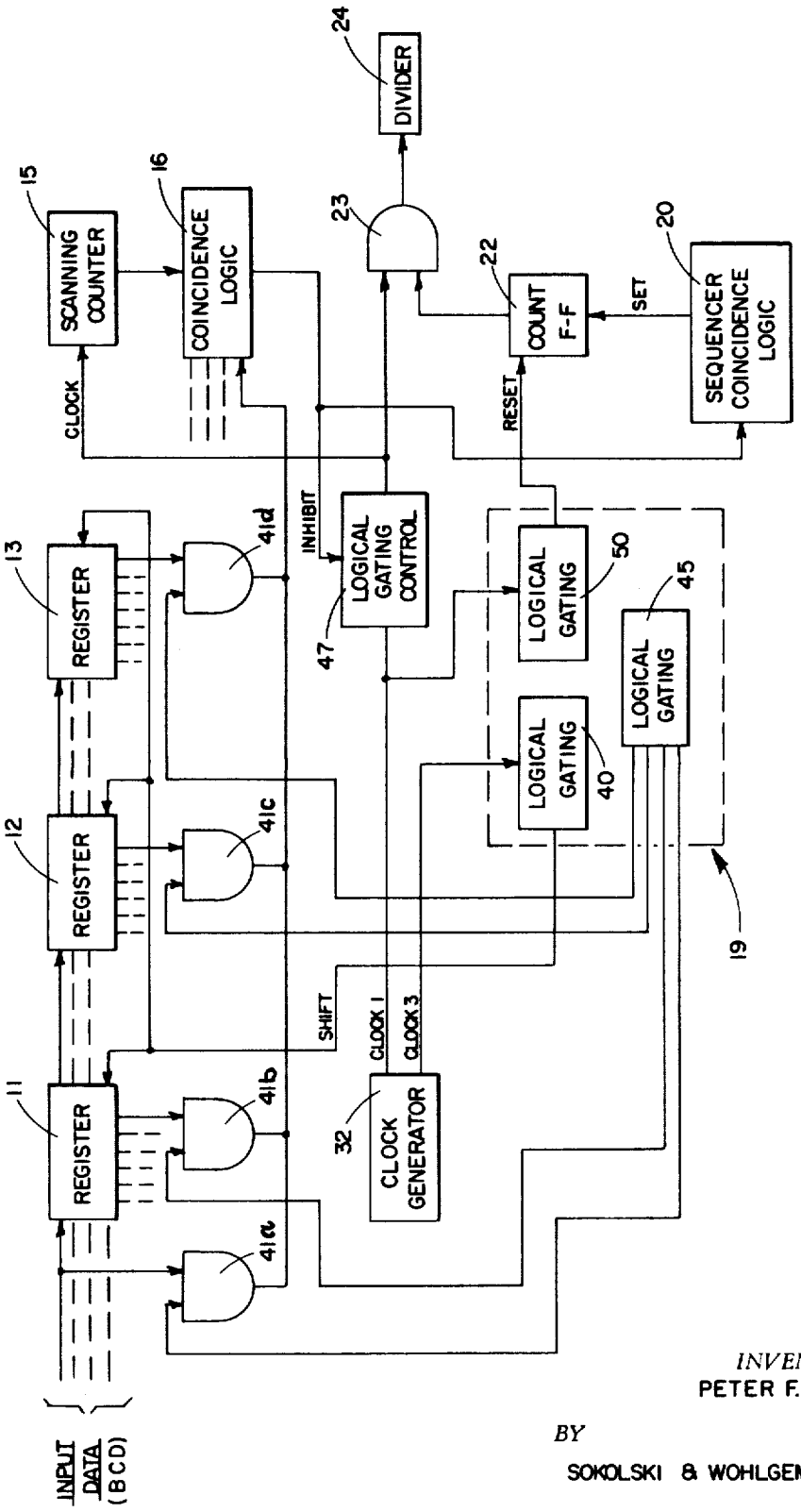


FIG. 4

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SYSTEM FOR COMPUTING THE AVERAGE OF SUCCESSIVE TRAFFIC MEASUREMENTS

This invention relates to traffic control computers, and more particularly to a system for digitally computing the average of a predetermined number of immediately preceding traffic measurements.

In making traffic control measurements, there often are disadvantages in responding to abrupt changes in traffic conditions which might be indicated by a single relatively short term measurement of traffic conditions. This is because a single sampling may not reflect a true traffic trend but may only indicate a very limited short term change in traffic conditions, such as might be occasioned by a vehicle stalled for a very short period of time, a caravan of cars as in a funeral procession, or brief malfunctioning of a traffic signal. Thus, it is desirable under many circumstances to use an average of several samplings of information in deriving the information to be used for display and computation purposes.

In my recently filed application for TRAFFIC VOLUME COMPUTER, successive sampling computations of the volume of traffic along a roadway as compared with a reference volume are made. The system of this invention may be used to derive an average of a predetermined number of such volume samplings or of any other similar such digital samplings of traffic conditions which may be taken in a digital traffic control system.

The system of this invention provides an accurate sliding average of the traffic control conditions being measured with an updating of the measurement being provided with each successive input sampling received. The system performs this function with only three memory registers to compute the average of five samples by time sharing these three registers. Further, a scanning counter is utilized which transforms the parallel input information received into serial pulses for easier processing. A sequencing technique is used in handling the successive samplings being averaged so as to accommodate the selection of various numbers of samples in the averaging. The system of the invention thus provides flexibility, high accuracy and continual updating of the sampling information to provide a true average of the traffic conditions under consideration.

It is therefore an object of this invention to provide more accurate information as to traffic conditions by averaging successively taken samples of traffic measurements.

It is still a further object of this invention to provide means for digitally computing the average of a predetermined number of immediately preceding traffic measurements.

It is still a further object of this invention to improve the reliability of traffic measurements.

Other objects of the invention will become apparent as the description proceeds in connection with the accompanying drawings, of which:

FIG. 1 is a functional block diagram illustrating the basic operation of the system of the invention;

FIG. 2 is a detailed block diagram illustrating a preferred embodiment of the system of the invention;

FIG. 3 is a series of waveforms illustrating clock pulses which may be utilized in implementing the preferred embodiment of the invention; and

FIG. 4 is a functional block diagram illustrating the operation of some of the gating control circuits utilized in the preferred embodiment.

Briefly described, the system of the invention utilizes a number of digital registers, this number being three in the preferred embodiment. Signals in accordance with successive samplings of a particular traffic parameter under consideration are fed to the first register, successive samplings being shifted into and retained for a time in each of the registers. A first sampling is scanned by means of a scanning counter to provide a pulse output in accordance with the digital count represented by the register signal in question. This digital signal is appropriately scaled in accordance with the number of samplings to be used in the averaging and this scaled output accumulated in an accumulator. When the first such sampling has been so processed, the samplings in the other registers are successively processed in the same manner, previous samplings having been successively shifted into the various registers. After the input to the first register and each of the other registers has been scanned in this fashion to provide the desired input to the accumulator, a new sampling input is received with the signals in each register being shifted into a succeeding register, this operation being controlled by means of a sequencer. The accumulator and control circuits are then reset to zero and a new averaging cycle commenced with the new sampling being used to replace the oldest sampling. In this manner, the average is continually updated to include the latest samplings made.

Referring now to FIG. 1, the basic operation of the system of the invention is illustrated. The output of traffic parameter computer 5, which may be a binary coded decimal signal representing traffic volume as described in my aforementioned patent application, is fed to digital register 11 which is connected to register 12, the output of register 12 being connected to register 13. Signals may be shifted from register to register by means of shift control 7, which operates in response to sequencer 18. Sequencer 18 is utilized to control successive sequences of operation in which the signals are appropriately processed to provide a digital signal in accordance with the average of the successive samplings, this signal being accumulated in accumulator 27.

It is to be noted that the various sequences of operation are synchronized by means of a series of successive clock pulses as shown in FIG. 3, these clock pulses being synchronized with those utilized in computer 5 such that a new sampling input will be provided from the computer 5 with each end of sampling pulse (EOS), these pulses appearing between a tenth and a first clock pulse (there being about one EOS pulse for each 10,000 clock pulses).

Let us assume that each of registers 11, 12 and 13 has a signal therein which represents a sampling and there also is a sampling at the input to register 11. During one of the sequences established by sequencer 18, register 13 will be scanned, that is to say, the output of the register is fed through control gates 6 to coincidence logic 16 where it is compared with the output of scanning counter 15. Scanning counter 15 during this sequence receives clock pulses from clock generator 32 through clock gating control 8. Also during this

sequence, clock pulses are passed from the clock generator through the gating control to scaling circuits 9 where they are appropriately scaled (divided by a factor in accordance with the number of samplings to be averaged) and fed to accumulator 27. When the count in register 13 is reached by the scanning counter 15, coincidence logic 16 produces a coincidence signal which provides an inhibit signal to clock gating control 8 which inhibits the further passage of clock pulses therethrough to both scanning counter 15 and scaling circuits 9. Thus, the number of pulses passed through the scaling circuits to accumulator 27 during this period is proportional to the count in register 13. Scaling circuit 9, as to be explained more fully in connection with FIG. 2, includes a selector switch for selecting a factor in accordance with the number of samplings to be used in making the average, this factor being divided into the count so that the count in accumulator 27 is appropriately weighted to represent the proportion of the total count in the accumulator contributed by each of the registers and the input to register 11. When the scanning of register 13 has been completed, sequencer 18 advances to a next sequence, scanning counter 15 being reset to zero. The signal in each register is then shifted to a succeeding register. Register 13 is then scanned again as thus described, only this time the signal to the accumulator will represent the sampling previously stored in register 12. In succeeding sequences, register 12, register 11 and the input to register 11 are scanned in similar fashion, with their pro-rated counts being accumulated in accumulator 27. The signal accumulated in the accumulator will then be the average of the immediately preceding five samples.

After all of the samplings to be used in the averaging have been appropriately scanned and their pro-rated portions accumulated in accumulator 27, the signal in the accumulator is fed to computer circuits 30 and display 31 for appropriate utilization. At the end of the averaging period the accumulator and the scanning counter are reset to zero. With the arrival of a new sampling input at the beginning of a new averaging period, the signals are shifted from register to register by means of shift control 7 in response to the sequencer so that the new sampling input replaces the oldest sampling which had previously been stored in register 13.

Referring now to FIG. 2, a preferred embodiment of the system of the invention is illustrated. Registers 11, 12 and 13 are connected to each other in cascade and receive a parallel shift command from parallel shift and multiplex logic 14. Clock generator 32 provides a series of clock pulses (1–5) and an end of sampling pulse (EOS) as illustrated in FIG. 3, these pulses being fed to sequence, decode and power-interrupt logic 19, from where they are appropriately distributed to control the various functions for each of the sequences of operation. The clock-1 pulses are utilized to provide the scanner clock and accumulator clock signals. As already noted, with each new sampling input to register 11, a parallel shift signal is provided in response to the output of sequence decode module 19 to shift the signals into each of the registers successively. Thus, once the system has been placed in operation for at least four input samplings, the registers will each contain one of the samplings with a fourth sampling sitting on the input line to register 11.

Let us now follow through a typical series of sequences. Let us assume that the sample switch of samples/average switch and decode logic 21 is set to 5 to indicate that five samples are to be used in the averaging. Then a first sequence initiated in response to sequencer 18 which provides a control signal to sequence decode and power interrupt logic 19 will cause parallel shift and multiplex logic 14 to couple the output of register 13 to coincidence logic 16 for comparison with the output of scanning counter 15. Scanning counter 15 during this sequence will receive clock pulses (clock-1) which are passed through the logic represented by boxes 17 and 19. These pulses are also fed to AND gate 23. AND gate 23 receives an enable signal from count flip-flop 22 which is set to provide this enable signal by the output of sequencer coincidence logic 20. The output of AND gate 23 is divided by means of divider 24 in accordance with the switch setting on the samples/average switch and decode logic 21 to provide clock pulses for accumulator 27 through divider control and accumulator advance logic 26.

Thus, during this sequence, scanning counter 15 receives clock pulses for each of the clock-1 inputs, while accumulator 27 receives inputs for each of these clock impulses divided by the division factor determined by the selected switch setting. When the count in scanning counter 15 reaches the count in register 13, a coincidence signal is developed in coincidence logic 16 which through the logical control circuitry of boxes 17, 18 and 19 provides a reset signal for count flip-flop 22. This produces an inhibit signal from the flip-flop to gate 23 terminating the passage of pulses therethrough to divider 24 and thus also terminates the pulse flow to accumulator 27. The coincidence signal also provides an inhibit signal to the logical control of box 17 and inhibits the further passage of clock pulses to scanning counter 15. The scanning of register 13 is thus completed and a new scanning sequence commenced.

Before the start of this next scanning sequence, a control signal is provided from sequence decode and power interrupt logic 19 to provide a parallel shift command to registers 11, 12 and 13 to shift these registers once. Thus the signal in register 12 is transferred to register 13 and the signal in register 11 is transferred to register 12. Register 13 is then scanned in the same fashion as just described to provide a new count representing the pro-rated succeeding sample for accumulator 27. When this sequence has been completed, control signals are provided from the sequence decode and power interrupt logic 19 to parallel shift and multiplex logic 14 to scan registers 12 and 11 in succession, in the same manner just described to provide succeeding signals for the accumulator in accordance with the counts in these registers. Finally, the signal on the input line is scanned and pro-ratedly appears in accumulator 27. The count in accumulator 27 thus represents the average of the five immediately preceding samples fed to the registers.

The contents of accumulator 27 are then parallel shifted into output register 28 in response to a control signal from sequence decode and power interrupt logic 19, this occurring with the initiation of a succeeding sequence. Also during this sequence, the count flip-flop 22, divider 24, accumulator 27 and scanning counter 15 are reset to zero. The signal in output register 28 is

fed through output gating logic **29** to computer circuits **30** and display **31** in response to enable signals fed to the output gating logic.

Referring now to FIG. **4**, the functioning of the logical circuitry in the preferred embodiment is illustrated. Input data which may be in binary coded decimal form is fed in parallel to register **11**. The signals are parallel shifted in response to a shift signal fed from logical gating **40** in response to clock-3 at appropriate sequences in the cycle. The outputs of the bits of each of the registers are each fed to a separate AND gate **41***a*–**41***d* (only one shown for each register and the input). The AND gates are sequentially enabled during successive sequences in response to enabling signals from logical gating **45**. Thus, coincidence logic **16** successively receives the outputs of each of registers **11**–**13** and the input lines. During each scanning sequence, clock pulses (clock-1) are fed through logical gating control **47** to scanning counter **15** and AND gate **23**.

The output of scanning counter **15** is fed to coincidence logic **16** and when the count in the counter reaches that fed to the coincidence logic from the appropriate register being scanned, a coincidence signal is generated by coincidence logic **16** to provide an inhibit signal to logical gating and control **47**, terminating the flow of clock pulses to scanning counter **15** and to gate **23**. Gate **23** as already noted provides pulses to divider **24** which are subsequently fed to the accumulator.

Gate **23** is controlled by the output of count flip-flop **22**. At the commencement of the scanning operation, a clock-1 pulse provides a reset signal to the count flip-flop through logical gating **50**, causing the flip-flop to provide an enable signal to gate **23**, thus permitting the passage of the clock pulses therethrough. When a coincidence condition has been reached, sequencer coincidence logic **20** provides a set signal to count flip-flop **22** in response to the output of coincidence logic **16**, thus causing the flip-flop to provide an inhibit signal to gate **23**, thus terminating the passage of clock pulses therethrough.

It is to be noted that the control switch of samples/ave switch and decode logic **21** (FIG. **2**) can be set to take any number of samples from 1 to 5. Thus, the system can be operated to use any number of samples up to **5** in the averaging.

The system of this invention thus provides a highly accurate technique for obtaining an average of immediately prior samplings of traffic condition. The number of samplings to be taken can be adjusted in the field to suit application requirements. A continuously updated averaging is provided by adding new samplings to the computation as they appear, with the oldest sampling being dropped.

While the system of this invention has been described and illustrated in detail, it is to be clearly understood that this is intended by way of illustration and example only, and is not to be taken by way of limitation, the spirit and scope of the invention being limited only by the terms of the following claims.

I claim:

1. A system for generating an output signal in accordance with the average of a selected number of successive samplings of a vehicle traffic parameter, each of said samplings comprising a coded digital signal, including

means for storing each of said signals,

means for sequentially generating trains of pulses, each of said trains having a number of pulses corresponding to a separate one of said stored signals,

means for dividing each of said pulse trains by a factor in accordance with the selected number of samplings, and

means for accumulating the output of said dividing means, the accumulated signal representing the average of said samplings.

2. The system of claim **1** wherein said storing means comprises a plurality of digital registers connected serially to each other and means for shifting the signals from register to register.

3. The system of claim **1** wherein said means for sequentially generating said trains of pulses comprises a clock pulse generator, scanning counter means for receiving the output of said clock pulse generator and means for comparing the count in said counter means with that in each of said storing means in turn and generating a coincidence signal when they are equal and means responsive to said coincidence signal for gating said clock pulses to said dividing means to form said pulse trains.

4. The system of claim **1** wherein is additionally included selector switch means for selecting the number of samplings to be averaged.

5. A system for generating a signal representing the average of a selected number of successive samplings of a vehicle traffic measurement, each of said samplings being represented by a coded digital signal, comprising

register means for registering each of said digital signals,

means for generating a train of clock pulses,

scanning counter means for counting said clock pulses,

means for comparing the count in each of said registers and that held at the input of one of said registers with the count in said scanning counter means and generating a gating control signal when there is coincidence therebetween,

gating means for gating clock pulses in accordance with said gating control signal,

scaling means for dividing the output of said gating means by a factor in accordance with the selected number of samplings, and

accumulator means for accumulating the output of said scaling means whereby the count in said accumulator means represents the average of the samplings.

6. The system of claim **5** wherein said scaling means includes switch means for selecting the number of samplings.

7. The system of claim **5** wherein is additionally included sequencer means for sequentially controlling the feeding of the signals in each of said registers and on the input line to one of said registers to said comparing means and for shifting the signals from register to register.

8. The system of claim **7** wherein said sequence means controls the feeding of a new successive sampling to said registers and the removal of the oldest sample from said registers as each new coded digital signal arrives at the input of said registers.

9. The system of claim 5 and further including display means and computer circuit means for receiving signals representing the count in said accumulator means.

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