United States Patent

Hill

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[54] OVERCURRENT TRANSIENT NON-RESPONSIVE TRIP DEVICE

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[73] Assignee: **Associated Electrical Industries Limited,** London, England

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[51] **Int. Cl.**.....**H02h 3/08**

[58] **Field of Search**.....317/36 TD, 27, 38, 46, 49, 317/14 A, 14 B, 14 C, 14 K

[56] **References Cited**

UNITED STATES PATENTS

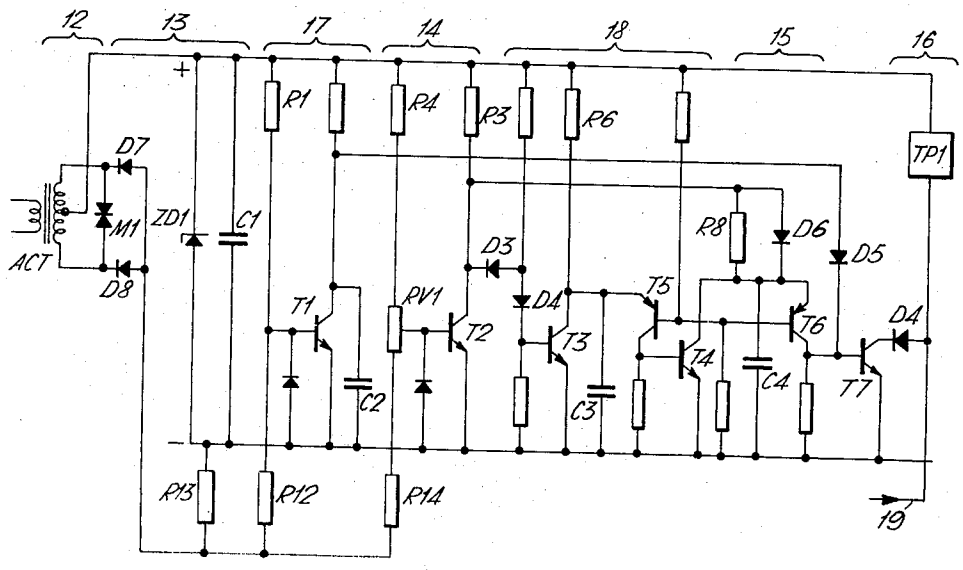
3,419,757 12/1968 Steen.....317/36 TD
3,202,876 8/1965 Mathews.....317/36 TD
3,262,017 7/1966 Ashenden.....317/36 TD X

Primary Examiner—J. D. Miller
Assistant Examiner—Harvey Fendelman
Attorney—Misegades & Douglas

[57] **ABSTRACT**

This invention relates to protective relays for systems with transformer loading, either power transformers or transmission lines with transformer feed-offs. In such systems, transformer inrush currents may cause relay tripping on initial energization. To prevent this false tripping, inrush currents may be detected and tripping inhibited. By the invention, inrush currents are detected by squaring the monitored quantity at the trip level, and determining whether the resulting rectangular pulses are separated from each other by more than a present amount. Inrush currents give peaky waveforms, with wide gaps between pulses, while genuine fault currents are roughly sinusiodal, and give wide pulses with only narrow gaps.

7 Claims, 8 Drawing Figures



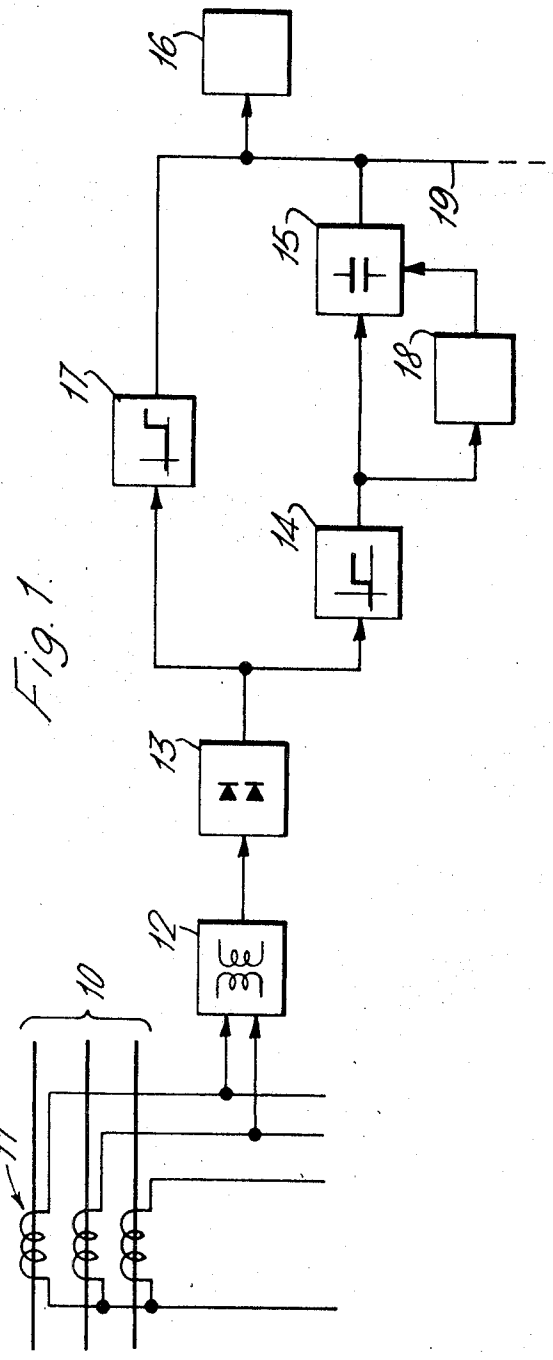
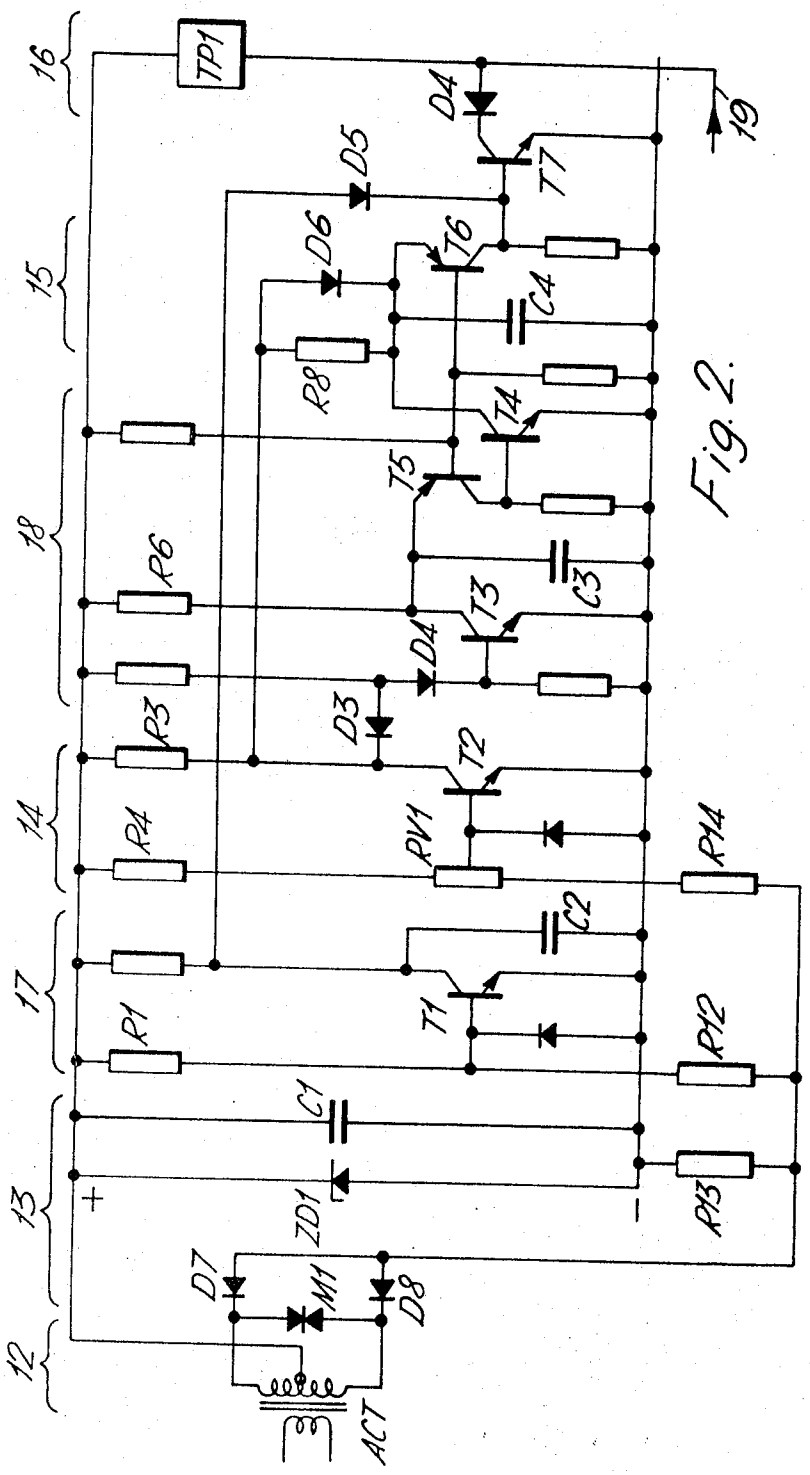


Fig. 1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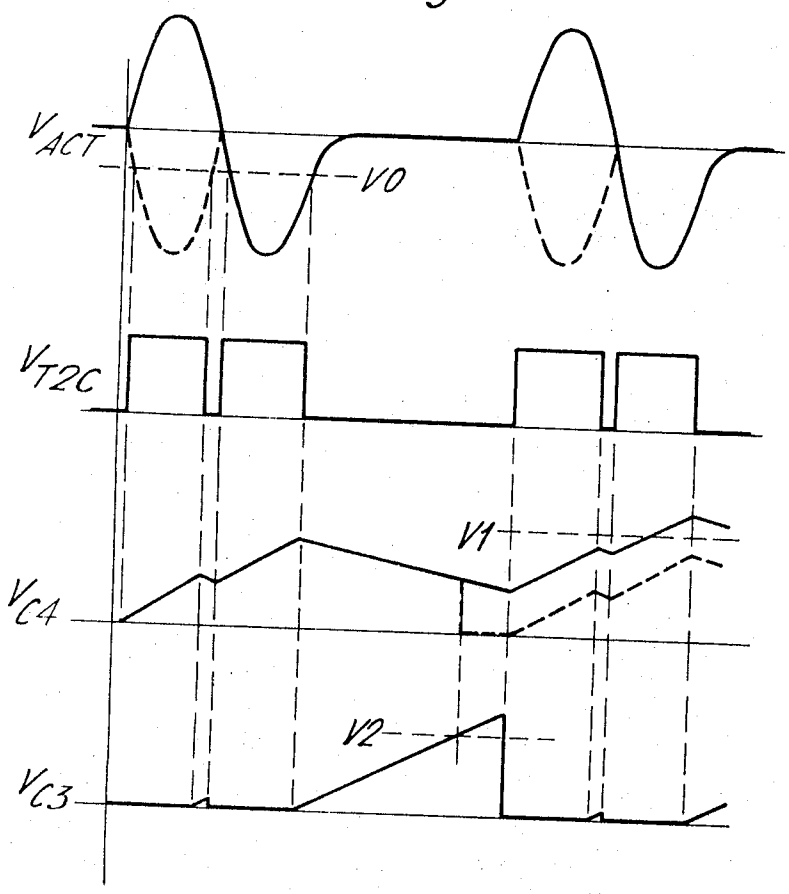
D4
T7
D5
D6
T6
C4
R8
T4
T5
R6
C3
T3
D4
D3
T2
R3
R4
PV1
R14
C2
T1
R1
R12
C1
ZD1
R13
D7
M1
D8
ACT
16
15
18
14
17
13
12
19
+
-

Fig. 2.

Fig. 3.



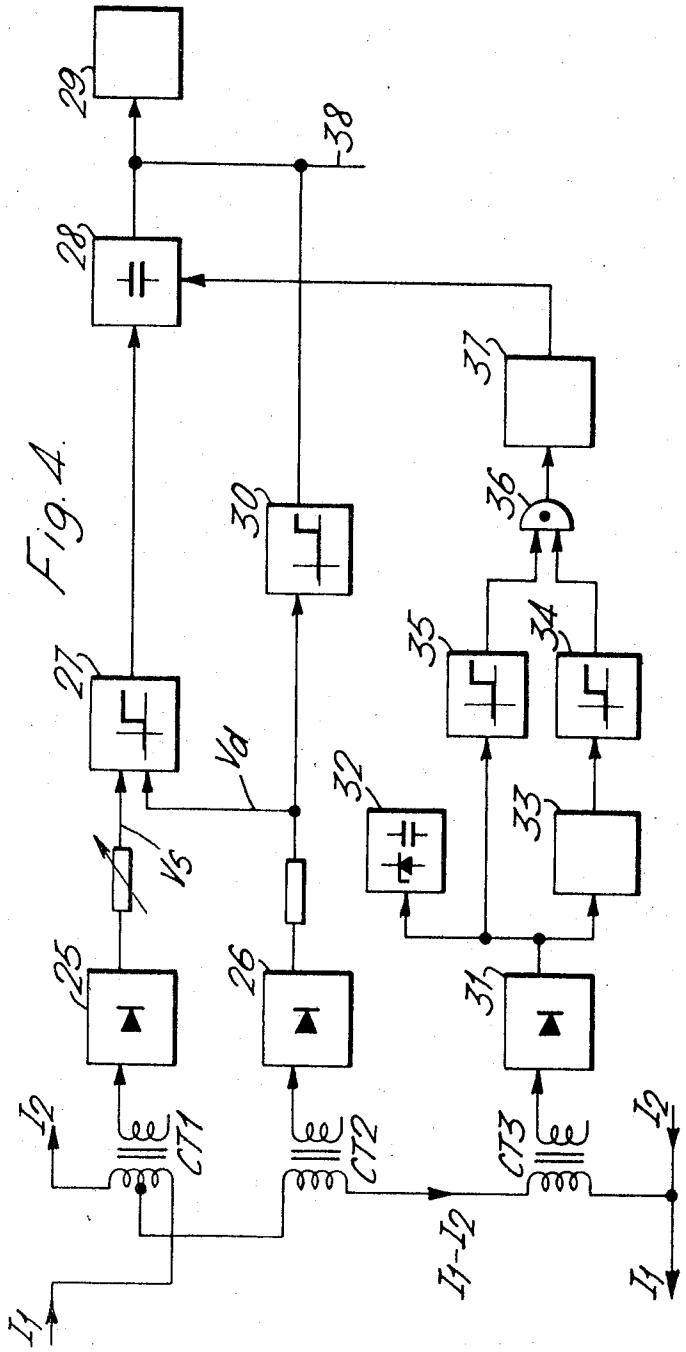

29
38
28
37
36
30
35
34
27
Va
32
33
Vs
25
26
31
12
CT1
CT2
CT3
12
11-12
11
11

Fig. 4.

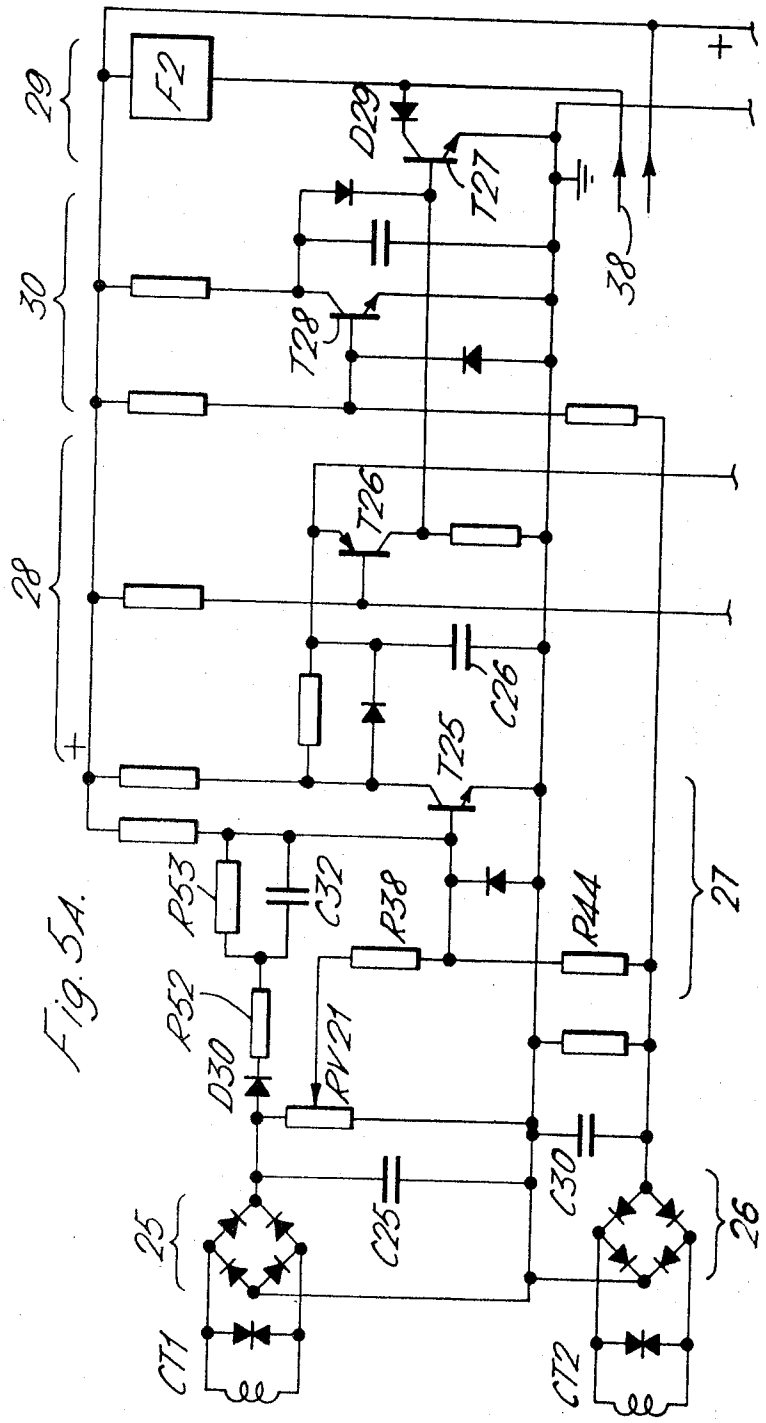

F2
D29
T27
38
T28
T26
C26
T25
R53
C32
R38
R44
R52
D30
RV21
C25
C30
CT1
CT2
29
30
28
27
25
26
+

Fig. 5A.

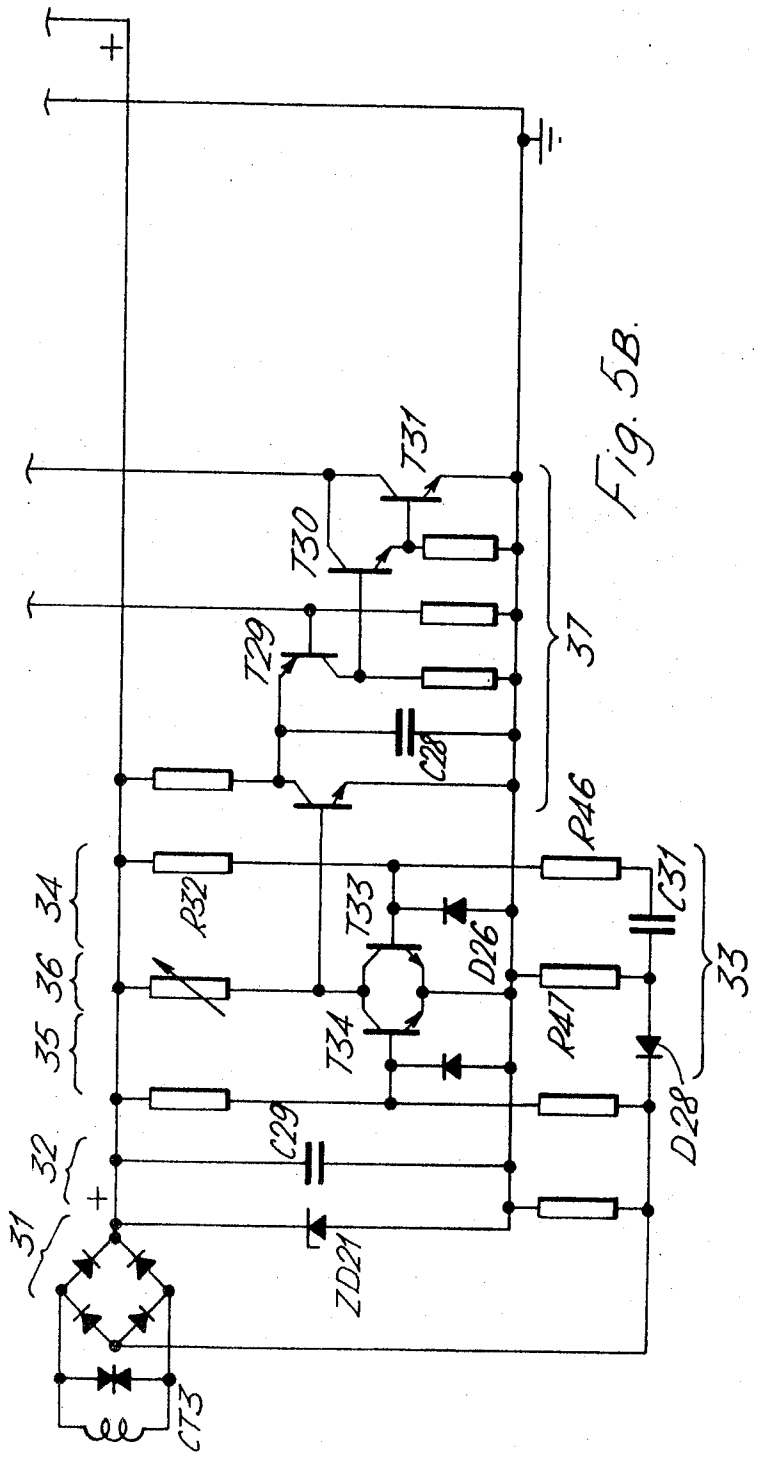

+
T31
T30
T29
C28
37
R46
C31
R32
T33
D26
34
36
35
T34
R47
33
C29
32
D28
31
+
ZD21
CT3

Fig. 5B.

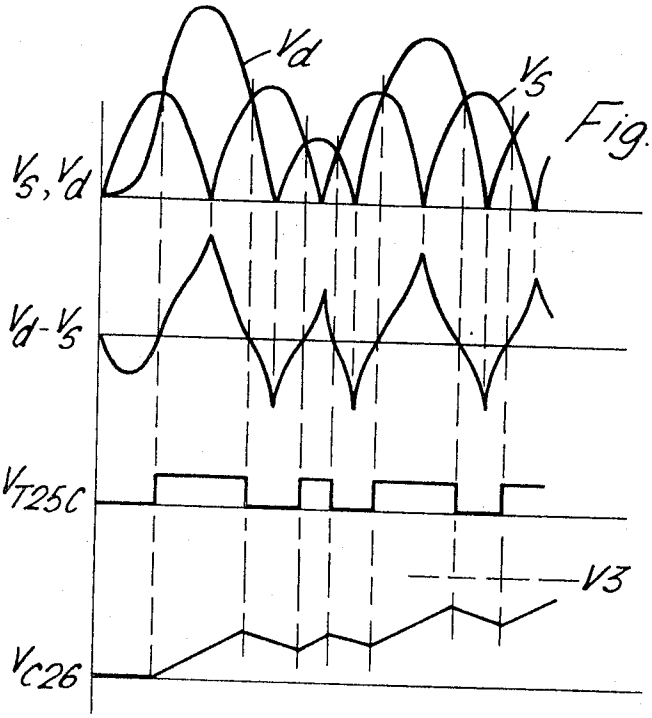


Fig. 6.

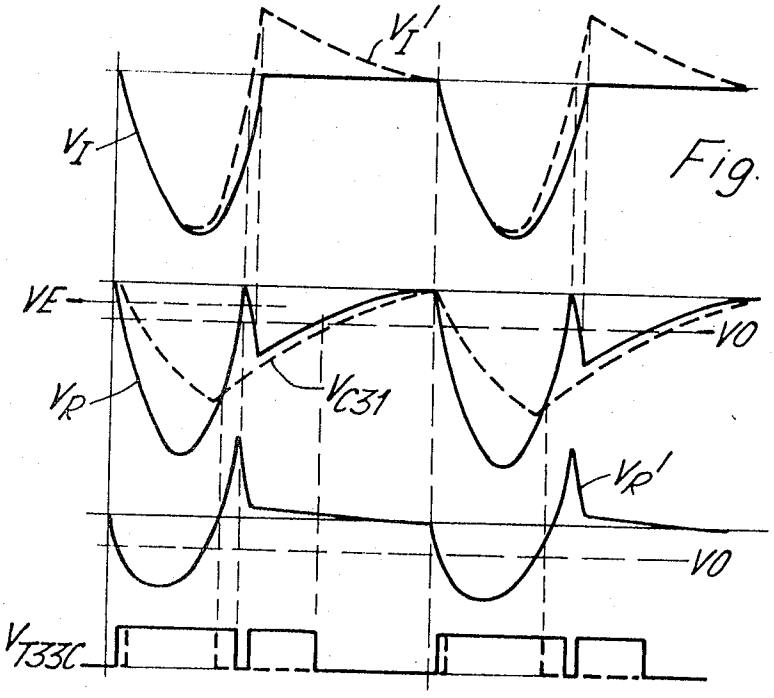


Fig. 7.

OVERCURRENT TRANSIENT NON-RESPONSIVE TRIP DEVICE

This invention relates to protective relays for transformer systems. A transformer system may be a power transformer which is to be protected, or a transmission system in which a supply line has several branches "teed" off by means of transformers.

The basic principle of many protective relays is that a suitable quantity, e.g. voltage or current, in the system to be protected is monitored, and the relays trips to isolate and thus protect the system if this monitored quantity exceeds a predetermined limit. The quantity may conveniently be full-wave rectified, so that the relay can respond within half a cycle. However, with transformer systems a difficulty arises, since when the system is first energized, large inrush currents flow into the transformers. With a simple limit value tripping, therefore, the relay will trip immediately on switching power into the system.

To overcome this, relays have been provided with means for detecting such inrush currents and inhibiting tripping when inrush currents are present. The inrush current detection has been achieved by detecting the amplitude of the second harmonic content of the monitored quantity. This second harmonic content is negligible when a "genuine" fault (e.g. a short circuit) occurs, but is high in transformer inrush currents. Thus tripping is inhibited when the second harmonic content is high. However, this technique is not wholly satisfactory, since if the fault current is too high, transformer saturation can occur and the second harmonic will then be generated. Thus a compromise has to be found between wrongly inhibiting tripping when a genuine fault occurs, and wrongly permitting tripping on transformer inrush currents.

The general object of the present invention is to provide improved means for detecting transformer inrush currents.

Thus according to the invention there is provided a protective relay including an inrush current detector which inhibits tripping when a transformer inrush current appears, wherein the inrush current detector determines whether the monitored quantity exceeds a predetermined limit for less than a predetermined part of the time. Thus the invention utilizes the fact that an inrush current waveform is extremely "peaky", whereas a fault current is much more nearly sinusoidal, by squaring the waveform of the monitored quantity at the predetermined limit level and determining whether the resulting rectangular pulses are sufficiently close together.

Two embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings, in which:

FIG. 1 is a block diagram of a protective relay for a transmission line;

FIG. 2 is a circuit diagram of the relay of FIG. 1;

FIG. 3 is a set of waveforms relating to the operation of the relay of FIG. 1 under inrush current conditions;

FIG. 4 is a block diagram of a protective relay for a power transformer;

FIGS. 5A and 5B, placed the former above the latter, are a circuit diagram of the relay of FIG. 4;

FIG. 6 is a set of waveforms relating to the operation of the relay of FIG. 4 under normal conditions; and

FIG. 7 is a set of waveforms relating to the operation of the relay of FIG. 4 under inrush current conditions.

Referring to FIG. 1, a transmission line 10 which has a substantial transformer loading is monitored by a set of three current transformers 11. A single relay circuit is shown, monitoring the difference between two phases of the line; in a complete system, further similar circuits are provided to ensure that all three phases are monitored. The relay circuit shown has an auxiliary current transformer 12 coupling the outputs of the current transformers 11 to a rectifier and power supply circuit 13. The circuit 13 supplies power for the rest of the circuit, and also full-wave rectifies the signal fed to it. This full-wave rectified signal is fed to a "low set" overcurrent detector 14, which produces a square pulse having a duration

equal to the time for which the rectified signal is more negative than a predetermined level which corresponds to the minimum operating level. The output square pulses from the circuit 14 are fed to a symmetric integrator and level detector 15, which smooths the signal applied to it by means of a capacitor and produces an output if the capacitor voltage exceeds a predetermined value. The output from the circuit 15 is fed to an output circuit 18 which initiates protective action, e.g. opening circuit breakers to isolate the line 10 from the supply.

The circuit 13 also feeds a "high set" overcurrent detector 17, which squares the signal at a predetermined level several times as great as the corresponding level of the similar circuit 14. The signal path through circuits 14 and 15 inherently involves a certain delay; the output from circuit 17 is fed directly to the output circuit 16 and appears without delay, to initiate immediate protective action, if the monitored signal exceeds the large overcurrent setting of the circuit 17.

The circuit 14 also feeds a gap detector circuit 18, which responds to the gaps between the pulses from circuit 14 and produces an output signal if these gaps are of more than a predetermined length. This output is fed to circuit 15 to inhibit it from producing an output. Thus if there are long gaps between the pulses from circuit 14, circuit 15 is inhibited and protective action is inhibited as a result.

Outputs from the circuitry for other phases are commoned into the output circuit 16 via line 19.

The specific circuitry is shown in FIG. 2, and will be described with the aid of the waveforms of FIG. 3. The first waveform, V_{ACT}, shows an idealized inrush current waveform. This consists essentially of a single cycle at a frequency substantially greater than the supply frequency, repeating at the supply frequency. The inrush current waveform may be of various forms, depending on the precise conditions, but always has a single peak or two peaks close together followed by a long gap before the waveform repeats. The normal supply line waveform is, of course, a sinusoid of the supply frequency and of much smaller amplitude, and the normal fault waveform is like the normal supply waveform but of amplitude comparable with the inrush current amplitude.

The circuit 12 comprises (FIG. 2) an auxiliary current transformer ACT with a centre-tapped secondary. A metrosil M1 is connected across it to limit the output signal on large overloads. The secondary feeds the circuit 13, in which diodes D7 and D8 form a full-wave rectifier and resistor R13, capacitor C1, and zener diode ZD1 form the power supply for the rest of the circuitry, of polarity as indicated. The effect of rectification is indicated in FIG. 3, first waveform, by the broken lines. Capacitor C1 is charged to the Zener voltage by each half-cycle from diodes D7 and D8 and maintains the power supply voltage substantially constant, provided of course that the input signal is big enough.

The "low set" circuit 14 comprises essentially a transistor T2 whose base is fed from a voltage divider consisting of resistors R4, RV1, and R14. With an input signal just sufficient to drive Zener diode ZD1 into conduction at the crest of each peak, the bottom end of resistor R13 will never be appreciably negative with respect to the negative power supply line, and transistor T2 will therefore always have a positive voltage on its base. This transistor is therefore normally conductive. However, if the input signal increases, the base of transistor T2 will eventually go negative at the peaks of the input signal, cutting it off. Therefore, the collector waveform of transistor T2 will consist of positive square pulses, rising from a base level near zero, when the rectified voltage from transformer ACT goes more negative than a predetermined level, indicated as VO in FIG. 3. The resulting collector waveform is shown as V_{T2C}.

These pulses are fed to a capacitor C4 via a resistor R8 connected in parallel with a diode D6. The resistances of resistors R8 and R3 (the collector resistor of transistor T2) are chosen to be equal, so that capacitor C4 charges (via resistor R3 and diode D6) and discharges (via resistor R8 and transistor T2)

through equal resistances. Capacitor C4 therefore acts as a symmetrical integrator or smoothing circuit. The resulting voltage on it is indicated by the full-line waveform V_{C4}. This capacitor drives a transistor T6, the capacitor, its charging and discharging components, and this transistor together forming the integrator 15. Transistor T6 is normally held cut off by its base bias, but turns on if the capacitor voltage exceeds this bias (indicated as V1 in FIG. 3). Transistor T6 drives a further transistor T7, which in turn drives an output device TP1 which forms the output circuit 16. If transistor T6 turns on, transistor T7 also turns on and the output device TP1 is energized.

It can be seen that the energization of the output device TP1 follows, with a delay in the integrating circuit 15, after the input waveform starts to exceed (negatively) the critical voltage VO (FIG. 3). With a normal fault, the gaps between the pulses from transistor T2 are narrow and the delay will be relatively short unless the critical voltage is only just exceeded.

The output from the rectifying circuit 13 is also fed to a voltage divider comprising resistors R1 and R12, which drives a transistor T1, forming the "high set" circuit 17. This transistor operates similarly to transistor T2, but with a critical voltage equal to several times VO. Its output, at the collector of transistor T1, is fed to the base of transistor T7 via an isolating diode D5. An input signal exceeding the critical voltage of the "high set" circuit will turn transistor T1 off, turn transistor T7 on, and energize the output device TP1 without delay. A small capacitor C2 prevents the circuit from operating on narrow noise spikes.

The output from transistor T2 is also fed, via diodes D3 and D4 and an inverting transistor T3, to a capacitor C3. Transistor T3 is normally nonconductive, and is turned on by the pulses from transistor T2. The capacitor C3 is therefore discharged by these pulses, but charges through a resistor R6 when transistor T3 is turned off. The voltage on this capacitor C3 is shown as waveform V_{C3} in FIG. 3. Provided that the pulses from transistor T2 are close together, the voltage on capacitor C3 will never rise much above zero. Should the pulses be widely spaced, however, then the voltage on capacitor C3 may rise to exceed a critical voltage V2 (FIG. 3). This is the voltage on the base of a transistor T5, which is normally cut off but turns on when the voltage on capacitor C3 rises sufficiently. This turns on transistor T4, which is shunted across capacitor C4, and therefore discharges capacitor C4. Thus when a long gap is detected, as indicated by transistor T5 turning on, capacitor C4 is discharged and the voltage on it actually follows the broken waveform VC4 of FIG. 3. The voltage on capacitor C4 therefore fails to reach V1, and the output device TP1 is not energized. That is the action of the integrating circuit 15 is inhibited.

The components from diode D3 to transistor T4 inclusive form the gap detection circuit 18.

Referring now to FIG. 4, a protective relay for a power transformer (not shown) will be described. In FIG. 4, only the circuitry for a single phase is shown; for a normal three-phase transformer, most of the circuitry will be triplicated for the three phases.

For the phase considered, I_1 and I_2 represent the currents in the primary and secondary windings, these currents being obtained from current transformers (not shown). These currents are applied to three auxiliary current transformers CT1 to CT3, the output of CT1 representing the sum $I_1 + I_2$ and the outputs of CT2 and CT3 representing the difference $I_1 - I_2$ of these currents. The sum signal from transformer CT1 and the difference signal from transformer CT2 are passed through respective full-wave bridge rectifiers 25 and 26 whose outputs are applied, via adjustable scaling resistors, to a comparator 27. This comparator produces an output signal when the "sum" signal V_s is less than the "difference" signal V_d applied to it. This output signal is fed to a symmetrical integrator and level detector 28, which smooths the signal applied to it by means of a capacitor and produces an output if the capacitor voltage exceeds a predetermined value. The output from the circuit 28 is fed to an output circuit 29, which initiates protective action.

The signal V_d from rectifier 26 is also fed to a "high set" circuit 30, which operates if the signal V_d is more than a predetermined multiple (e.g. 10 times) the minumum relay setting, and causes immediate protective action, its output being fed to the output circuit 29.

The output of transformer CT3 is fed to a bridge rectifier circuit 31 which feeds a power supply circuit 32 which provides DC power for the rest of the circuitry. The rectifier 31 also feeds a level detector 34 via a filter 33 which compensates for distortion introduced by the transformer CT3. The rectifier 31 also feeds a further level detector 35. The outputs from level detectors 34 and 35 are fed to an AND gate 36 which feeds a gap detector circuit 37, which in turn feeds the integrator circuit 28 to inhibit it.

Outputs from other phases are commoned onto the line 38.

The comparator 27 and integrator 28 act similarly to the "low set" circuit 14 and integrator 15 of FIG. 1. The "high set" circuit 30 is similar to the "high set" circuit 17 of FIG. 1. The circuitry from rectifier 31 to the gap detector 37 performs a similar function the gap detector 18 of FIG. 1, inhibiting the integrator 28 when an inrush current is detected, but is rather more complicated. The level detector 35 is set to operate at a value at least twice the maximum steady state magnetizing current, and gates the output of the level detector 34. Thus if there is no output from level detector 35, no pulses pass through the AND gate 36 to the gap detector 37, and the integrator 28 is accordingly inhibited. Thus the level detector 35 acts in effect as a primary operating component of the system.

If the setting of level detector 35 is exceeded, then the pulses from level detector 34 (which is set to operate at a much lower level) pass through the AND gate 36 to the gap detector 37. If an inrush current is present, the gap detector will detect long gaps and again inhibit the integrator 28; if a "normal" overload or fault current is present, the gap detector will not operate and the integrator 28 will operate.

The specific circuitry is shown in FIGS. 5A and 5B, and will be described with the aid of the waveforms of FIGS. 6 and 7.

The bridge rectifiers 25 and 26 are fed from the transformer secondaries CT1 and CT2, which have metrosils connected across them to limit excess voltages, and have small capacitors C25 and C30 connected across them to limit noise spikes. Their outputs are compared by means of the voltage divider RV21, R38, and R44, resistor RV21 having an adjustable tapping. This voltage divider drives transistor T25, which in turn drives capacitor C26 forming the integrating capacitor of the smoothing circuit 28.

The voltages V_s and V_d are related by scaling factors to the outputs of the bridges 25 and 26 respectively. In normal operation, these voltages will be roughly in phase with each other, and if V_s is less than V_d then transistor T25 will be turned on nearly all the time. However, under some conditions these voltages can be out of phase. The top graph of FIG. 6 shows two waveforms V_s and V_d with the same AC amplitude, and waveform V_d being shown with reversed (positive) polarity, but 90° out of phase with each other, and with an exponential transient component in V_d. The next graph shows the difference $V_d - V_s$ which is applied to the base of transistor T25, which squares this waveform at substantially the zero level. The waveform at the collector of T25 is shown in the next graph, as V_{T25C}, and the waveform of the voltage on the integrating capacitor C26 is shown in the last graph, as V_{C26}. It will be seen that, although the mark: space ratio of the waveform V_{T25C} varies, this ratio is on average about 1:1, For equal AC amplitudes is V_s and V_d, it is exactly 1:1 regardless of the phase difference in the absence of any exponential DC component; and, as can be seen from FIG. 6, an exponential DC component alternately widens and narrows the pulses, so that such DC components are largely compensated for, and affect the ratio only slightly. For a 1:1 mark: space ratio, the voltage on capacitor C26 will rise to some maximum level. By choosing a critical level just above this for transistor T26 to turn on, e.g. the level V3 shown in FIG. 6, the integrator 28 will not produce an output for equal amplitude inputs to the comparator 27, regardless of their phase, but will respond to

V_s being less than V_d. For inequality of inputs, the mark: space ratio will vary with phase, but the range of variation will never extend to include the 1:1 value. The system thus has a substantially circular characteristic in the complex plane.

The response time of this relay is short compared to that of electromechanical systems. For through faults, i.e. faults in the circuitry fed by the transformer being protected, it is found that transient disturbances may cause the relay to operate. This is because the line current transformers produce a substantial spill current for a time comparable with operating time of the system. To prevent this, a transient bias circuit is included. This transient bias circuit consists of diode **D30**, resistors **R52** and **R53**, and capacitor **C32**. At the instant of a through fault the bias at the base of transistor **T25** is increased for a short time, increasing the stability of the system without loss of either sensitivity or speed of operation for internal faults of the transformer.

The two level detectors **34** and **35** fed from the rectifier **31** are constituted by transistors **T33** and **T34** respectively. These transistors have their collectors commoned together, so forming the AND gate **36**. The gap detector includes a capacitor **C28**, this controlling a transistor **T29** which turns on when the capacitor voltage exceeds a predetermined level. The output of transistor **T29** is amplified by the two transistors T **30** and **T31**, which when turned on discharge the capacitor **C26** of the integrator.

The transformers **CT1** to **CT3** are, for practical reasons, made as physically small as possible. With a decrease in size, the output may become somewhat distorted. A typical inrush current waveform is shown in the first graph of FIG. **7**, full line waveform V_I; the overshoot distortion resulting from a small transformer **CT3** is shown by the broken line waveform V_I', on the same graph. This distortion if of no consequence as far as transformers **CT1** and **CT2** are concerned. However, with transformer **CT3** the waveform becomes rectified, as shown by the full-line waveform V_R in the second graph, and the overshoot portions may exceed the setting level VO of the level detector **34**. The pulses from this detector will then be as shown in the fourth graph, full line waveform. The gaps between these pulses are relatively short, and the gap detector circuit may therefore fail to recognize the waveform as an inrush current waveform. The relay may therefore trip incorrectly on an inrush current.

To prevent this, the filter **33** is provided, consisting essentially of resistors **R46** and **R47**, diodes **D26** and **D28**, and capacitor **C31**. The voltage at the base of transistor **T33** is loosely clamped near zero, by diode **D26** and the base-emitter junction of transistor **T33**.

Hence the right-hand side of capacitor **C31** is always at a voltage near earth. In FIG. **7**, second graph, the base line is the positive supply line of FIG. **5**, and the earth level is shown as VE. As the voltage V_R goes negative, diode **D28** will turn on when this voltage falls below the earth level VE. When this happens, capacitor **C31** will begin to charge through **D26**, **R46**, and **D28** with a relatively short time constant. Its voltage will therefore follow the broken line wave form V_{C31} of the second graph of FIG. **7**, until the voltage V_R returns towards zero and differs from the voltage on **C31** by the supply voltage, i.e. the voltage across the zener diode **ZD21** and the capacitor **C29**. At this point diode **D28** becomes non-conductive, and capacitor **C31** will discharge through **R46**, **R47**, and the base-emitter junction of transistor **T33** with a relatively long time constant.

The voltage V_R' applied to the bottom end of resistor **R46** will therefore be the difference between the voltages V_R and V_{C31}, as shown in the third graph of FIG. **7**. The output from transistor **T33** will therefore be that shown by the broken waveform of the fourth graph of FIG. **7**. By a suitable choice of the time constants for charging and discharging **C31**, the overshoot of waveform V_R can be eliminated from waveform V_R', as shown. The gaps between the pulses from an inrush current will therefore be long, and inrush currents will be properly detected.

It can be seen that this filter circuit reduces the widths of all pulses — for example, the first pulse in waveform V_{T33C} has been narrowed. The same effect will occur for genuine fault current waveforms. However, if the circuit **34** has its parameters suitably adjusted, discrimination at the desired level between genuine fault currents and inrush currents can still be achieved. The discharge time constant of capacitor **C31** is preferably matched fairly closely to the effective time constant of the overshoot of waveform V_I'.

The "high set" circuit **30** comprises a transistor **T28**. The output from this transistor and the output from a transistor **T26** controlled from the capacitor **C26** are combined at transistor **T27**, whose output is fed via a diode **D29** to the output circuit **F2**. Outputs from other phases are commoned onto line **38** via corresponding diodes; the circuits for these other phases share the positive supply line and not the "earth" line with the circuitry shown.

I claim:

1. A protective relay for a transformer system, including an inrush current detector which inhibits tripping when a transformer inrush current appears, characterized in that the inrush current detector comprises

means for producing a square wave pulse having a duration equal to the time for which the instantaneous monitored quantity is above a predetermined level, and

timing means for determining whether there are intervals greater than a predetermined value between the square wave pulses.

2. A protective relay according to claim **1**, wherein the monitored quantity is rectified before being fed to the square wave pulse producing means.

3. A protective relay according to claim **1**, wherein the timing means comprise a capacitor which is discharged during the duration of the square wave pulse and charged when the square wave pulse ceases, and a level detector which inhibits tripping when the capacitor is charged to above a predetermined value.

4. A protective relay according to claim **1**, including a symmetrical integrator fed by the square wave pulse and including a capacitor which is charged and discharged as the monitored quantity exceeds and falls short of the predetermined level,

an output circuit which operates when the capacitor is charged above a predetermined value, and

coupling means between the inrush current detector and the symmetrical integrator for discharging the capacitor on an inrush current being detected.

5. A protective relay according to claim **1**, including a high overload detector for causing immediate tripping when the monitored quantity exceeds a predetermined high overload level, the high overload detector not being inhibited by the inrush current detector.

6. A protective relay according to claim **1**, including a small coupling transformer for coupling the monitored quantity to the squaring means, and

a diode-capacitor filter for eliminating overshoot of inrush current waveforms introduced by the coupling transformer.

7. A protective relay for a transformer, including means responsive to the sum and difference currents of the transformer to cause tripping on overload, and

an inrush current detector responsive to the difference current of the transformer for inhibiting tripping, the inrush current detector comprising

means for producing a square wave pulse having a duration equal to the time for which the instantaneous difference current is above a predetermined level, and

timing means for determining whether there are intervals greater than a predetermined value between the square wave pulses.

* * * * *