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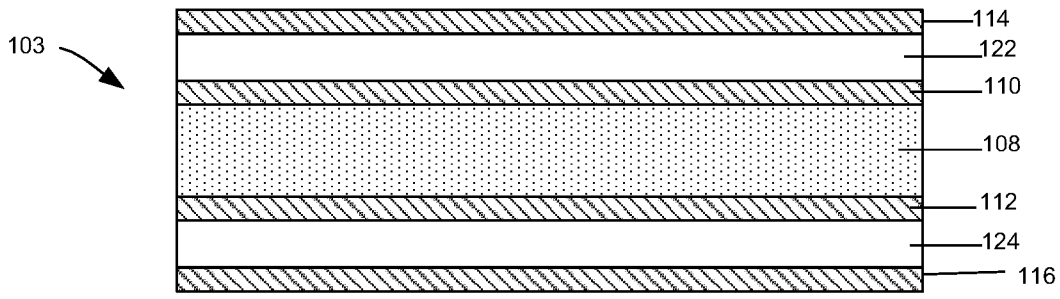
(54) **Title:** MICROELECTRONIC SUBSTRATE INCLUDING EMBEDDED COMPONENTS AND SPACER LAYER AND METHOD OF FORMING SAME



(57) **Abstract:** A microelectronic substrate, a method of forming the same, and a system including the same. The microelectronic substrate comprises: a conductive layer; a spacer layer disposed onto the conductive dielectric layer; a dielectric build-up layer disposed onto the spacer layer, the spacer layer being made of a material that has a lower shrinkage than a material of the embedding dielectric-build-up layer during curing, and a higher viscosity than a material of the embedding dielectric build-up layer in its pre-cure form and during curing; and active or passive microelectronic components embedded within the dielectric build-up layer.

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MICROELECTRONIC SUBSTRATE INCLUDING EMBEDDED COMPONENTS AND SPACER LAYER AND METHOD OF FORMING SAME

FIELD

Embodiments of the present invention relate generally to the field of microelectronic fabrication. More specifically, embodiments of the present invention relate to microelectronic substrates including active or passive components embedded therein.

BACKGROUND

The embedding of preformed active or passive components onto a microelectronic substrate, such as, for example, for decoupling, RF tuning or voltage regulation applications require a precise positioning of such components onto the substrate in order to allow a reliable connection of the electrical contacts, such as vias, on those components to existing conductive interconnect layers of the substrate.

Currently, embedded active and/or passive components are positioned onto a panel sized dielectric build-up layer of the substrate, and the build-up layer subsequently cured. However, disadvantageously, the viscous nature of the pre-cure dielectric build-up layer can cause significant shifts during the embedding process, and therefore cause appreciable positional errors with respect to the embedded components. Thus, prior art methods of embedding components onto microelectronic substrates can be unpredictable with respect to a reliable electrical connection and/or physical positioning of such components onto the substrate onto which they are being embedded, in this manner negatively affecting performance and yield.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic cross-sectional view of a conventional intermediate substrate including a core, conductive layers and dielectric build-up layers;

Fig. 2 is a schematic view of a first intermediate structure including the intermediate substrate of Fig. 1 further having a spacer layer thereon according to an embodiment;

Fig. 3 is a schematic view of a second intermediate structure including the structure of Fig. 2 further having an pre-cure dielectric build-up layer thereon;

Fig. 4 is a schematic view of a third intermediate structure including the structure of Fig. 3 in the process of being provided with components being embedded into the pre-cure dielectric build-up layer;

Fig. 5 is a schematic view of a fourth intermediate structure including the structure of Fig. 4 after a curing of the pre-cure dielectric build-up layer;

Fig. 6 is a schematic view of a package including a microelectronic substrate formed from the structure of Fig. 5;

Fig. 7 is a schematic view of a system including a microelectronic substrate similar to the substrate of Fig. 6.

For simplicity and clarity of illustration, elements in the drawings have not necessarily been drawn to scale. For example, the dimensions of some of the elements may be exaggerated relative to other elements for clarity. Where considered appropriate, reference numerals have been repeated among the drawings to indicate corresponding or analogous elements.

DETAILED DESCRIPTION

In the following detailed description, a microelectronic substrate, a microelectronic package, a method of forming the substrate, a method of forming the package, and a system including the substrate are disclosed. Reference is made to the accompanying drawings within which are shown, by way of illustration, specific embodiments by which the present invention may be practiced. It is to be understood that other embodiments may exist and that other structural changes may be made without departing from the scope and spirit of the present invention.

The terms on, onto, above, below, and adjacent as used herein refer to the position of one element relative to other elements. As such, a first element disposed on, onto, above, or below a second element may be directly in contact with the second element or it may include one or more intervening elements. In addition, a first element disposed next to or adjacent a second element may be directly in contact with the second element or it may include one or more intervening elements.

Aspects of this and other embodiments will be discussed herein with respect to Figs. 1-7, below. The figures, however, should not be taken to be limiting, as they are intended for the purpose of explanation and understanding.

Reference is first made to Fig. 6, which shows a package 100 including a microelectronic substrate 102 having embedded components 104 therein according to an embodiment, a microelectronic die 106 being flip-chip mounted onto the substrate 102 using solder joints 101 and an underfill material 101' in a well known manner. Other mounting configurations for the die 106 are within the purview of embodiments. As will be explained in further detail below, a package according to embodiments, such as, for example, package 100 shown in Fig. 6, is different from similar prior art packages by virtue of the presence of at least one spacer layer, such as spacer layers 138 and 140, disposed between embedded components of the substrate and the underlying conductive layer, such as between embedded components 104 and respective underlying conductive layers 114 and 116. The spacer layer according to embodiments mitigates positional errors with respect to a positioning of the embedded components as compared to a prior art structure where a spacer layer would not be used.

Referring in more detail to Fig. 6, package 100 may be used for example to couple the components 104 and/or the die 106 to a circuit board, or to couple a processor or processing system to a motherboard according to application needs. The substrate 102 includes a core 108, which may be a commercially available core using, for example, FR4, FR5 or organic materials such as Bismaleimide Triazine (BT) as the dielectric material. The core may further include a glass-reinforced epoxy PCB material with copper cladding. Other types of cores are within the purview of embodiments. The substrate 102 as shown further includes conductive layers 110, 112, 114, 116, 118 and 120, and, in addition, dielectric build-up layers 122, 124, 126, 128, 130 and 132, which layers may conform to conventional configurations for such layers as commonly used in multilayer substrate structures. The conductive layers and build-up layers are shown schematically in the figure, and it is to be understood that those layers are not necessarily continuous layers as seems to be suggested in the schematic depiction, but have a configuration adapted to allow the routing of electricity/signals at various levels within a multilayer substrate as would be readily recognized by one skilled in the art. Thus, by way of example, each of the conductive layers 110-120 may have been plated onto a corresponding build-up layer and then patterned to form traces therefrom according to application needs, each layer of traces being referred to herein as a conductive layer. Similarly, each of the dielectric build-up layers 122-132 may have been provided with vias extending therethrough, such

as, for example, vias 134, in order to connect respective conductive layers to one another. Vias 136 may further be provided through the core 108 as shown according to application needs. As seen in Fig. 6, build-up layers 126 and 128 each include microelectronic components 104 embedded therein, each of the components 104 being either active or passive as dictated by a particular predetermined design for the substrate. An embedding of microelectronic components into a dielectric build-up layer, such as layers 126 or 128, is well known in the art. To the extent that the dielectric build-up layers 126 and 128 as shown in the embodiment of Fig. 6 include embedded microelectronic components therein, they may hereinafter be referred to herein as embedding dielectric build-up layers 126 and 128. The microelectronic components 104 may include preformed active or passive components. Active components would include, for example, transistors, MOSFETs, junction diodes, etc. Passive components would include, for example, capacitors, inductors, resistors, etc. The microelectronic components 104 may include components for decoupling, radio frequency tuning or voltage regulation, as would be recognized by one skilled in the art. To the extent that the conductive layers 114 and 116 "underlie" respective ones of the embedding dielectric build-up layers 126 and 128 in the sense of being adjacent to the embedding dielectric build-up layers, conductive layers 114 and 116 may sometimes be referred to herein as underlying conductive layers 114 and 116. The dielectric build-up layers 122, 124, 126, 128, 130 and 132 may for example be made of a polymeric dielectric material including, for example, ABF, such as, for example, ABF GX13.

Referring still to Fig. 6, substrate 102, according to the shown embodiment, further comprises spacer layers 138 and 140 respectively separating each of embedding build-up layers 126 and 128 from a corresponding underlying conductive layer 114 and 116. Each of the spacer layers may be made of a material that has a lower shrinkage than a material of the embedding dielectric-build-up layer during curing, and a higher viscosity than a material of the embedding dielectric build-up layer in its pre-cure form and during curing. A material of the embedding dielectric build-up layers is in a "pre-cure" form as used herein when it is in a phase thereof prior to a full curing of the same, at which point it would yield the material of the embedding dielectric build-up layers. Thus, during a curing of the embedding dielectric build-up layers, such as layers 126 and 128, while the embedding dielectric build-up layers may shrink and flow during and after curing, the

material of the spacer layer would shrink less and flow less during such curing according to embodiments, in this way ensuring a more reliable positioning of the microelectronic components being embedded within the embedding dielectric build-up layers after a curing of the layers 126 and 128 has been effected. A spacer layer according to embodiments may further: (1) be made of a material that is adapted to bond with the underlying conductive layer of a substrate, such as, for example, by being laminated thereon or through other bonding processes as would be recognized by one skilled in the art; (2) have a viscosity adapted to allow the spacer material to flow within discontinuities present in the underlying conductive layer of the substrate; (3) have a dielectric constant that is within about 20% of a dielectric constant of the embedding dielectric build-up layer corresponding thereto, and, preferably, within a percentage between about 5% and about 20% of a dielectric constant of the embedding dielectric build-up layer corresponding thereto; (4) made of a material having a cure temperature that is lower than or equal to a cure temperature of the pre-cure dielectric material; and/or (5) made of a material that is adapted to be laser drilled for the formation of via holes. According to one embodiment, the material of the spacer layer may have a dielectric constant that is substantially identical to a dielectric constant of the embedding dielectric build-up layer corresponding thereto. According to a preferred embodiment, the spacer layers 138 and 140 are made of a prepreg material, such as, for example, a polyamide prepreg or an epoxy prepreg having a silicon or glass filler. Where the spacer layer includes a prepreg according to an embodiment, a choice of the specific type of prepreg would depend on application requirements, such as, for example, requirements (1)-(5) listed above for the material of the spacer layer. An embodiment contemplates using prepreg (GX13-PP) along with ABF (GX13) as the dielectric build-up layer overlying the same. A presence of particulate matter in a prepreg according to an embodiment, such as, for example, the presence of silicon oxide particles, allow the prepreg to be more viscous than a material of the corresponding embedding dielectric build-up layer before and during curing of the embedding dielectric build-up layer. Embodiments are not limited to the use of a spacer layer made of a single material, but include within their scope a spacer layer made of differing materials throughout a volume thereof, such as, for example, a spacer layer including a number of sublayers of differing materials.

The spacer layer advantageously allows the maintenance of a predetermined separation between two successive conductive layers sandwiching a given embedding dielectric build-up layer therebetween. The predetermined separation refers to a total thickness of all of the layers present between the two successive conductive layers mentioned above. Hereinafter, for ease of reference, the totality of all of the layers present between the two successive conductive layers will be referred to as "component support layer," which is shown by way of example in Fig. 6 as either component support layer 142 including spacer layer 138 and embedding dielectric build-up layer 126, or as component support layer 144 including spacer layer 140 and embedding dielectric build-up layer 128. The predetermined separation according to an embodiment in particular refers to a minimum thickness of the component support layer adapted to achieve a desired signal integrity within the substrate. An exemplary value for the predetermined separation is about 30 microns. Such minimum thickness may be determined among others from an effective dielectric constant of the component support layer. By "effective dielectric constant," what is meant in the context of the instant description is a value of a dielectric constant applicable to the component support layer as if the component support layer were made of a single material throughout a volume thereof. In determining the predetermined separation, both capacitance and resistance of the embedded components may be taken into consideration. A person skilled in the art would recognize that resistance would need to be relatively high in order to prevent a high leakage and capacitance/dielectric constant needs to be relatively low to prevent a high signal impedance. A determination of the predetermined separation would then result from impedance matching, which would be brought about by ascertaining that there are no significant impedance changes along signal pathways through the substrate. Impedance matching is well known in the art. Choosing a spacer layer having a material that has a similar dielectric constant to that of the capacitor dielectric build-up layer would allow the spacer layer to effectively replace the capacitor dielectric-build-up layer for electrical purposes. Another factor in determining the predetermined separation is a consideration of a density and thickness of the underlying conductive layer 114 by ensuring that the spacer layer is thick enough to penetrate in discontinuities present in layer 114. The use of a spacer layer according to embodiments, such as spacer layers 138 and 140, allows the maintenance of a predetermined separation as defined above while advantageously decreasing a thickness of

the embedding dielectric build-up layer such as layers 126 and 128, respectively. Less embedding dielectric build-up layer along with the use of a spacer layer advantageously lead to a reduced viscous flow of the component support layer during a curing of the embedding dielectric build-up layer, thus bringing about a more reliable positioning of the embedded components in the final product. According to embodiments, a spacer layer may have a thickness that is about 30% to about 70% of the component support layer.

Reference will next be made to Figs. 1-5, which show different stages in the formation of a substrate such as substrate 102 of Fig. 6 described above. Although Figs. 1-5 show the provision of a component support layer, including spacer layer and embedding dielectric build-up layer, on one side of an intermediate substrate, such as intermediate substrate 103 of Fig. 1, it is to be understood that processes described in relation to Figs. 1-5 may be used to provide component support layers on both sides of an intermediate substrate. In addition, the processes described in relation to Figs. 1-5 may equally as well be applied to provide any number of component support layers on any given side of an intermediate substrate, as would be recognized by one skilled in the art. To the extent that the structures shown in Figs. 1-5 represent stages in the fabrication of a substrate such as substrate 105 of Fig. 6, components in Figs. 1-5 corresponding to similar components in Fig. 6 have been indicated with like reference numerals. It is further noted that a depiction of the conductive vias shown in Fig. 6 have been omitted from the structures of Figs. 1-5 for the sake of clarity of illustration.

Referring first to Fig. 1, a method embodiment comprises providing an intermediate substrate, such as intermediate substrate 103. By "intermediate substrate," what is meant in the context of the instant description is a multilayer substrate structure prior to the provision thereon of an embedding dielectric build-up layer. The intermediate substrate in Fig. 1 includes the core layer 108, the conductive layers 110, 112, 114 and 116, and the dielectric build-up layers 122 and 124 already described above with respect to the embodiment of Fig. 6. The provision of an intermediate substrate such as substrate 103 is well known in the art, and, as a result, a fabrication of the same will not be described herein. A provision of an intermediate substrate as shown by way of example in Fig. 1 entails the provision of conductive layer 114, which corresponds to underlying conductive layer 114 as described above in relation to Fig. 6.

Referring next to Fig. 2, a method embodiment comprises providing a spacer layer, such as spacer layer 138, onto the underlying conductive layer, such as underlying conductive layer 114. Preferably, as noted above in relation to Fig. 6, the spacer layer includes a prepreg layer. The spacer layer 138 may be laminated onto the underlying conductive layer 114 in a well known manner. According to a preferred embodiment, the provision of the spacer layer comprises laminating a prepreg layer 138 onto the underlying conductive layer 114. Lamination of the prepreg layer may take place according to an embodiment within a temperature range of about 100 degrees Celsius to about 150 degrees Celsius. The spacer layer may be provided onto the underlying conductive layer in any other well known manner, such as through the use of a spin-on/spray-on and cure technique, depending on the material of the spacer layer. A determination of process parameters for the lamination of a prepreg layer onto a conductive layer would depend among other things on the type of prepreg material being used, as would be recognized by one skilled in the art. Embodiments are not, however, limited to the provision of a spacer layer via lamination, and include within their scope the provision of a spacer layer according to any one of well known methods of providing one layer onto another layer as would be recognized by one skilled in the art. During a provision of the spacer layer 138, preferably, the spacer layer possesses a viscosity of allow a flowing of a material of the same in between irregularities on the surface of the underlying conductive layer 114. After the provision of spacer layer 138, the spacer layer may be provided with conductive vias (shown in Fig. 6), such as, for example, by way of laser drilling and electroplating, in a well known manner.

Referring next to Fig. 3, a method embodiment comprises providing a pre-cure dielectric build-up layer, such as pre-cure dielectric build-up layer 146, onto the spacer layer, such as onto spacer layer 138. The pre-cure dielectric build-up layer 146 shown in Fig. 3 in its "pre-cure" form, that is, as described above, in a phase prior to its full curing after embedding of components 104 therein (as will be described in further detail in relation to Figs. 4 and 5). The pre-cure dielectric build-up layer 146 may correspond to a pre-cure form of any of possible materials listed for the embedding dielectric build-up layer 126 described in relation to Fig. 6 above. Preferably, the pre-cure dielectric build-up layer 146 is laminated onto the spacer layer 138 in a well known manner. Optionally, the pre-cure dielectric build-up layer 146 may be partially cured in a well known manner in

order to increase its viscosity prior to and during an embedding of components 104 therein.

Referring next to Fig. 4, a method embodiment comprises embedding active or passive components, such as components 104, within the pre-cure dielectric build-up layer, such as layer 146. Embedding may take place according to any one of conventional methods for embedding active or passive components within a dielectric layer, such as, for example, by using a mounter 148.

Referring next to Fig. 5, a method embodiment comprises curing the pre-cure dielectric build-up layer after embedding, such as curing the layer 146. Curing may take place according to any one of conventional methods for curing a dielectric material. For example, the structure shown in Fig. 4 may be placed in a cure oven at a temperature range of about 200 degrees Celsius in order to bring about a curing of the dielectric layer 146 in a well known manner. A curing of the pre-cure dielectric build-up layer 146 yields the embedding dielectric build-up layer 126 as described in relation to Fig. 6 above. A curing of the pre-cure dielectric build-up layer 146 may also bring about a curing of the spacer layer. Before and during curing, both the pre-cure dielectric build-up layer and the spacer layer may exhibit some flow, and the components 104 may sink into the pre-cure dielectric build-up layer, and, in some embodiments, into the spacer layer as shown in Fig. 5. After curing, the embedding dielectric build-up layer may be provided with conductive vias (shown in Fig. 6), such as, for example, by way of laser drilling and electroplating, in a well known manner. Subsequent to curing, additional layers, such as additional conductive and dielectric build-up layers may be provided onto the embedding dielectric build-up layer 126 in a conventional manner, and provided with conductive vias in a conventional manner, in order to yield a substrate similar to substrate 102 of Fig. 6.

Advantageously, embodiments provide a spacer layer between an underlying conductive layer and an embedding dielectric build-up layer of a multilayer substrate in order to mitigate positional errors of components embedded in the build up layer while maintaining a predetermined separation between two successive conductive layers sandwiching the embedding dielectric build-up layer therebetween. Moreover, advantageously, embodiments provide a mitigation of positional errors while at the same time allowing the use of existing and established processes for forming a multilayer substrate. Furthermore, advantageously, embodiments allow the use of enough dielectric

build-up material as the embedding build-up layer to provide adequate adhesion of the embedded components to the rest of the substrate.

Referring to Fig. 7, there is illustrated one of many possible systems 900 in which embodiments of the present invention may be used. In one embodiment, the electronic assembly 1000 may include a microelectronic package such as package 100 of Fig. 6. Assembly 1000 may further include a microprocessor. In an alternate embodiment, the electronic assembly 1000 may include an application specific IC (ASIC). Integrated circuits found in chipsets (e.g., graphics, sound, and control chipsets) may also be packaged in accordance with embodiments of this invention.

For the embodiment depicted by Fig. 7, the system 900 may also include a main memory 1002, a graphics processor 1004, a mass storage device 1006, and/or an input/output module 1008 coupled to each other by way of a bus 1010, as shown. Examples of the memory 1002 include but are not limited to static random access memory (SRAM) and dynamic random access memory (DRAM). Examples of the mass storage device 1006 include but are not limited to a hard disk drive, a compact disk drive (CD), a digital versatile disk drive (DVD), and so forth. Examples of the input/output module 1008 include but are not limited to a keyboard, cursor control arrangements, a display, a network interface, and so forth. Examples of the bus 1010 include but are not limited to a peripheral control interface (PCI) bus, and Industry Standard Architecture (ISA) bus, and so forth. In various embodiments, the system 90 may be a wireless mobile phone, a personal digital assistant, a pocket PC, a tablet PC, a notebook PC, a desktop computer, a set-top box, a media-center PC, a DVD player, and a server.

The various embodiments described above have been presented by way of example and not by way of limitation. Having thus described in detail embodiments of the present invention, it is understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many variations thereof are possible without departing from the spirit or scope thereof.

WHAT IS CLAIMED IS:

1. A microelectronic substrate comprising:

a conductive layer;

a spacer layer disposed onto the conductive dielectric layer;

a dielectric build-up layer disposed onto the spacer layer, the spacer layer being made of a material that has a lower shrinkage than a material of the embedding dielectric-build-up layer during curing, and a higher viscosity than a material of the embedding dielectric build-up layer in its pre-cure form and during curing; and

active or passive microelectronic components embedded within the dielectric build-up layer.

2. The substrate of claim 1, wherein the spacer layer comprises a prepreg layer.

3. The substrate of claim 1, wherein the spacer layer has a thickness that is between about 30% and about 70% of a thickness of the spacer layer and of the dielectric build-up layer combined.

4. The substrate of claim 1, wherein the prepreg layer comprises one of a polyamide and an epoxy resin and a filler material.

5. The substrate of claim 1, wherein the conductive layer is a second conductive layer and the dielectric build-up layer is a second dielectric build-up layer, the substrate further comprising a core layer, a first conductive layer disposed onto the core layer, and a first dielectric build-up layer disposed onto the first conductive layer, the second conductive layer being disposed onto the first dielectric build-up layer.

6. The substrate of claim 5, wherein the core comprises an organic material.

7. The substrate of claim 5, wherein the dielectric build-up layers comprise ABF.

8. A microelectronic package comprising:

a microelectronic substrate comprising:

a conductive layer;

a spacer layer disposed onto the conductive dielectric layer;

a dielectric build-up layer disposed onto the spacer layer, the spacer layer being made of a material that has a lower shrinkage than a material of the embedding dielectric-build-up layer during curing, and a higher viscosity than a material of the embedding dielectric build-up layer in its pre-cure form and during curing; and

active or passive microelectronic components embedded within the dielectric build-up layer; and

a microelectronic die mounted onto the microelectronic substrate.

9. The package of claim 8, wherein the spacer layer comprises a prepreg layer.

10. The package of claim 8, wherein the spacer layer has a thickness that is between about 30% and about 70% of a thickness of the spacer layer and of the dielectric build-up layer combined.

11. The package of claim 8, wherein the prepreg layer comprises one of a polyamide and an epoxy resin and a filler material.

12. The package of claim 8, wherein the conductive layer is a second conductive layer and the dielectric build-up layer is a second dielectric build-up layer, the substrate further comprising a core layer, a first conductive layer disposed onto the core layer, and a first dielectric build-up layer disposed onto the first conductive layer, the second conductive layer being disposed onto the first dielectric build-up layer.

13. The package of claim 12, wherein the core comprises an organic material.

14. The package of claim 12, wherein the dielectric build-up layers comprise ABF.

15. A method of forming a microelectronic substrate comprising:

providing a conductive layer;

providing a spacer layer onto the conductive layer;

providing a pre-cure dielectric build-up layer onto the spacer layer, the spacer layer being made of a material that has a lower shrinkage than a material of the embedding dielectric-build-up layer during curing, and a higher viscosity than a material of the embedding dielectric build-up layer in its pre-cure form and during curing;

embedding active or passive components within the pre-cure dielectric build-up layer; and

curing the pre-cure dielectric build-up layer after embedding to yield an embedding dielectric build-up layer.

16. The method of claim 15, wherein providing a spacer layer comprises providing a prepreg layer.

17. The method of claim 15, wherein providing a spacer layer comprises laminating the spacer layer onto the conductive layer.

18. The method of claim 15, wherein providing a spacer layer comprises providing a spacer layer having a thickness that is between about 30% and about 70% of a thickness of the spacer layer and of the embedding dielectric build-up layer combined.

19. The method of claim 15, wherein the conductive layer is a second conductive layer and the embedding dielectric build-up layer is a second dielectric build-up layer, the method further comprising:

providing a core layer;

providing a first conductive layer onto the core layer;

providing a first dielectric build-up layer onto the first conductive layer, wherein the second conductive layer is disposed onto the first dielectric build-up layer.

20. The method of claim 19, wherein the core comprises an organic material.

21. The method of claim 19, wherein the dielectric build-up layers comprise ABF.

22. The method of claim 15, wherein providing a pre-cure dielectric build-up layer comprises laminating the pre-cure dielectric build-up layer onto the spacer layer.

23. The method of claim 15, further comprising partially curing the pre-cure dielectric build-up layer prior to embedding.

24. A method of providing a microelectronic package comprising:

providing a microelectronic substrate including:

providing a conductive layer;

providing a spacer layer onto the conductive layer;

providing a pre-cure dielectric build-up layer onto the spacer layer, the spacer layer being made of a material that has a lower shrinkage than a material of the embedding dielectric-build-up layer during curing, and a higher viscosity than a material of the embedding dielectric build-up layer in its pre-cure form and during curing;

embedding active or passive components within the dielectric build-up layer; and

curing the dielectric build-up layer after embedding;

mounting a microelectronic die onto the microelectronic substrate.

25. The method of claim 24, wherein the spacer layer comprises a prepreg layer.

26. The method of claim 24, wherein the spacer layer has a thickness that is between about 30% and about 70% of a thickness of the spacer layer and of the dielectric build-up layer combined.

27. The method of claim 8, wherein the prepreg layer comprises one of a polyamide and an epoxy resin and a filler material.

28. The method of claim 8, wherein the conductive layer is a second conductive layer and the dielectric build-up layer is a second dielectric build-up layer, the substrate further comprising a core layer, a first conductive layer disposed onto the core layer, and a first dielectric build-up layer disposed onto the first conductive layer, the second conductive

layer being disposed onto the first dielectric build-up layer.

29. A system comprising:

an electronic assembly including:

a microelectronic substrate comprising:

a conductive layer;

a spacer layer disposed onto the conductive dielectric layer;

a dielectric build-up layer disposed onto the spacer layer, the spacer layer being made of a material that has a lower shrinkage than a material of the embedding dielectric-build-up layer during curing, and a higher viscosity than a material of the embedding dielectric build-up layer in its pre-cure form and during curing; and

active or passive microelectronic components embedded within the dielectric build-up layer; and

a main memory coupled to the electronic assembly.

30. The system of claim 29, wherein the spacer layer comprises a prepreg layer.

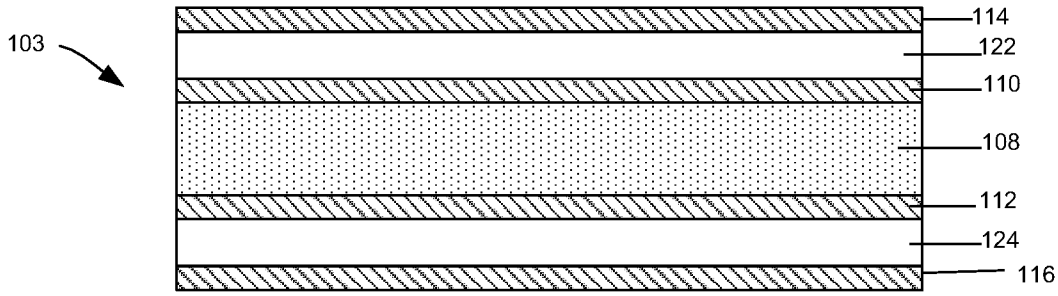

Fig. 1

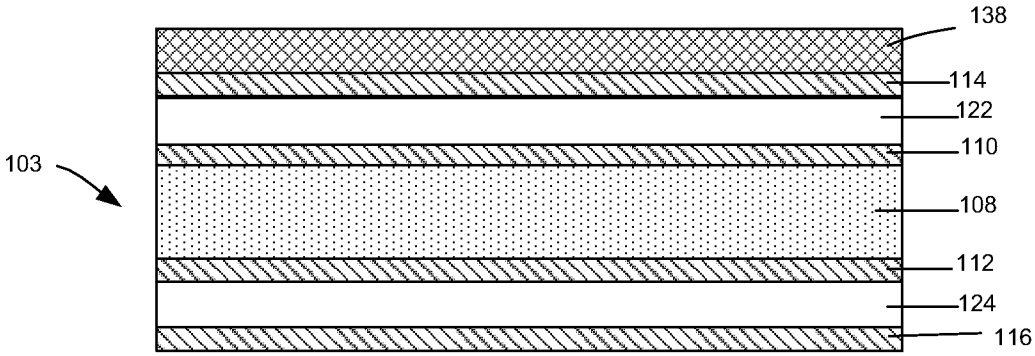

Fig. 2

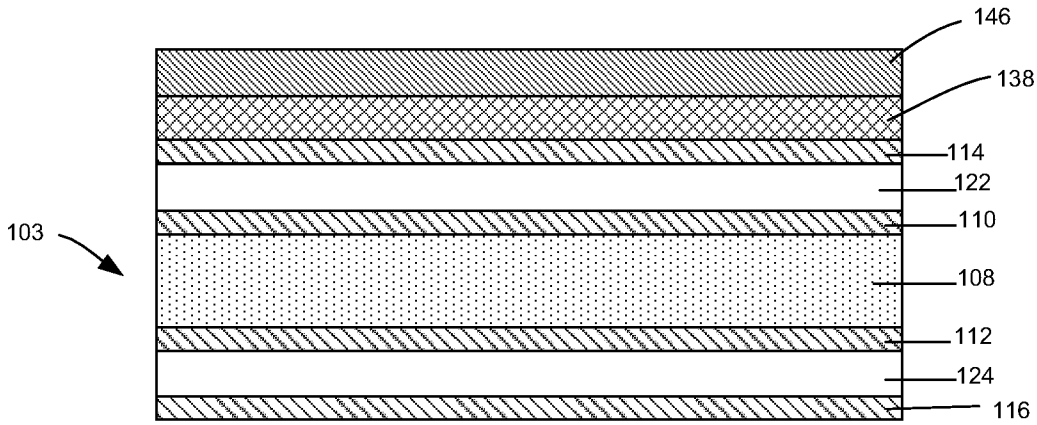

Fig. 3

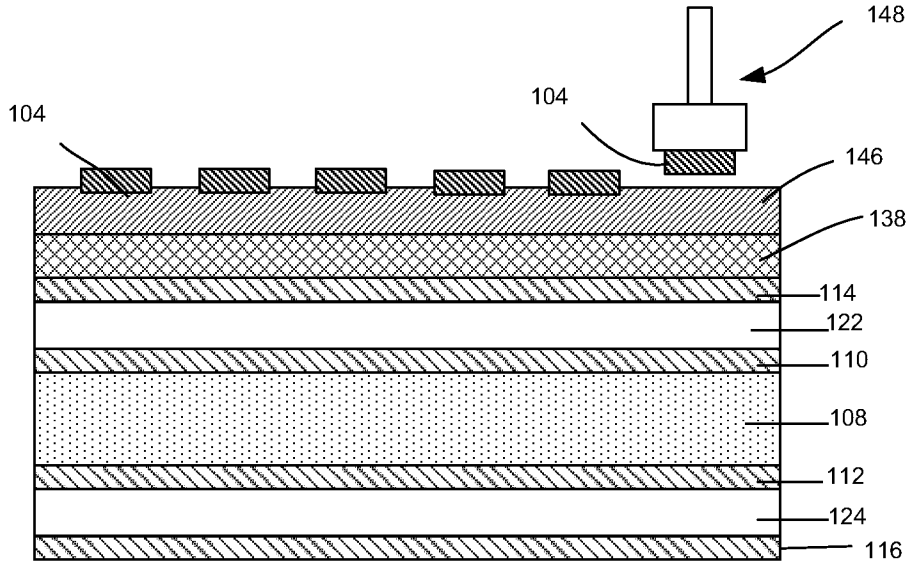
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Fig. 4

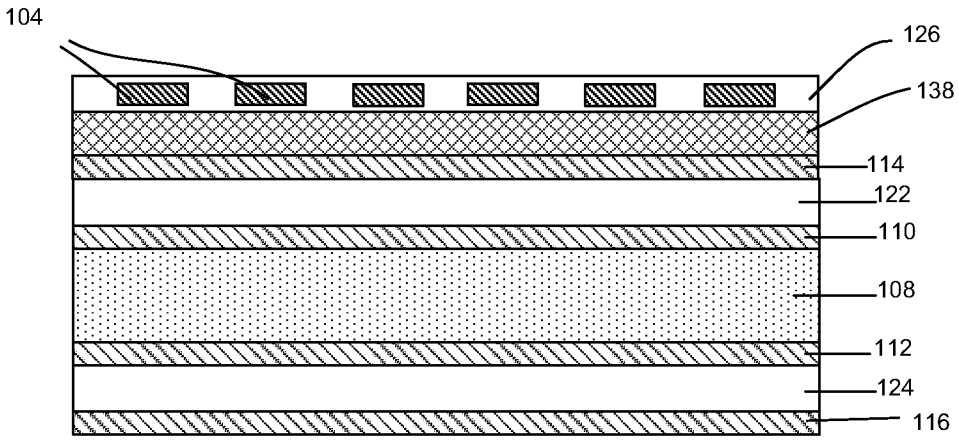
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Fig. 5

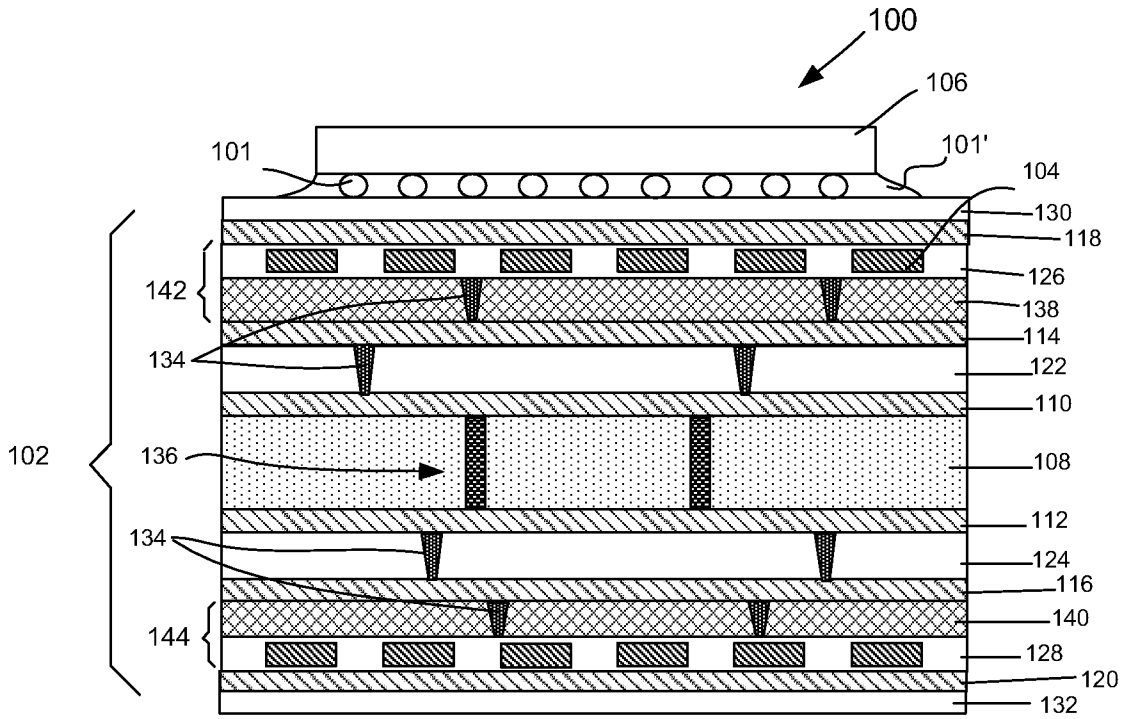
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Fig. 6

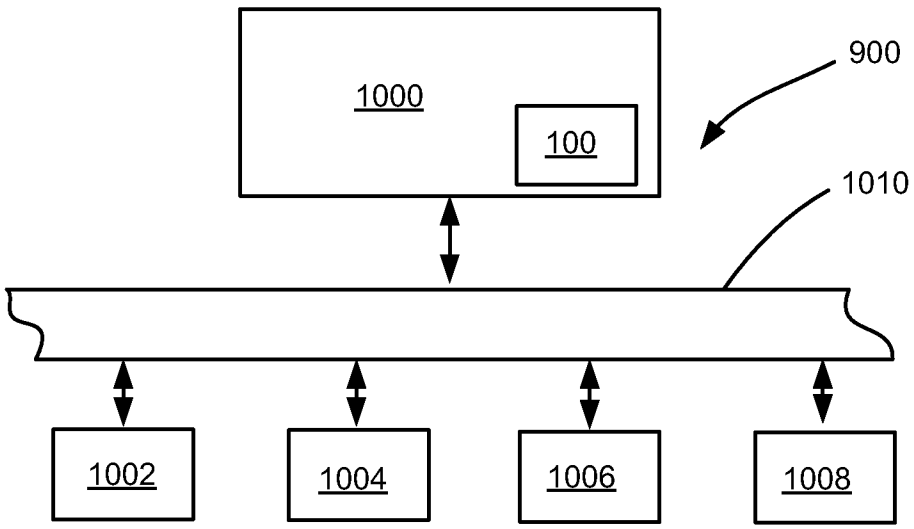
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Fig. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2007/085071

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/31(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 8 H01L 21/31

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean Utility models and applications for Utility models since 1975

Japanese Utility models and applications for Utility models since 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

e-KIPASS(KIPO Internal); "conductive layer", "spacer layer", "dielectric", "viscosity"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6,291,763 B1 (SHIGERU NAKAMURA) 18 September 2001 see the abstrate, claims 1-15, Figs. 1-3	1-30
A	US 6,879,507 B2 (TODD R. ABBOTT) 12 April 2005 see the abstract, claims 1,2, Figs. 1-13	1-30
A	US 6,019,658 A (PAUL N. LUDWIG et al.) 01 February 2000 see the abstract, claim 1, Figs. 4 -7	1-30

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
09 MAY 2008 (09.05.2008)	**09 MAY 2008 (09.05.2008)**

Name and mailing address of the ISA/KR

Korean Intellectual Property Office
Government Complex-Daejeon, 139 Seonsa-ro, Seo-gu, Daejeon 302-701, Republic of Korea

Facsimile No. 82-42-472-7140

Authorized officer

BAEK, Yang Gyu

Telephone No. 82-42-481-5732

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2007/085071

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US06291763 B1	18.09.2001	JP12294306 JP13102104	20.10.2000 13.04.2001
US06879507 B2	12.04.2005	US20040029331A1 US2005167700A1	12.02.2004 04.08.2005
US6019658 A	01.02.2000	NONE	