ABSTRACT: A bowling scorer including pinfall-counting system for receiving information relative to the number of pins knocked down after the first ball in a frame and relative to the number of pins knocked down by both balls in a frame and for providing an indication of first ball pin count only and second ball pin count only. The system includes a binary counter and a memory for receiving the complement of first ball pin count from the count. The provision of second ball only pin count is accomplished by loading the counter complement of first ball pin count into the counter from the memory, a count of one is added thereto and thereafter, the pinfall information relative to pins knocked down by both balls is provided to the counter resulting in the same containing second ball only pin count.
INCREMENTAL PINFALL SYSTEM

BACKGROUND OF THE INVENTION

Recent years have seen a number of proposals for automatic scoring systems to provide the bowler with a variety of information relative to his game. In accordance with the regulation of the American Bowling Congress, such automatic scoring systems must provide a permanent record of the complete pinfall history for each bowler.

In implementing this requirement, some systems have proposed indications of first ball only pin count and both ball pin count while others have provided first ball only pin count and second ball only pin count. Finally, some proposals have been adaptable to either.

However, the American Bowling Congress has generally felt it to be preferably to utilize the system wherein first ball only pin count and second ball only pin count are recorded and such a system is known in the art as incremental pinfall scoring.

The copending application of Jerome F. Walker, U.S. Ser. No. 612,665, filed Jan. 30, 1967, now U.S. Pat. No. 355,939, entitled "Electronic Scorer for Bowling Games" and assigned to the same assignee as the instant application there is disclosed a system wherein incremental pinfall information is computed and printed. The system works well for its intended purpose but its nature is such that it has one possible drawback insofar as a bowler may become confused when using the manual system and is not familiar with the system therein disclosed.

More specifically, the Walker application system for computing incremental pinfall during manual entry requires that first ball pinfall information only be provided to the computer and for second ball in a frame, both ball pin count be provided. Thereafter, the system records second ball only pin count.

Inasmuch as the system records second ball pinfall information incrementally, it has been considered that it would be more consistent also to enter second ball information incrementally during a manual entry sequence to avoid confusing those making manual entries.

SUMMARY OF THE INVENTION

This invention seeks to provide a new and improved incremental pinfall counting and indicating system.

In the exemplary embodiment, the system is particularly suited for use with an electronic scoring system such as that disclosed in the above-identified Walker application. In the exemplary embodiment of the invention, there is provided a four-bit binary counter counting on a count of 16 and which is adapted to receive a string of pulses equal in number to the number of pins downed by the first ball in a frame or by both balls in a frame. Upon the completion of the receipt of the string of pulses following a first ball in a frame, the binary number contained in the counter is equal to the first ball only pin count. Thereafter, this number is decoded and recorded in accordance with American Bowling Congress requirements, and the complement of the binary-coded number contained in the pinfall counter is then retained in a portion of a bowler's memory reserved for that purpose.

Following the second ball in a frame, the first ball pinfall complement is read back into the pinfall counter. Thereafter, a count of one is added to the count contained in the pinfall counter and this is, in turn, followed by the receipt of a string of pulses equal in number to the pinfall achieved by both balls in a frame. As a result, following the second ball in a frame, the pinfall counter will have received information corresponding to a count equal to decimal 16 plus second ball only pinfall information. Instead, as only a four-bit counter is used the binary digit representing 16 (fifth bit) will be lost and the count then contained in the pinfall counter will equal the second ball only pin count. This quantity is then decoded and recorded.

Other objects and advantages of the invention will become apparent from the following specification taken in conjunction with the following drawings.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a computing system in which the invention is particularly suited to be used;

FIG. 2 is comprised of FIGS. 2a and 2b with FIG. 2b to be disposed to the right of FIG. 2a and is a logic diagram of a 10-bit recirculating shift register used in the invention;

FIG. 3 is a logic diagram of a four-bit pinfall counter used in the invention;

FIG. 4 is a block diagram of a memory plane and associated circuitry utilized in the invention;

FIG. 5 is a logic diagram illustrating gating employed in conjunction with the direction of information to the memory;

FIG. 6 is a logic diagram similar to FIG. 5;

FIG. 7 is a logic diagram illustrating a source of manual entry pinfall information;

FIG. 8 is a block diagram of a bowler score cycle control; and

FIG. 9 is a logic diagram of certain gating employed in the practice of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

One form of a bowling score computer in which an exemplary embodiment of an incremental pinfall-scoring system may be used is shown in block form in FIG. 1 and is generally of the type disclosed in the above-identified Walker application. For specific details of the environment in which the invention is used and not set forth hereinafter in detail, reference may be had to the Walker application.

The computing system is operative for scoring a plurality of lanes and, in its preferred form, to control the scoring of four lanes. To this end, there are provided four sets of pin detecting means 20, 22, 24 and 26, one for each lane. Operative in conjunction with respective ones of the pin detecting means 20, 22, 24 and 26 are respective pinfall buffers and steering gates 28, 30, 32 and 34. The pinfall buffers 28–34 receive information from the respective pin detecting means 20–26 relative to the position of standing pins. This information is gated through the steering gates 28–34 respectively to a pinfall register 36 in such a manner that the pinfall register 36 receives the information from only one lane at a time. The purpose of the pinfall buffers is to preserve pinfall information for short periods of time in the event that an automatic pinsetter having the pin-detecting means thereon or independent pin-detecting means thereon or independent pin-detecting means used in conjunction with the pinsetter is cycled before the information may be channeled to the pinfall register 36. Additionally, the pinfall buffers 28–34 serve to preserve pinfall achieved by the first ball in a frame such that it may be utilized for computing the pinfall corresponding to the pinfall of the latter will indicate the particular position of each pin and whether that pin is standing or down. The infor-
mation relative to all pins on a lane is read simultaneously into the pinfall register by control of the steering gates 28-34 as mentioned above. The arrangement of standing and fallen pins as it appears in the information contained within the pinfall register 36 is sensed by split detecting means 42. If the arrangement of the pins is such that a split exists, the split detecting means 42 will send the same to ultimately cause the printing of a split symbol on a score sheet.

In order to determine the number of fallen pins for box score purposes and for addition to the bowler's cumulative score, an arithmetic register 44 is provided. The arithmetic register consists of a pinfall counter 46 and a three decade binary coded decimal up counter 48. The pinfall counter 46 counts the pins achieved by the first ball in each frame and by means of a system associated therewith according to the invention, also counts the pinfall achieved solely by the second ball in a frame except in the case of a spare. This information is then printed in a box score position on a score sheet as is well known.

The binary-coded decimal up counter 48 adds the pinfall achieved by both balls in a frame to the bowler's cumulative score such that the cumulative score may be printed at a frame score position on a score sheet as is well known.

A pinfall register control 50 causes the pinfall information present in the pinfall register 36 to be placed in the pinfall counter 46 after each ball in a frame and into the binary coded decimal up counter 48 after either a strike in a frame, a second ball in a frame, or after the first ball in a frame preceded by updating frame in which a spare was achieved.

A bowler state control 52 includes a bowler state register which contains information relative to the state or relevant scoring history of a bowler's game. The bowler state control 52 is also provided with a bowler's state decoding matrix which decodes the information contained in the bowler state register. Finally, the bowler state control 52 includes bowler state updating matrix which redetermines and updates the bowler state information contained in the bowler state register after each ball in a frame is rolled. The bowler state information contained in the bowler state control is utilized to control the computation and printing of bowler's scores. In this connection, a bowler's score cycle control 54 receives bowler state information from the bowler state control and in conjunction with a computer cycle control 56 causes such functions as may be necessary to compute a bowler's score and enable the reading out of a bowler's score such that a printed record thereof will be formed.

When it is necessary to score a bowler, the bowler's score cycle control 54 and the computer cycle control 56 issue appropriate signals to the printer cycle control 58 which controls four printers 60, 62, 64 and 65 associated with respective ones of the four lanes which are in operation to score. The printer cycle control 58 in conjunction with the computer cycle control directs one of the printers 60-66 to print in a thousands, hundreds, tens or units column within a frame column and to print at a box score level or at a frame score level in each scoring column. The particular frame column which pinfall information is to be printed is determined by a frame counter 68, a printer frame control 70 and a frame selection matrix 72 together with the computer cycle control 56. Frame information relative to the bowler to be scored is contained in the frame counter 68. The frame information therein corresponds to the frame in which the bowler is bowling as opposed to the frame in which he is to be scored. It will be apparent that this is necessary distinction as when a bowler working on a spare, a strike or two successive strikes, the cumulative score for the frame in which the mark or marks were made will not be complete until the bowler has rolled one or more balls in one or more succeeding frames.

The printer frame control 70 receives information from the frame counter relative to the bowler's current frame. The computer cycle control 55 in conjunction with the bowler state control 52 causes the printer frame control 70 to assume a condition indicative of the frame in which a printed cumulative score is to be placed. The resulting condition of the printer frame control 70 is sensed by the frame selection matrix 72 which thereby issues a signal to a particular one of the printers 60-66 to direct the same to print the cumulative score in a particular frame column while the computer cycle control 56 enables the particular one of the printers 60-66 to print.

A character selection matrix 74 is arranged to sense the condition of the pinfall counter 46. In the case of box scores, the condition of the pinfall counter 46 is decoded by the character selection matrix 74 which, in turn, causes the printer cycle control 58 to direct a particular printer 60-66 to print a particular character. In the case of printing cumulative scores, each digit of the cumulative score is decoded individually and printed in a serial manner. As set forth in detail in the Walker application, the printing of such digits occurs with the thousands digit being printed first if necessary, the hundreds digit printed second, the tens digit printed third and the units digit printed last. In order to achieve the serial decoding of the digits of the cumulative score in the required order, the printer cycle control 58 causes the cumulative score information contained in the binary-coded decimal up counter 48 to be shifted, one digit at a time, into the pinfall counter 46 where it is decoded by the character selection matrix 74 and ultimately printed by a selected one of the printers 60-66. In the printing of cumulative scores, the printer's cycle control has the additional function of suppressing leading or nonsignificant zeros.

In order to direct a selected one of the printers 60-66 to print in a selected bowler lane, bowler identification means 76 are provided. The bowler identification means 76 serve to direct a corresponding printer 60-66 to print at a particular box score level for a particular bowler. When it is necessary to print at the frame score level for that bowler, the bowler identification means 76 together with the computer cycle control 56 serve to indicate that printing should be accomplished at the frame score level.

The bowler identification means 76 provide yet another function. A memory 78 includes a word for each of the 24 bowlers that may be accommodated by this system. The bowler identification means 76 serve to connect the appropriate bowler word in the memory 78 to the computer when that bowler is to be scored.

Each bowler word therein includes information relative to bowler's cumulative score, the frame in which he is bowling, the state of the game, and the complement of the pinfall achieved by his first ball in a frame. Through appropriate gating 80, the particular bowler word is selected and the frame information that is in each word is directed to the frame counter 68. By the same token, the state information in the selected bowler word is directed to the bowler state control 52 and the bowler score information is directed to binary coded decimal up counter 48. Finally, the first ball pinfall complement is directed to the pinfall counter 46.

The first three types of information mentioned above are used in each respective register to control the computation and read out of a bowler's score in the manner previously described, is then updated and subsequently written back into the memory 78. In the case of the first ball pinfall complement information, the same is used following the second ball in a frame for ascertaining pinfall achieved by the second ball only in that frame.

Since there may be as many as four different bowler identification at any given instant (one on each of the four lanes), and the computer is arranged to handle the scoring of only one bowler at a time, means are provided in the form of a scanning cycle control 82 for permitting association of the computer with but a single bowler word in the memory 78 at any given time. The scanning cycle control 82 scans the pin detection systems 20-26 together with the manual input system 40 and senses when one of the aforementioned information sources is ready to provide information for computation. When such a
situation is detected, the scanning cycle control 82 locks on that particular information source and enables the gating 80 to select only the bowler word or the bowler associated with that particular source.

When the scanning cycle control 82 is locked on a particular information source, it, together with the computer cycle control 56 will cause the team total information from the memory 78 for the selected bowler to be directed to the various registers as mentioned previously. Additionally, the computer cycle control 56 will cause the bowler score cycle control 54 to score the bowler which will cause the printing cycle control 58 to cause such printing as may be necessary. In the latter respect, the scanning cycle control 82 causes computer cycle control to select the particular one of the printers 60–66 for the lane for which the pinfall information is being made available or for the team with which the bowler is associated. Upon completion of the scoring of a bowler, the computer cycle control 56 causes such updating of bowler information as may be necessary and the writing of such information back into the memory 78.

The computer is also provided for computing and printing running team totals when incurred including the team total control 64, a frame buffer 66, a frame comparator 88 and a binary-coded decimal down counter 90. The various instrumentalties used and enumerated above are not of significance with respect to the instant invention and thus will not be described further. It is merely sufficient to note that the memory 78 includes four words for team totalizing purposes which words receive team total information from binary-coded decimal up counter 38 as well as the least significant bit of the pinfall counter 46 in the manner generally set forth in the Walker application except as expressly modified hereinafter.

In conjunction with the provision of team totals, the computer also includes means whereby the manual pinfall input 40 may be used to provide handicap information for each team. Again, there is little need to explore the logic utilized for this purpose in detail, it being sufficient to note that the memory 78 additionally includes four words for handicap information.

Finally, the computer additionally includes a pinsetter control 92 which receives information from the foul detection verification means 38 together with information from the bowler's state control 52 in the scanning cycle control 82. Upon the occurrence of a first ball foul, the pinsetter control 92 under the direction of the scanning cycle control 82 will cause the pinsetter on the lane in which the foul occurred to spot a new set of pins and prepare itself to undergo a second ball cycle when the next ball is rolled. Thus, when the second ball in a frame is rolled, if pins are left standing, the pinsetter will undergo a second ball cycle and spot a new set of pins in readiness for the next bowler. Similarly, in certain 10th frame situations wherein bonus balls are rolled, the pinsetter control 92 under direction of the bowler state control 52 will cause the pinsetter to undergo a second ball cycle after the third ball in the tenth frame is rolled such that a new set of pins will be spotted by the pinsetter in readiness for the following bowler or the initiation of a new game. This arrangement automatically anticipates recycling of the pinsetters in such situations and thereby speeds up the bowling game.

Turning now to FIGS. 2a and 2b, there is seen a pinfall register generally similar to the pinfall register disclosed in the above-identified Walker application. As mentioned previously, the pinfall register receives pinfall information from each of the lanes as well as manual entry information. In the exemplary embodiment, the pinfall register is comprised of 10 flip-flops PR1–PR10 corresponding to the number one pin through the number 10 pin respectively.

Each flip-flop PR1–PR10 includes an input line 100 which is taken from the output of a gate performing an OR function (not shown) which, in turn, receives its inputs from each of the pinfall buffers and steering gates 28–34. The arrangement is such that whenever the corresponding pin on the particular frame for which computation is taking place is standing, that flip-flop PR1–PR10 in the pinfall register will be set. That is, a reset one of the flip-flops PR1–PR10 corresponds to a downed pin while a set flip-flop corresponds to a standing pin.

Each of the flip-flop PR1–PR10 additionally includes an input on a line 102 taken from the output of a gate 104 which performs an AND function. One input to each of the gates 104 is taken from the error correction system in a manner to be described in greater detail hereinafter while the second is received on a pulse forming input which is adapted to receive a READ ENTRY SWITCH signal from the computer cycle control in a manner described in the Walker application.

The flip-flops PR1–PR10 are further interconnected to form a 10-bit recirculating shift register by means of gates 106 and 108, both performing AND functions, which are interconnected as inputs to the set and reset sections of each flip-flop PR1–PR10 and which receive their inputs from the reset and set sections, respectively, of the next lowest flip-flop in the series, with the exception of the flip-flop PR1, which receives corresponding inputs from the flip-flop PR10. Additionally, one output of the flip-flop PR10 is connected through gating (not shown) as an input to both the pinfall counter and the binary-coded decimal up counter.

Each of the gates 106 and 108 is provided with an enabling input from pulse-forming gate 110, which, in turn, is driven by the pinfall register control in the manner described in the Walker application and when such occurs, a string of pulses equal to the number of downed pins following the first ball in a frame or both balls in a frame as the case may be is issued to the pinfall counter or the binary coded decimal up counter from the flip-flop PR10.

Additionally, each of the flip-flops PR1–PR10 has an input to its reset section from a gate 112 performing an AND function, which gates includes an input on a pulse forming lead from one bit in the memory and the second, enabling input taken from the output of a NAND-gate 114. As illustrated in FIGS. 2a and 2b, the flip-flop PR1 includes an input ultimately from the line for the number 10 in the memory while the flip-flop PR2 includes an input from the line including the number nine bits in the memory while the flip-flop PR10 receives a corresponding input from a line associated with the number one bit in the memory.

Each of the flip-flops PR1–PR10 has outputs taken from both its set section and its reset section. These outputs are utilized by the split detecting means 42 in the manner described in the Walker application and are additionally utilized as inputs to bits one through 10 of a memory word used exclusively for incremental pinfall computation during manual entry. Specifically, output lines 118 from the reset sections of the flip-flops PR1–PR10 provide signals 1PD through 10PD, respectively, which are utilized in a manner to be seen in greater detail hereinafter.

Each of the lines 118 is also connected as an input to a NAND-gate 120 which performs a NOR function. When any one of the flip-flops PR1–PR10 is set corresponding to a standing pin condition, the gate 120 issues a signal indicative of the fact that the pinfall is not equal to ten. However, if all of the flip-flops PR1–PR10 are in the reset condition, the output of the gate 120 is indicative of the fact that a pinfall of 10 has been achieved.

The output of the gate 120 is taken as an input by a NAND-gate 122 and is additionally used for other purposes to be seen in greater detail hereinafter. The NAND-gate 122 provides an enabling output periodically for the gates 112 so that, under certain situations, information contained in bits one through ten of the word for incremental pinfall error correction computation in the memory can be read into the bits PR1–PR10 of the pinfall register. Other inputs to the NAND-gate 122 include a 3+5+9 signal generated in a manner described in the Walker application which is indicative of the fact that computation for a second ball in a frame is about to proceed. Finally, a NAND-gate 122 receives a SCORER ERROR CORRECTION signal in the computer cycle control which also is generated in the manner described in the Walker application.
Summarizing, the gate 112 are enabled to allow pinfall information in the error correction word in the memory to be read into the pinfall register only when both ball pinfall is not enabled. When a second ball situation and when an error correction manual entry situation is taking place.

FIG. 3 illustrates the pinfall counter used in the invention and the same comprises a four bit binary coded up counter comprised of flip-flops PC1, PC2, PC4, and PC8. Various gating is provided so that the pinfall counter may be used for straight counting purposes or, as mentioned previously, may form a recirculating shift register with the binary coded decimal up counter during read out of the cumulative score. Thus, a number of gates 140 and 142 associated with the set and reset sections of the flip-flops respectively are connected to a line 144 which receives pulses when the counter is used as a shift register. Similarly, a number of gates 146 which perform AND functions are associated with the trigger inputs of each of the flip-flops PC1 and PC8 as well as a line 148 which is connected through an inverter 150 to a NOR-gate 152 which is arranged to either allow the pinfall counter to count or disable the same from counting. To this end, two inputs are provided to the NOR-gate 152 for receiving the indicated signals which are provided in the manner mentioned in the Walker application. The least significant bit in the pinfall counter, namely the flip-flop PC1, includes an OR-gate 154 associated with its trigger input and one of the inputs to the same is a line 156 which may receive an ADD ONE TO PINFALL signal which is used during team totaling and incremental pinfall computing following the second ball in a manner to be described in greater detail hereinafter. A second input to the OR-gate 154 is received from a gate 157 which receives the above-mentioned pulse string from the pinfall register.

Additionally, the flip-flop PC1 includes an input to its set section from a gate 158 utilized as an AND gate while the flip-flops PC2-PC8 include similar inputs from gates 160. The gate 158 includes an input on the pulse forming lead from the memory line associated with bit 11 and a second input on which an anded BLOCK STATE and SEQUENCE CYCLE C signal may be received. The gates 160 associated with the flip-flops PC2-PC8 have respective inputs from memory lines associated with bits 12, 13 and 14 respectively as well as a common input on which a BLOCK STATE signal may be received.

Finally, each of the flip-flops PC1-PC8 includes an input for resetting the same token from a line 162. FIG. 4 illustrates, in block form, a modified memory system for use in the invention. That is, the memory system as illustrated in FIG. 4 should be substituted for that utilized in the Walker application in order to take advantage of the present invention. As illustrated, there is a memory plane generally designated 200, which is of the conventional coincident current type and in the exemplary embodiment is 33 by 22 bits.

There are provided 24 bowler words, four lanes words for team totaling purposes and which are used in the manner described in the Walker application, four team handicap words which are used in the same manner described in the Walker application and one word for manual entry of incremental pinfall which has no counterpart in the Walker application.

Each of the 24 bowler words uses bits one through 10 to store cumulative score information while bits 11-14 are used to store the complement of first ball pinfall. Bits 15 to 18 are used to store bowler state information while bits 19-22 are used to store bowler frame information.

With respect to the four lane words, bits 19 through 22 are again used to store frame information which is used in the manner described in the Walker application. In order to store team total score information, 13 bits are required. Contrary to the use of bits 1-13 in the Walker application, the instant invention utilizes bits 1-11 and 15 and 16. Specifically, bits one through 10 are associated with the first 10 bits of the binary coded decimal up counter while bits 15 and 16 in the memory are associated with bits 11 and 12 of the binary-coded decimal up counter. Bit number 11 in the memory is associated with the first bit of the pinfall counter.

The bits of the four team handicap words are used identically to those disclosed in the Walker application and further explanation is not required.

With respect to the manual entry word, ten bits are used with each bit corresponding to one of the bits of the pinfall register. That is, bit number 1 of this word is loaded from flip-flop PR1 of the pinfall register while bit number 2 of this word is loaded from tee flip-flop PR2 of the pinfall register, etc. However, as will be seen, bit number 1 of the memory word is utilized to load the flip-flop PR10 of the pinfall register; bit number 2 of the memory word is utilized to load the flip-flop PR9 of the pinfall and bit number 10 of the memory word is used to load the flip-flop PR1 of the pinfall register. The purpose of this arrangement will become apparent hereinafter.

In order to select the desired word in the memory 200, there is provided memory word selection logic 202 which is along the general lines of that disclosed in the Walker application with the exception that it is expanded to accommodate the additional word for manual entry of incremental pinfall. Utilizing the principles disclosed in the Walker application as well as the disclosure hereinafter, those skilled in the art will fully appreciate the construction of the memory word selection logic 202.

There additionally is provided a read amplifier 204 which is adapted to receive the READ MEMORY signal which is used to read the contents of the selected memory word into the various registers required.

Also provided is a write amplifier 206 which is adapted to receive a WRITE signal to write information contained in the various registers into a selected memory word. The output of the write amplifier 206 is fed to a write amplifier 208 which is associated with the memory word selection logic 202 and 22 horizontal one-half write amplifiers 210 which are associated with respective ones of the bits 1-22 in the memory 200. The manner in which the half-write amplifiers 208 and 210 operate is well known in the art and need not be described further.

Inputs to the horizontal half-write amplifiers 210 are received from the frame counter for bits 19-22, from the state register for bits 17 and 18, from the state register or from the binary-coded decimal up counter through gating 212 to be described in greater detail hereinafter for bits 15 and 16, from the pinfall counter for bits 11-14, and, through gating 214 to be described in greater detail hereinafter, from either the binary-coded decimal up counter or from the pinfall register for bits 1-10.

There are also provided 22 sense amplifiers associated with each of the respective bits 1-22. The 22 sense amplifiers are generally designated 216 in FIG. 4 and provide outputs to the various registers in the same manner described previously with respect to the inputs to the horizontal half-write amplifiers 210. It is to be noted that in the case of bits 15 and 16, gating 218 is utilized while in the case of bits 1-10, gating 220 is utilized. In actuality, the gating 218 is formed by the gates 276 illustrated in FIG. 9c of the above-identified Walker application and associated with the bits BCD400 and BCD900 of the binary-coded decimal up counter illustrated therein. Also, the gating 218 is provided by the gates 300 illustrated in FIG. 11 of the walker application and associated with the flip-flops BSR1 and BSR2 described in the above-identified Walker application.

With respect to the gating 220, the same is provided by the gates 276 illustrated in FIGS. 9a, 9b, and 9c and associated with the bits BCD1 through BCD200 for the binary coded decimal up counter shown therein in the walker application; and it is additional provided by the gates 112 illustrated in FIG. 2 of the instant application.

As will become apparent in greater detail hereinafter, blocking level signals are applied to the above-mentioned gates for the purpose of determining which register receives the information contained in the particular memory word
being read at a given instant if, in fact, any of the word should receive such information. For as noted in the Walker application, in some instances, entry into any register is blocked to accomplish clearing of the memory. For the present it is sufficient to note that during a bowler scoring cycle (cycle C), the information contained in bits 15 and 16 will be fed to the bowler state register while during a team total cycle (cycle D), such information will be fed to the binary-coded decimal up counter. With respect to the gating 220, during each bowling cycle, information from bits 1 through 10 will be fed to the binary-coded decimal up counter. Additionally, during error correction procedures taking place during a bowler cycle, information from bits 1–10 of the manual entry word will be blocked from the binary coded decimal up counter and fed to the pinfall register.

As mentioned previously, the first 10 bits of each word with the exception of the error correction word in the memory comprises 10 bits of information which are fed from binary coded decimal up counter. However, in the case of the error correction word, bits one through ten should receive their information from the pinfall register. More specifically, downed pin information is read from the corresponding bits in the pinfall register into the corresponding bits in the error correction incremental pinfall memory word. Thus, the outputs from the set sections of the pinfall counter or the bowler state register will be placed in the 15 bit of the memory and the AND-gates 320 and 324. The AND-gates 318 and 320 determine whether information from the binary-coded decimal up counter or the bowler state register will be placed in the 15 bit of the memory and the AND-gates 322 and 324 determine whether the same information will be placed in the 16 bit of the memory. Accordingly, the NAND gates 318 and 322 include inputs on which a CYCLE D signal (team totalizing cycle) may be received so that the same are enabled during team totalizing while the AND-gates 320 and 324 have inputs on which they may receive enabling CYCLE C signals (bowler scoring cycle) so that bowler state information will be directed to the memory during a regular bowler cycle.

FIG. 7 illustrates manual entry means including 12 manually operable, normally closed switches ECO, EC1, EC2, EC3, EC4, EC5, EC6, EC7, EC8, EC9, ECX and E/C. The switches ECO–EC9 are for the purpose of introducing pinfall achieved on any particular ball into the computer for error correction purposes while the switch ECX is utilized to indicate to the computer that a strike was obtained by a particular ball. By the same token, the switch EC/C may be operated when a spare was obtained on the second ball in a frame.

AND-gates 330, 331, 332, 333, 334, 335, 336, 337, 338 and 339 are associated with the switches EC0–EC9, respectively, and receive an enabling input on a second line when it is desired to score error correction. The outputs of the gates 330–339 are respectively associated with the inputs to the pinfall register for the flip-flops PR1 through PR10, respectively and the manner of operation of the same is described in detail in the above-identified Walker application except that for second ball error correction entry, the switches ECO-EC/ are operated for incremental pinfall rather than cumulative pinfall as was the case in either the incremental pinfall or the cumulative pinfall embodiment of Walker. That is, according to this invention, if seven pins were achieved on the first ball in a frame and two pins were achieved on the second ball in a frame, rather than operate the switches EC7 and EC9 following first and second ball, respectively, as would be the case using the logic disclosed in the Walker application, to enter the first ball pinfall, the switch EC7 would be operated and to enter the second ball pinfall, the switch EC2 would be operated.

The gates 330–339 may be enabled in the manner described in the Walker application during an error correction procedure to cause the setting of certain of the flip-flops PR1–PR10 of the pinfall register. For example, if four pins were knocked down by the first ball in a frame and such information was entered manually, the switch EC4 would be depressed and assuming all other conditions to be present, the gates 334–339 would be enabled to set the flip-flops PR1–PR6 of the pinfall register.

FIG. 8 illustrates, in block form, a bowler score cycle control which is somewhat modified from the form disclosed by Walker and which is comprised of a four-bit, 10-count feedback counter 350 and a decoding matrix 352 having outputs which issue signals 1, 2, 3, 4, 5, 6, 7, and 8. The arrangement is such that when all bits of the counter 350 are at zero, none of the 1 through 8 signals will be issued but as the counter 350 is stepped from zero, the signals 1 through 8 will sequentially issued.

The foregoing represent a departure from the bowler score cycle control arrangement described in the Walker application insofar as the only employed signals 1 through 8. However, the signals 1 and 2 through 8 correspond exactly to the functions 1/f6 described in Walker. The functions accomplished during the functions 1/f6 will be appreciated from the following table.

<table>
<thead>
<tr>
<th>TABLE I</th>
</tr>
</thead>
<tbody>
<tr>
<td>f1—if a split exists, print a split symbol</td>
</tr>
<tr>
<td>f2—select manual entry memory word</td>
</tr>
<tr>
<td>f3—read or write in the manual entry word</td>
</tr>
<tr>
<td>f4—count incremental pinfall</td>
</tr>
<tr>
<td>f5—print the bowler’s box score</td>
</tr>
<tr>
<td>f6—add the bowler’s pinfall to his previous total</td>
</tr>
<tr>
<td>f7—print the bowler’s frame score</td>
</tr>
</tbody>
</table>
add the bowler's score second time if his present pinfall is a strike and his present state is state 6 or state 8, add an additional 10 to his score

From the foregoing, it will be recognized that functions $f_3$, $f_5$, and $f_6$ correspond approximately to the three functions performed during the so-called incremental pinfall cycle disclosed in the Walker application. However, the selection and the writing and reading of a memory word in the increment pinfall control is restricted to use during error correction and is at all other times ignored.

In view of the foregoing, it will be appreciated that the bowler's score and control including the counter 350 may be constructed as a four-bit 10 count feedback counter as mentioned utilizing the principles disclosed in the Walker application or, if desired, could be formed by using the bowler's score cycle control therein disclosed in conjunction with the incremental pinfall control described therein with appropriate modifications of the read and write gating during functions $f_3$, $f_5$, and $f_6$ as mentioned in the preceding paragraph.

FIG. 9 illustrates various gating that is employed to incorporate the instant incremental pinfall system. The ADD ONE TO PINFALL signal mentioned previously is generated by a pulse gate 369 which receives an input from an OR-gate 362. A first input to the OR-gate 362 is taken from a NAND-gate 364 which has as an input, a CYCLE C signal, a $t_5$ signal and a $3+5+9$ signal. The NAND-gate 364 performs AND function and the result is that whenever CYCLE C (the bowler scoring cycle) is occurring, at $t_5$ thereof and when the bowler state is a second ball state, the ADD ONE TO PINFALL signal will be issued to thereby step the pinfall counter one count.

The second input to the OR-gate 362 is taken from the output of a NAND-gate 366 which receives CYCLE C and a $t_5$ signal. Thus whenever a cycle other than CYCLE C, usually CYCLE D, is occurring, and at $t_5$ thereof, the pinfall counter will be stepped by one.

The output of the NAND-gate 366 is also utilized as an input by a NOR-gate 368 which also receives a CYCLE C signal. The arrangement is such that at $t_5$ during a cycle other than CYCLE C (the CYCLE C input to the NOR-gate 364 is for the purpose of sensing the absence of a CYCLE C signal), the NOR-gate 368 will issue a signal which is fed to the blocking gates of the arithmetic register.

The gating also includes a pulse generating gate 370 which may issue a READ PINFALL COUNTER signal to reset the pinfall counter to its all bits zero condition. The pulse-forming gate 370 receives its input form a two-input OR-gate 372. The OR-gate 372 receives one input from the computer cycle control gating disclosed in the Walker application and specifically, receives a RESET REGISTER signal which is generated in the manner set forth therein. The second input to the OR-gate 372 is derived from the output of a NAND-gate 374 which receives as one input, a BOWLER CYCLE signal. The second input to the NAND-gate 374 is derived from an AND-gate 376 which has equal inputs.

The first input receives a $3+5+9$ signal which is generated in the manner described in the Walker application and the second input receives a pinfall register PF10 which is generated by the NAND-gate 120 illustrated in FIG. 2b.

Other gating includes an OR-gate 380 which may issue a READ MANUAL ENTRY WORD signal on two different occasions. To this end, a first input to the OR-gate 380 is derived from the output of an AND-gate 382 which includes a pulse forming input on which $f_3$ is received. As a result, the AND-gate 382 may be enabled only on the trailing edge of the pulse. The second input to the AND-gate 382 receives a FIRST ERROR CORRECTION signal so that the READ MANUAL ENTRY WORD signal will be generated just prior to $f_3$ and during the first manual entry in a sequence. At this time, entry of pinfall information from the memory to the pinfall register is blocked so that the reading of the manual entry word at this time has the effect of clearing the same.

The second time at which a READ MANUAL ENTRY WORD signal may be generated occurs during an error correction procedure when the bowler is in a second ball state and at $f_3$ thereof at which time, first ball incremental back into the pinfall register so that pinfall information contained in the manual entry word is read back into the pinfall register so that incremental pinfall on the second ball may be determined. To this end, a second input to the OR gate 380 is received from an AND-gate 384 which receives $f_3$, SECOND BALL STATE AND SCORE ERROR CORRECTION signals.

As mentioned previously, during the function $f_3$, it is desired to select the manual entry word if an error correction procedure is taking place. Accordingly, an AND-gate 386 is provided and the same generates an output effective to select the manual entry word in the memory when both $f_3$ and a SCORE ERROR CORRECTION signals are present.

As mentioned previously, at $f_3$ it is then desirable to write in the manual entry word in certain instances. Accordingly, there is provided an AND-gate 388 which may issue a WRITE MANUAL ENTRY WORD signal when function $f_3$ is occurring during an error correction procedure and when the bowler is in a first ball state.

The above-described logic provides for incremental pinfall indication when pinfall is detected by automatic pin-detecting means; when pinfall information is entered manually as for error correction purposes and the same is entered incrementally; and when pinfall information is provided by an out-of-range pin detection system such as that described in the copending application of Gauthier et al. U.S. Ser. No. 761,577, filed Sept. 23, 1968, entitled "Pin Detecting System," and assigned to the same assignee as the instant application.

The manner by which pinfall is counted incrementally for an out-of-range pin situation is disclosed in the Gauthier application and need not be described in detail herein. However, for the other two situations, namely, conventional automatic pin detection and manual entry wherein the pinfall information is manually entered incrementally, the operation of the device is as follows.

Let it be assumed that on the first ball in a frame, four pins were knocked down, and, on a second ball in the frame three additional pins were knocked down. The computer will cycle in the normal manner, and as a result the pinfall counter will contain the first ball pinfall or four which will be present in binary form as 0100. Thereafter, the gating will operate in a manner described previously to write the complement of the first ball pinfall, 1011, in the corresponding four bits of that bowler's memory word. On a second ball cycle, initially, the complement of first ball pinfall will be loaded into the pinfall counter. Thus, the same will contain the binary coded number 1011. Before the pinfall is counted, at $t_5$ for the second ball cycle, a count, a one will be added so that the condition of the pinfall counter at this time will be binary 1100. Thereafter, and at $f_6$, the total, both ball pinfall contained in the pinfall register will be shifted and seven pulses will be applied to the pinfall counter. As a result, the binary number 0111 will be added to the the binary number 1100 already contained in the pinfall counter and the result will be binary 1001.

Inasmuch as the pinfall counter only contains four bits, the fifth digit or "carry" will be lost and only the binary number 0011, corresponding to decimal three, will remain in the pinfall counter. As a result, a "3" will be printed indicating second ball incremental pinfall. The foregoing example is summarized in table 2 below.

<table>
<thead>
<tr>
<th>Step</th>
<th>Function</th>
<th>Binary number</th>
<th>Decimal number</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>First ball pinfall signals 6</td>
<td>0000</td>
<td>4</td>
</tr>
<tr>
<td>2</td>
<td>Write complement in memory (6)</td>
<td>1001</td>
<td>11</td>
</tr>
<tr>
<td>3</td>
<td>Second ball pinfall is 3</td>
<td>1001</td>
<td>11</td>
</tr>
<tr>
<td>4</td>
<td>Second ball, load complement</td>
<td>1001</td>
<td>11</td>
</tr>
<tr>
<td>5</td>
<td>Add &quot;1&quot; (2) of second ball</td>
<td>1100</td>
<td>12</td>
</tr>
<tr>
<td>6</td>
<td>At $t_5$, count total pinfall</td>
<td>0011</td>
<td>7</td>
</tr>
<tr>
<td>7</td>
<td>Remsindae</td>
<td>1001</td>
<td>19</td>
</tr>
<tr>
<td>8</td>
<td>The &quot;carry&quot; is lost and the total number in the pinfall counter is 3</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
It will be recalled from the Walker application that the first bit of the pinfall counter, PF1, is used for the thousands digit of a team total. Since the complement of this bit is written in a memory, for team total sequences there must be an appropriate adjustment. That is, if the team total is not in excess of 1,000, the thousands digit or 13th bit will be a binary zero but a binary one will be written into the memory and ultimately read back into the pinfall counter as a one during team totaling period. Similarly, if a team total is in excess of 1,000, a binary zero will be written into the memory and ultimately written back into the pinfall counter.

Therefore, for any sequence wherein the pinfall counter may be used for a function other than counting pinfall, the first bit of the same is switched by the ADD ONE TO PINFALL signal which, as will be recalled, is generated whenever $s_4$ is reached during a cycle other than CYCLE C. Effectively, the "complement of the complement" of the bit $PC1$, or, in other words the original number in the bit, is placed in the first bit of the pinfall counter before any arithmetic sequence occurs.

The operation during manual entry of pinfall information is as follows. Again, let it be assumed that four pins were achieved by the first ball. As a result, the switch EC4 would be opened and the flip-flops PR–PR10 would be reset corresponding to downed pins. In other words, the flip-flops PR1–PR6 would be set corresponding to standing pins. At $fe$, the manual entry word would be selected and at $fe$, the reset condition of the flip-flops PR7–PR9 would be written into the seven through 10 bits of the manual entry word in the memory. At $fe$, the pinfall would be counted normally in the pinfall counter the first ball pinfall ultimately printed.

For second ball, let us again assume that three pins were knocked down for a total, both ball, pinfall of seven. However, since pinfall information is to be entered incrementally for second ball pinfall according to this invention the switch EC3 would be pressed rather than switch EC7 as disclosed in the walker device. Again at $fe$, the manual entry word is selected, and at $fe$, the memory is read inasmuch as it is a second ball situation.

It will be recalled that when the manual entry word of the memory is read, the 10th bit of the memory word is directed to the first bit of the pinfall register rather than to the tenth bit from which the information initially came; the ninth bit of the word is directed to the second bit of the register, etc. As a result, back into the operation at $fe$, the flip-flops PR1–PR4 will be reset and in view of the operation of the switch EC3, the flip-flops PR8, PR9 and PR10 will be reset. Thus seven of the flip-flops in the pinfall register are reset corresponding to seven downed pins. At $fe$, normal counting place and the incremental pinfall determination of three pins for second ball pinfall is accomplished in the manner mentioned previously in conjunction with the description of the operation for automatic pin detection.

Having described the preferred embodiment of our invention, we do not wish to be limited to the details set forth, but rather, to have the same construed as set forth in the following claims.

We claim:
1. In a bowling scoring system including pinfall detecting means for providing pinfall information, manual entry means for providing pinfall information, score counting means for receiving pinfall information from either said pinfall detecting means or said manual entry means, control means for said counting means for causing said counting means to compute, frame-by-frame cumulative scores, and a pinfall counter having at least four bits for providing binary-coded pin counts after each ball in a frame, the improvement comprising: pinfall memory means; means associated with said pinfall counter and operative after said pinfall counter has determined first ball count for writing the counter complement of first ball pin count in said memory means; means operative after the second ball in a frame has been bowled for reading said memory means to load the first ball pinfall counter complement into said pinfall counter; means operative after the loading of said first ball pinfall counter complement into said pinfall counter for increasing the count contained therein by one; and feeding means operative to provide said pinfall counter with combined first and second ball pinfall information whereby said four bits of said counter will contain second ball pin count only.
2. A bowling scoring system according to claim 1 wherein said feeding means comprises a 10-bit recirculating shift register, and means for shifting said shift register, said pinfall counter being connectable to one bit of said shift register, and further including a score counter connectable to one bit of said shift register.
3. A bowling scoring system according to claim 2 further including pinfall detecting means for
a. after the first ball in a frame, providing first ball pinfall information, and
b. after the second ball in a frame, providing combined first and second ball pinfall information,
said feeding means receiving pinfall information said pinfall-detecting means.
4. A bowling scoring system according to claim 3 wherein said manual entry means include manually operable pinfall information providing means adapted to be actuated by bowler to
a. provide first ball pinfall information only, and
b. provide second ball pinfall information only, means for introducing said first ball pinfall information into said feeding means; second memory means; means operative to write said first ball pinfall information from said feeding means into said second memory means; means for introducing said second ball pinfall information only into said feeding means; means for reading second memory means to introduce said first ball information into said feeding means; said feeding means thereafter being operative to feed said pinfall counter with the combined first and second ball pinfall information contained therein whereby said counter will contain second ball pin count only, and to feed said score counter with combined first and second ball pinfall information to count a bowler's score.
5. In a bowling scoring system for computing bowling scores bowled on a plurality of bowling lanes, the combination comprising: a plurality of pin detecting means for providing first ball pinfall information after the first ball in a scoring frame, and combined first and second ball pinfall information after the second ball in a scoring frame; a single register means connectable to any one of said pinfall detecting means for receiving
a. first ball pinfall information therefrom, and
b. combined first and second ball pinfall information therefrom; a four-bit binary-coded pinfall counter connectable to said register means for receiving first ball and combined first and second ball pinfall information therefrom to provide pin counts after each ball in a scoring frame; a plurality of bowler memory words each individually connectable to said pinfall counter for receiving the counter complement of first ball pin count contained therein for the associated bowler and for temporarly storing the same; means operative when the second ball in a frame has been bowled by the bowler for introducing the counter complement of first ball pin count contained in that bowler memory word into said pinfall counter; means for thereafter increasing the count in said pinfall counter by one; and means for thereafter introducing combined first and second ball information into said pinfall counter from said register means whereby second ball pin count only is contained in said pinfall counter.
6. The bowling scoring system of claim 5 further including binary to decimal decoding means associated with said pinfall counter for decoding first ball pin count and second ball pin
count contained therein; and a plurality of printers, one for each lane for printing at different locations on a score sheet, first ball pin count and second ball pin count.

7. A bowling scoring system according to claim 5 wherein said register means comprises a 10-bit recirculating shift register, one bit for each pin position; and wherein said system further includes manual pinfall entry means for manually providing first ball pinfall information and second ball only pinfall information to said shift register, means for introducing pinfall information from said manual entry means into said register beginning at one predetermined bit and toward bits adjacent thereto in one direction; a 10-bit memory means connectable to said pinfall register for receiving first ball pinfall information introduced therein by said manual entry means; means operative following second ball only pinfall information entry by said manual entry means for reloading first ball pinfall information into said shift register beginning at a bit adjacent said predetermined bit in a direction opposite said one direction toward bits adjacent thereto in said opposite direction; and score-counting means connectable to said shift register for periodically receiving combined first and second ball pinfall information therefrom to compute individual bowling scores.

8. In a bowling scoring system including a pinfall counter for receiving pinfall information and for providing binary coded pin counts after each ball in a scoring frame, the improvement comprising pinfall memory means; means associated with said pinfall counter and operative after said pinfall counter has determined first ball count for writing the complement of first ball pin count in said memory means; means operative after the second ball in a frame has been bowled for reading said memory means to load the counter complement of first ball pinfall into said pinfall counter; means operative after the loading of said first ball pinfall counter complement into said pinfall counter for increasing the count contained therein by one; and means operative to feed said pinfall counter with combined first and second ball pinfall information whereby said counter will contain second ball pin count only.

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