

[54] **BOWLING SCORE COMPUTER**
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[22] Filed: **June 14, 1971**
[21] Appl. No.: **152,833**
[52] U.S. Cl. **235/168, 235/92 GA, 235/151, 273/54 C**
[51] Int. Cl. **G06f 7/50, G06f 15/20, A63d 5/04**
[58] Field of Search **235/168, 152, 151, 92 GA; 273/54 C**

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Primary Examiner—**Malcolm A. Morrison**
Assistant Examiner—**David H. Malzahn**
Attorney—**Marvin Reich**

[57] **ABSTRACT**

A bowling score computer system having manual input of pinfall data via thumb-wheel switches. The switches are sequentially scanned to derive data for use by a solid-state electronic computer to derive individual and team scores. At regular periodical intervals, the switches are rescanned to derive up-to-date output values in case the output should be changed. The system has the capability of operating in a handicap mode or in a scratch mode. The input switches serve as an input storage memory and eliminate the need for most other internal memory within the system.

9 Claims, 37 Drawing Figures

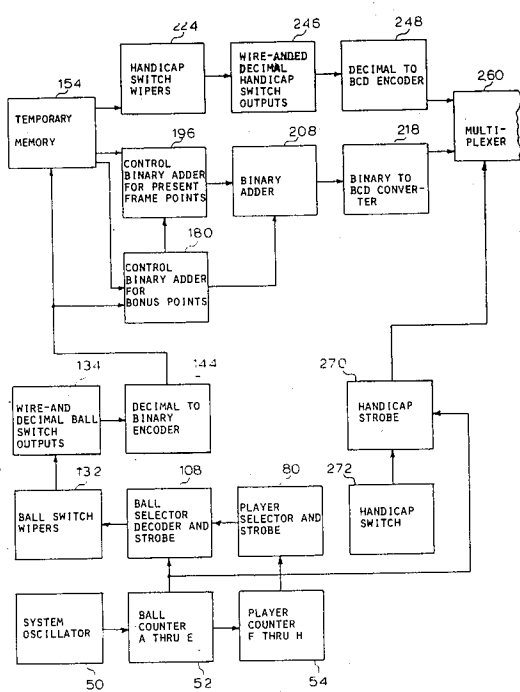
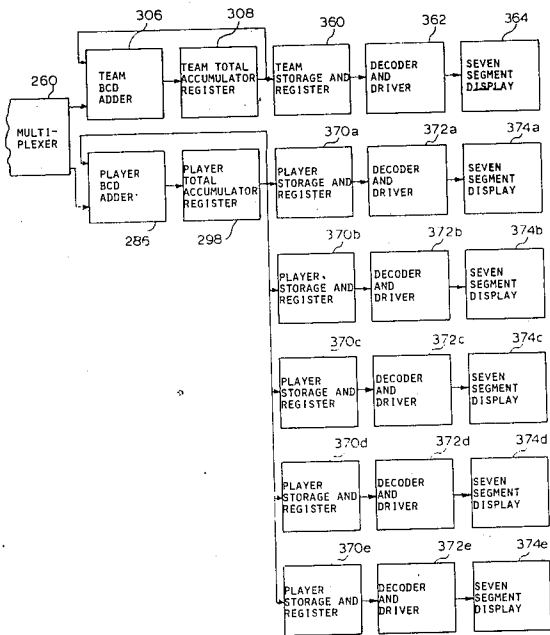
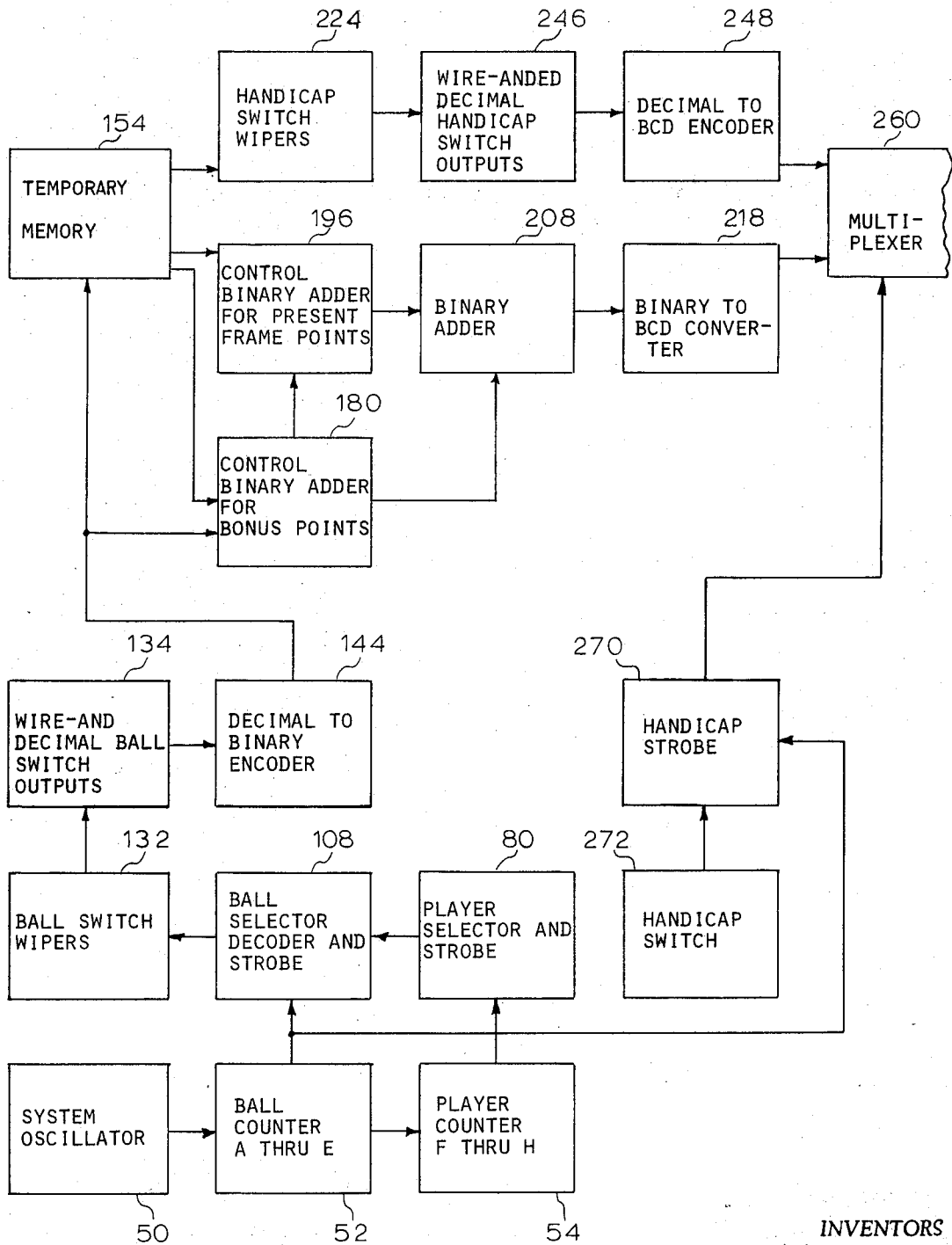


FIG. 1a



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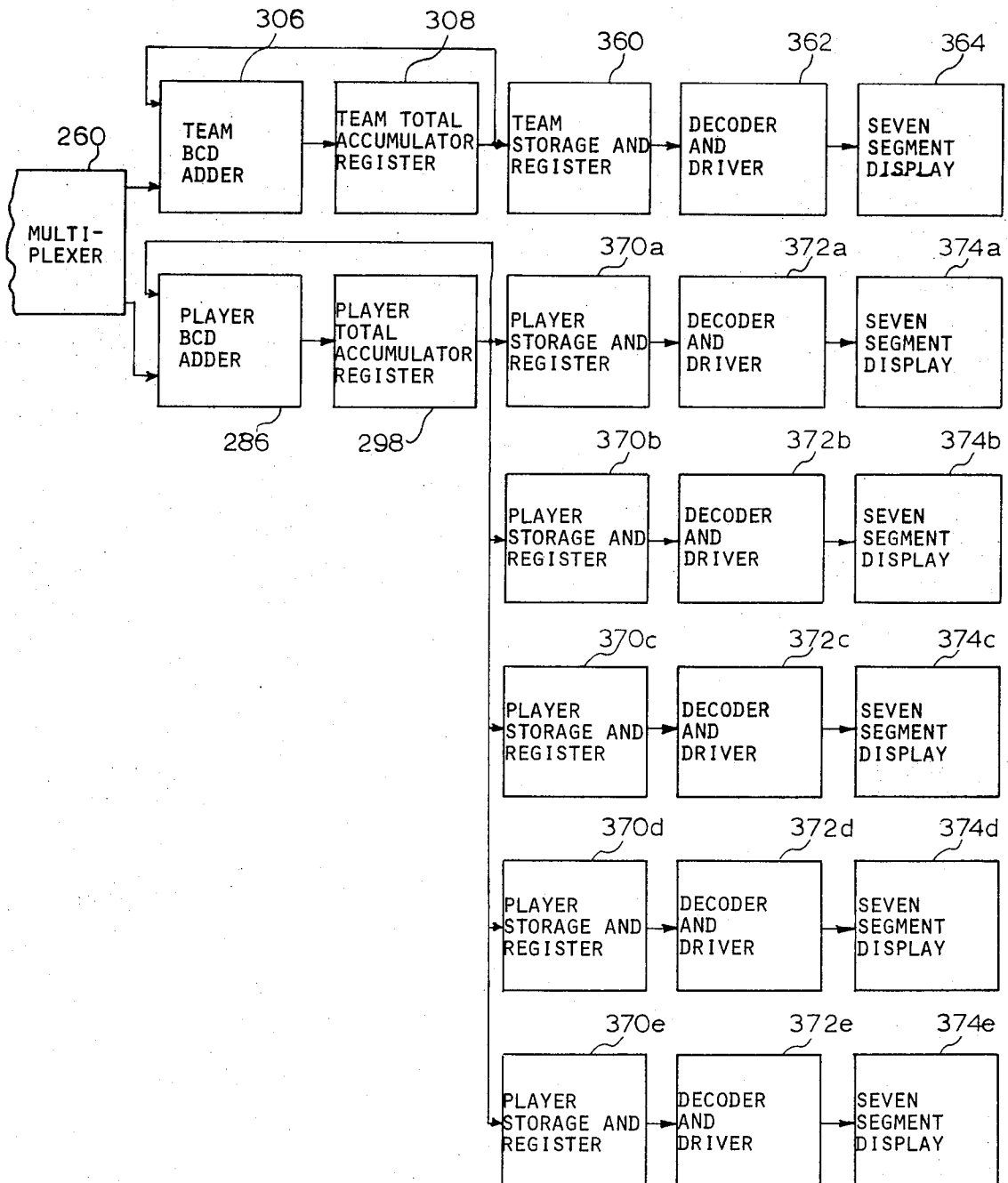
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FIG. 1b



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FIG. 2

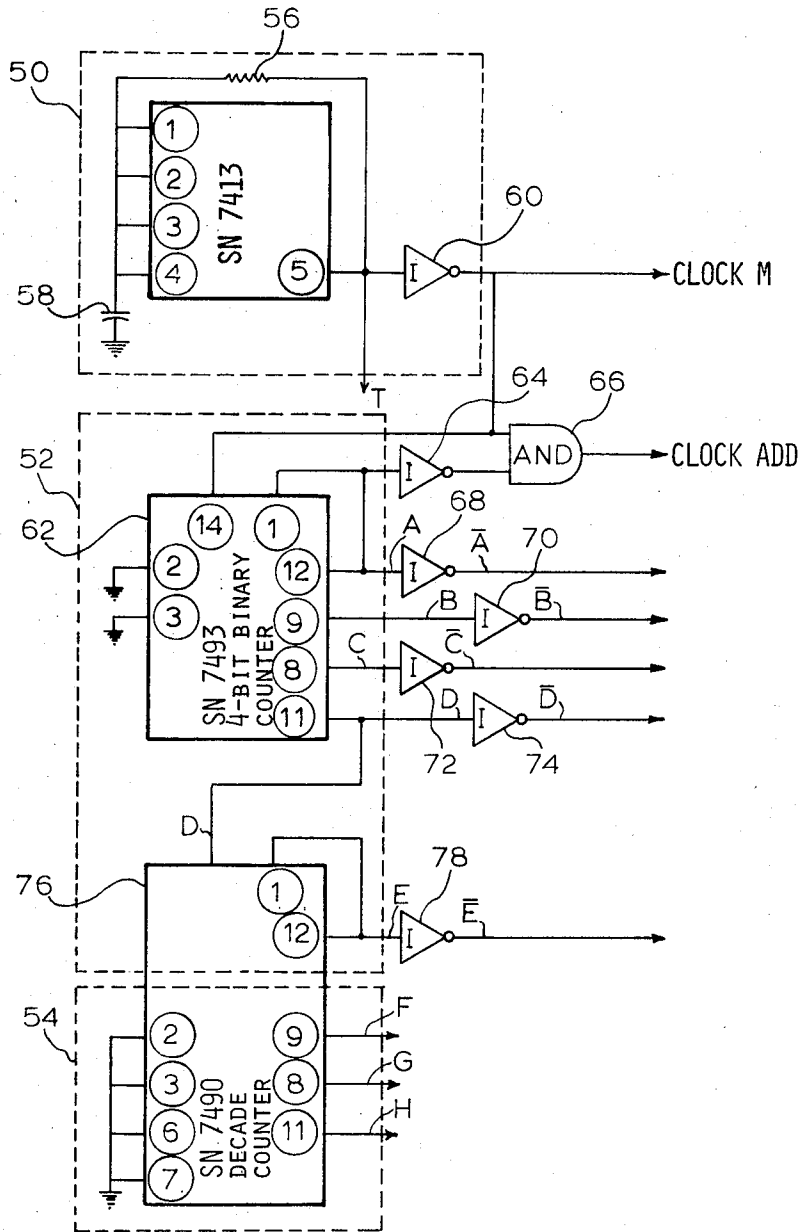
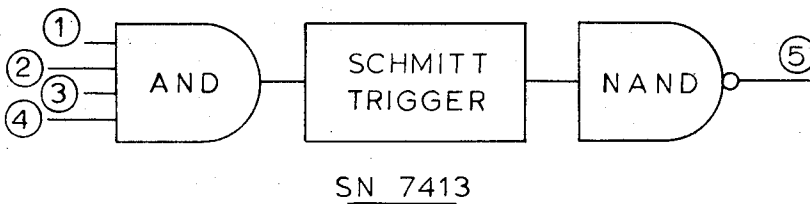


FIG. 3



SN 7413

BY

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FIG. 4

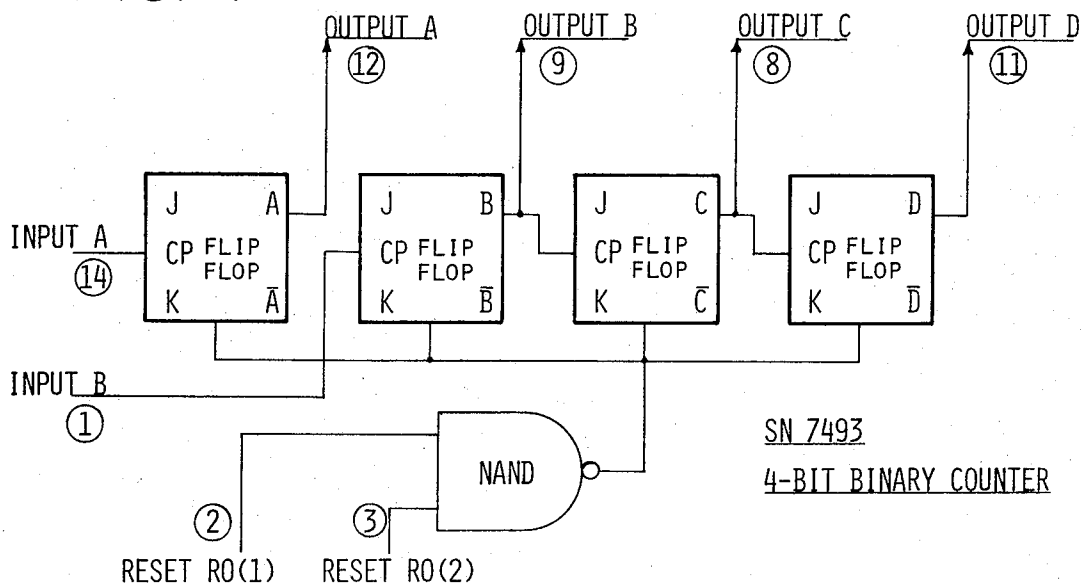
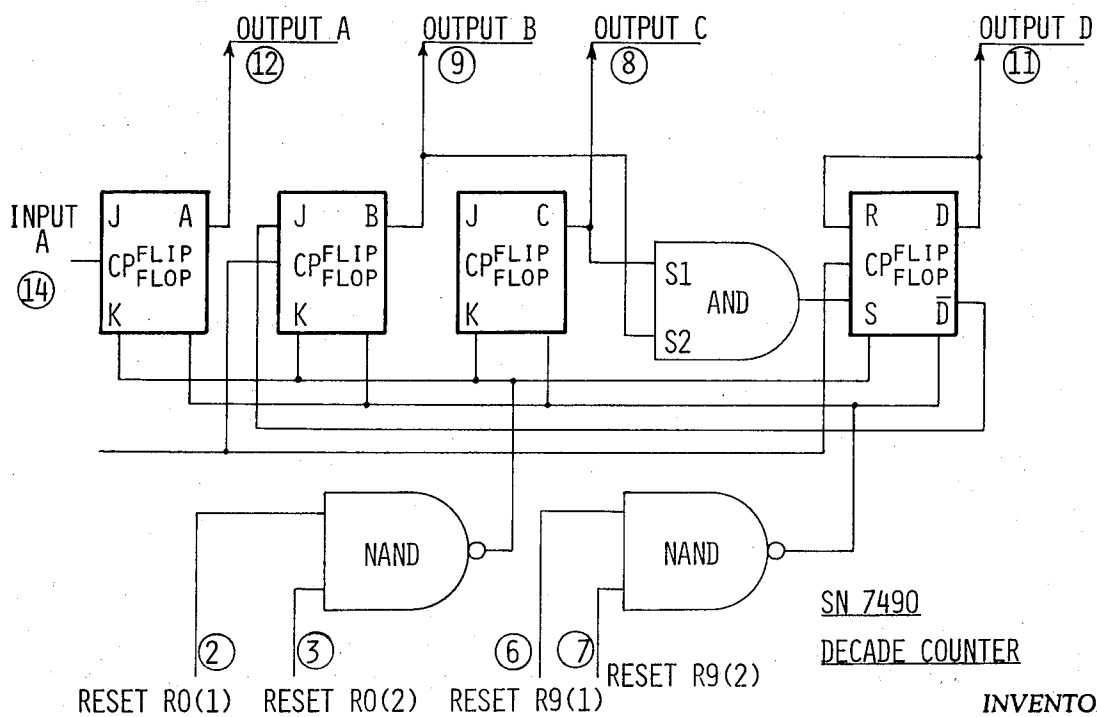


FIG. 5



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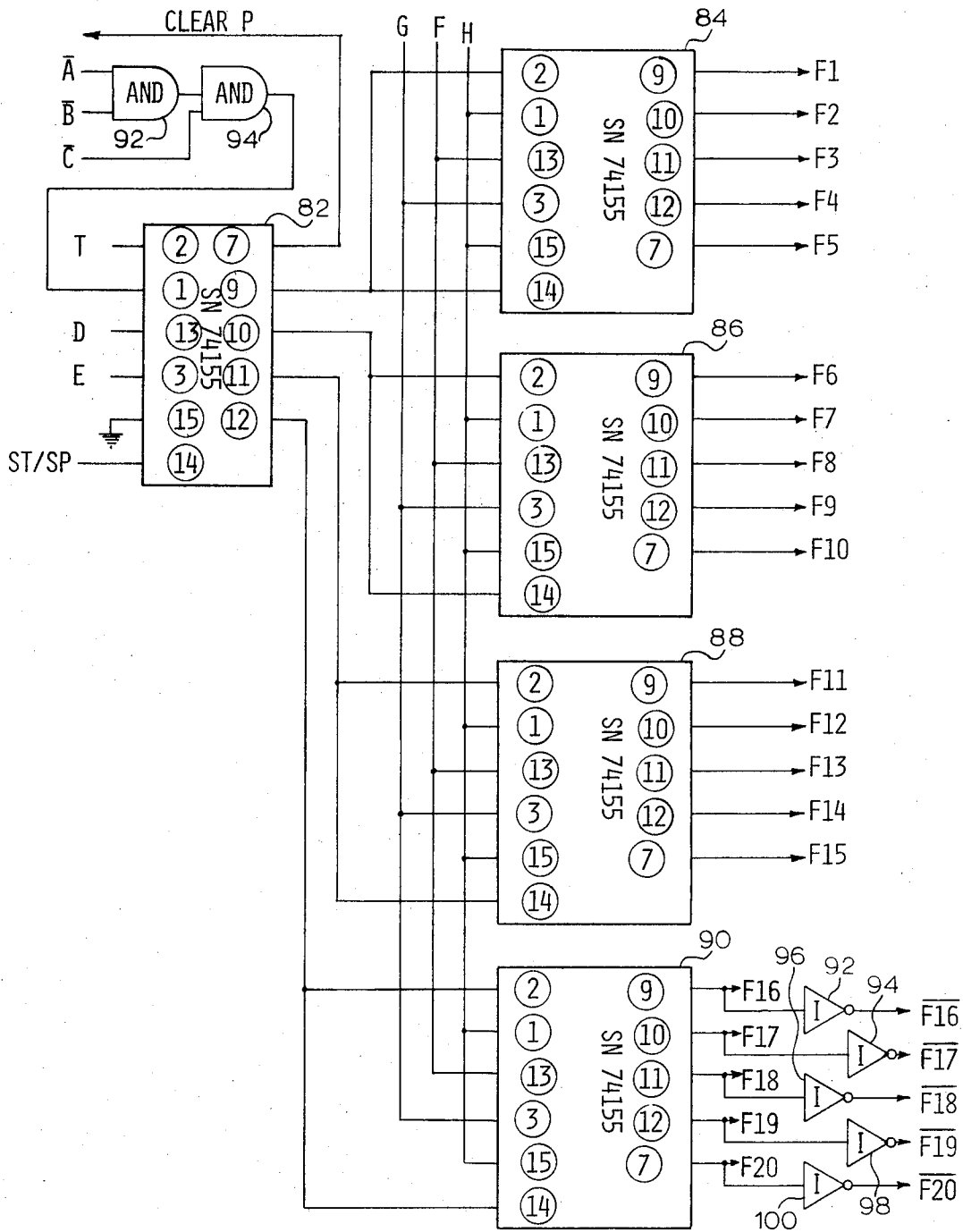
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FIG. 6



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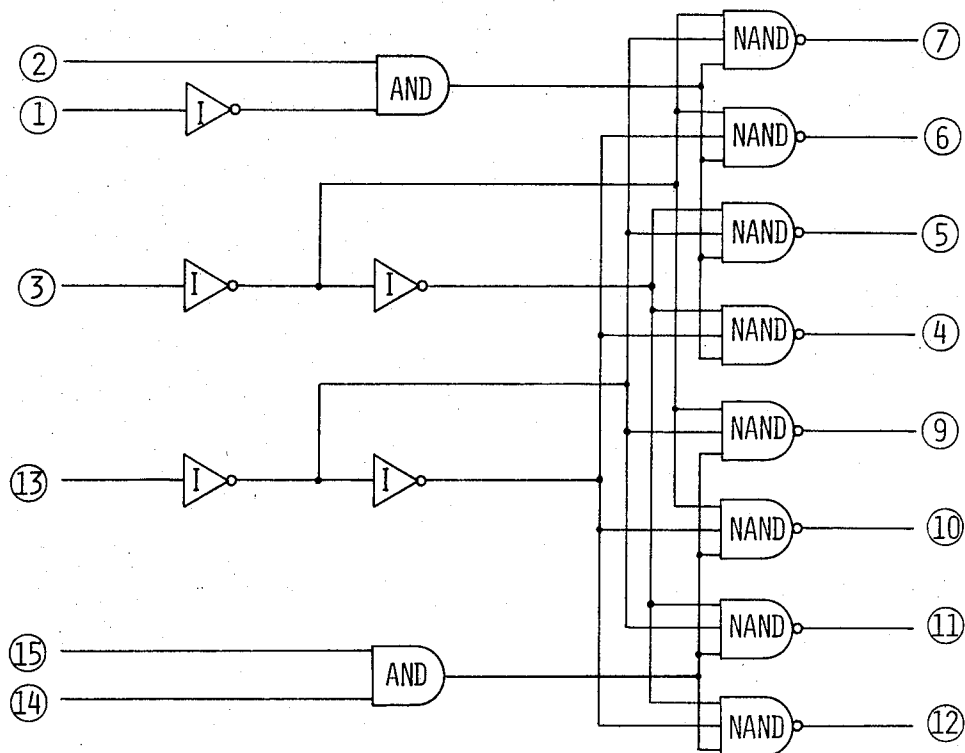
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FIG. 7



SN 74155 OR SN 74156
2-LINE TO 4-LINE
DECODER/DEMULPLEXER

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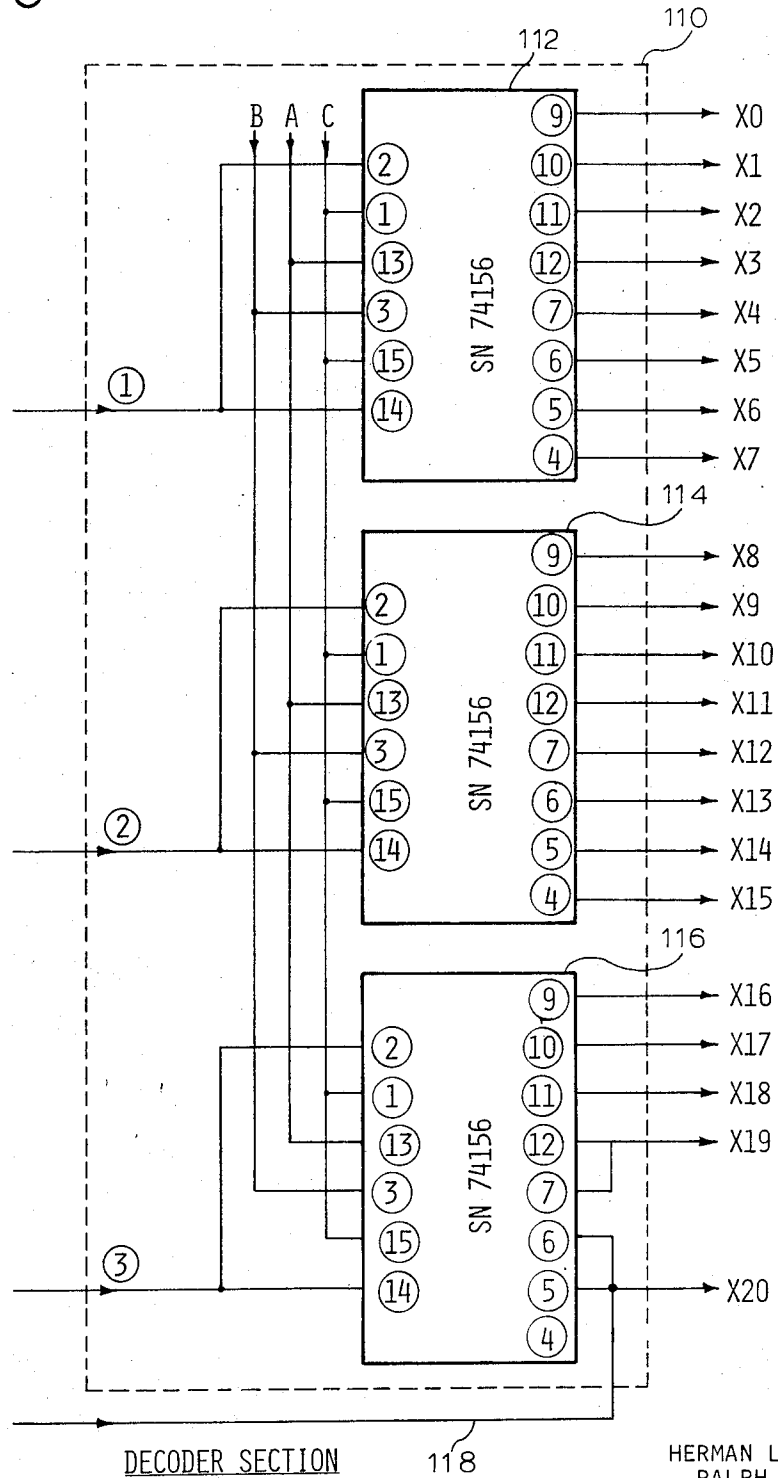
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FIG. 9



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FIG. 10

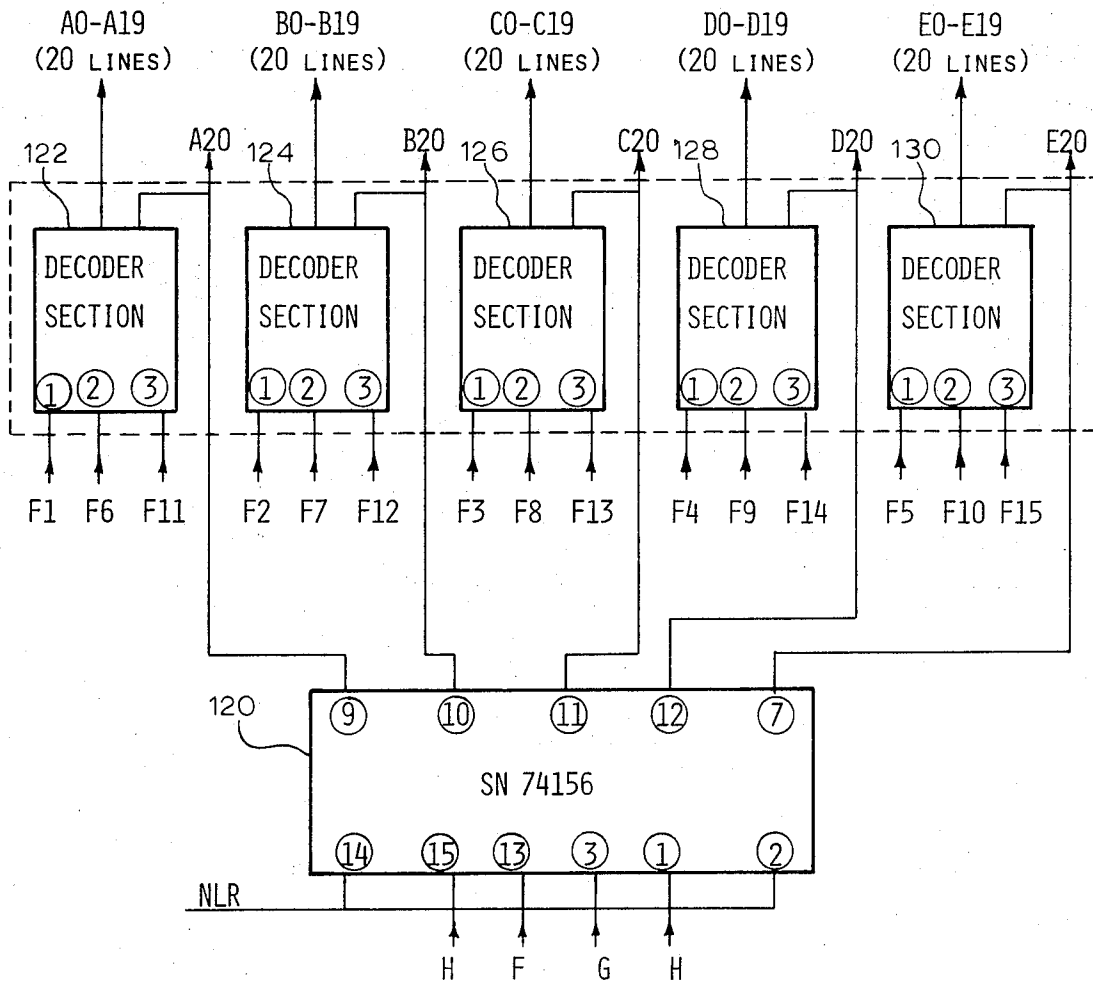
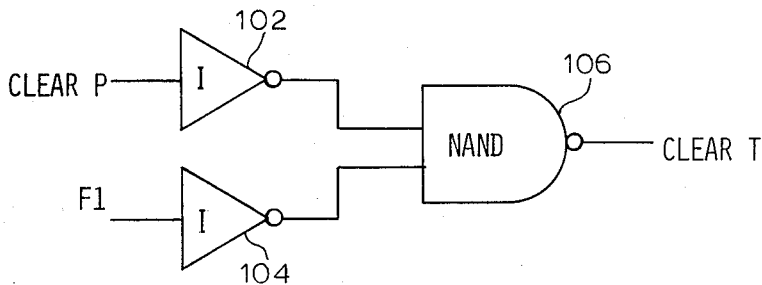


FIG. 8



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FIG. 11

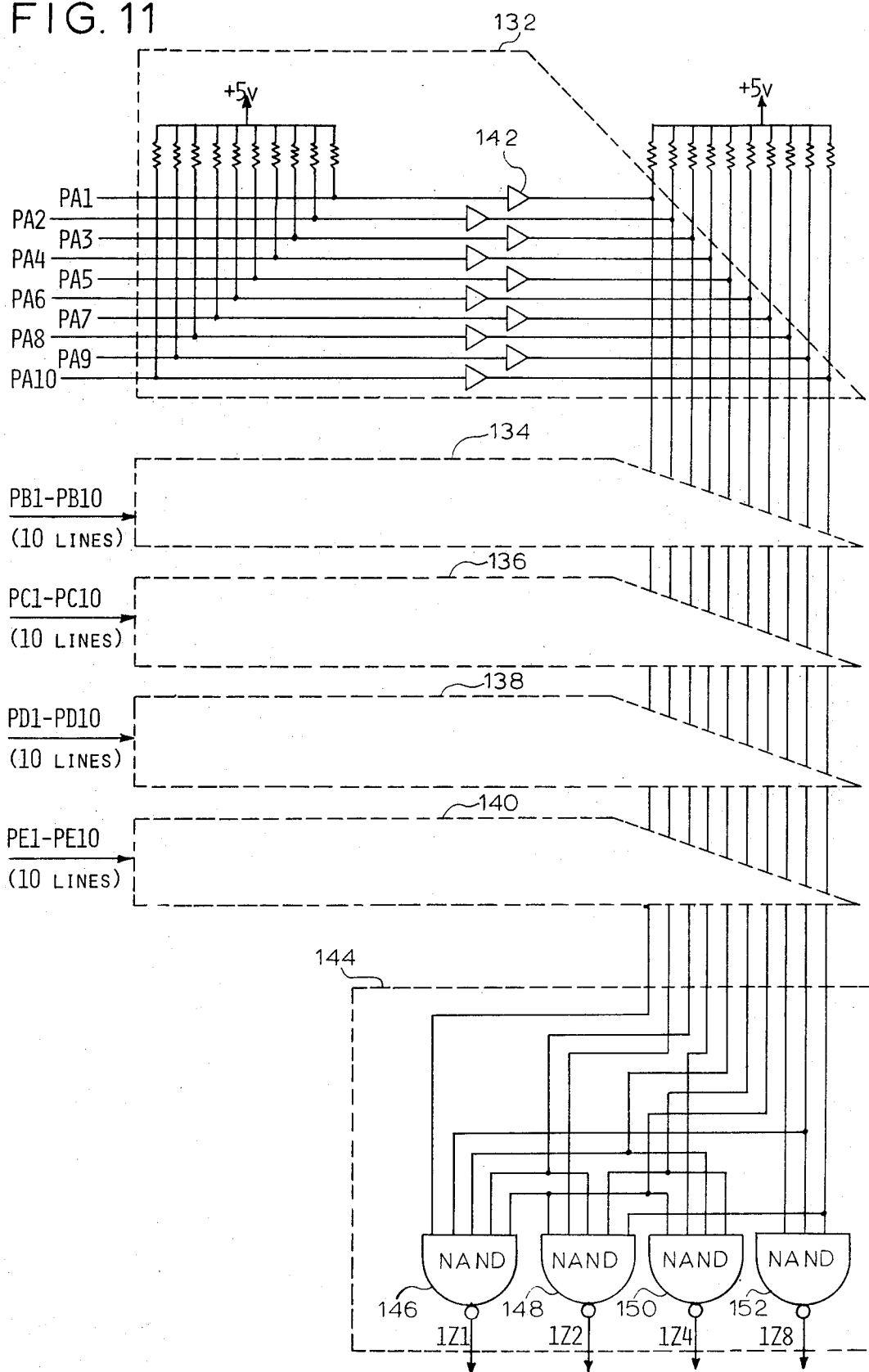
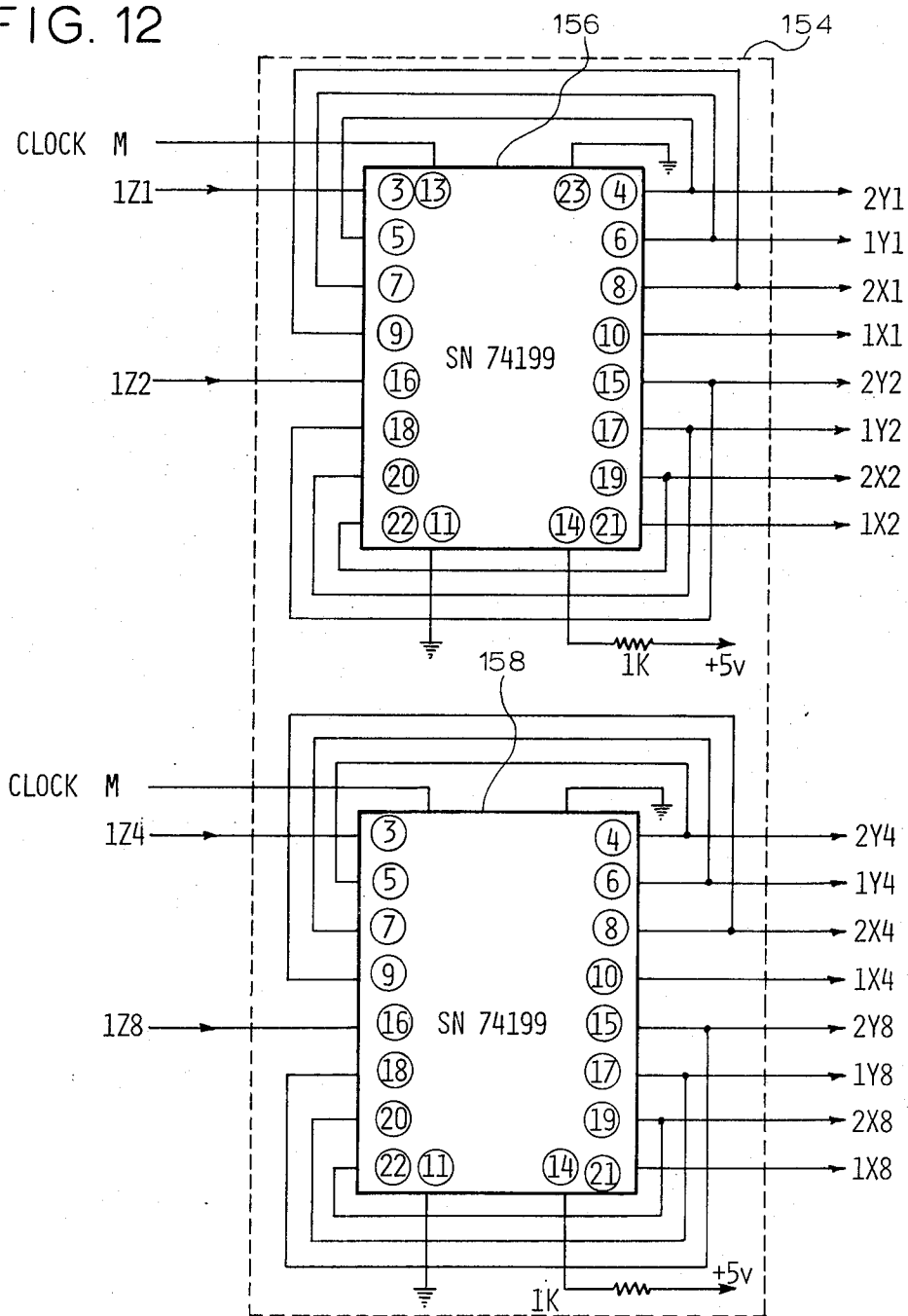


FIG. 12



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FIG. 13

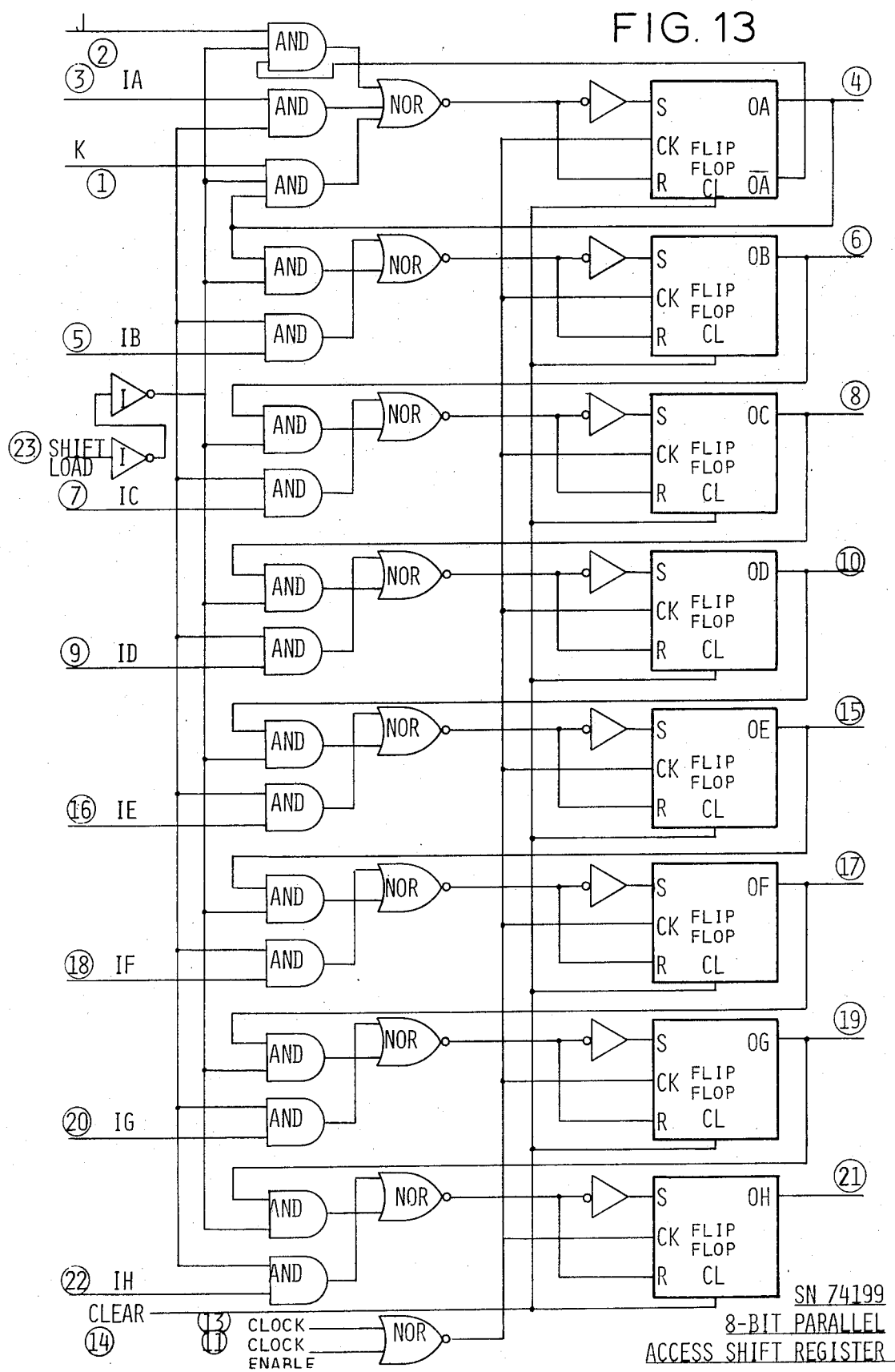


FIG. 14

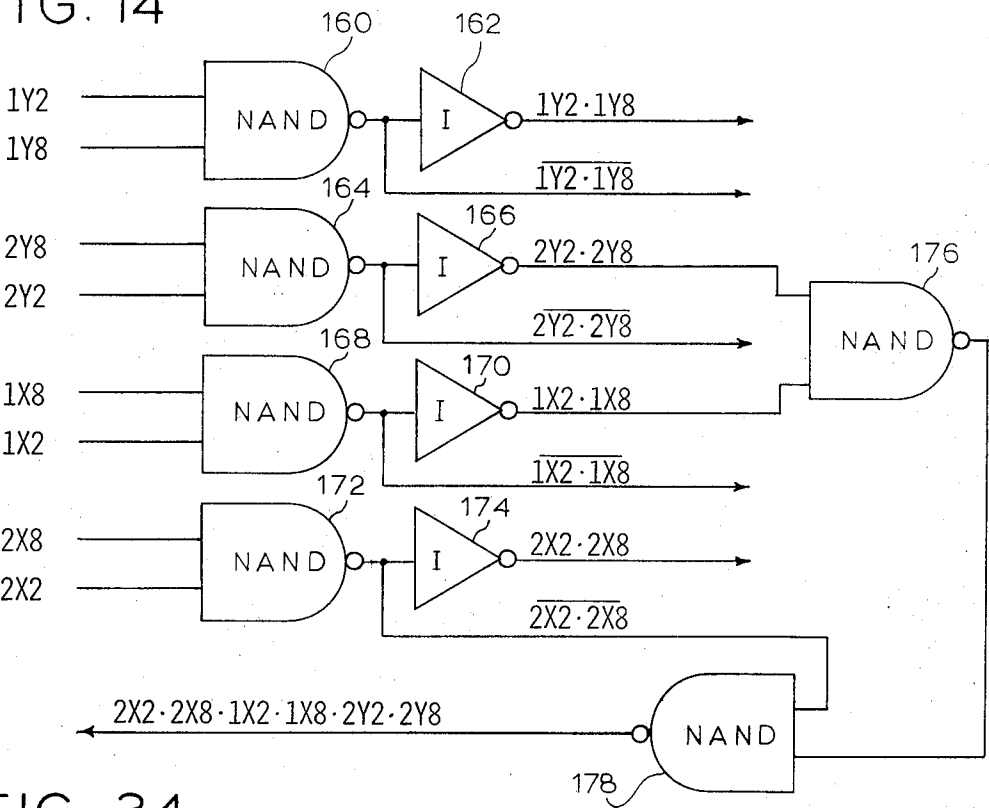
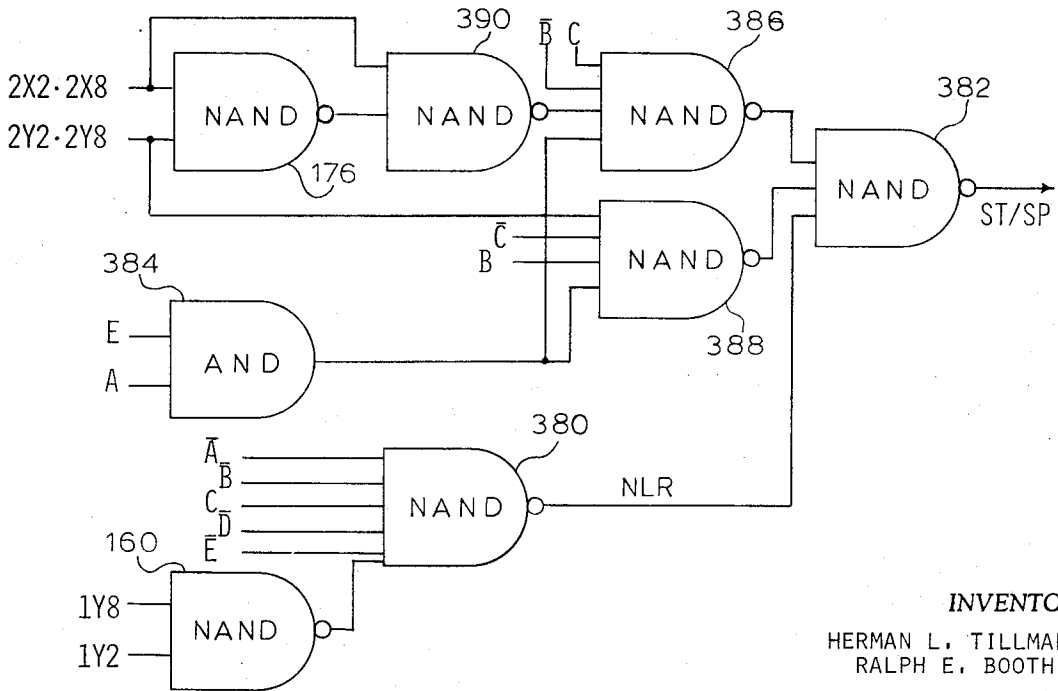


FIG. 34



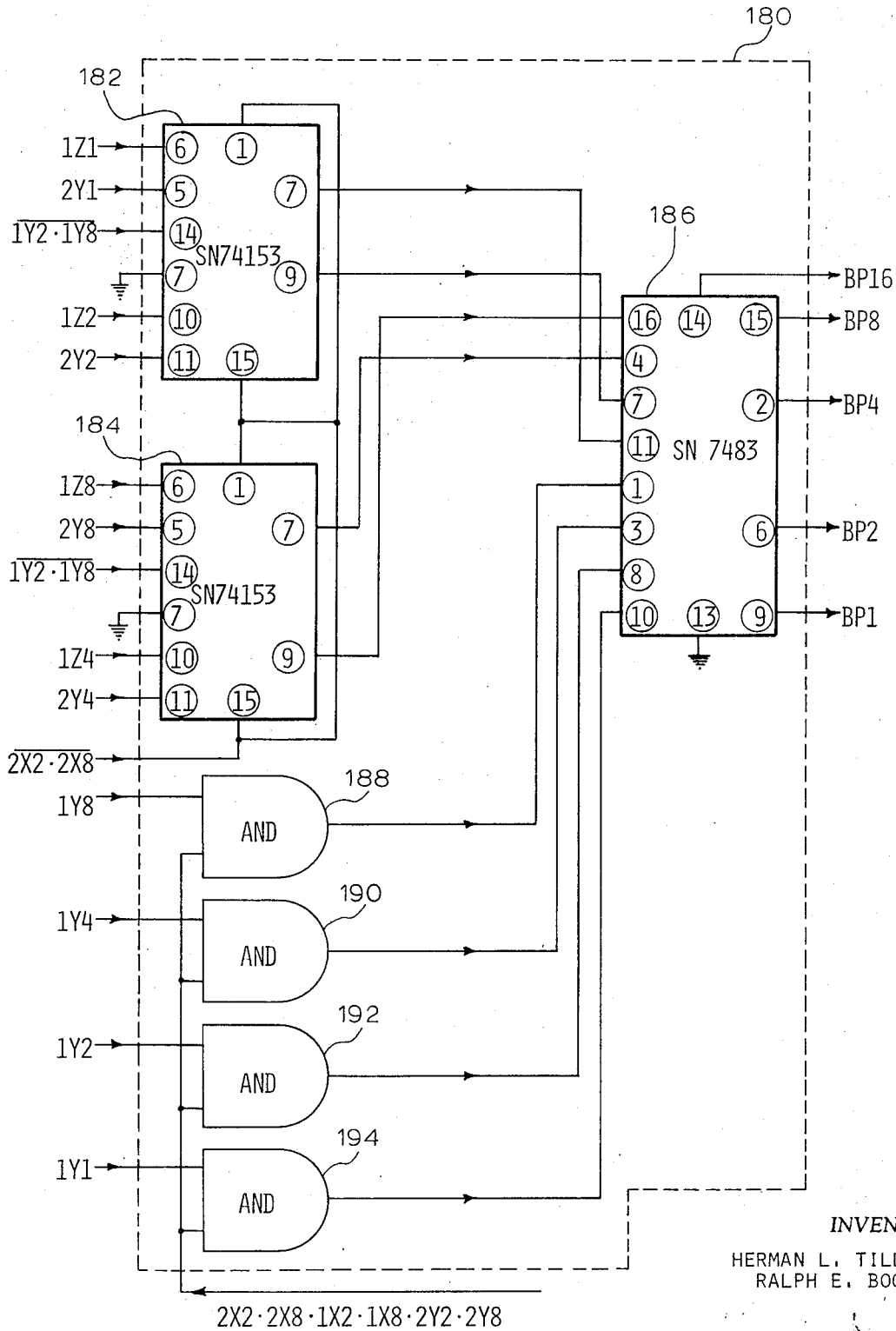
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FIG. 15



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FIG. 16

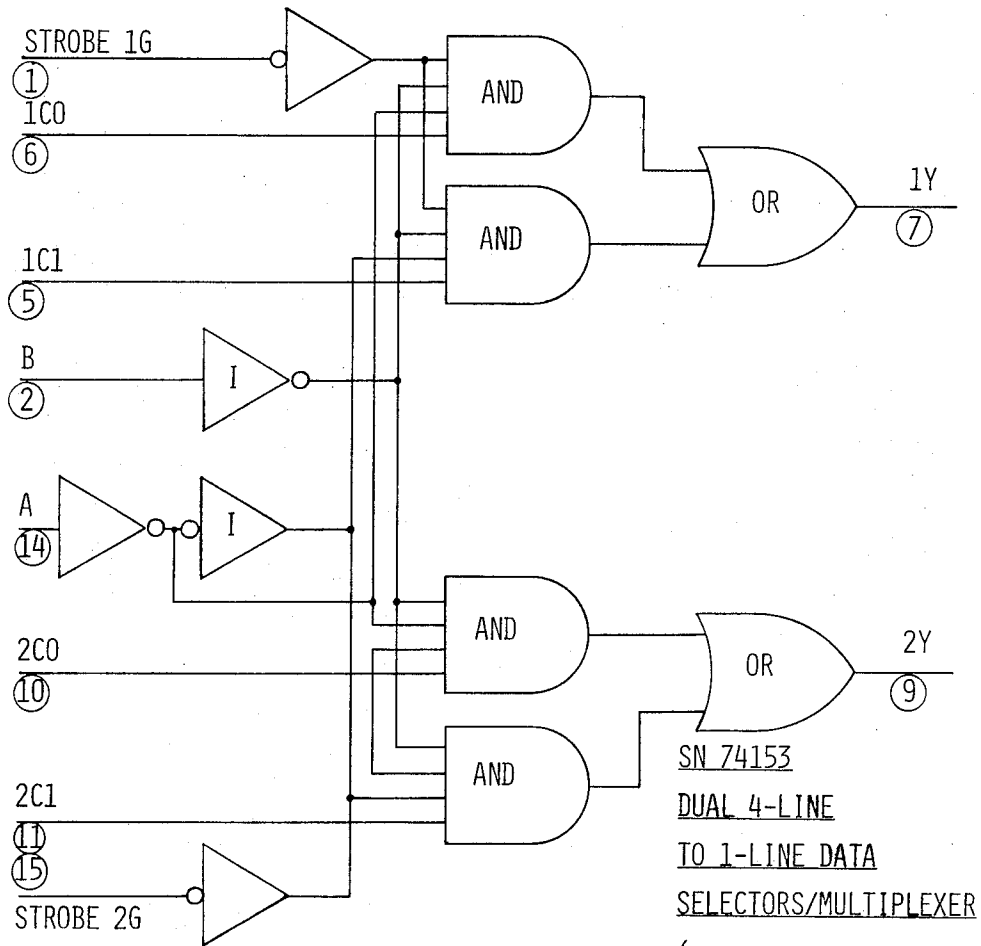
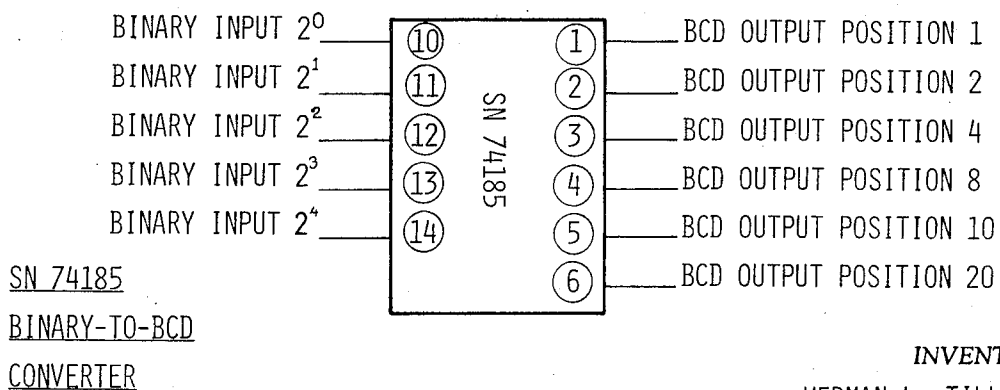


FIG. 20



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FIG. 17

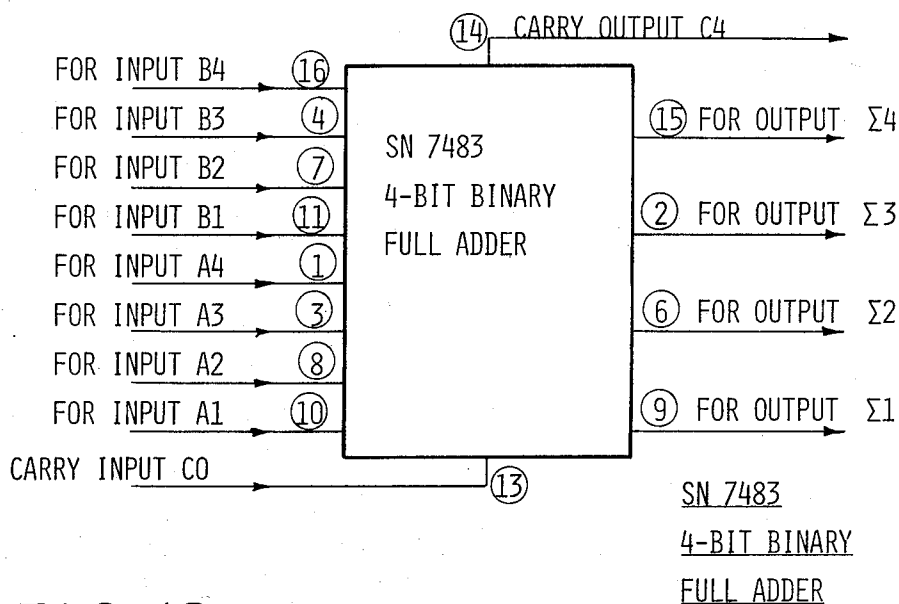
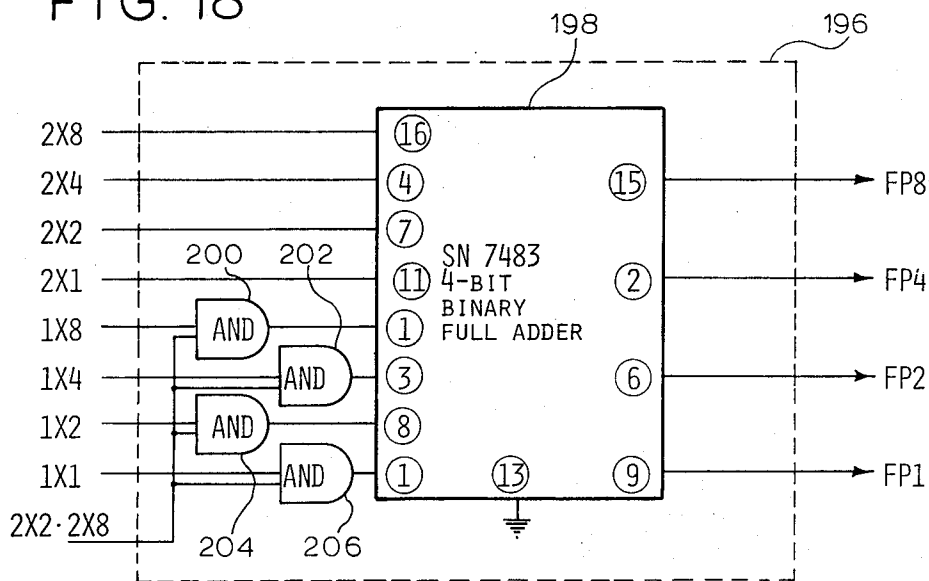


FIG. 18



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FIG. 19

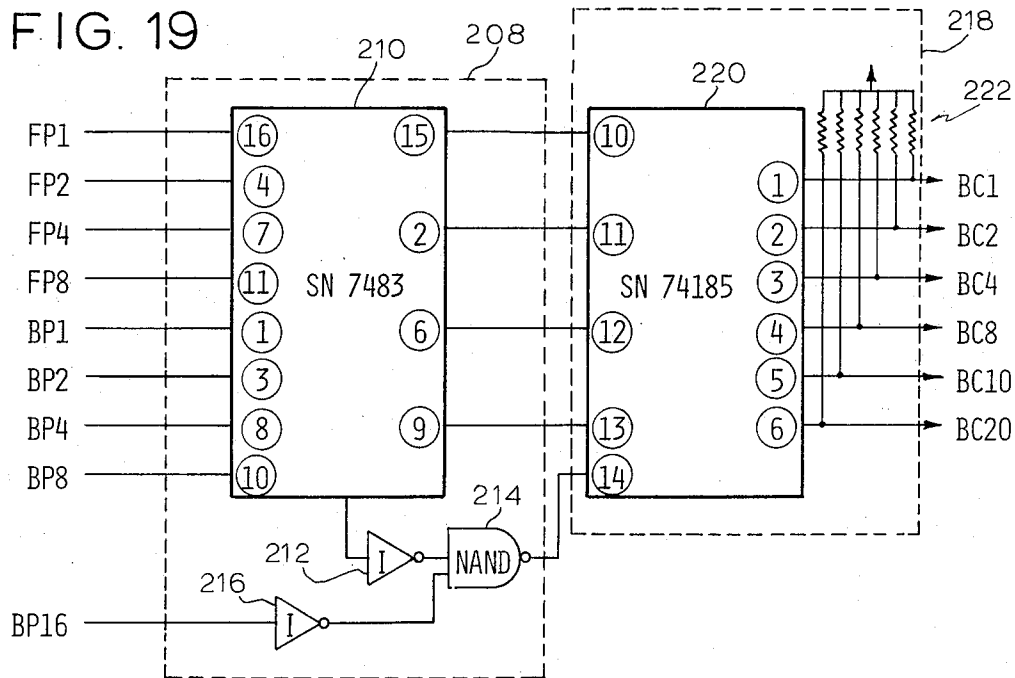
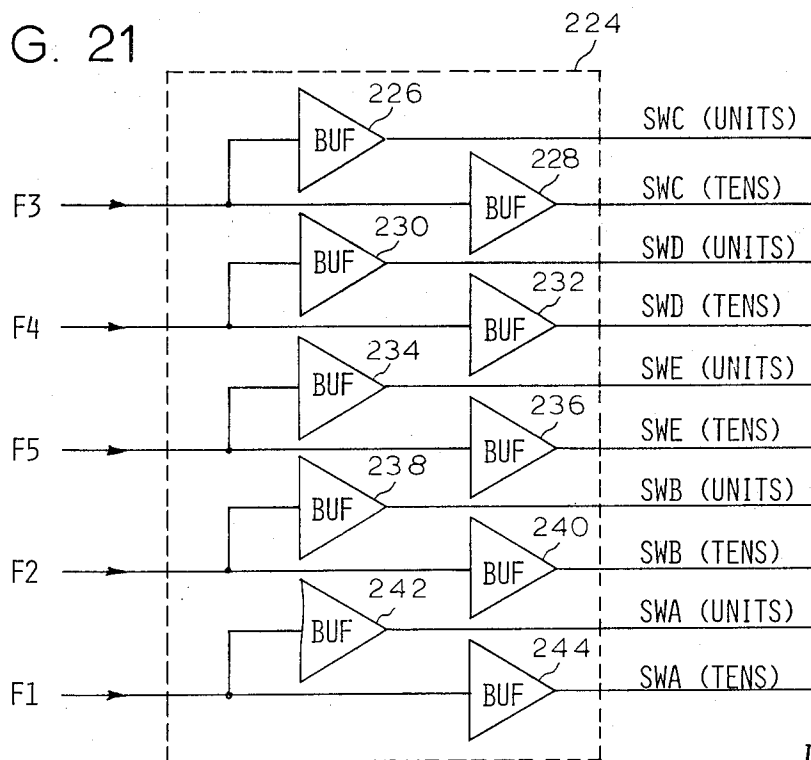


FIG. 21



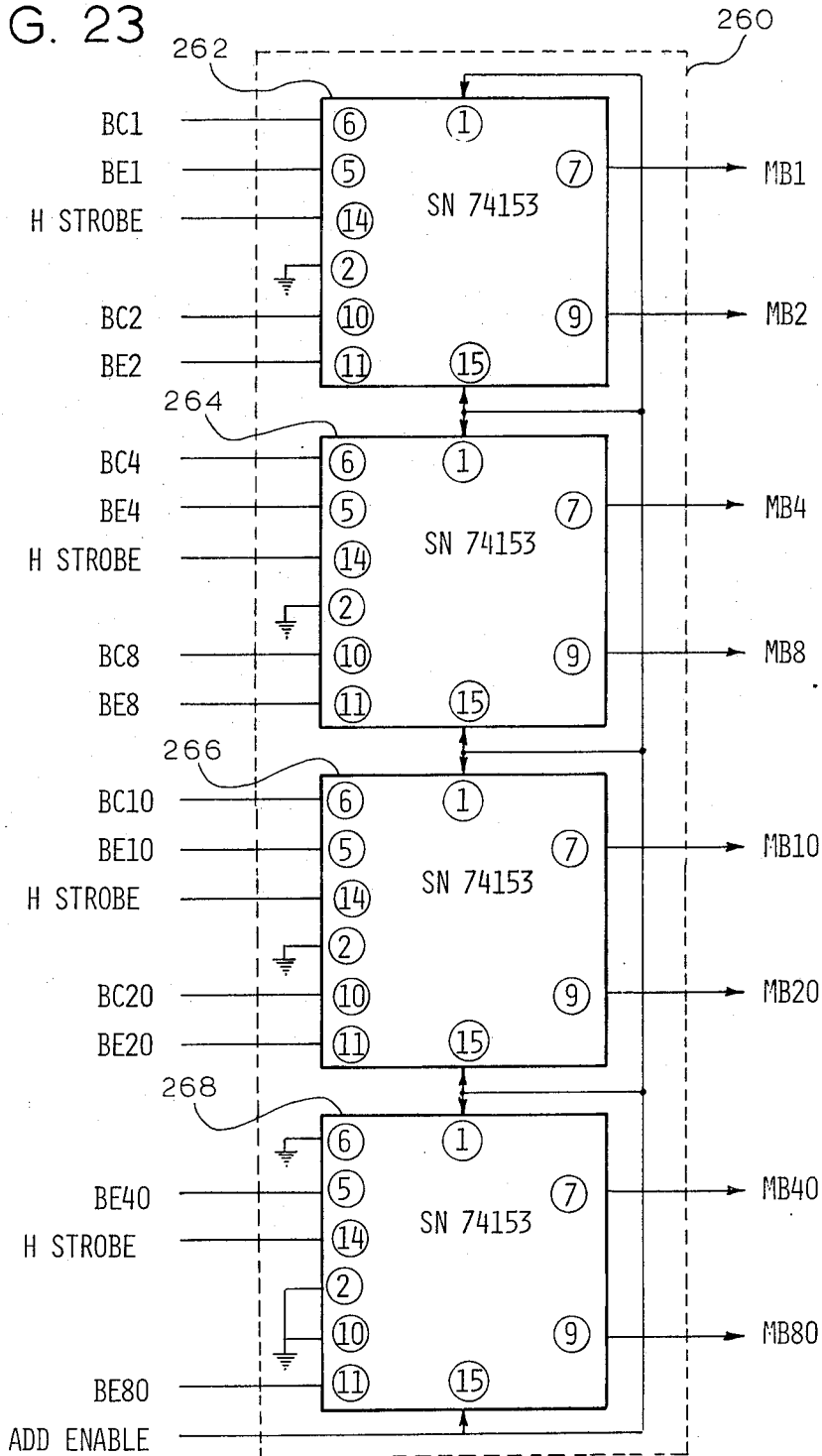
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FIG. 23



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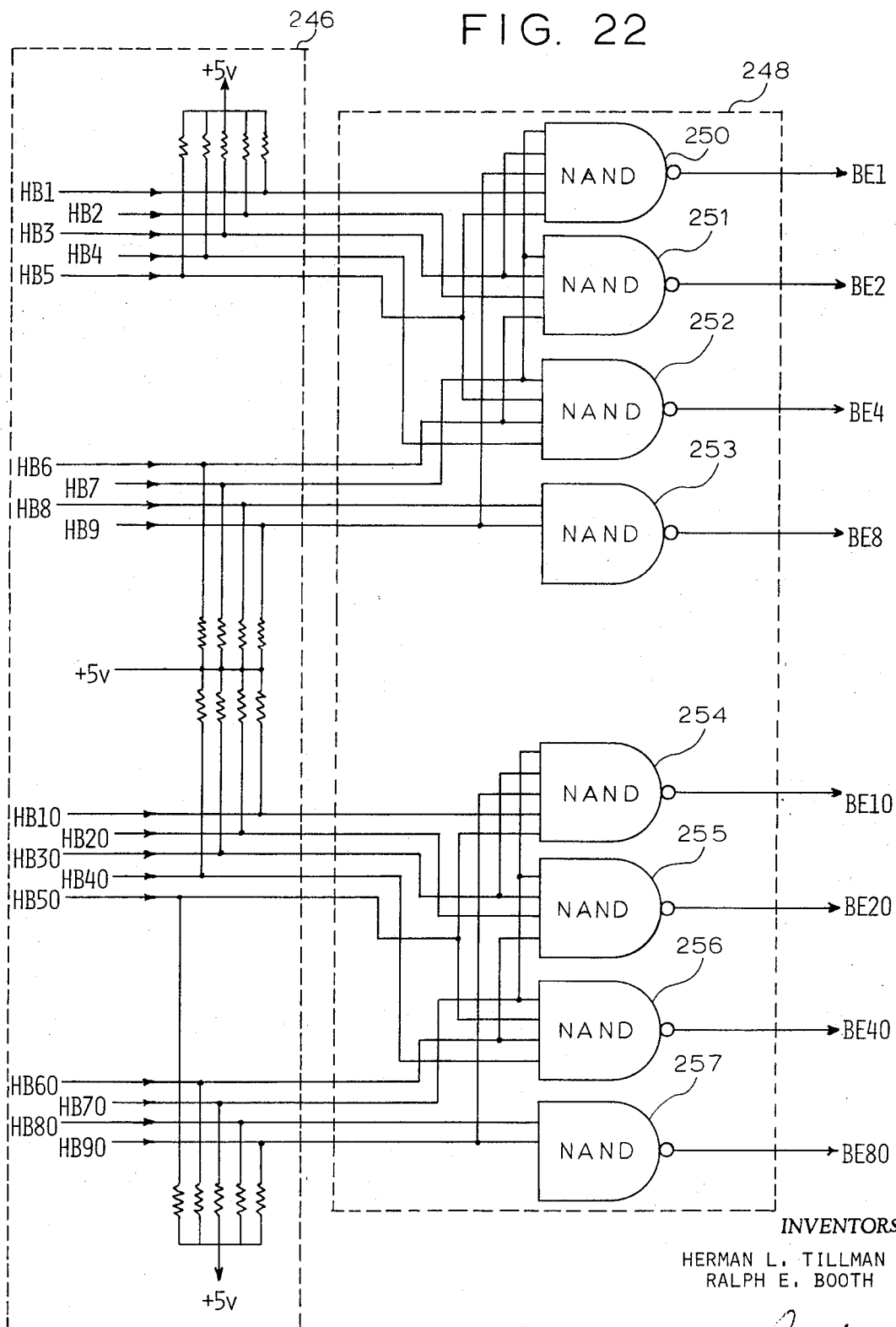
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FIG. 22



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FIG. 24

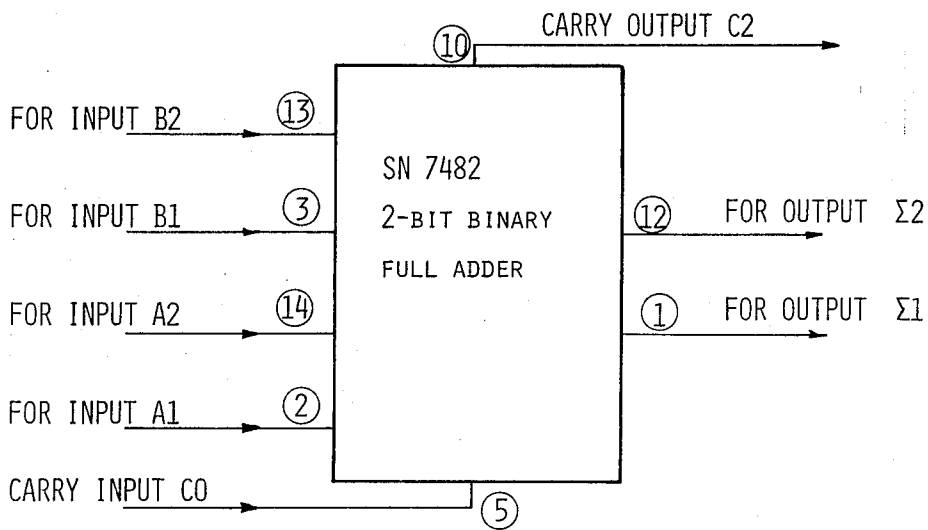
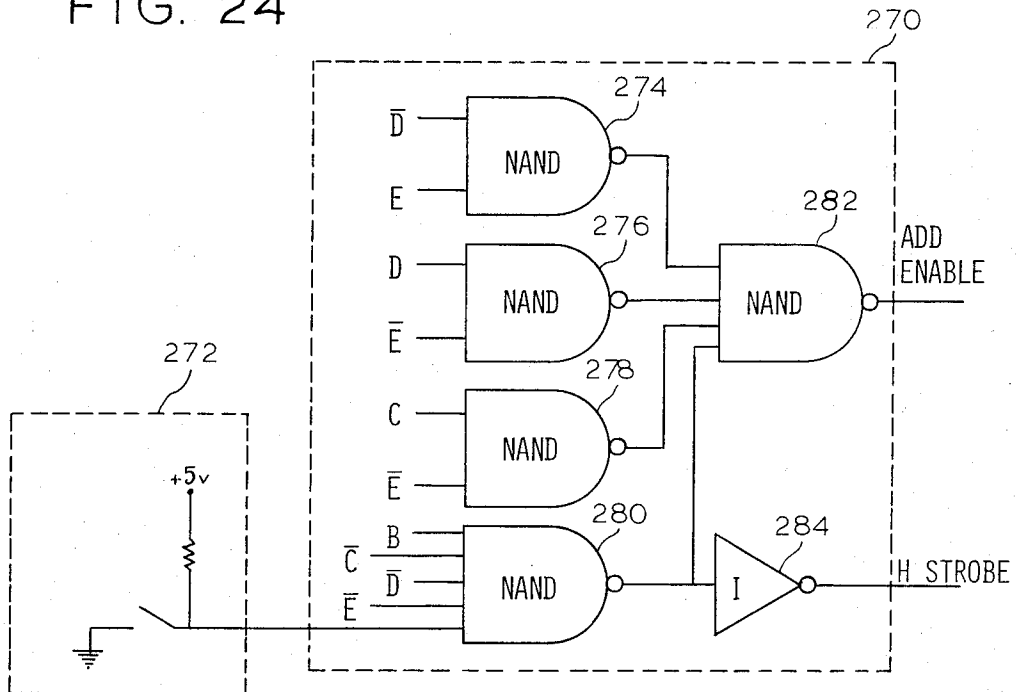


FIG. 26

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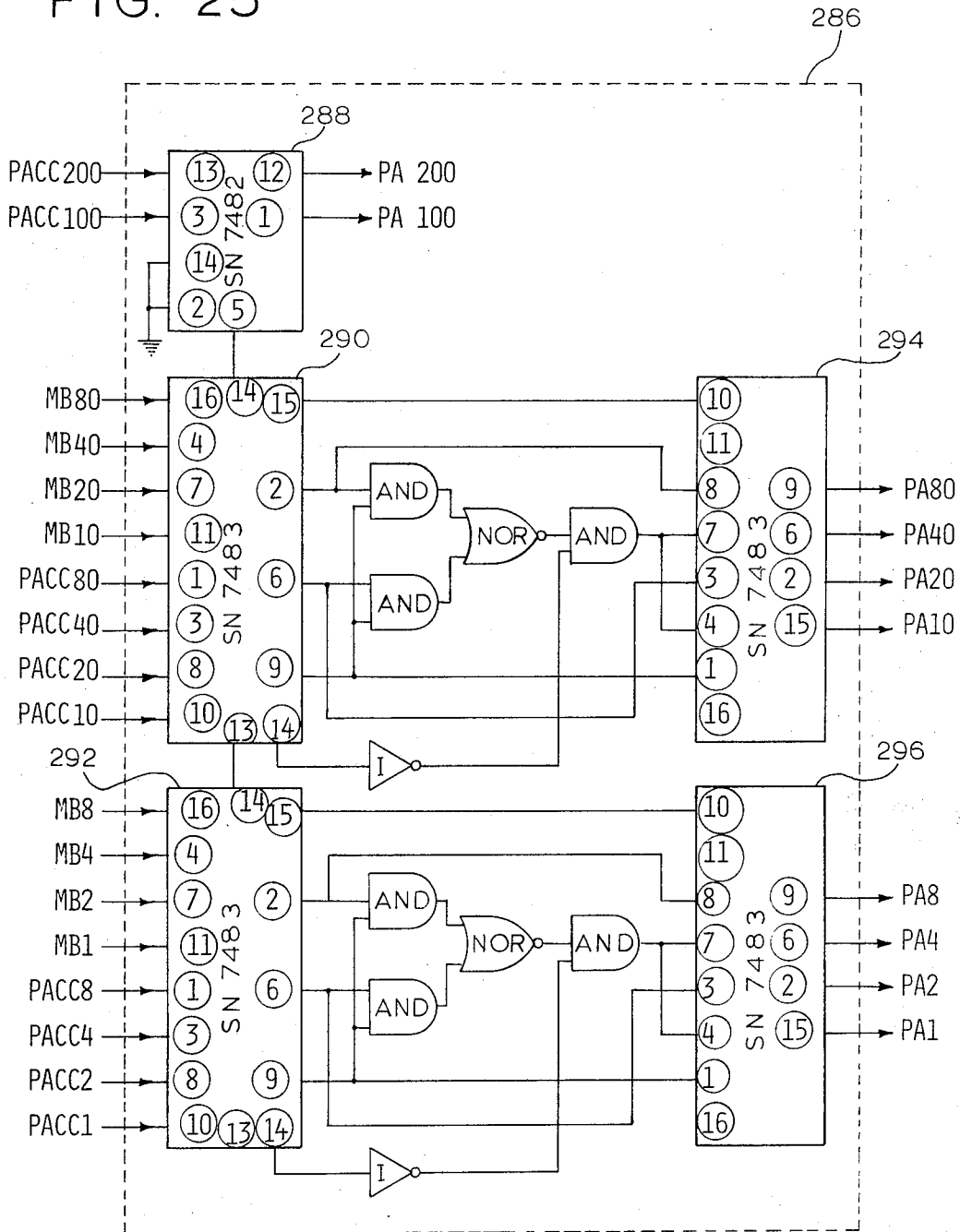
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FIG. 25



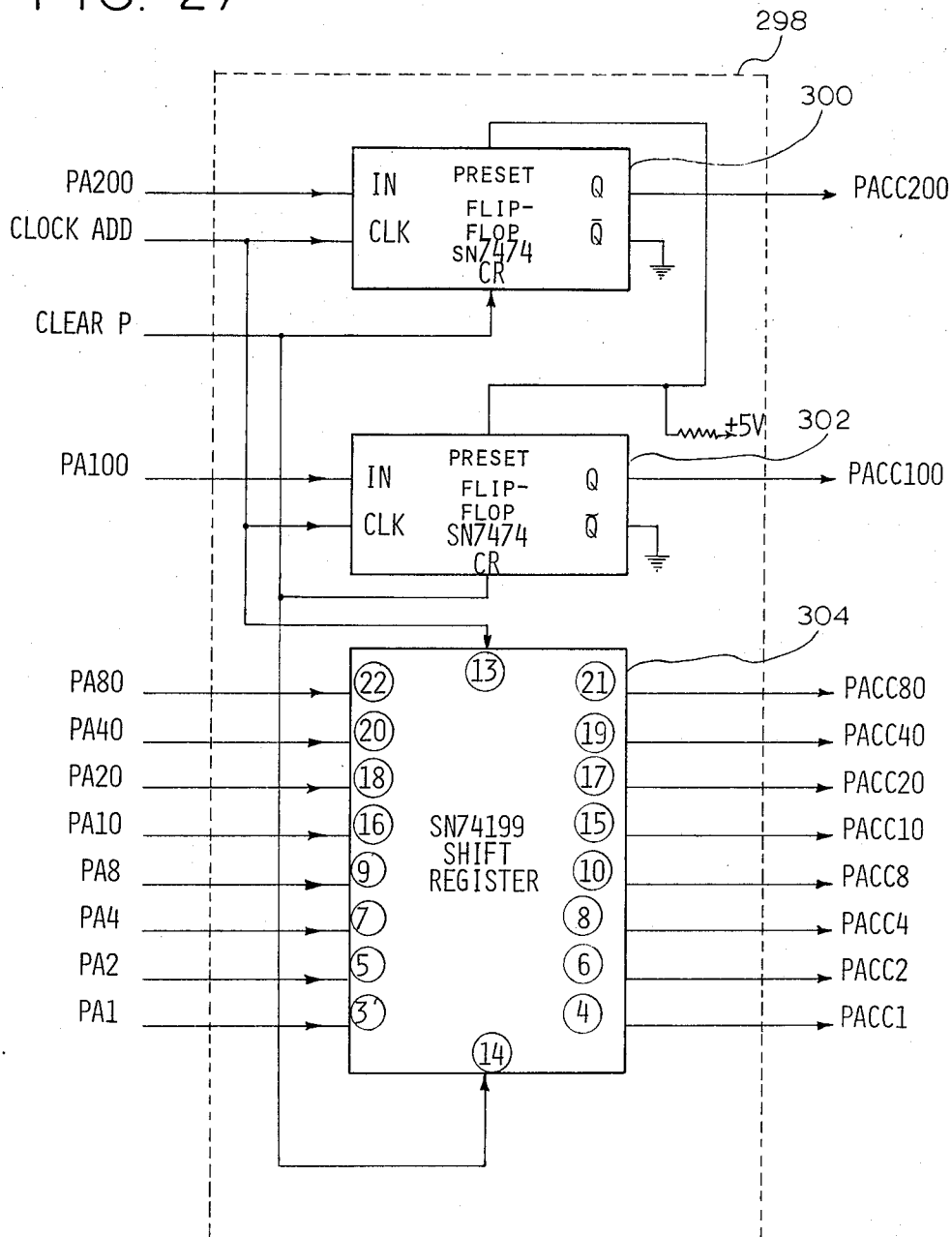
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FIG. 27



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FIG. 28

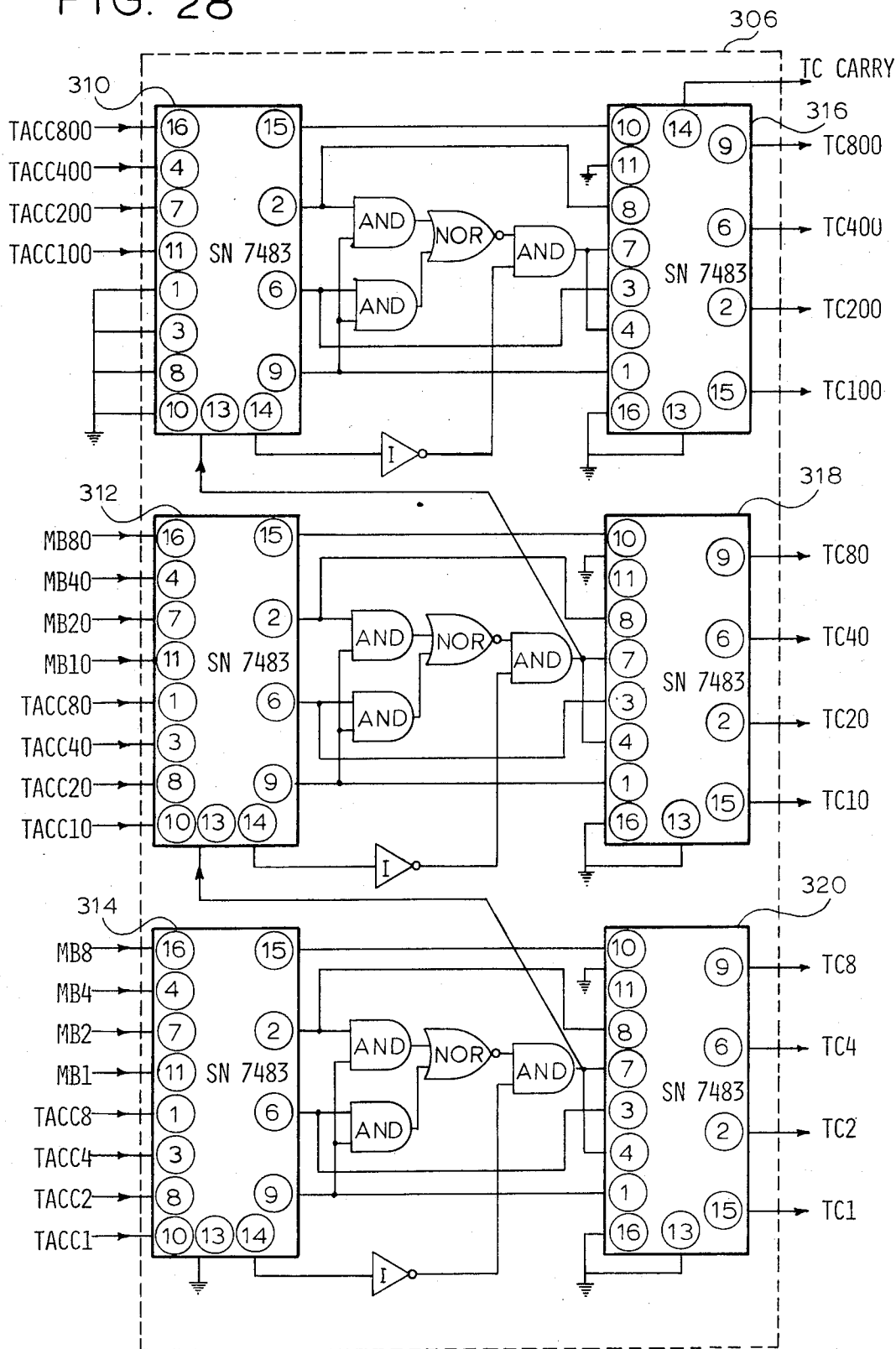
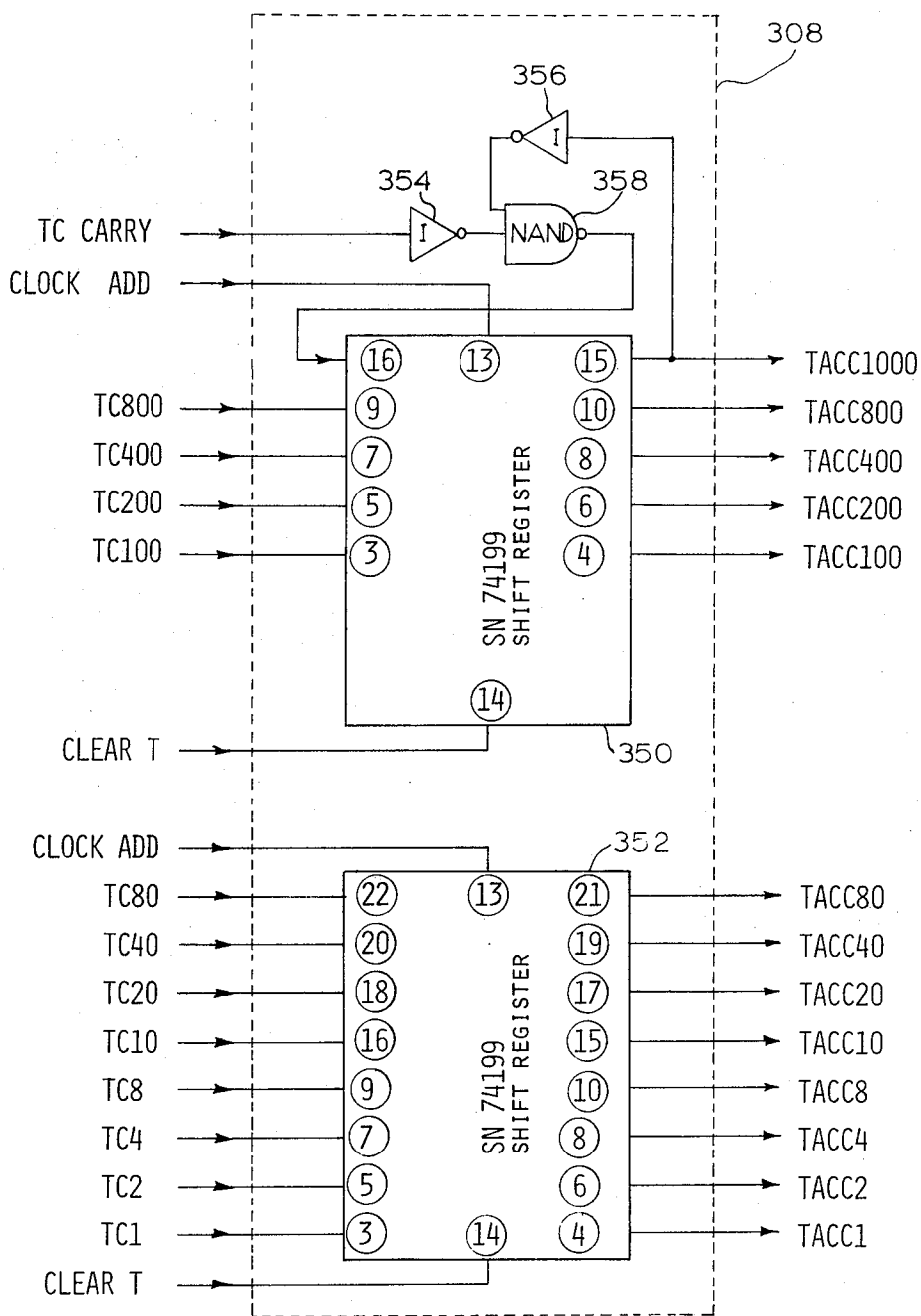


FIG. 29



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FIG. 30

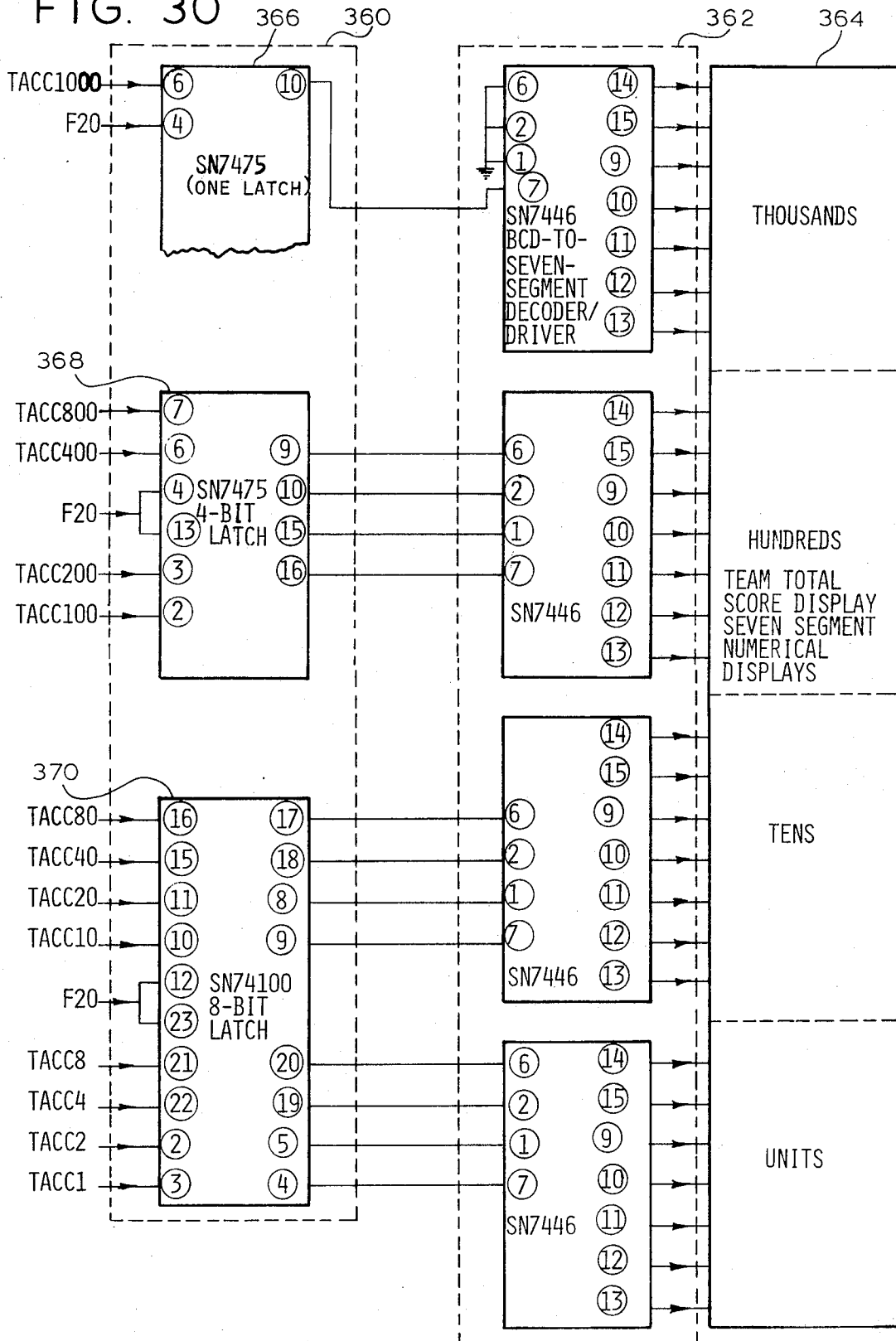


FIG. 31

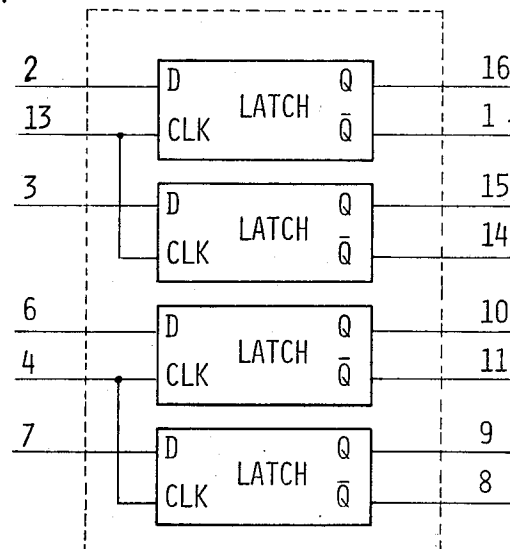
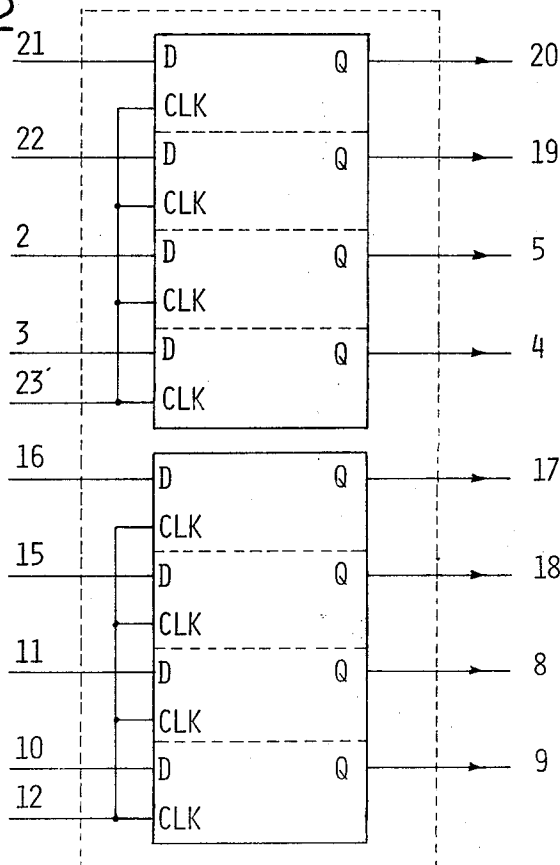


FIG. 32



SN74100
8-BIT BISTABLE
LATCH

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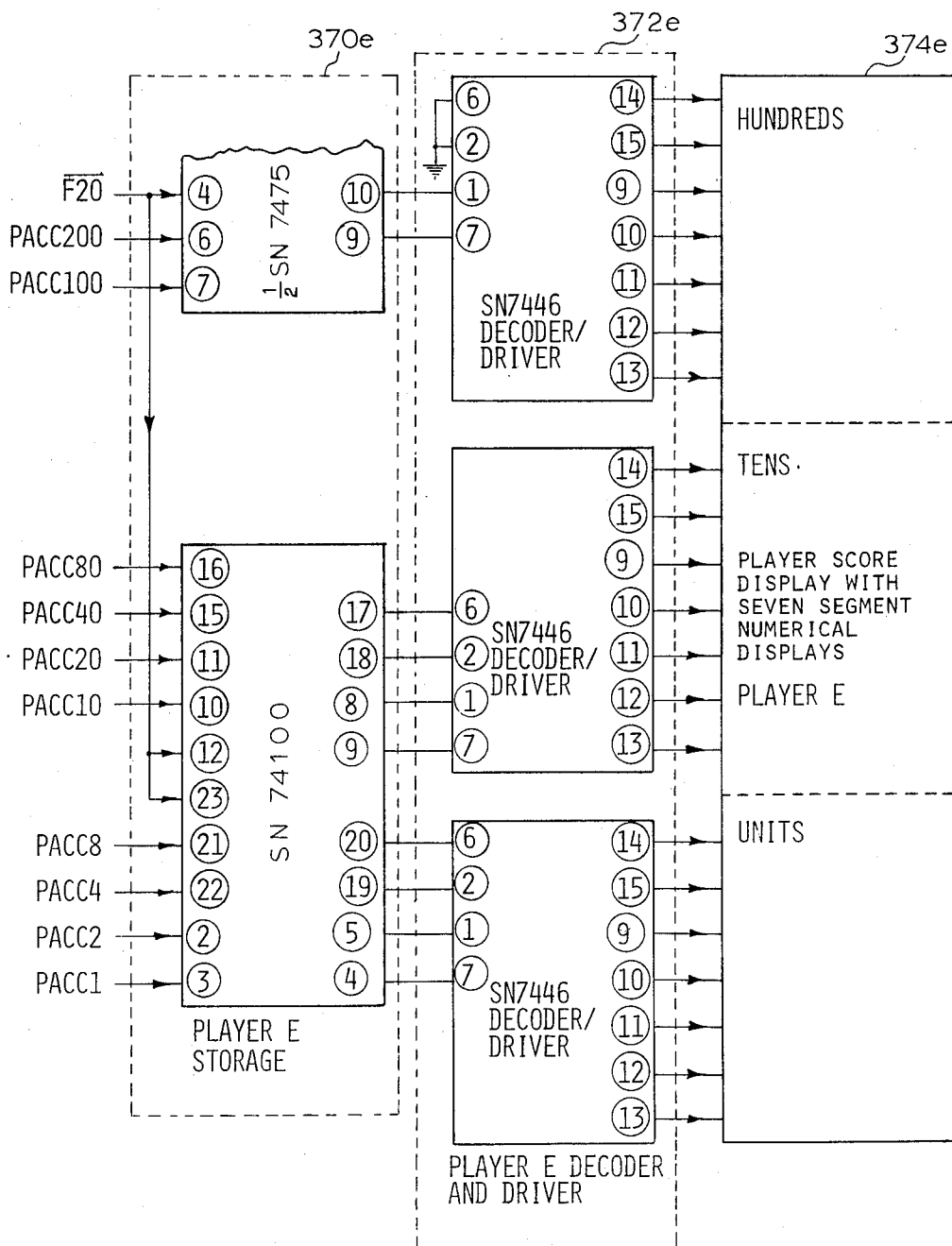
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FIG. 33a



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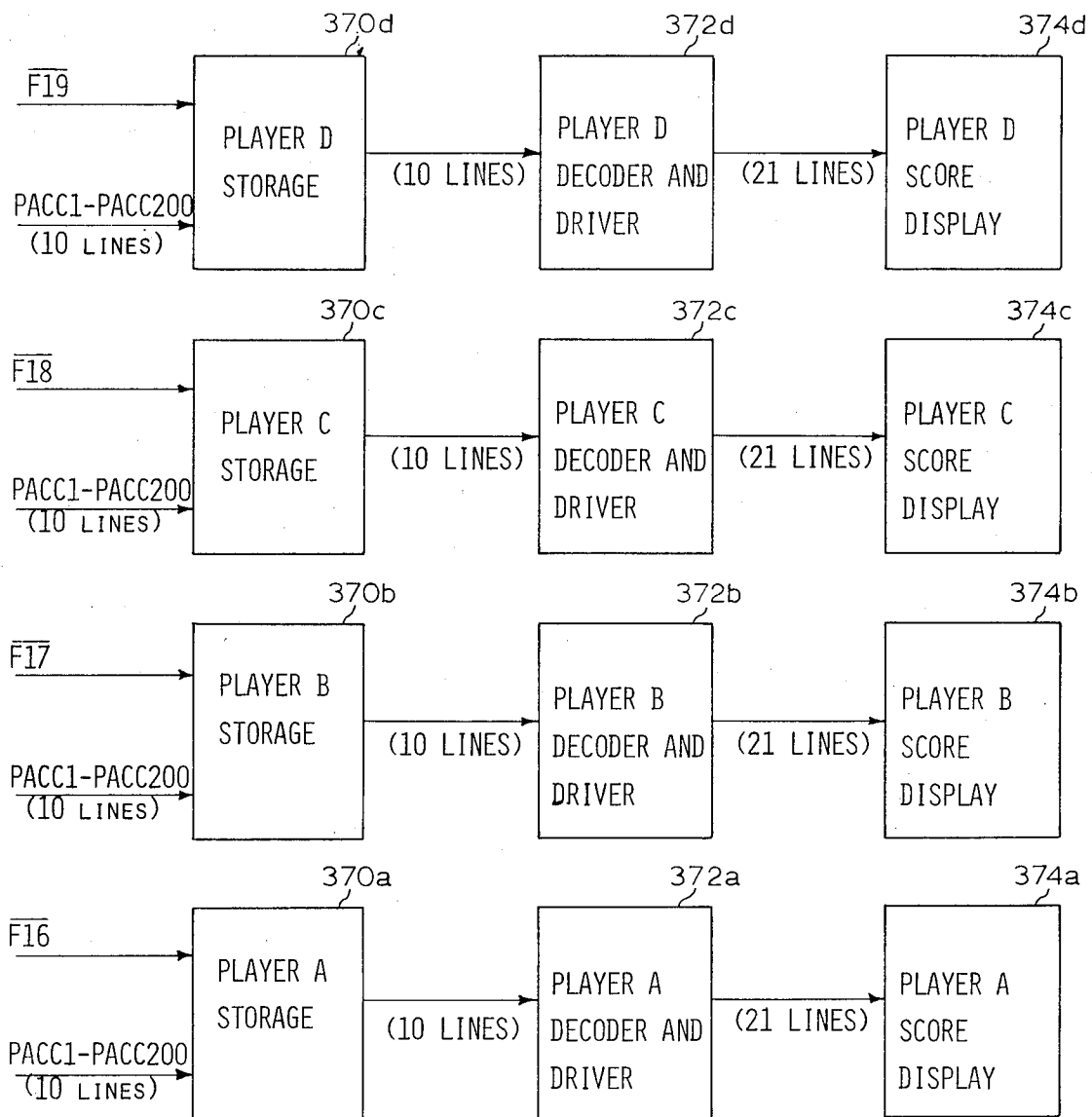
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FIG. 33b



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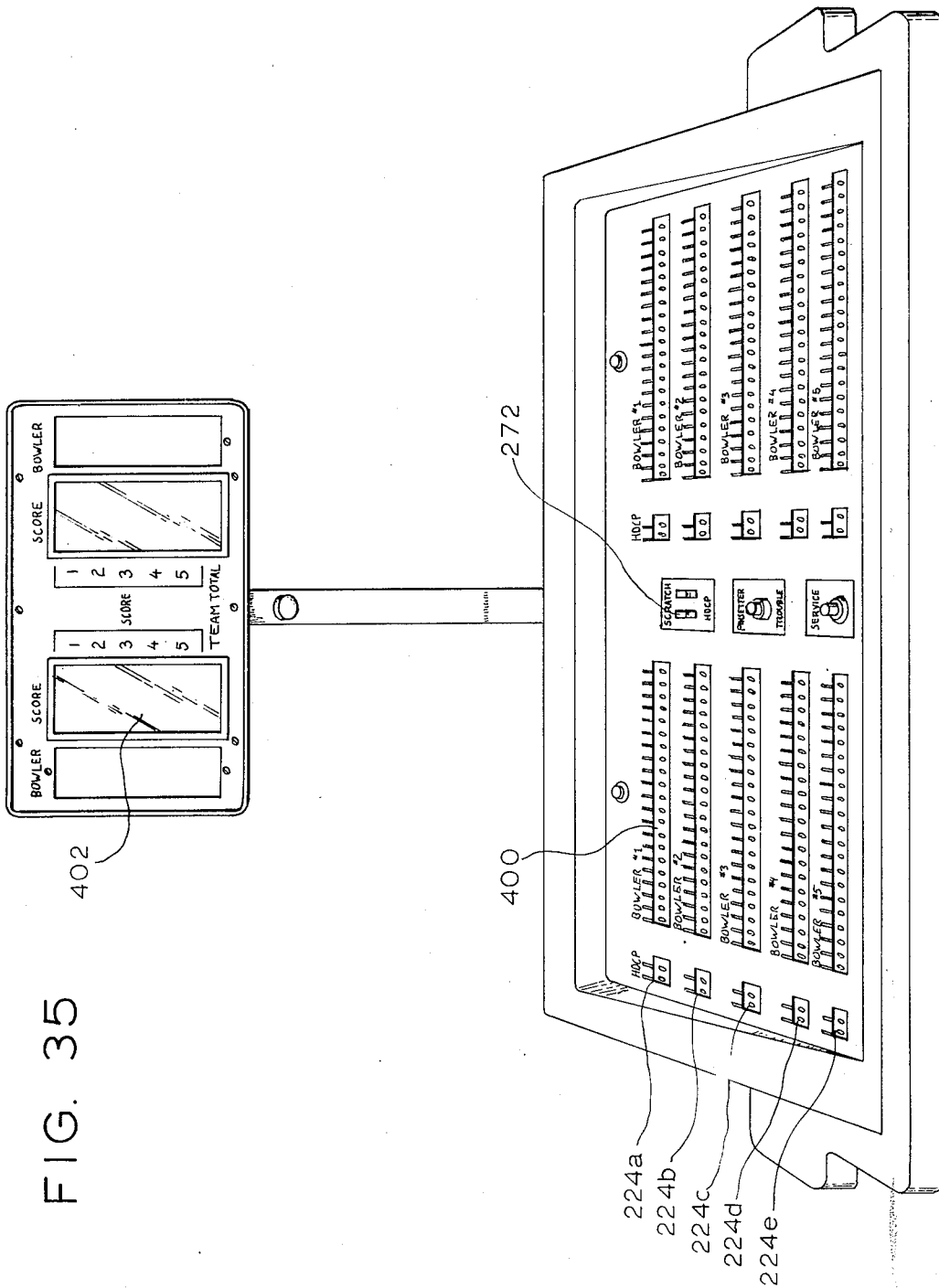


FIG. 35

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BOWLING SCORE COMPUTER**BACKGROUND OF THE INVENTION**

This invention relates to a computer for automatically calculating the score of a bowling game.

Most prior-art bowling scorers operate by automatically sensing the pinfalls which take place after a ball has been rolled, and by feeding this information into a computer which stores all of the information received and calculates resulting totals from this information. The expense of installing an automatic scoring system such as these in an existing bowling lane is increased by the necessity of remodeling the building in order to install the wiring which must run from the pin-sensing devices to the computer and to the controls.

Typically, in such prior art systems, one must choose initially whether the computer will calculate handicap or scratch bowling, and the subsequent calculations are limited to the initially chosen mode of operation.

SUMMARY OF THE INVENTION

In the preferred embodiment of the invention, there are 21 independent ball switches for each player of the plurality of players for whom the system is designed. Each ball switch is a thumb-wheel switch having a plurality of numerical positions for indicating the number of pinfalls caused by each of the balls, each switch representing the pinfalls caused by the ball associated with it. Not all of the thumb-wheel switches are actually used during the course of a typical game. The second switch in a frame is frequently bypassed because of a strike occurring for the preceding switch.

When the scoring system is operating, very little internal memory or alternative programming is necessary because the system operates in sequence to read each number entered on a ball switch as that number is needed for a running internal calculation. This running calculation of a player score calculates the score during the present frame and the associated bonus points for each new frame, and adds this new value to an accumulated total score for previous frames. Thus, other than the switches and the temporary memory needed for calculating the bonus points, the preferred embodiment requires for the calculation of the individual player's scores only the accumulator storage plus the individual storage for the display outputs.

It is a noteworthy feature of the preferred embodiment of the invention that, as soon as the switches have been read sequentially to allow calculation of resulting total scores during one sequential operation, the entire calculation is restarted in a periodical manner, thereby changing the outputs in accordance with any changes which may have been made in the condition of the input switches. For example, if an error has been made in entering an early score value, and this error is later discovered, it can be corrected by changing the switch, and the system will very quickly have reached another periodical calculation cycle during which a new value is calculated to eliminate the result of the error.

The preferred embodiment also has a handicap switch for each player. This switch is another thumb-wheel switch which allows a value to automatically be added to the score of the designated player. It is a feature of this invention that a handicap mode switch can be turned on or off, indicating that the scoring should be done in the handicap mode or the scratch mode.

Whenever such a change in this handicap mode switch condition is made, the periodic recalculation will soon take place and provide a new output value in the newly chosen mode. It should be noted that in the preferred embodiment the periodic recalculation does not take place because a change is made in the input conditions, but takes place regularly and can be expected to follow soon after any change in input conditions.

Thus the preferred embodiment of the invention operates sequentially in that it attends, step by step, to input information at each of the relevant ball switches and other input switches in a sequential manner. The calculations which take place also follow in a sequential manner from the reading of the input data from the switches. The system also operates in a periodical manner in that, after the completion of a sequential pattern of calculation, it then begins another similar pattern of calculation, which may or may not have the same result depending upon whether or not any of the input data has been changed since it was last sequentially read.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1, which comprises FIGS. 1a and 1b, is an overall block diagram of the bowling scorer computer system.

FIG. 2 is a block diagram of the system oscillator, the ball counter and the player counter of the overall diagram.

FIG. 3 is a diagram of a commercially available oscillator for use in the preferred embodiment.

FIG. 4 is a diagram of a commercially available 4-bit binary counter for use in the preferred embodiment.

FIG. 5 is a diagram of a commercially available decade counter for use in the preferred embodiment.

FIG. 6 is a more detailed diagram of the player selector and strobe unit.

FIG. 7 is a diagram of a commercially available decoder/demultiplexer for use in the preferred embodiment.

FIG. 8 is a diagram of a logic circuit for deriving a CLEAR T signal from a CLEAR P signal.

FIGS. 9 and 10 together illustrate the details of a decoder and strobe unit for use in the preferred embodiment.

FIG. 11 illustrates the ball switch outputs used in the preferred embodiment.

FIG. 12 is a diagram of a temporary memory used in the preferred embodiment.

FIG. 13 is a diagram of a commercially available 8-bit parallel-access shift register for use in the preferred embodiment.

FIG. 14 is a diagram of certain logic circuitry for use with the ball switches in the preferred embodiment.

FIG. 15 is a more detailed block diagram of the control binary adder for bonus points for use in the preferred embodiment.

FIG. 16 is a diagram of a commercially available dual 4-line to 1-line data selector/multiplexer for use in the preferred embodiment.

FIG. 17 is a diagram of a commercially available 4-bit binary full adder for use in the preferred embodiment.

FIG. 18 is a block diagram of the control binary adder for present-frame points for use in the preferred embodiment.

FIG. 19 is a more detailed block diagram of a binary adder for use in the preferred embodiment.

FIG. 20 is a block diagram illustrating the input and output values of a binary-to-BCD converter for use in the preferred embodiment.

FIG. 21 illustrates the input system for handicap switch wipers in the preferred embodiment.

FIG. 22 illustrates the wire-ANDed decimal handicap switch outputs for use in the preferred embodiment.

FIG. 23 illustrates in greater detail the multiplexer arrangement for use in the preferred embodiment.

FIG. 24 illustrates the handicap strobe unit and handicap switch for use in the preferred embodiment.

FIG. 25 illustrates the player BCD adder for use in the preferred embodiment.

FIG. 26 illustrates the commercially available two-bit binary full adder for use in the preferred embodiment.

FIG. 27, illustrates the player total accumulator register for use in the preferred embodiment.

FIG. 28 illustrates the team BCD adder for use in the preferred embodiment.

FIG. 29 illustrates the team total accumulator register for use in the preferred embodiment.

FIG. 30 illustrates the team storage and register unit for use in the preferred embodiment.

FIG. 31 illustrates a commercially available 4-bit bistable latch unit for use in the preferred embodiment.

FIG. 32 illustrates a commercially available 8-bit bistable latch unit for use in the preferred embodiment.

FIG. 33, comprising FIGS. 33a and 33b, illustrates the output system for the scores of the various individual players, for use in the preferred embodiment.

FIG. 34 illustrates a logic circuit for use when ball switches 19 and 20 are being strobed.

FIG. 35 is a perspective drawing of the console unit for input data to and output data from the scorer system.

DESCRIPTION OF THE PREFERRED EMBODIMENT

FIGS. 1a and 1b are an overall block diagram of the bowling score computer. Oscillator 50 is the master clock of the system and drives a ball counter 52, which in turn drives a player counter 54. The ball counter successively counts through the possible balls rolled by each player, and the player counter, upon the completion of the count of the balls rolled by one player counts up to the next succeeding player in the computational order.

The outputs of the player counter and the ball counter are respectively applied to player selector and strobe unit 80 and ball selector decoder and strobe unit 108. These strobe units are used to successively detect the position of the individual ball switch wipers of the individual players, one at a time, in a predetermined order. The outputs of the strobe units are applied to the ball switch wipers 132 to provide an output from the single chosen wiper to wire-ANDed decimal ball switch outputs 134 as a decimal-output signal related to the value set on the chosen switch. This decimal output value is converted by a decimal-to-binary encoder 144 to a binary signal, which is applied to and stored in temporary memory 154.

Temporary memory 154 stores the number of pin-falls from two complete frames (i.e., four balls) as these

values are sequentially read from the ball switches. The scored values are used in connection with the incoming value of the first ball of a third frame in order to derive the strike/spare information needed to determine the number of bonus points resulting from strikes or spares. Control binary adder for bonus points 180 receives information from memory 154 corresponding to the stored values and information from encoder 144 corresponding to the first ball in the third frame to derive the value of the bonus points determined during a given frame. The stored information from memory 154 for the given frame is also applied to control binary adder for present frame points 196 to determine the total number of points scored in a present frame by both balls. The outputs from adders 180 and 196 are applied to a binary adder 208 to determine the total points to be entered for a given frame. The binary-value output from adder 208 is applied to binary-to-binary-coded-decimal converter 218 to derive a BCD frame value for application to a multiplexer 260.

In order to allow the addition of handicap points to the scores of individual players, the player selector and strobe 80 provides an indication of the player whose score is being totalled to handicap-switch wipers 224. These switches are thumb-wheel switches on which the handicap of the player is numerically set up. The handicap value of the particular player is strobed from the switches onto wire-ANDed decimal handicap switch outputs 246 in a manner similar to that of element 134. The outputs from element 246 are applied to a decimal-to-binary-coded-decimal encoder to provide a BCD handicap signal to the multiplexer 260. In order to add in the handicap value only once during the sequential determination of ball values, an output from the ball counter is applied to handicap strobe unit 270 to cause the handicap strobe unit to gate the signal from encoder 248 through multiplexer 260 at the appropriate time. A handicap switch 272 controls the handicap strobe, thereby allowing the system to operate in either the handicap mode or the scratch mode, as the situation warrants.

Multiplexer 260 provides outputs to player BCD adder 286 and team BCD adder 306. The output to the player adder is summed, using a player total accumulator register 298 in a manner such that frame by frame the score of an individual player is totalled in the accumulator with the previously stored value from the accumulator for preceding frames. At the appropriate time, the handicap score is also added to the individual player's score.

Following the accumulation in register 298 of the total score of an individual player, this accumulated value is gated into the appropriate one of five player storage and register units 370a through 370e, corresponding to whichever player's score has been accumulated. The stored value is continuously read out through the decoder and driver and seven-segment display unit associated with the respective player storage and register unit.

The same information is also read out into the team BCD adder 306. However, the team total accumulator register 308 is allowed to accumulate the entire score of the team, rather than to be strobed at the end of each player score to empty its contents into the succeeding storage and register unit. With the team total accumu-

lator register, the strobing of the output takes place after the entire team score has been accumulated, at which time the accumulated value is strobed as a team storage and register 360. The contents of storage and register unit 360 are continuously decoded by decoder and driver-unit 362 for continuous display by a seven-segment display unit 364.

FIG. 2 illustrates, in greater detail, the system oscillator 50, the ball counter 52, and the player counter 54. The oscillator 50 operates as the master clock of the system and generates a square-wave signal at a preferred frequency of 200 kp/s. In the preferred embodiment, the oscillator is constructed of an integrated circuit of the type sold by Texas Instruments under the circuit number SN7413, and which is more fully illustrated in FIG. 3. The circuit SN7413 is a Schmitt-trigger circuit functioning as a 4-input NAND gate, and having a different input threshold levels for positive- and negative-going signals. In the oscillator of FIG. 3, the four inputs are connected together to provide a common input for connection by resistive feedback to the output of the circuit SN7413. Capacitive connection is provided between the interconnected input circuits and ground in order to provide an oscillator. The frequency of oscillation of this element can be adjusted by varying the values of resistor 56 and capacitor 58. A direct output T is taken from the output from the circuit SN7413. An additional output CLOCK M is provided through inverter 60.

The output from inverter 60 is provided to the input of ball-counter circuit 52. The active element in ball-counter 52 is a 4-bit binary counter of the type provided by the Texas Instrument as an integrated circuit under the circuit number SN7493, and illustrated in FIG. 4. By the interconnection of terminals 12 and 1 of this counter illustrated as elements 62, the counter is caused to function as a serial interconnection of four flip-flops. As the details of this integrated circuit are so well known in the commercial embodiment of Texas Instrument, no further discussion or disclosure other than that shown in FIG. 4 is considered necessary for an adequate understanding of the binary counter circuit. The output from the first stage flip-flop of counter 62 is labelled throughout this disclosure as signal A, that from the second stage as signal B, that from the third stage as signal C, and that from the fourth stage as signal D. Signal A is inverted in an inverter 64 and combined with the CLOCK M signal in an AND gate 66 to provide a CLOCK ADD signal at the output of this AND gate. Inverters 68, 70, 72, and 74 are respectively provided with input signals A, B, C, and D to provide as output signals $\bar{A}$, $\bar{B}$, $\bar{C}$ and $\bar{D}$. The D output is also provided to the first stage of a decade counter 76 of the type sold by Texas Instrument as circuit number SN7490, and more fully illustrated in FIG. 5. The first stage of the counter in element 76 operates as the fifth serial stage of counter 62 and provides the fifth output E which is inverted in inverter 78 to provide an additional output $\bar{E}$. The first stage of decade counter 76 is a divide-by-2 counter.

Player counter 54 is made up of the second, third, and fourth stages of the decade 76, which are connected as a divide-by-8 counter. The input to the divide-by-8 counter is connected to the output E of the first stage of the counter. The outputs from the three

stages of the divide-by-8 counter are labelled respectively and FIG. 1 as signals F, G, and H.

FIG. 6 illustrates in more detail the player selector and strobe unit 80. Unit 80 uses five integrated circuits 82, 84, 86, 88, and 90, which are 2-line to 4-line decoder/demultiplexers of the type sold by Texas Instrument under the circuit number SN4155. This integrated circuit is more fully illustrated in FIG. 7. Signals received at terminal 1 of this circuit are demultiplexed onto four lines beginning at terminals 4, 5, 6 and 7. The signals received on terminal 15 are demultiplexed on to four lines 9, 10, 11, and 12. Terminals 2 and 14 are used to strobe the respective circuits. Terminals 3 and 13 are used to select the inputs of the respective circuits. After player counter 54 has determined which of the five players the system is operating on, and ball counter 52 has determined which ball position the bowling scores are operating in, the ball position data $\bar{A}$, $\bar{B}$, and $\bar{C}$ is ANDed into data terminal 1 of demultiplexer 82, through AND gates 92 and 94. The signal T from the output of oscillator 50 is applied to strobe input 2 of demultiplexer 82 and the signal E is applied to the selection input terminal 3 of demultiplexer 82. The signal D and a strike/spare signal ST/SP are respectively applied to terminals 13 and 4 of demultiplexer 82. The strike/spare signal is developed in FIG. 34 as described below. A CLEAR P signal is derived from terminal 7 of circuit E2. This CLEAR P signal is used to clear the player accumulator 298 of FIG. 27. The output signals from terminals 9, 10, 11 and 12 of circuit 82 are used to strobe the inputs 2 and 14 of circuits 84, 86, 88 and 90. Signals F, G, and H are applied to the other input terminals of circuit 84, 86, 88, and 90 to be demultiplexed as signals F1 through F20. Inverters 92, 94, 96, 98, and 100 respectively invert signals F16 through F20 to provide respective output signals $\bar{F16}$ through $\bar{F20}$.

In the circuit of FIG. 8, the CLEAR P signal is applied to an inverter 102 and the F1 signal is applied to an inverter 104 to provide the input to a NAND circuit 106, the output of which provides the CLEAR T signal.

FIGS. 9 and 10 illustrate more fully the ball-selector decoder and strobe unit 108. FIG. 9 is a schematic illustration of a decoder section 110 designed for use in the decoder in FIG. 10. Decoder section 110 includes three 2-line to 4-line decoder/demultiplexers of the type sold by Texas Instrument as circuit number SN4156 and as more fully illustrated in FIG. 7. These integrated circuits are numbered as circuits 112, 114, and 116, and are respectively strobed by input signals at input terminals 1, 2, and 3 of the decoder section. The signals A, B and C are provided, as illustrated, at the other input terminals 1, 13, 3 and 15 of the demultiplexers 112, 114, and 116. The outputs of the demultiplexers are shown as outputs X0 through X20 of the decoder section. The X in the indication of output signals is representative of letters A through E which actually occur from the decoder sections as illustrated in FIG. 10. The output X20 is wire-ANDed with an additional output signal on line 118 from one of the output terminals of another demultiplexer 120 illustrated in FIG. 10.

In FIG. 10, the demultiplexer 120, constructed of an integrated circuit multiplexer, Texas Instrument circuit type SN74156, receives a NAND logic result signal

NLR from element 380 in FIG. 34 as a strobe signal. It also receives input signals F, G, and H. Five decoder sections of the type illustrated in FIG. 9 are combined into a decoder, controlled by the signals A, B and C illustrated in FIG. 9 and the strobe signals F1 through F15 derived from the circuits 84, 86, and 88 in FIG. 6. The five decoder sections 122, 124, 126, 128, and 130 respectively provide signals A0 through A19, B0 through B19, C0 through C19, D0 through D19, and E0 through E19 on twenty lines from each decoder section corresponding to those twenty lines in FIG. 9 carrying signals X0 through X19. Additionally the respective decoder sections provide output signals A20, B20, C20, D20, and E20 corresponding to signal X20 in FIG. 9. This signal includes an output value from the demultiplexer corresponding to 116 in FIG. 9 and the output from the corresponding one of output terminals 9, 10, 11, 12, and 7 of element 120, which are wire-ANDed to provide the resulting output signals. The outputs of ball selector decoder and strobe unit 108, as illustrated in FIG. 10, are applied to the wipers 132 of 11- or 12-position decimal switches (illustrated only in FIG. 1) where the value of a ball is manually stored mechanically. A total of 21 such ball switches is used for each of the five players, making 105 such switches used totally. The open-collector outputs of the ball-selector decoder and strobe 108 are connected directly to these wipers. Using the ENABLEing action of the strobe 108 on the ball switch wipers 132, output can be taken from wire-AND decimal ball switch outputs 134. Switch outputs 134 are more fully illustrated in FIG. 11.

In FIG. 11 are illustrated five sets 132, 134, 136, 138 and 140 of ball switch outputs, one set for each player. Each set includes ten parallel-wired lines. Only set 132 is completely illustrated, but the remaining sets are of identical construction. Set 132 illustrates ten parallel-wired lines PA1 through PA10, which have their inputs connected to the ball-switch decimal outputs. Each of these lines is fed through an open-collector buffer-gate such as buffer-gate 142. The respective 1 outputs from each set of switch outputs are tied together on a common line; thus PA1, PB1, PC1, PD1, and PE1 are all tied to a common line. Likewise all outputs numbered 2 are connected together and so on through the 10 outputs. This is the principle of wire-ANDing the outputs. This technique keeps the circuit elements to a minimum for strobing of the switches. The wire-ANDed outputs are connected to the inputs of the decimal-to-binary coder 144. This coder comprises NAND gates 146, 148, 150 and 152 for receiving the appropriate inputs, as illustrated, from the wire ANDed outputs and for providing, respectively, outputs 1Z1, 1Z2, 1Z4, 1Z8. This output is a 4-bit binary (binary 0 through binary 10). Its use permits more efficient data handling and storage. The output of block 144 always represents the value on the ball switch chosen by ball-selector strobe 108.

FIG. 12 is a more detailed diagram of temporary memory 154. It is constructed using two 8-bit parallel-access shift registers of the type sold by Texas Instrument as integrated circuit number SN74199. This integrated circuit is more fully illustrated in FIG. 13. This memory stores the binary equivalent of the four immediately preceding ball-switch outputs which were

strobed by ball-selector decoder and strobe unit 108. This strobing occurs sequentially beginning at the first ball at player A, then proceeding to the second ball of player A, the third ball of player A, etc. The strobing proceeds in like manner through player B, player C, player D, and player E. This temporary memory 154 permits two complete frames (four balls) to be stored while a fifth ball (the first ball of a third frame) is examined for its value. In scoring a bowling game, it may be necessary to examine this number of balls (two complete frames plus the first ball of a third frame) in order to derive certain strike-spare information. In the storage system of element 154, there are two 8-bit parallel-access shift registers 156 and 158 used. In each register, the output of the first three of a group of four flip-flops is fed back to the input of the next succeeding flip-flop in the series to allow the data to be shifted through four bit positions. Thus the data which appears at the position 1Z1 is successively shifted to appear at output positions 2Y1, 1Y1, 2X1 and 1X1. The same situation exists with respect to the other three inputs of the system— 1Z2, 1Z4, and 1Z8. Shifting is under the control of the CLOCK M signal.

FIG. 14 illustrates a small section of logic circuitry which does not appear as such in FIG. 1 but which provides certain feedback information for use with ball switches 19 and 20 to define whether or not the switches represent a strike or a spare. The last two balls in the tenth frame of a bowling match can be either a strike or a spare. The switches can only tell that the frame is a 10. This additional logic circuitry is necessary to determine whether or not the 10 includes a strike or a spare. In FIG. 14, a NAND circuit 160 receives input signals 1Y2 and 1Y8 to generate an output signal 1Y2·1Y8. This signal is also applied to an inverter 162 to generate a signal 1Y2·1Y8. A NAND gate 164 receives input signals 2Y2 and 2Y8 to derive an output signal 2Y2·2Y8. This signal is also applied to an inverter 166 to derive an output signal 2Y2·2Y8. A NAND gate 168 receives input signals 1X2 and 1X8 and derives an output signal 1X2·1X8. This signal is also applied to an inverter 170 to derive an output signal 1X2·1X8. A NAND circuit 172 receives input signals 2X2 and 2X8 to generate an output signal 2X2·2X8. This signal is also applied to an inverter 174 to generate an output signal 2X2·2X8. A NAND gate 176 receives the outputs from inverters 166 and 170 to generate an output signal which is applied as one input to a NAND gate 178. The other input to gate 178 is taken from the non-inverted output of gate 172. The output of NAND gate 178 has the Boolean function $2X2 \cdot 2X8 \cdot 1X2 \cdot 1X8 \cdot 2Y2 \cdot 2Y8$.

FIG. 15 illustrates in more detail the control binary adder for bonus points 180. This circuit includes integrated circuits 182 and 184, which are dual 4-line to 1-line data selector /multiplexers of the type sold by Texas Instrument as integrated circuit number SN 74153, more fully illustrated in FIG. 16. Circuit 180 also includes a 4-bit binary full adder 186 of the type sold by Texas Instrument as integrated circuit number SN 7483, which has its inputs and outputs more fully illustrated in FIG. 17. The circuit also includes four AND gates 188, 190, 192, and 194. The control-and-binary adder for bonus points 180 provides information concerning points for strikes or spares earned in the

present frame to be carried forward to later frames. These extra numbers are stored in the four 1Y and the four 2Y positions of the output of temporary memory 154. The two multiplexers 182 and 184 receive their input signals from circuit 154 in FIG. 12 and from the circuit of FIG. 14. The four AND gates 188, 190, 192, and 194 receive their inputs from the same sources. The outputs from these four AND gates and two multiplexers are applied to respective inputs of the 4-bit binary full adder 186 to derive binary bonus point signals at the output, called BP1, BP2, BP4, BP8, BP16. The numerical values of these signals are related in order of increasing powers of two. The following conditions may occur to affect the output values assumed by circuit 180.

- A. If the present frame is not a strike and is not a spare, then the output has a value of 0, which is indicated by the five BP output signals which assume a value of 0.
- B. If the present frame is a strike and the first next frame 1Y is a strike, then the output assumes a numerical value equal to the sum of the first ball of the first next frame (1Y=10) plus the numerical value of the first ball of the second next frame 1Z. The total value represented by the five output lines from unit 180 will fall in the range of 10 to 20 points.
- C. If the present frame is a strike and the first next frame is not a spare, then the output assumes a value equal to the sum of the points scored by the first ball 1Y and the second ball 2Y of the first next frame. In this case, the sum of the values represented by the five output lines will fall in the range of 0 to 9 points.
- D. If the present frame is a strike and the first next frame is a spare, then the output equals 10, representing the sum of 0 plus the second ball 2Y of the first next frame.
- E. If the present frame is a spare, then the output equals the value of the first ball of the first next frame, which is equivalent to the sum of the first ball of the first next frame plus zero. Thus the output sum will fall in the range of 0 to 10 points.

FIG. 18 more fully illustrates the control binary adder for present-frame points 196. This binary adder includes a four-bit binary full adder 198, Texas Instrument integrated circuit type SN 7483, of the type illustrated in FIG. 17, and four AND gates 200, 202, 204, and 206. The input for one four-bit binary number is derived directly from the 2X outputs of circuit 156 in FIG. 12, and the other four-bit binary number is derived from the outputs of the AND gates. The AND gates respectively receive the 1X outputs from the circuit 158 of FIG. 12 at one of their input terminals, and each AND gate receives, at its other input terminal, the signal 2X2-2X8 from inverter 174 in FIG. 14. The 4-bit binary full adder provides a four binary-bit output signal comprising signal bits FP1, FP2, FP3, and FP4, representing present frame points.

The outputs from circuit 180 in FIG. 15 and circuit 196 in FIG. 18 are applied to the input terminals of a binary adder 208, which is more fully illustrated in FIG. 19. The four-bit signal FP1 through FP8 and the 4-bit signal BP1 through BP8 are applied to the inputs of a 4-bit binary full adder, Texas Instrument integrated cir-

cuit type SN 7483, more fully illustrated in FIG. 19 as circuit 210. The 4-bit binary output from circuit 210, from its terminals 15, 2, 6, and 9 provide four bits of the output from circuit 208. The CARRY signal from this circuit 210 is inverted in an inverter 212 and applied to one input of NAND gate 214. The BP16 signal from the CARRY output of circuit 186 in FIG. 15 is applied to a second inverter 216 to provide a second input to the NAND gate 214. The output from NAND gate 214 supplies the fifth bit of the output signal from binary adder 208. The resulting five bit binary signal from adder 208 is applied to the binary-to-binary-coded-decimal (BCD) converter 218. Converter 218 is constructed using binary-to-BCD converter, integrated circuit type SN74185, which has its input and output signal values more fully illustrated in FIG. 20. The integrated binary-to-BCD converter integrated circuit is numbered 220 and provides outputs which are generally biased by resistor network 222. These outputs are binary-coded-decimal values BC1, BC2, BC4, BC8, BC10, and BC20.

FIG. 21 illustrates, in more detail, the input system 224 for the handicap switch wipers (which are not individually illustrated). Unit 224 comprises ten buffer amplifiers 226, 228, 230, 232, 234, 238, 240, 242, and 244 which receive the F1, F2, F3, F4, and F5 signals from circuit 84 in FIG. 6 as input signals in the manner illustrated. The outputs from these buffer amplifiers go to the wipers of the switches for setting the handicaps of players A-E. Each player has a units handicap switch and a tens handicap switch, thereby allowing a handicap to be set as high as 99 points.

FIG. 22 illustrates in greater detail the wire-ANDed decimal handicap switch outputs 246 and the decimal-to-binary-coded-decimal encoder 248. The resistor network in circuit 246 receives, as input signals, HB1 through HB9 and HB10 through HB90. These signals represent the wire-ANDed outputs of the handicap switches of the various players. The signals are biased by the resistor networks illustrated and are then applied to the decimal-to-binary-coded-decimal encoder 248. In the encoder, the HB signals are applied in the manner illustrated to eight NAND gates 250 through 257 to provide binary-coded-decimal outputs BE1 through BE8 and BE10 through BE80. These binary-coded outputs represent respectively the units and tens position in a binary-coded-decimal form of the handicap points for the player under consideration.

FIG. 23 illustrates in greater detail the multiplexer arrangement 260. The multiplexer is constructed of four integrated circuits 262, 264, 266, and 268. These integrated circuits are dual 4-line to 1-line data-selector/multiplexers, circuit type SN 74153, more fully illustrated in FIG. 16. The circuit 260 receives the two 4-bit binary-coded-decimal numbers from each of the two circuits 218 and 248. The BC signals come from circuit 218 in FIG. 19 and the BE signals come from circuits 248 in FIG. 22. The circuits are strobed by the H STROBE signal from the handicap strobe unit 270 of FIG. 24. The outputs from this system represent multiplexed binary-coded-decimal information, including both actual and handicap points. The outputs are MB1 through MB8 and MB10 through MB80.

FIG. 24 illustrates in greater detail the handicap strobe unit 270 and the handicap switch 272. The han-

dicap strobe unit comprises NAND gates 274, 276, 278, 280, and 282 and an inverter 284. NAND gates 274, 276, 278, and 280 receive inputs B, C, D, E, $\bar{C}$, $\bar{D}$, and $\bar{E}$, from circuit 62 in FIG. 2 and its associated inverters. NAND gate 280 also receives an ENABLEing signal from handicap switch 272, which activates the strobe when switched to cause a preset handicap score to be added to each player's score and to the team score. The strobe unit 270 switches multiplexer 260 at the proper time to pass information from the handicap switches via units 246 and 248 through the multiplexer.

FIG. 25 is a more detailed diagram of the player binary-coded-decimal adder 286. Circuit 286 includes a 2-bit binary full adder 288 of the type illustrated in FIG. 26 and sold by Texas Instrument as circuit number SN 7482, and four 4-bit binary full adders 290, 292, 294, and 296, of the type illustrated in FIG. 17 and sold by Texas Instrument under the integrated circuit number SN 7483. Circuit 286 also includes logic circuitry to be discussed herein. The inputs to circuit 286 are the multiplexed binary-coded-decimal signals MB1 through MB8 and MB10 through MB80 from circuit 260 in FIG. 23 and PACC feed-back signals from the output of player total accumulator register 298, which will be discussed in connection with a later figure. The CARRY output signal from circuit 292 is connected to the CARRY input terminal of circuit 290, and the CARRY output signal from circuit 290 is connected to the CARRY input terminal of circuit 288, thereby allowing the binary adders to operate in their appropriate modes, including a CARRY-forward signal to the next higher decimal value.

FIG. 27 illustrates more fully the player total accumulator register 298. This circuit is constructed of two flip-flops 300 and 302, of the type sold by Texas Instrument as integrated circuit number SN 7474, and a shift register 304 of the type sold by Texas Instrument as integrated circuit number SN 74199 and more fully illustrated in FIG. 13. This circuit has the effect, when used in conjunction with adder 286, of adding an entire frame at a time (0 to 30 points) to the previously accumulated score. The player BCD adder 286 and the player-total accumulator register 298 are used to total the score for each of the five players sequentially. At the beginning of determining the score for a player, the player-total accumulator register is cleared to zero, and then the accumulation sequence occurs through all twenty-one ball positions of the player. The contents of the player-total accumulator register are then strobed into the appropriate player output-storage register, to be discussed in more detail below, at the end of the accumulation for that player.

FIG. 28 illustrates in more detail the team BCD adder 306. The team BCD adder adds the PACC signals fed back from the output of team-total accumulator register 308 to the output signals MB received from the multiplexer 260. The team BCD adder is constructed of six four-bit binary full adders 310, 312, 314, 316, 318, and 320, available from Texas Instrument as integrated circuit number SN 7483. The circuit also uses various interconnecting logic circuitry. The output from circuit 306 is in the form of three four-bit binary-coded-decimal numbers TC1 through TC8, TC10 through TC80, and TC100 through TC800, plus a TC CARRY output signal.

FIG. 29 discloses in more detail the team-total accumulator register 308. Circuit 308 comprises two integrated-circuit shift registers 350 and 352, of the type sold by Texas Instrument as integrated circuit number SN 74199, plus two inverters 354 and 356 and a NAND gate 358. The TC signals from the output of circuit 306 in FIG. 28 are connected to the inputs of shift register 350, shift register 352, and inverter 354, as illustrated. Team total accumulator register 308, in connection with team BCD adder 306, operates to store the total score of the entire team. It operates by adding an entire frame at a time (0 through 30 points) to the previously accumulated score. The team accumulator register is cleared to zero only at the beginning of player A accumulation time. Afterwards, it adds the scores of all five players together, a frame at a time, to get a team-total score. Its contents are strobed to its output point only when the scores of all five players have been summed and stored in the accumulator.

FIG. 30 illustrates in more detail the team storage and register unit 360, the decoder-and-driver unit 362 for the information from the team storage and register unit, and the seven-segment display unit 364 for displaying the team total score. The team storage and register unit 360 includes two bit-segments of a 4-bit latch unit 366, a complete 4-bit latch unit 368, and an 8-bit latch unit 370. The 4-bit bistable latch units are of the type sold by Texas Instrument as circuit number SN7475, and are more fully illustrated in FIG. 31. The 8-bit bistable latch units are of the type sold by Texas Instrument under the circuit number SN74100 and are more fully illustrated in FIG. 32. All of the latch units are clocked by signal $\bar{F}20$ and receive the binary-coded-decimal TACC signals from team-total accumulator register 308 during the time when circuit 308 is supplying the appropriate signals, and then hold them for constant display by the display units which follow. Decoder-and-driver unit 362 includes one binary-coded-decimal to seven-segment decoder/driver unit for each numeral to be displayed. There are four such decoder/drivers in the team-total decoder-and-driver unit, since, theoretically, the team total for five players could rise to 1500 points, requiring a display in the thousands position. The decoder/drivers receive the constantly available output signal from the respective latch position in storage-and-register unit 360, and develop from this a decoded signal of the sort suitable for driving the conventional seven-segment numerical displays in the numerical output unit 364. The decoder/drivers are of the type sold by Texas Instrument as integrated circuit number SN7446.

FIG. 33, comprising FIGS. 33a and 33b, illustrates in more detail the output system for the scores of the various individual players. Player storage units 370a through 370e correspond in function to the team storage and register unit 360 of FIG. 30. Since there is less information to store because the individual player's score can never rise above 300, the latch units used in the various storage units 370 require only sufficient room to store 10 bits of binary-coded-decimal information, and therefore need not be so large as those shown for the team score. Storage unit 370e is the only unit illustrated, but the remaining units 370 are of equivalent construction. The construction of unit 370e is equivalent in structure and in function to that of unit

360 in FIG. 30. Decoder-and-driver units 372a through 372e are provided to decode the binary-coded-decimal output from the various unit 370 and to provide outputs to the players score display units 374a through 374e, each of which consists of set of three seven-segment numerical display units of the same type used in connection with unit 364 in FIG. 30.

FIG. 34 illustrates a section of logic circuitry designed to be used during those periods of time when ball switches 19 and 20 are being strobed. This logic circuit defines information to determine whether or not the switches represent a strike or a spare during the 10th frame of bowling. The last two balls in the 10th frame can be either a strike or a spare. The input switches can only tell the computer that the number is a 10. This logic circuit then provides the information to show whether it is a strike or spare. NAND circuits 160 and 176 have already been described in connection with FIG. 14. NAND circuit 380 receives as input signals the signals $\bar{A}$, $\bar{B}$, $\bar{C}$, $\bar{D}$, and $\bar{E}$ from unit 52 in FIG. 2 and a signal from the output of NAND gate 160. NAND gate 380 provides as an output signal the NLR or NAND logic result signal at its output for application to the input of unit 120 in FIG. 10, and for application to one input of a NAND gate 382. An AND gate 384 receives input signals A and E from unit 52 in FIG. 2 and generates an output signal for application to one input terminal each of NAND gate 386 and 388. The 2X2:2X8 input signal to NAND gate 176 is also applied to one input of NAND gate 390 together with the output signal from NAND gate 176 to derive an output signal from NAND gate 390 for application to a second input terminal of NAND gate 386. The other input signals to NAND gate 176, 2Y2:2Y8, is applied to a second input of NAND gate 388. Signals $\bar{B}$ and $\bar{C}$ are also applied to inputs of NAND gate 386. Signals B and $\bar{C}$ are applied to inputs of NAND gate 388. The output signals from NAND gate 386 and NAND gate 388 are also applied to input terminals of NAND gate 382 to generate an output signal therefrom called ST/SP, representing the strike-spare information to be fed back to terminal 14 of integrated circuit 82 in FIG. 6.

FIG. 35 is a perspective drawing of the console unit for the scorer. Thumb-wheel switches 400 are used to set the number of pinfalls for each ball. The thumb-wheel switches are arranged in rows for each of five bowlers, and are divided into frames. Nine frames for each bowler contain two balls each and the tenth and final frame contains three balls to allow for the possibility of several successive strikes. Thumb-wheel switch sets 224a through 224e are the handicap switches, and are used to preset the handicap scorers for each of the five players. Switch 272 is the handicap/scratch mode switch, and is used to determine whether the scorer shall operate in the handicap mode or the scratch mode. The seven-segment displays are located preferably behind a translucent panel, in position 402. This provides an output display of the scores of each of the individual players and of the team as a whole.

In the preferred embodiment of the invention, two computers of the type illustrated are used in the same console. Thus, two teams in two adjacent lanes can play against each other and have their respective scores kept on the same scorer.

It is understood that a lever switch, which is the electrical equivalent of the thumbwheel switch, may be substituted for the thumbwheel switch in this invention. Both thumbwheel switch and lever switch have rotatable indicator wheels.

We claim:

1. A system for automatically calculating and displaying the score accumulated by each of a plurality of players during the progress of a bowling game which consists of a number of frames, each frame including pinfalls resulting from the rolling of at least one ball by a player, comprising:
 - A. a plurality of independent ball switch means associated with each player for independently manually entering the number of pinfalls for each of the balls either actually used or bypassed because of strikes,
 - B. reading means for periodically and sequentially reading each ball switch means for each player,
 - C. present-frame point determining means responsive to said reading means for periodically and sequentially determining for each player from the number of actual pinfalls, the number of points scored in each frame,
 - D. bonus point determining means responsive to said reading means for periodically and sequentially determining for each player the number of bonus points scored in each frame because of strikes and spares,
 - E. adding means responsive to the number of points determined by the present-frame point determining means and by the bonus point determining means for periodically and sequentially adding the present frame points plus bonus points scored in each frame by a given player to the total such points scored previously in a given game by the given player to derive a new total of points scored to the end of a given frame, and
 - F. means for displaying said new total of points for each player where the given frame is the last frame completed.
2. A system according to claim 1 further comprising:
 - A. a handicap switch means associated with each player for entering a selected number of handicap points to be added to the score of that player, and
 - B. handicap mode switch for selectively ENABLEing the system to operate in the handicap mode in which the handicap points are added to the score or in a scratch mode in which the handicap points are not added to the score.
3. A system according to claim 2 wherein said adding means further comprising:
 - A. a first adder device for adding said present frame points to said bonus points scored in each frame by a given player to derive the player-scored frame points,
 - B. successive addition means including an accumulator for successively adding applied signals to the contents of the accumulator, to provide a totalized output signal, and
 - C. multiplexer means for sequentially applying the player-scored frame points and the handicap points of the scoring player to the successive addition means to cause the successive addition means to provide a player point total as said totalized output signal.

4. A system according to claim 3 further comprising:
 - A. a second successive addition means including a second accumulator for successively adding applied signals to the contents of the second accumulator to provide a second totalized output signal, and
 - B. means for causing the multiplexer to apply the player-scored frame points and the handicap points of each player in turn to the second successive addition means to cause the second successive addition means to provide a team point total as said second totalized output signal.
5. In a system for calculating and displaying the score accumulated by each of a plurality of players during the process of a bowling game, during which game there are varying numbers of pinfalls resulting from each of a plurality of balls rolled by each of a plurality of players, the improvement comprising:
 - A. a plurality of input storage means associated respectively with each allowable rolling of a ball by each of the players for entering the number of pinfalls resulting from the associated ball rolling in the corresponding storage means,
 - B. computation means for sequentially reading out the number entered in each storage means and calculating therefrom the resulting total score of each player to the present frame of the game and for periodically re-reading the number and recalculating said total score at regular time intervals, and
 - C. display means for displaying said total score.
6. A system as disclosed in claim 5 wherein the plurality of input storage means is a plurality of manually operated switches.
7. A system for automatically calculating and displaying the score accumulated by each of five players on a team during the progress of a bowling game which consists of ten frames, each frame including the possibility of 0 to 10 pinfalls resulting from the rolling of at least one ball by a player, comprising:
 - A. twenty-one independent rotatable indicator-wheel switches associated with each player for manually entering the number of pinfalls for each of the balls actually used or bypassed because of strikes, each switch having a plurality of separate switch positions corresponding to a number of pinfalls from zero to ten,
 - B. an oscillator clock,
 - C. a ball counter driven as a frequency divider by an output signal from said oscillator clock for successively counting through the possible balls rolled by each player to generate a ball selection control signal and a player counter drive signal,
 - D. a player counter for successively counting through the five players at the completion of a count by said ball counter of 21 balls associated with an individual player for generating a player selection control signal,
 - E. a player selector and strobe unit responsive to said player selection control signal for generating a player strobe output signal,
 - F. a ball selector decoder and strobe unit responsive to said player strobe output signal and to said ball selection control signal for generating a ball selection strobe signal for application to said rotatable indicator-wheel switches for selecting, one at a time, the rotatable indicator-wheel switch to be read out,

- G. wire-AND output means for combining the outputs of the various rotatable indicator-wheel switches into a single ANDed decimal ball switch output signal,
- H. a decimal-to-binary encoder responsive to said ANDed decimal ball switch output signal for providing a binary encoded output signal,
- I. a temporary memory responsive to said binary encoded output signal for storing the value of ten balls in the last two complete frames read from said rotatable indicator-wheel switches to provide bonus point control output signals and present-frame point indicating signals,
- J. a control binary adder for present frame points responsive to said present-frame-point indicating signals for producing, by binary addition, added present-frame point signals,
- K. a control binary adder for bonus-point signals responsive to said bonus point control output signals and to said binary encoded output signal for producing, by binary addition, added bonus point signals,
- L. a third binary adder responsive to said added present-frame point signals and to said added bonus point signals for producing, by binary addition, frame total-points signals,
- M. a binary-to-binary-coded-decimal converter for receiving said frame total-points signals in binary form and for producing BCD total-points signals,
- N. a set of handicap rotatable indicator-wheel switches associated with each of said players for adding a predetermined point value to each of their scores, said handicap rotatable indicator-wheel switches being strobed by said player strobe output signal to produce a handicap switch output signal,
- O. wire-AND handicap output means for producing an ANDed handicap output signal corresponding to the player whose score is then being calculated,
- P. a decimal-to-binary encoder responsive to said ANDed handicap output signal for producing binary handicap signals,
- Q. a switchable handicap strobe unit responsive to said ball selection control signal for one of the possible balls for producing a handicap strobe signal,
- R. a multiplexer responsive to said BCD total points signals and, under the influence of said handicap strobe signal, to said binary handicap signals for providing both the binary handicap signals and the BCD total-points signals as multiplexer output signals in a time-division multiplex fashion,
- S. a team-total accumulator register for providing a team-total signal, in response to a team-total accumulator register input signal,
- T. a team BCD adder responsive to said multiplexer output signals and to said team-total signal for periodically and sequentially generating new-team total accumulator register input signals, U. means for storing and displaying the team-total signal,
- V. a player-total accumulator register for periodically and sequentially generating a player-total signal corresponding to each of the players in response to a player-total accumulator register input signal,

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W. a player BCD adder responsive to said multiplexer output signals and to said player-total signal for periodically and sequentially generating a new player-total accumulator register input signal, and
X. means for storing and displaying each player-total

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signal.

8. A system as claimed in claim 7 wherein said rotatable indicator-wheel switches are thumb-wheel switches.

9. A system as claimed in claim 7 wherein said rotatable indicator-wheel switches are lever switches.

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