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Method and apparatus for calibration of digital down converters in a signal processing system

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(56) Related Art
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US 5982819
US 5493581

ABSTRACT OF THE DISCLOSURE

A calibration technique for digital down converters in a signal processing system, wherein a digital down converter is selected by a system controller for calibration. The digital down converter's settings are copied into a calibration digital down converter which mimics the operation of the selected digital down converter. A best polarization diversity detector signal path, an optimal phase offset value for an in-phase data signal, an optimal phase offset value for a quadrature phase data signal, and a normalized gain value for the in-phase and quadrature phase signals of the selected digital down converter are determined. The system controller updates the selected digital down converter with the determined optimal settings. This procedure is repeated for each digital down converter in the signal processing system, while the signal processing occurs simultaneously.

AUSTRALIA

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LITTON SYSTEMS, INC.

ORIGINAL

COMPLETE SPECIFICATION
STANDARD PATENT

Invention Title:

Method and apparatus for ~~*calibraton*~~ calibration *of digital down converters in a signal processing system*

The following statement is a full description of this invention including the best method of performing it known to us:-

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to the field of signal processing, and more specifically to a method and apparatus for calibration of digital down converters in a signal processing system.

2. Description of Related Art

Acoustic listening systems for underwater applications are well known in the art. For example, modern military submarines are equipped with arrays of acoustic sensors which provide sensitive underwater listening capabilities and even relative position information. Each sensor reacts to an incoming pressure wave by modulating an input signal and the outputs of all the sensors are processed to determine the sound and position information. These sensor arrays are generally either attached to the submarine hull or are towed behind the submarine. Ideally, the sensors would be attached to the submarine hull, but prior art acoustic sensors were simply too heavy for many submarine applications. Recent advances in acoustic sensor array technology, however, have produced arrays which are light enough to be mounted on a submarine hull and which still provide very sensitive signal response. This weight reduction has also allowed the number of sensors to be increased.

Another application for underwater acoustic sensors is in the

geological survey industry, specifically, for underwater oil exploration. Vast arrays of sensors may be placed on the ocean bottom in the vicinity of known oil reserves. A surface ship then initiates an acoustic pressure wave (i.e. a large air burst). The acoustic pressure wave and its reflection off the ocean floor are detected by the sensor arrays. The data from the sensors is then processed and analyzed to determine optimum drilling locations or to monitor the status of known reservoirs.

As the number and complexity of the acoustic sensors in these and related applications have increased, the associated signal processing electronics have likewise increased. Prior art systems use analog circuitry to interrogate the sensors, but these analog systems are subject to drift and are very difficult to accurately calibrate. Also, recent developments have provided fiber optic interferometric sensors which provide unique signal processing problems (see "Homodyne Demodulation Scheme for Fiber Optic Sensors Using Phase Generated Carrier" by Anthony Dandridge, Alan B. Tveten, and Thomas G. Giallorenzi, IEEE Journal of Quantum Electronics, Vol. QE-18, No. 10, October 1982, herein incorporated by reference). Note that this reference teaches a modulation/demodulation technique in which the I and Q frequencies are different. This technique is employed in the present invention.

Thus, there is a need for a signal processing system which overcomes the shortcomings of the analog systems and can be used with fiber optic interferometic sensor arrays. Specifically, there is a need for an improved calibration system for use with a digital demodulation system.

OBJECTS AND SUMMARY OF THE INVENTION

It is thus an object of the present invention to provide an apparatus and method for calibration of digital down converters in a signal processing system.

This and other objects of the present invention may be met by a calibration technique for digital down converters in a signal processing system, wherein a digital down converter is selected by a system controller for calibration. The digital down converter's settings are copied into a calibration digital down converter which mimics the operation of the selected digital down converter. A best polarization diversity detector signal path, an optimal phase offset value for an in-

phase data signal, an optimal phase offset value for a quadrature phase data signal, and a normalized gain value for the in-phase and quadrature phase signals of the selected digital down converter are determined. The system controller updates the selected digital down converter with the determined optimal settings. This procedure is repeated for each digital down converter in the signal processing system, while the signal processing occurs simultaneously. The process of selecting the best polarization diversity detector signal path further comprises the steps of selecting a first signal path, obtaining in-phase or quadrature phase data samples, determining a maximum in-phase or quadrature phase peak-to-peak value, saving the determined maximum in-phase or quadrature phase peak-to-peak value, repeating the above steps for each signal path, comparing the saved maximum in-phase or quadrature phase peak-to-peak values, and selecting a signal path with a largest peak-to-peak value as the best polarization diversity detector signal path.

The process of determining an optimal in-phase offset value comprises the steps of writing a phase offset to the calibration digital down converter, obtaining in-phase and quadrature phase data samples, calculating a peak-to-peak value when the quadrature signal is near zero, comparing the calculated peak-to-peak value with a previously determined peak-to-peak value, saving whichever peak-to-peak value is larger, and repeating the above steps for each possible phase offset.

The process of normalizing a gain value for the in-phase and quadrature phase signals of the selected digital down converter comprises the steps of reading an in-phase and a quadrature phase gain setting, obtaining in-phase and quadrature phase data samples, comparing the in-phase and quadrature phase data samples, calculating a new in-phase gain, when the in-phase data is larger than the quadrature phase peak-to-peak value, by multiplying the in-phase gain setting by the quotient [Q/I], and calculating a new quadrature phase gain, when the quadrature phase peak-to-peak value is larger than the in-phase peak-to-peak value, by multiplying the quadrature phase gain setting by the quotient [I/Q].

BRIEF DESCRIPTION OF THE DRAWINGS

The exact nature of this invention, as well as its objects and advantages, will become readily apparent from consideration of the following specification as illustrated in the accompanying drawings, in which like reference numerals designate like parts throughout the figures thereof, and wherein:

Figure 1(A) is a high-level block diagram of a submarine system incorporating the present invention;

Figure 1(B) is a block diagram illustrating a preferred configuration for the laser modules driving the sensor arrays;

Figure 2 is a hardware block diagram of the present invention;

Figure 3 is a flowchart illustrating the operation of the system controller of the present invention;

Figure 4 is flowchart illustrating the phase shift algorithm for the in-phase signal (I data);

Figure 5 is a flowchart illustrating the phase shift algorithm for the quadrature phase signal (Q data);

Figure 6 is a flowchart illustrating the functional flow of the polarization diversity detector (PDD) selection procedure; and

Figure 7 is a flowchart illustrating the I/Q balance algorithm.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The following description is provided to enable any person skilled in the art to make and use the invention and sets forth the best modes contemplated by the inventor for carrying out the invention. Various modifications, however, will remain readily apparent to those skilled in the art, since the basic principles of the present invention have been defined herein specifically to provide a method and apparatus for calibration of digital down converters in a signal processing system.

Figure 1(A) is a high-level block diagram of a submarine system 100 incorporating the present invention. An inboard receiver module 102 contains the requisite electronic control and processing circuitry and is located inside the

submarine. A light weight array of fiber optic interferometric sensors 104 is located on the hull (i.e operates in the water) of the submarine. Each sensor reacts to an incoming acoustic pressure wave by modulating a light signal 118 sent from the inboard receiver 102. Modulated signals from different sensors (each operating at a different carrier frequency) are passively multiplexed onto a single fiber optic cable and sent back to the receiver. The channel signals are then demultiplexed and demodulated by the receiver 102.

The inboard receiver 102 is connected to the submarine's power system via a power connection 106. The inboard receiver 102 has a power distribution and conditioning block 112 to provide the necessary power requirements for the receiver components. The input light signal 118 is generated by a laser module 116. The laser module includes a laser, a phase modulator, a laser driver card and a laser controller card. The laser used in the preferred embodiment is a Model 125 200 mW Nd:YAG laser available from Lightwave Electronics of Palo Alto, California.

As shown in Figure 1(B), the preferred embodiment uses eight lasers 117a - 117h which drive eight corresponding sensor arrays 104a - 104h. Each laser powers 56 sensors (channels), 28 channels on each side of the submarine. Each laser is modulated by a phase modulator 119a - 119h injecting a sine wave signal. Each phase modulator 119a - 119h injects a different frequency sine wave [1.5 MHz to 2.2 MHz in the preferred embodiment]. Each laser's wavelength is nominally at 1319 nanometers, but each laser operates at a different "color" around 1319 nanometers. The frequency synthesizer 142 controls the temperature of each laser separately, as is well known in the art, in order to produce eight different "colors." The first channels from each sensor array are multiplexed via a signal multiplexor 121. This a total of 56 fiber optic cables return from the sensor array 104, with each fiber carrying eight multiplexed signals. This multiplexed signal is then processed by a receiver card 122. Depending upon the number of sensors used, several receiver cards may be needed.

The frequency synthesizer 142 contains the master system clock and controls the operation of the laser module, specifically, such parameters as laser

color, power, temperature monitoring, etc. Timing information is provided to the receiver card via a signal line 144. A CPU 130 and associated memory 140 provide system level control and status information to the other receiver 102 components via data lines 132, 134, 138. The CPU 130 also controls a "gross" calibration procedure for the laser modules, a detailed description of which is beyond the scope of the present invention.

The receiver card 122 demultiplexes and demodulates the return signal 120 and outputs a signal to a common beamformer card 124 which provides additional signal processing. A fiber channel card 126 provides the signal information to an external fiber bus 110. In the preferred embodiment, each receiver card 122 processes the signals from 7 return fibers, or a total of 56 channels.

Figure 2 is a detailed block diagram of the receiver card 122 shown in Figure 1. The signal $\lambda(\phi(t))$ 120 (containing 8 channels) output by the acoustic sensor array is input to a polarization diversity detector (PDD) 200. An example of a PDD which has three outputs is described in U.S Patent No. 5,448,058, entitled "OPTICAL SIGNAL DETECTION APPARATUS AND METHOD FOR PREVENTING POLARIZATION SIGNAL FADING IN OPTICAL FIBER INTERFEROMETRIC SENSOR SYSTEMS." In the preferred embodiment, a bi-cell or two output PDD is used. The PDD 200 prevents polarization signal fading in the return signal 120. The PDD 200 converts the photonic energy of the return optical fiber signal 120 into two separate electrical currents 200a, 200b via two photodiodes (not shown). In each opto-receiver 202a, 202b, a transimpedance amplifier converts the input current to a voltage. A variable gain amplifier sets the voltage level to maximize the signal-to-noise level and to ensure that the voltage level is below the saturation level of the ADCs 204a, 204b. Anti-aliasing filters in the opto-receivers 202a, 202b filter the signal which then passes to the ADCs 204a, 204b. A digital-to-analog converter (DAC) 234 creates a gain value from a digital gain value output by the system controller 226 for each variable gain amplifier in each opto-receiver 202a, 202b.

The analog outputs of the opto-receivers 202a, 202b are then digitized by high speed (>25.6 MSPS), high resolution (>12-bit) analog-to-digital converters (ADCs) 204a, 204b. The ADC used in the preferred embodiment is part number 9042, manufactured by Analog Devices, Inc. The number of ADCs used is directly dependent upon the number of outputs from the PDD 200. Typically, there are two outputs, but three is possible. At this point, the digitized output contains a complex signal comprised of all channels of the frequency division multiplexed phase generated carriers with their information carrying sidebands on the return optical fiber signal 120.

Each ADC 204a, 204b output is buffered and passed through to a multi-throw, multi-pole bus switch 206 which taps into each ADC 204a, 204b signal path. One output of the bus switch 206 goes to a digital down converter (DDC) 228, via signal path 238, which is employed as part of a calibration channel, as described below. The outputs of the bus switch 206 go to the signal channel DDCs 208a, 208b, 208n. The purpose of the bus switch 206 is to allow each of the DDCs to be able to connect to any ADC output. This is required by the PDD selection algorithm, discussed below with reference to Figure 6.

Each DDC 208a, 208b, 208n acts as a digital demultiplexer by performing mix down and filtering of the digital information, separating one channel out of the composite signal. The DDC chip employed in the presently preferred embodiment is the GC4014 chip manufactured by Graychip, Inc. This particular device has 2 channel capability. In other embodiments, each chip may only have 1/2 channel capability. The number of DDCs needed depends upon the number of channels used in a given application. For example, if the input signal 120 has 8 multiplexed channels, then 4 DDC chips are needed. In the present embodiment, 28 DDCs (56 channels) are used per receiver card 122, but only one calibration DDC and system controller are required (as described below). Thus, seven channel groups are needed to process all 56 multiplexed signals (8 channels per multiplexed array output signal).

Each DDC 208a, 208b, 208n outputs both in-phase (I) and quadrature phase (Q) words that represent the rectangular components of the phase. These I and

Q components from the DDCs 208a, 208b, 208n are time division multiplexed (TDM) onto separate I and Q buses. The output signal paths 210, 212 (which are serial, unidirectional data paths in the preferred embodiment) output the I and Q 8-bit words to a buffer 214 which buffers the words and also converts the 8 bit words into 16 bit words.

The I and Q words are demodulated from all of the DDCs in a time sequence. The I and Q words are converted from Cartesian to polar form by the coordinate transformer 216. The coordinate transformer 216 of the preferred embodiment is a TMC2330A chip manufactured by Raytheon Corp., but may be any similar device. The output of the coordinate transformer 216 is the instantaneous phase angle, whose change is directly related to the change in acoustic pressure of the acoustic signal from the environment and whose rate of change is directly related to the frequency of the acoustic signal from the environment for a given fiber optic sensor. The channel-by-channel instantaneous phase angles are further processed in an acoustic signal processor 218 with integration and filtering algorithms. The output of the acoustic signal processor 218 may then be provided to a visual display or further signal processing blocks, as desired. Two DACs 222, 224 provide I and Q signals which can be used for testing or viewing the output signal. For example, the I and Q signals may be connected to the X and Y inputs of an oscilloscope in order to view a graphical representation of the I and Q signals.

The operation of the calibration procedure will now be described. The output 238 of the bus switch 206 feeds the calibration channel DDC 228. If there is more than one PDD 200, there will be more than one bus switch 206 feeding the calibration channel DDC 228 in a TDM manner. The calibration channel DDC 228 is set to mimic each signal channel in turn. The calibration channel provides a way to check PDD output selection, phase shift adjustment and I/Q balance on a per signal channel basis in a non-obtrusive way. The data is processed by the DDC 228 into I and Q words similar to the signal channel DDCs 208a, 208b, 208n. The I and Q words are processed by the system controller 226 to extract the information necessary to determine channel performance. The system

controller 226 of the preferred embodiment is a ADSP 2181 manufactured by Analog Devices, Inc.

The operation of the system controller 226 will now be described with reference to the flowchart of Figure 3. The following steps are performed by software which is stored in the system controller's ROM 232 or the code may be downloaded by the system CPU 130 to a RAM upon system initialization. Upon power initialization or a system re-initialization 300, all interrupts are disabled at step 302. The digital signal processing (DSP) is initialized, along with any associated RAM memory and the DDCs at step 304. The interrupts are then enabled at step 306. A signal channel and a calibration channel are selected at step 308. Then, the best PDD signal is selected at step 310. This PDD selection step is further described below with reference to Figure 6. A phase shift algorithm for the I component is performed at step 312, which is shown in detail in Figure 4. Similarly, a phase shift algorithm for the Q component is performed at step 314, as shown in Figure 5. An I/Q balance algorithm is executed at step 316, which is shown in detail in Figure 7. Steps 308 – 316 are repeated for each channel, until all the channels have been calibrated. In one embodiment, calibration is performed only at system start-up. In the preferred embodiment, however, the calibration procedure continues for each DDC for as long as the system is operating. This results in a dynamic calibration system which unobtrusively calibrates the system, while signal processing functions are unaffected.

The procedure for selecting the best PDD signal (step 310) is illustrated by the flowchart of Figure 6. At step 602, the first ADC 204a is selected, and I and Q data samples are obtained at step 604. A maximum $I_{peak\text{-}to\text{-}peak}$ value is calculated at step 606. The maximum $I_{peak\text{-}to\text{-}peak}$ value determined at step 606 is then stored at step 608. Then the second ADC 204b is selected at step 610. I and Q data samples are then obtained for the second ADC 204b at step 612. Again, a maximum $I_{peak\text{-}to\text{-}peak}$ value is calculated at step 614, and this value is stored at step 616. The two stored maximum $I_{peak\text{-}to\text{-}peak}$ values are then compared at step 618. The ADC which produces the larger $I_{peak\text{-}to\text{-}peak}$ value is then selected (steps 620, 622). Since selecting different ADCs will affect the I and Q signal levels symmetrically,

only one signal (I or Q) needs to be examined. Note that the PDD selection step is performed for each channel separately. Thus, different DDC may actually be using different ADC inputs, which is why each DDC needs to be connected to both ADCs.

The phase shift algorithm for the I component (step 312) and the Q component (step 314) are shown in Figures 4 and 5, respectively. The purpose of this algorithm is to determine the phase offsets that result in a maximum phase signal (I data) and quadrature phase signal (Q data) for each channel. This is accomplished by programming the calibration DDC's 228 channel control registers with different phase offsets having equal phase increments and reading the corresponding I and Q data from the channel output registers. The I and Q data generated by the calibration DDC 228 will be read by the system controller 226 and stored into two separate buffers. Once a sufficient number of data samples have accumulated, the phase shift algorithm will be performed on the I and Q data. The output of the phase shift algorithms will generate an I-phase offset and a Q-phase offset, which are the offsets that result in maximum amplitude I and Q signals. These optimal offset values will then be stored in the associated signal channel DDC.

At step 404 a phase increment is stored in the calibration DDC 228, and the I and Q data values are obtained. At step 406, a maximum peak-to-peak value for I is calculated. In the present embodiment 32 samples are used, but depending upon the application, either more or less samples may be used. If the I value calculated at step 406 is greater to or equal to a previous value, then a MAX $I(n)_{peak\text{-}to\text{-}peak}$ variable is set equal to the current I value, and the corresponding phase is also saved at step 410. Otherwise, at step 412, the MAX I(n) variable is set equal to the previous value of I, and the corresponding phase value is saved. This procedure is repeated at step 402 until all I phase increments have been tested. The resulting MAX I(n) value is then stored into the corresponding DDC chip associated with the current channel.

The procedure for determining the Q phase shift value is exactly the same as the procedure for determining the I phase shift value, as shown in Figure 5, and a detailed analysis of the flowchart will not be repeated.

Figure 7 is a flowchart illustrating the I/Q balance algorithm (step 316 of Figure 1). This procedure is necessary in order to normalize the maximum I and Q vectors in order to minimize the errors in angle calculations. At step 700, the current I and Q gain settings for the current signal channel are read and the I and Q data samples are obtained for the current channel. At step 704, the I and Q values are compared. If I is greater than Q, then a new I gain is calculated at step 706. The new I gain value is equal to the current I gain value multiplied by the quotient [Q/I]. If, however, I is not greater than Q, then a new Q gain value is calculated at step 708. The new Q gain value is equal to the current Q gain value multiplied by the quotient [I/Q]. The gain values are then re-written to the DDC of the current signal channel.

In the preferred embodiment, the control signal bus and the data bus for the DDCs are separate. The control signal path between the DDCs and the system controller is a separate bi-directional parallel bus. The data signals are output onto a separate serial bus. By using different buses to move data into and out of the DDCs, the background calibration operations are processed in parallel to the high speed signal data process flow. As a result, both high speed signal processing and background calibration processing can occur at the same time. In a second embodiment , both signal and control information share the same parallel bus, and, due to throughput limitations on the bus, the calibration routines are run only during startup or when there is a break in normal system operations.

Those skilled in the art will appreciate that various adaptations and modifications of the just-described preferred embodiments can be configured without departing from the scope and spirit of the invention. Therefore, it is to be understood that within the scope of the appended claims, the invention may be practiced other than as specifically described herein.

THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:-

1. A calibration method for digital down converters in a signal processing system, the calibration method comprising the steps of:

selecting a digital down converter to calibrate;

copying the selected digital down converter's settings into a calibration digital down converter;

selecting a best polarization diversity detector signal path for the selected digital down converter;

calculating an optimal phase offset value for an in-phase data signal of the selected digital down converter;

calculating an optimal phase offset value for a quadrature phase data signal of the selected digital down converter;

normalizing a gain value for the in-phase and quadrature phase signals of the selected digital down converter;

updating the selected digital down converter with a determined best signal path, optimal in-phase offset value, optimal quadrature phase offset value, and normalized gain value; and

repeating each above step for each digital down converter in the signal processing system while the signal processing occurs simultaneously.

2. The method of Claim 1, wherein the steps are performed only once for each digital down converter at a system start-up.

3. The method of Claim 1, wherein the steps are repeated for each digital down converter for as long as the signal processing system is operating.

4. The method of Claim 3, wherein the step of selecting the best polarization diversity detector signal path further comprises the steps of:

selecting a first signal path;

obtaining in-phase or quadrature phase data samples;

determining a maximum in-phase or quadrature phase peak-to-peak value;

saving the determined maximum in-phase or quadrature phase peak-to-peak value;

repeating the above steps for each signal path;

comparing the saved maximum in-phase or quadrature phase peak-to-peak values; and

selecting a signal path with a largest peak-to-peak value as the best polarization diversity detector signal path.

5. The method of Claim 4, wherein the step of determining an optimal in-phase offset value comprises the steps of:

writing a phase increment to the calibration digital down converter;

obtaining in-phase and quadrature phase data samples;

calculating a peak-to-peak value when the quadrature signal is near zero;

comparing the calculated peak-to-peak value with a previously determined peak-to-peak value;

saving whichever peak-to-peak value is larger; and

repeating the above steps for each possible phase increment.

6. The method of Claim 5, wherein the step of determining an optimal quadrature offset value comprises the steps of:

writing a phase increment to the calibration digital down converter;

obtaining in-phase and quadrature phase data samples;

calculating a peak-to-peak value when the in-phase signal is near zero;

comparing the calculated peak-to-peak value with a previously determined peak-to-peak value;

saving whichever peak-to-peak value is larger; and

repeating the above steps for each possible phase increment.

7. The method of Claim 6, wherein the step of normalizing a gain value for the in-phase and quadrature phase signals of the selected digital down converter comprises the steps of:

reading an in-phase and a quadrature phase gain setting;

obtaining in-phase and quadrature phase data samples;

comparing the in-phase and quadrature phase data samples;

calculating a new in-phase gain, when the in-phase data is larger than the quadrature phase data, by multiplying the in-phase gain setting by the quotient [Q/I]; and

calculating a new quadrature phase gain, when the quadrature phase data is larger than the in-phase data, by multiplying the quadrature phase gain setting by the quotient [I/Q].

8. An apparatus for calibrating a digital down converter in a signal processing system, the apparatus comprising:

a calibration digital down converter connected to receive in-phase and quadrature phase data for a selected digital down converter;

a system controller connected to the digital down converter and the calibration digital down converter, wherein the calibration digital down converter, controlled by the system controller, mimics an operation of the digital down converter in order to determine optimal digital down converter settings, and the system controller updates the determined optimal settings for the digital down converter so that the digital down converter is calibrated according to the optimal settings.

9. The apparatus of Claim 8, wherein the optimal settings to be determined include a best polarization diversity detector path, a best in-phase phase offset value, a best quadrature phase offset value, and a normalized in-phase and quadrature phase gain value.

DATED THIS 8 DAY FEBRUARY 1999

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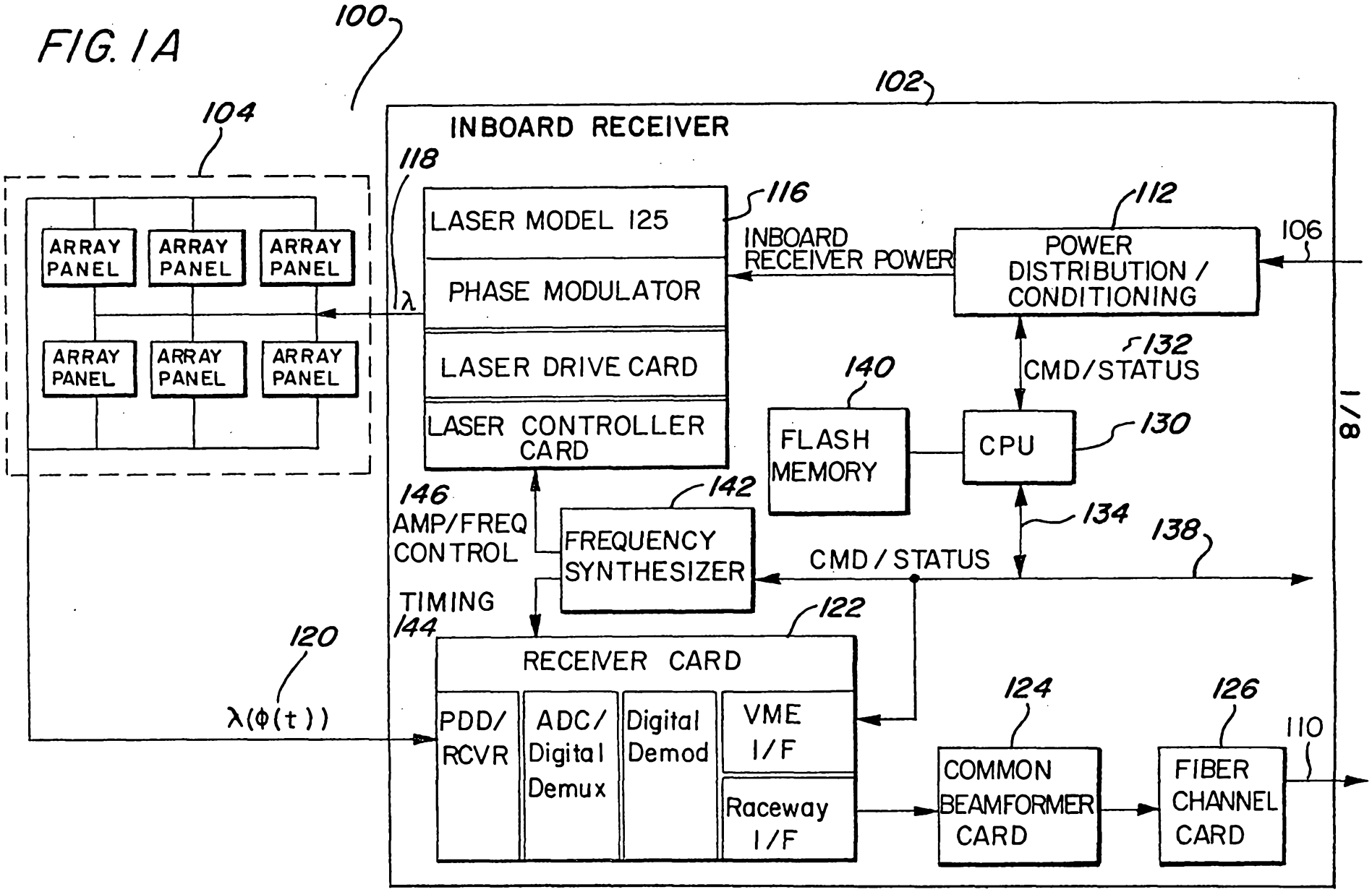
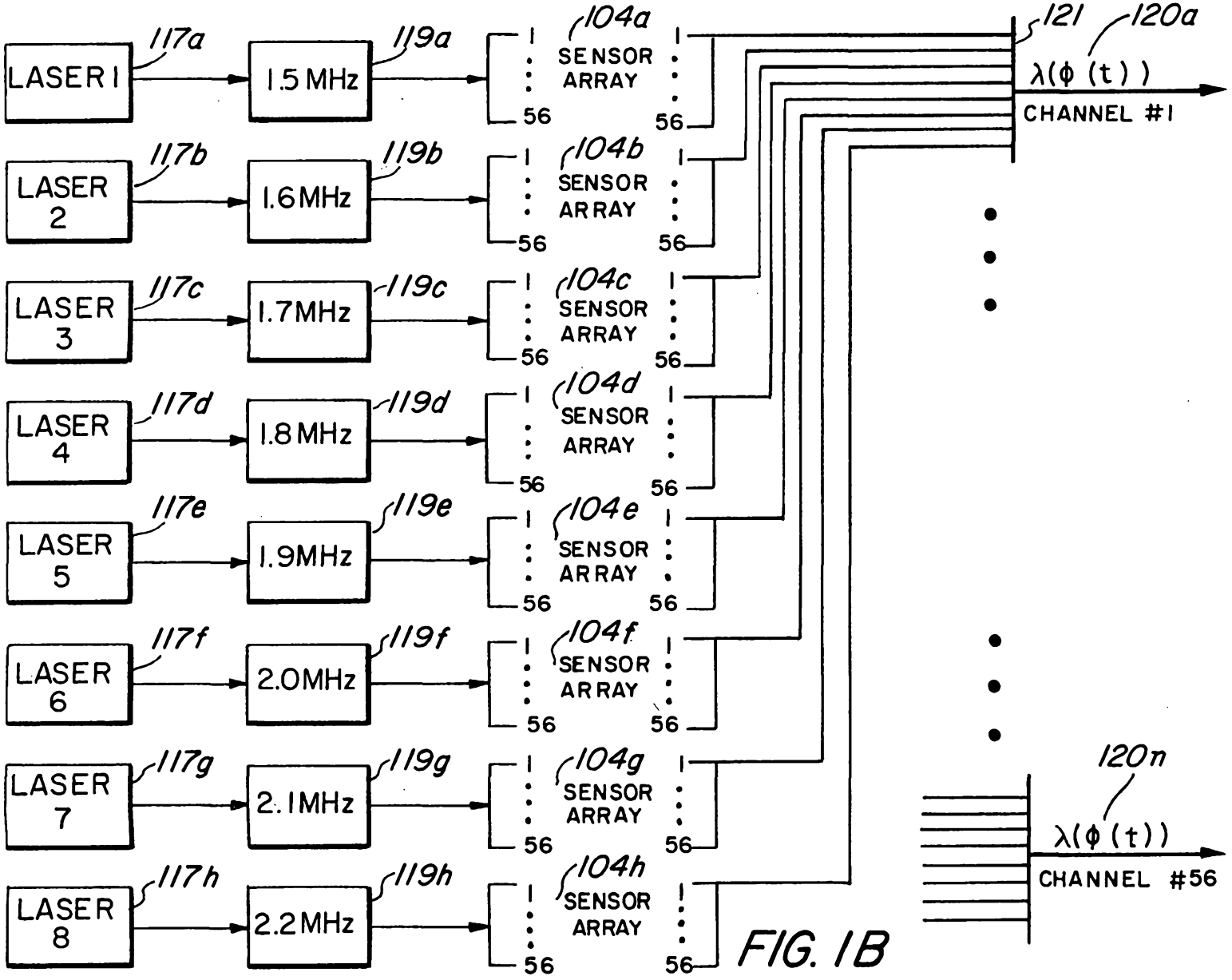
FIG. 1A




LASER 1
LASER 2
LASER 3
LASER 4
LASER 5
LASER 6
LASER 7
LASER 8
117a
117b
117c
117d
117e
117f
117g
117h
1.5 MHz
1.6MHz
1.7MHz
1.8 MHz
1.9MHz
2.0MHz
2.1MHz
2.2MHz
119a
119b
119c
119d
119e
119f
119g
119h
104a SENSOR ARRAY
104b SENSOR ARRAY
104c SENSOR ARRAY
104d SENSOR ARRAY
104e SENSOR ARRAY
104f SENSOR ARRAY
104g SENSOR ARRAY
104h SENSOR ARRAY
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120n
λ(φ (t))
CHANNEL #56

FIG. 1B

FIG. 2

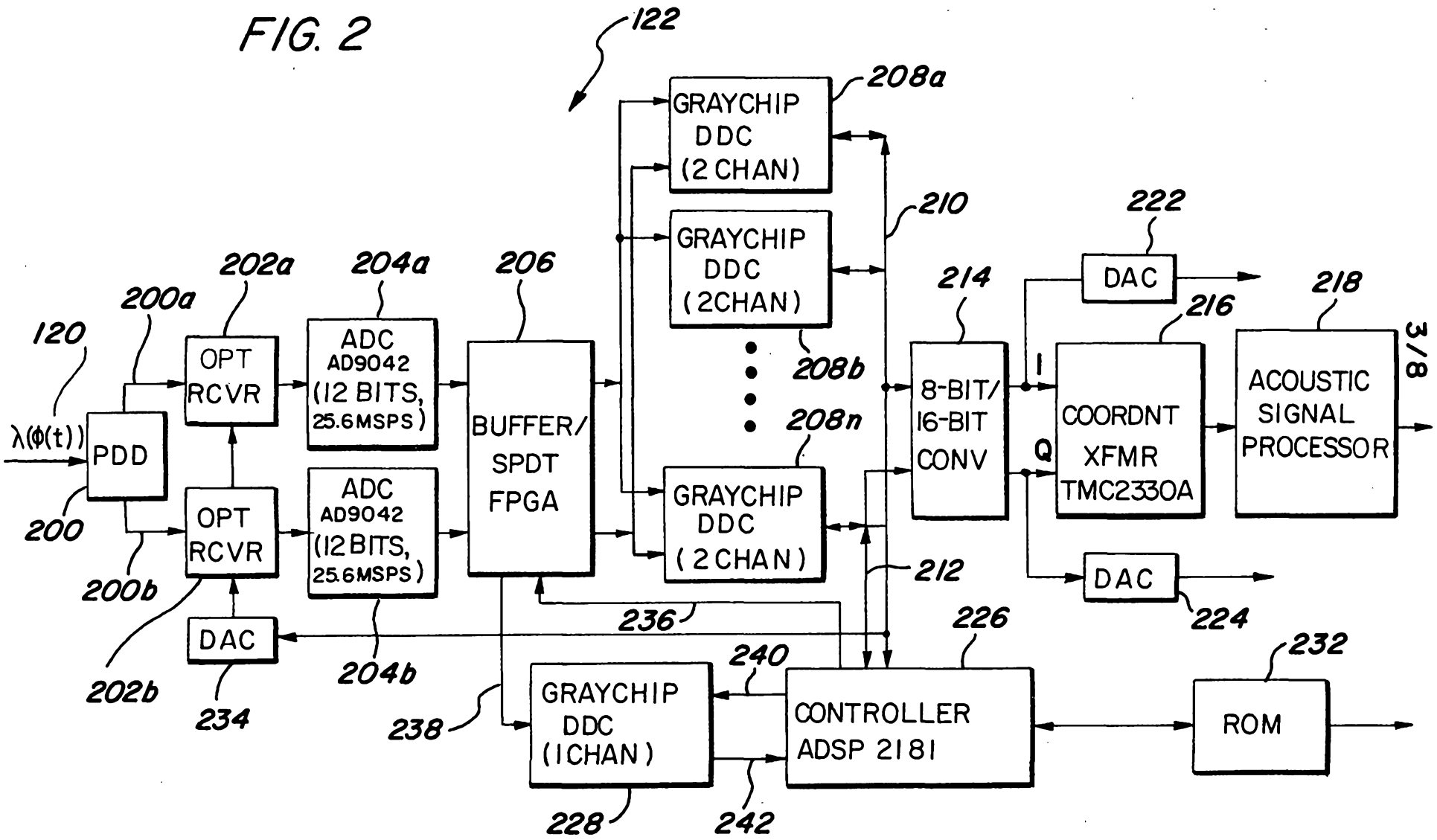


FIG. 3

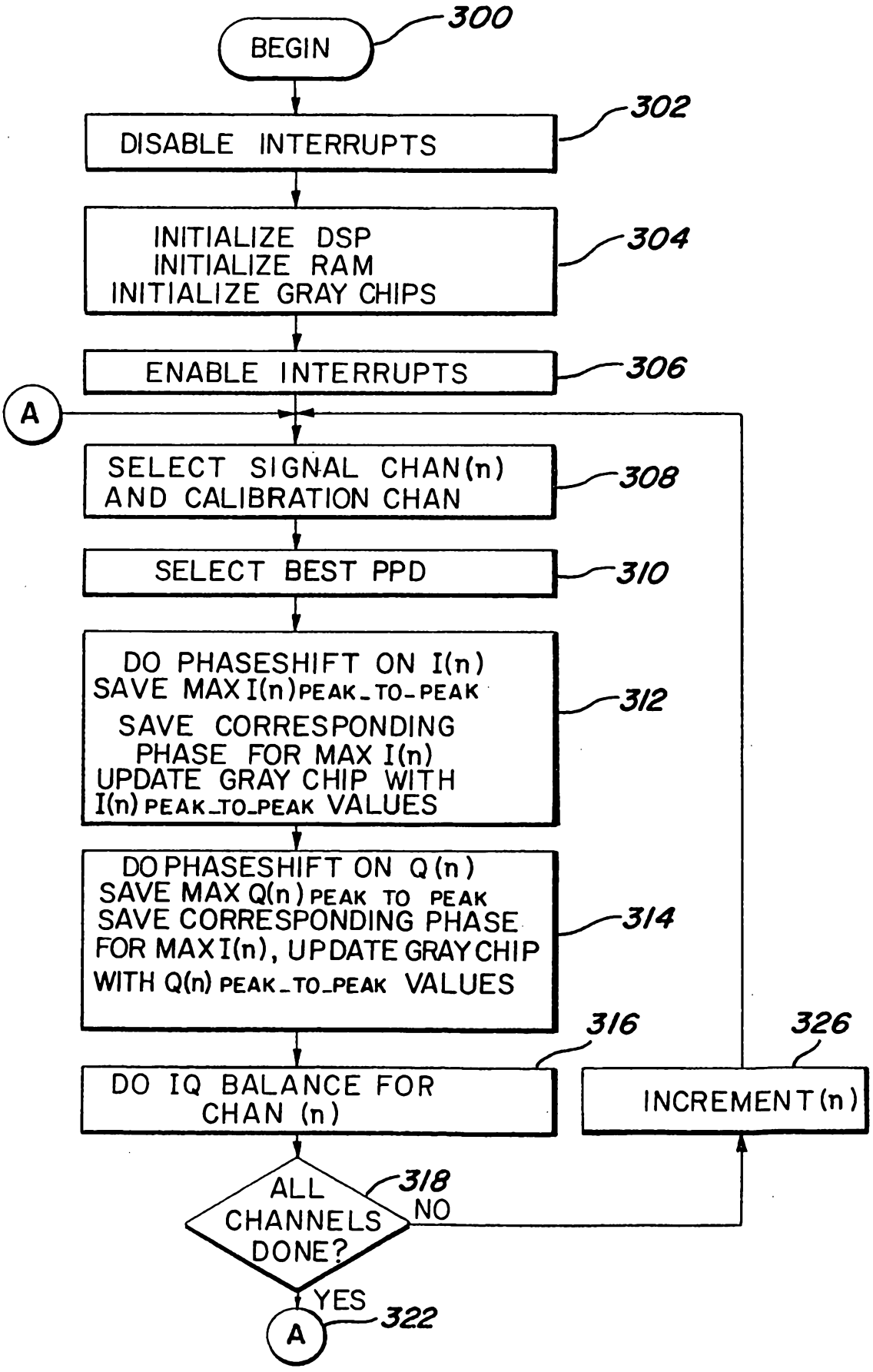

BEGIN
300
DISABLE INTERRUPTS
302
INITIALIZE DSP
INITIALIZE RAM
INITIALIZE GRAY CHIPS
304
ENABLE INTERRUPTS
306
A
SELECT SIGNAL CHAN(n)
AND CALIBRATION CHAN
308
SELECT BEST PPD
310
DO PHASESHIFT ON I(n)
SAVE MAX I(n) PEAK_TO-PEAK
SAVE CORRESPONDING
PHASE FOR MAX I(n)
UPDATE GRAY CHIP WITH
I(n) PEAK_TO_PEAK VALUES
312
DO PHASESHIFT ON Q(n)
SAVE MAX Q(n) PEAK TO PEAK
SAVE CORRESPONDING PHASE
FOR MAX I(n), UPDATE GRAY CHIP
WITH Q(n) PEAK_TO_PEAK VALUES
314
316
DO IQ BALANCE FOR
CHAN (n)
326
INCREMENT(n)
ALL
CHANNELS
DONE?
318
NO
YES
A
322

FIG. 4

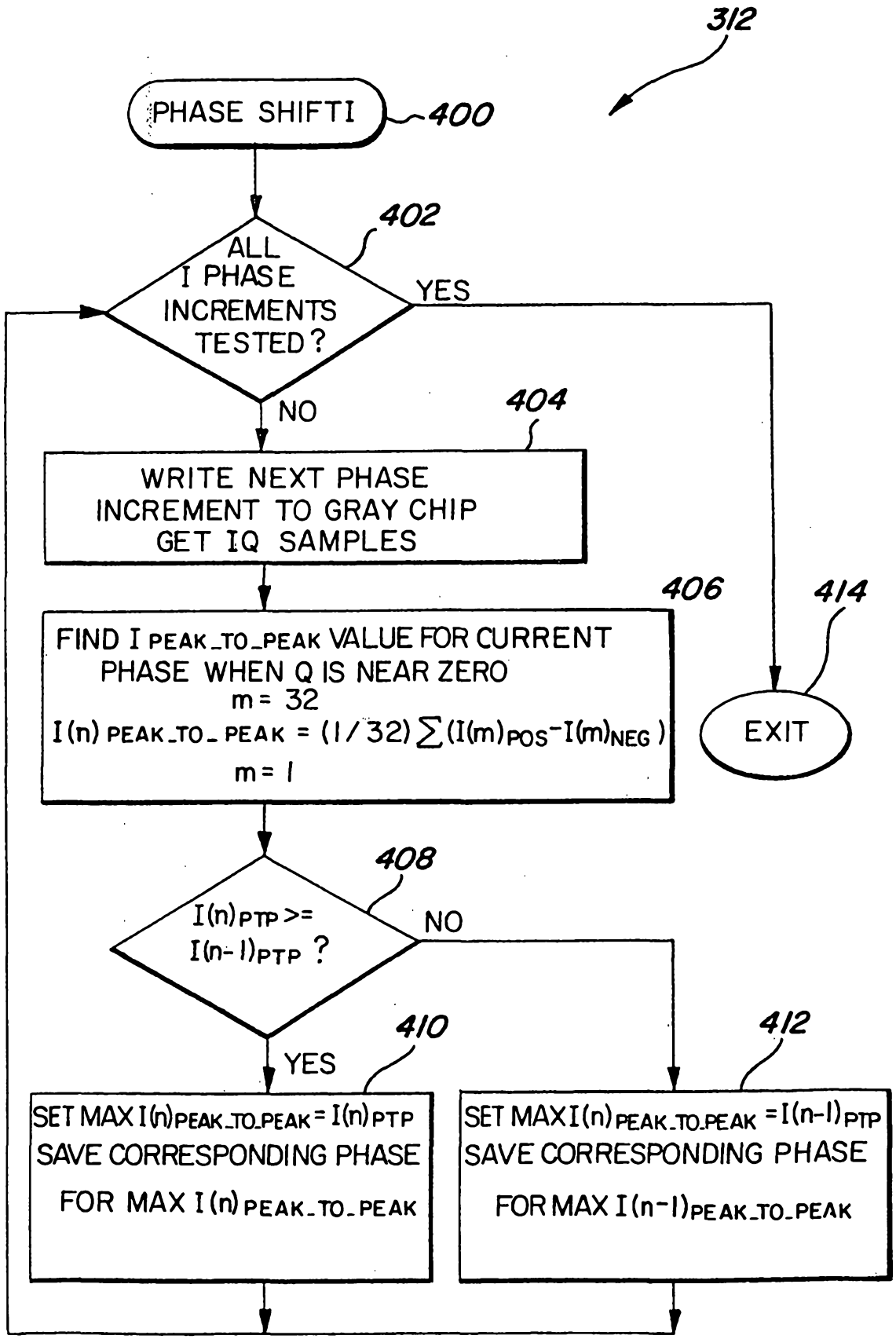
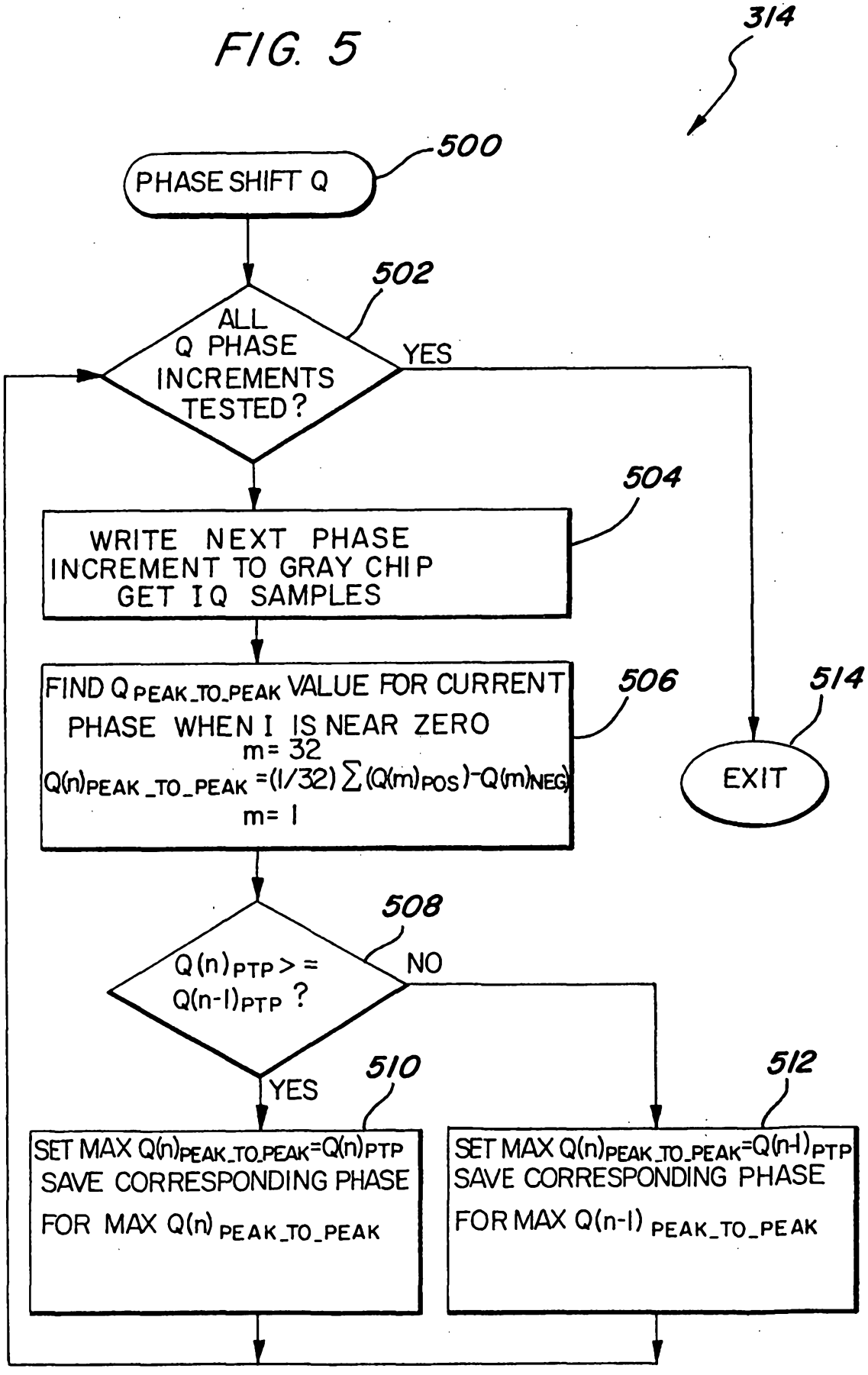

312
PHASE SHIFTI
400
402
ALL I PHASE INCREMENTS TESTED?
YES
NO
404
WRITE NEXT PHASE INCREMENT TO GRAY CHIP GET IQ SAMPLES
406
FIND I PEAK_TO_PEAK VALUE FOR CURRENT PHASE WHEN Q IS NEAR ZERO
m = 32
I(n) PEAK_TO_PEAK = (1/32) ∑ (I(m)POS - I(m)NEG)
m = 1
414
EXIT
408
I(n)PTP >= I(n-1)PTP ?
NO
YES
410
SET MAX I(n)PEAK_TO_PEAK = I(n)PTP
SAVE CORRESPONDING PHASE FOR MAX I(n)PEAK_TO_PEAK
412
SET MAX I(n)PEAK_TO_PEAK = I(n-1)PTP
SAVE CORRESPONDING PHASE FOR MAX I(n-1)PEAK_TO_PEAK

FIG. 5


314
500
PHASE SHIFT Q
502
ALL Q PHASE INCREMENTS TESTED?
YES
504
WRITE NEXT PHASE INCREMENT TO GRAY CHIP GET IQ SAMPLES
506
FIND Q PEAK_TO_PEAK VALUE FOR CURRENT PHASE WHEN I IS NEAR ZERO
m= 32
Q(n)PEAK_TO_PEAK =(1/32) Σ (Q(m)POS)-Q(m)NEG)
m= 1
514
EXIT
508
Q(n)PTP >= Q(n-1)PTP ?
NO
YES
510
SET MAX Q(n)PEAK_TO_PEAK=Q(n)PTP
SAVE CORRESPONDING PHASE
FOR MAX Q(n) PEAK_TO_PEAK
512
SET MAX Q(n)PEAK_TO_PEAK=Q(n-1)PTP
SAVE CORRESPONDING PHASE
FOR MAX Q(n-1) PEAK_TO_PEAK

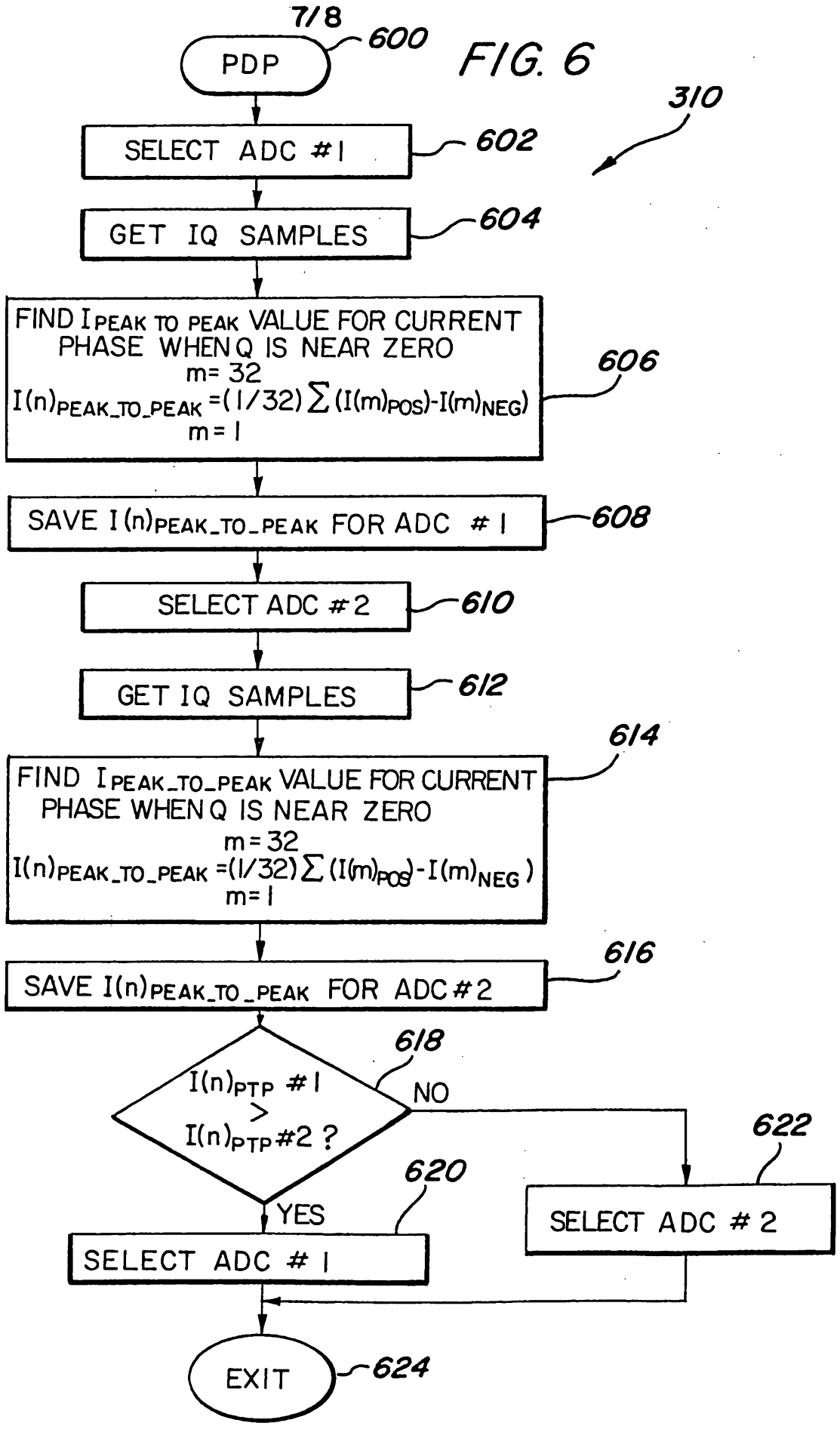
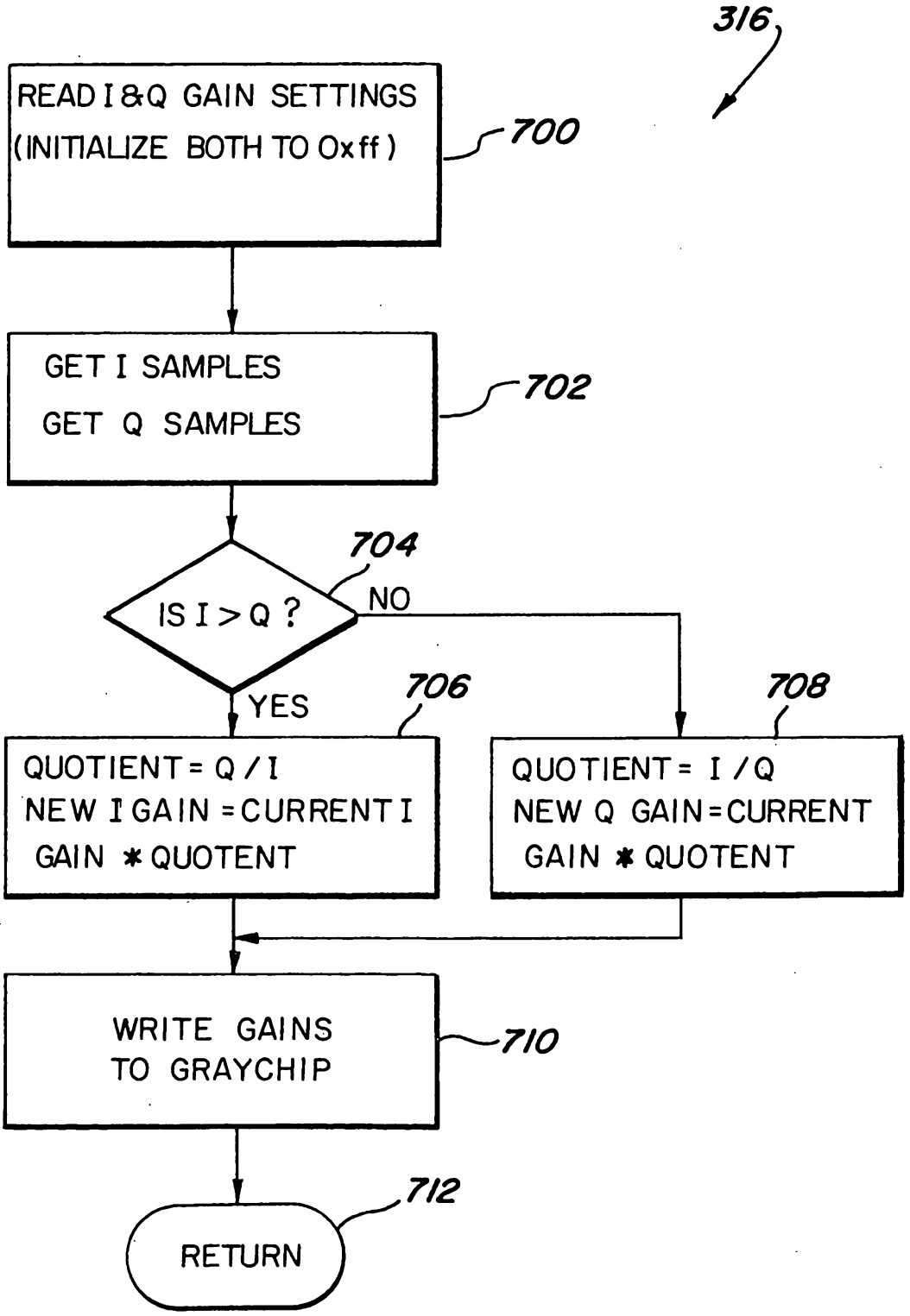

718
600
PDP
FIG. 6
310
SELECT ADC #1
602
GET IQ SAMPLES
604
FIND I PEAK TO PEAK VALUE FOR CURRENT PHASE WHEN Q IS NEAR ZERO
m= 32
I(n)PEAK_TO_PEAK =(1/32) Σ (I(m)POS)-I(m)NEG)
m= 1
606
SAVE I(n)PEAK_TO_PEAK FOR ADC #1
608
SELECT ADC #2
610
GET IQ SAMPLES
612
614
FIND I PEAK_TO_PEAK VALUE FOR CURRENT PHASE WHEN Q IS NEAR ZERO
m= 32
I(n)PEAK_TO_PEAK =(1/32) Σ (I(m)POS)-I(m)NEG)
m= 1
SAVE I(n)PEAK_TO_PEAK FOR ADC#2
616
618
I(n)PTP #1
>
I(n)PTP#2 ?
NO
622
YES
620
SELECT ADC #2
SELECT ADC #1
EXIT
624

FIG. 7


316
READ I&Q GAIN SETTINGS
(INITIALIZE BOTH TO 0xff)
700
GET I SAMPLES
GET Q SAMPLES
702
704
IS I > Q ?
NO
YES
706
708
QUOTIENT = Q / I
NEW I GAIN = CURRENT I
GAIN * QUOTENT
QUOTIENT = I / Q
NEW Q GAIN = CURRENT
GAIN * QUOTENT
WRITE GAINS
TO GRAYCHIP
710
712
RETURN