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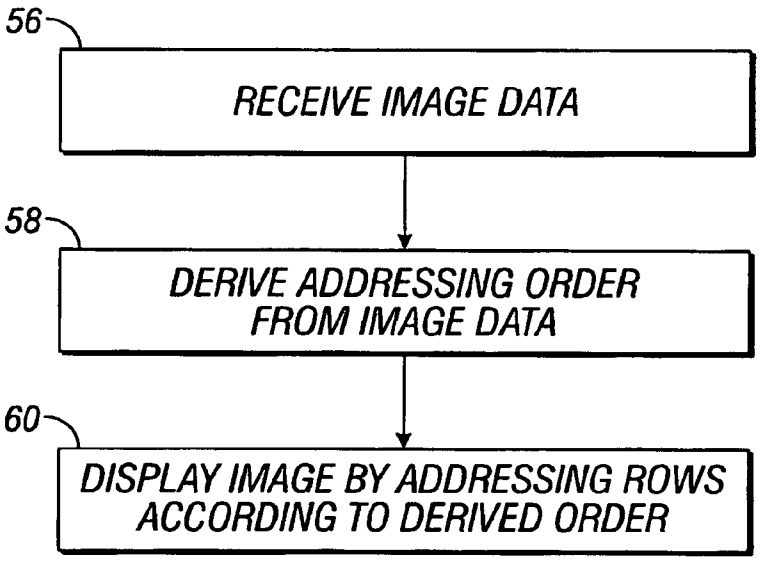
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(54) **Title:** POWER CONSUMPTION OPTIMIZED DISPLAY UPDATE



(57) **Abstract:** Systems and methods for reducing the power consumption necessary for updating a display are provided. The methods include determining a row addressing order based on an attribute of the image data that minimizes the number of column charging transitions necessary to write the image data to the display. In some embodiments, the row-addressing order is determined based on a determination of a whiteness value for the row. In some embodiments, a power-optimized row-addressing order is embedded in image data, allowing a display device to write the image data to the display more efficiently.

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POWER CONSUMPTION OPTIMIZED DISPLAY UPDATE

BACKGROUND OF THE INVENTION

[0001] Microelectromechanical systems (MEMS) include micro mechanical elements, actuators, and electronics. Micromechanical elements may be created using deposition, etching, and or other micromachining processes that etch away parts of substrates and/or deposit material layers or that add layers to form electrical and electromechanical devices. One type of MEMS device is called an interferometric modulator. As used herein, the term interferometric modulator or interferometric light modulator refers to a device that selectively absorbs and/or reflects light using the principles of optical interference. In certain embodiments, an interferometric modulator may comprise a pair of conductive plates, one or both of which may be transparent and/or reflective in whole or part and capable of relative motion upon application of an appropriate electrical signal. In a particular embodiment, one plate may comprise a stationary layer deposited on a substrate and the other plate may comprise a metallic membrane separated from the stationary layer by an air gap. As described herein in more detail, the position of one plate in relation to another can change the optical interference of light incident on the interferometric modulator. Such devices have a wide range of applications, and it would be beneficial in the art to utilize and/or modify the characteristics of these types of devices so that their features can be exploited in improving existing products and creating new products that have not yet been developed.

SUMMARY OF THE INVENTION

[0002] The system, method, and devices of the invention each have several aspects, no single one of which is solely responsible for its desirable attributes. Without limiting the scope of this invention, several of its features will now be discussed briefly.

[0003] One aspect of the invention includes a method of writing a display image to a display having an array of pixels. The method includes receiving image data, deriving a row-addressing order based at least in part on at least some of the stored image data, and writing the display image to the display by addressing rows in the array of pixels according to the row-addressing order.

[0004] In another embodiment, a method of determining a row-addressing order for an image includes determining one or more row attributes for one or more rows of the data in the image; and determining, based one or more row attributes, the row-addressing order.

[0005] In another embodiment, a method of displaying an image on a display is provided. The method includes receiving an image data file, the image data file including a row-addressing order. The method further includes creating the display image on the display by addressing the rows on the display according to the row-addressing order.

[0006] In yet another embodiment, a display apparatus is provided. The display apparatus includes a memory storing image data and a processor configured to receive the image data and calculate a row-addressing order based on a row attribute for one or more rows of the image data. The apparatus further includes a controller configured to present the image data to a display on a row-by-row basis according to the calculated row-addressing order.

[0007] In yet another embodiment, a display apparatus comprising means for receiving image data is provided. The display apparatus also includes means for deriving an addressing order based at least in part on one or more attributes of the image data and means for presenting the processed image data to a display in accordance with the derived addressing order.

[0008] In still another embodiment, a system is provided for displaying data on an array of interferometric modulators. The system may include a server configured to calculate an addressing order for image data. The system further includes a client device comprising a display and configured to receive the image data and the calculated addressing order from the server, and to display the image data on the array by addressing the array according to the addressing order.

[0009] In yet another embodiment, a computer-readable medium having computer-executable instructions stored thereon which, when executed cause a computing device to perform method of displaying an image on a display is provided. The method performed by the computer comprises receiving an image data file, the image data file including a row-addressing order, and creating the display image on the display by addressing the rows on the display according to the row-addressing order.

[0010] In another embodiment, a computer-readable medium having computer-executable instructions stored thereon which, when executed cause a computing device to

perform a method writing a display image to a display having an array of pixels is provided. The method includes receiving image data and deriving a row-addressing order based at least in part on at least some of the stored image data. The method further includes writing the display image to the display by addressing rows in the array of pixels according to the row-addressing order.

[0011] In still another embodiment, a computer-readable medium having computer-executable instructions stored thereon, which when executed cause a computing device to perform a method of determining a row-addressing order for an image is provided. The method performed by the computing device comprises determining one or more row attributes for one or more rows of the data in the image, and determining, based one or more row attributes, the row-addressing order.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] FIG. 1 is an isometric view depicting a portion of one embodiment of an interferometric modulator display in which a movable reflective layer of a first interferometric modulator is in a relaxed position and a movable reflective layer of a second interferometric modulator is in an actuated position.

[0013] FIG. 2 is a system block diagram illustrating one embodiment of an electronic device incorporating a 3x3 interferometric modulator display.

[0014] FIG. 3 is a diagram of movable mirror position versus applied voltage for one exemplary embodiment of an interferometric modulator of FIG. 1.

[0015] FIG. 4 is an illustration of two sets of row and column voltages that may be used to drive an interferometric modulator display.

[0016] FIG. 5A illustrates one exemplary frame of display data in the 3x3 interferometric modulator display of FIG. 2.

[0017] FIG. 5B illustrates one exemplary timing diagram for row and column signals that may be used to write the frame of FIG. 5A.

[0018] FIGS. 6A and 6B are system block diagrams illustrating an embodiment of a visual display device comprising a plurality of interferometric modulators.

[0019] FIG. 7A is a cross section of the device of FIG. 1.

[0020] FIG. 7B is a cross section of an alternative embodiment of an interferometric modulator.

[0021] FIG. 7C is a cross section of another alternative embodiment of an interferometric modulator.

[0022] FIG 7D is a cross section of yet another alternative embodiment of an interferometric modulator.

[0023] FIG. 7E is a cross section of an additional alternative embodiment of an interferometric modulator.

[0024] FIGs. 8A-8F form an example of a prior art implementation of top to bottom row addressing.

[0025] FIGs. 9A-9B form an example of implementing a row-addressing order based on the whiteness of each row.

[0026] FIGs. 10A-10C form an example of determining a row addressing order using whiteness of sub-rows.

[0027] FIG. 11 is a flowchart illustrating a method for writing a display image on a display array.

[0028] FIG. 12 is a flowchart illustrating a method of determining a row-addressing order in a display device.

[0029] FIG. 13 illustrates a method for receiving and displaying an image using an addressing order included in the received image data.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0030] The following detailed description is directed to certain specific embodiments of the invention. However, the invention can be embodied in a multitude of different ways. In this description, reference is made to the drawings wherein like parts are designated with like numerals throughout. As will be apparent from the following description, the embodiments may be implemented in any device that is configured to display an image, whether in motion (e.g., video) or stationary (e.g., still image), and whether textual or pictorial. More particularly, it is contemplated that the embodiments may be implemented in or associated with a variety of electronic devices such as, but not limited to, mobile telephones, wireless devices, personal data assistants (PDAs), hand-held or portable computers, GPS receivers/navigators, cameras, MP3 players, camcorders, game consoles, wrist watches, clocks, calculators, television monitors, flat panel displays, computer monitors, auto displays (e.g., odometer display, etc.), cockpit controls and/or displays, display of camera views (e.g., display of a rear view camera in a vehicle),

electronic photographs, electronic billboards or signs, projectors, architectural structures, packaging, and aesthetic structures (e.g., display of images on a piece of jewelry). MEMS devices of similar structure to those described herein can also be used in non-display applications such as in electronic switching devices.

[0031] Conventional approaches to reducing power consumption in MEMS display devices have included various techniques that each tend to compromise the user experience by decreasing the quality of the image displayed to the user. These approaches have included decreasing the resolution or complexity of displayed images, decreasing the number of images in the sequence over a given time period, and decreasing the greyscale or color intensity depth of the image. In one or more embodiments of the present invention, a system and method is provided which allows a display device to be configured to reduce power consumption by determining a row-addressing order based on attributes of the image data, and reducing the number of column charging transitions necessary to write an image to the display. In other embodiments, the invention provides methods of adjusting pixel actuation patterns to minimally impact image quality but at the same time reduce the number of column charge transitions necessary to raster an image on a display.

[0032] One interferometric modulator display embodiment comprising an interferometric MEMS display element is illustrated in Figure 1. In these devices, the pixels are in either a bright or dark state. In the bright ("on" or "open") state, the display element reflects a large portion of incident visible light to a user. When in the dark ("off" or "closed") state, the display element reflects little incident visible light to the user. Depending on the embodiment, the light reflectance properties of the "on" and "off" states may be reversed. MEMS pixels can be configured to reflect predominantly at selected colors, allowing for a color display in addition to black and white.

[0033] Figure 1 is an isometric view depicting two adjacent pixels in a series of pixels of a visual display, wherein each pixel comprises a MEMS interferometric modulator. In some embodiments, an interferometric modulator display comprises a row/column array of these interferometric modulators. Each interferometric modulator includes a pair of reflective layers positioned at a variable and controllable distance from each other to form a resonant optical cavity with at least one variable dimension. In one embodiment, one of the reflective layers may be moved between two positions. In the first position, referred to herein as the relaxed position, the movable reflective layer is positioned at a relatively large distance from a fixed partially reflective layer. In the second

position, referred to herein as the actuated position, the movable reflective layer is positioned more closely adjacent to the partially reflective layer. Incident light that reflects from the two layers interferes constructively or destructively depending on the position of the movable reflective layer, producing either an overall reflective or non-reflective state for each pixel.

[0034] The depicted portion of the pixel array in Figure 1 includes two adjacent interferometric modulators 12a and 12b. In the interferometric modulator 12a on the left, a movable reflective layer 14a is illustrated in a relaxed position at a predetermined distance from an optical stack 16a, which includes a partially reflective layer. In the interferometric modulator 12b on the right, the movable reflective layer 14b is illustrated in an actuated position adjacent to the optical stack 16b.

[0035] The optical stacks 16a and 16b (collectively referred to as optical stack 16), as referenced herein, typically comprise of several fused layers, which can include an electrode layer, such as indium tin oxide (ITO), a partially reflective layer, such as chromium, and a transparent dielectric. The optical stack 16 is thus electrically conductive, partially transparent and partially reflective, and may be fabricated, for example, by depositing one or more of the above layers onto a transparent substrate 20. The partially reflective layer can be formed from a variety of materials that are partially reflective such as various metals, semiconductors, and dielectrics. The partially reflective layer can be formed of one or more layers of materials, and each of the layers can be formed of a single material or a combination of materials.

[0036] In some embodiments, the layers of the optical stack are patterned into parallel strips, and may form row electrodes in a display device as described further below. The movable reflective layers 14a, 14b may be formed as a series of parallel strips of a deposited metal layer or layers (orthogonal to the row electrodes of 16a, 16b) deposited on top of posts 18 and an intervening sacrificial material deposited between the posts 18. When the sacrificial material is etched away, the movable reflective layers 14a, 14b are separated from the optical stacks 16a, 16b by a defined gap 19. A highly conductive and reflective material such as aluminum may be used for the reflective layers 14, and these strips may form column electrodes in a display device.

[0037] With no applied voltage, the cavity 19 remains between the movable reflective layer 14a and optical stack 16a, with the movable reflective layer 14a in a mechanically relaxed state, as illustrated by the pixel 12a in Figure 1. However, when a

potential difference is applied to a selected row and column, the capacitor formed at the intersection of the row and column electrodes at the corresponding pixel becomes charged, and electrostatic forces pull the electrodes together. If the voltage is high enough, the movable reflective layer 14 is deformed and is forced against the optical stack 16. A dielectric layer (not illustrated in this Figure) within the optical stack 16 may prevent shorting and control the separation distance between layers 14 and 16, as illustrated by pixel 12b on the right in Figure 1. The behavior is the same regardless of the polarity of the applied potential difference. In this way, row/column actuation that can control the reflective vs. non-reflective pixel states is analogous in many ways to that used in conventional LCD and other display technologies.

[0038] Figures 2 through 5B illustrate one exemplary process and system for using an array of interferometric modulators in a display application.

[0039] Figure 2 is a system block diagram illustrating one embodiment of an electronic device that may incorporate aspects of the invention. In the exemplary embodiment, the electronic device includes a processor 21 which may be any general purpose single- or multi-chip microprocessor such as an ARM, Pentium®, Pentium II®, Pentium III®, Pentium IV®, Pentium® Pro, an 8051, a MIPS®, a Power PC®, an ALPHA®, or any special purpose microprocessor such as a digital signal processor, microcontroller, or a programmable gate array. As is conventional in the art, the processor 21 may be configured to execute one or more software modules. In addition to executing an operating system, the processor may be configured to execute one or more software applications, including a web browser, a telephone application, an email program, or any other software application.

[0040] In one embodiment, the processor 21 is also configured to communicate with an array driver 22. In one embodiment, the array driver 22 includes a row driver circuit 24 and a column driver circuit 26 that provide signals to a display array or panel 30. The cross section of the array illustrated in Figure 1 is shown by the lines 1-1 in Figure 2. For MEMS interferometric modulators, the row/column actuation protocol may take advantage of a hysteresis property of these devices illustrated in Figure 3. It may require, for example, an 8 volt potential difference to cause a movable layer to deform from the relaxed state to the actuated state. However, when the voltage is reduced from that value, the movable layer maintains its state as the voltage drops back below 8 volts. In the exemplary embodiment of Figure 3, the movable layer does not relax completely until the

voltage drops below 1 volt. There is thus a range of voltage, about 2 to 6 V in the example illustrated in Figure 3, where there exists a window of applied voltage within which the device is stable in either the relaxed or actuated state. This is referred to herein as the "hysteresis window" or "stability window." For a display array having the hysteresis characteristics of Figure 3, the row/column actuation protocol can be designed such that during row strobing, pixels in the strobed row that are to be actuated are exposed to a voltage difference of about 8 volts, and pixels that are to be relaxed are exposed to a voltage difference of close to zero volts. After the strobe, the pixels are exposed to a steady state voltage difference of about 4 volts such that they remain in whatever state the row strobe put them in. After being written, each pixel sees a potential difference within the "stability window" of 2-6 volts in this example. This feature makes the pixel design illustrated in Figure 1 stable under the same applied voltage conditions in either an actuated or relaxed pre-existing state. Since each pixel of the interferometric modulator, whether in the actuated or relaxed state, is essentially a capacitor formed by the fixed and moving reflective layers, this stable state can be held at a voltage within the hysteresis window with almost no power dissipation. Essentially no current flows into the pixel if the applied potential is fixed.

[0041] In typical applications, a display frame may be created by asserting the set of column electrodes in accordance with the desired set of actuated pixels in the first row. A row pulse is then applied to the row 1 electrode, actuating the pixels corresponding to the asserted column lines. The asserted set of column electrodes is then changed to correspond to the desired set of actuated pixels in the second row. A pulse is then applied to the row 2 electrode, actuating the appropriate pixels in row 2 in accordance with the asserted column electrodes. The row 1 pixels are unaffected by the row 2 pulse, and remain in the state they were set to during the row 1 pulse. This may be repeated for the entire series of rows in a sequential fashion to produce the frame. Generally, the frames are refreshed and/or updated with new display data by continually repeating this process at some desired number of frames per second. A wide variety of protocols for driving row and column electrodes of pixel arrays to produce display frames are also well known and may be used in conjunction with the present invention.

[0042] Figures 4, 5A, and 5B illustrate possible actuation protocols for creating a display frame on the 3x3 array of Figure 2. Figure 4 illustrates a possible set of column and row voltage levels that may be used for pixels exhibiting the hysteresis curves of

Figure 3. In the second row of the Figure 4 embodiment, actuating a pixel involves setting the appropriate column to $-V_{bias}$, and the appropriate row to $+\Delta V$, which may correspond to -4 volts and +4 volts respectively Relaxing the pixel is accomplished by setting the appropriate column to $+V_{bias}$, and the appropriate row to the same $+\Delta V$, producing a zero volt potential difference across the pixel. In those rows where the row voltage is held at zero volts, the pixels are stable in whatever state they were originally in, regardless of whether the column is at $+V_{bias}$, or $-V_{bias}$. The last row of Figure 4 illustrates an alternate embodiment, in which $-V_{bias}$ may correspond to 2 volts and $+\Delta V$ may correspond to 10 volts. The embodiment shown in the last row of Figure 4 differs from the second row of Figure 4 only in that each value is increased by 6 volts. One of skill in the art will appreciate that it is the voltage difference across the pixels that govern actuation/release patterns, and that the absolute values can be shifted.

[0043] As is also illustrated in Figure 4, it will be appreciated that voltages of opposite polarity than those described above can be used, e.g., actuating a pixel can involve setting the appropriate column to $+V_{bias}$, and the appropriate row to $-\Delta V$. In this embodiment, releasing the pixel is accomplished by setting the appropriate column to $-V_{bias}$, and the appropriate row to the same $-\Delta V$, producing a zero volt potential difference across the pixel.

[0044] Figure 5B is a timing diagram showing a series of row and column signals applied to the 3x3 array of Figure 2 which will result in the display arrangement illustrated in Figure 5A, where actuated pixels are non-reflective. Prior to writing the frame illustrated in Figure 5A, the pixels can be in any state, and in this example, all the rows are at 0 volts, and all the columns are at +5 volts. With these applied voltages, all pixels are stable in their existing actuated or relaxed states.

[0045] In the Figure 5A frame, pixels (1,1), (1,2), (2,2), (3,2) and (3,3) are actuated. To accomplish this, during a "line time" for row 1, columns 1 and 2 are set to -4 volts, and column 3 is set to +4 volts. This does not change the state of any pixels, because all the pixels remain in the 2-6 volt stability window. Row 1 is then strobed with a pulse that goes from 0, up to 4 volts, and back to zero. This actuates the (1,1) and (1,2) pixels and relaxes the (1,3) pixel. No other pixels in the array are affected. To set row 2 as desired, column 2 is set to -4 volts, and columns 1 and 3 are set to +4 volts. The same strobe applied to row 2 will then actuate pixel (2,2) and relax pixels (2,1) and (2,3). Again, no other pixels of the array are affected. Row 3 is similarly set by setting columns 2 and 3

to -4 volts, and column 1 to +4 volts. The row 3 strobe sets the row 3 pixels as shown in Figure 5A. After writing the frame, the row potentials are zero, and the column potentials can remain at either +4 or -4 volts, and the display is then stable in the arrangement of Figure 5A. It will be appreciated that the same procedure can be employed for arrays of dozens or hundreds of rows and columns. It will also be appreciated that the timing, sequence, and levels of voltages used to perform row and column actuation can be varied widely within the general principles outlined above, and the above example is exemplary only, and any actuation voltage method can be used with the systems and methods described herein.

[0046] Figures 6A and 6B are system block diagrams illustrating an embodiment of a display device 40. The display device 40 can be, for example, a cellular or mobile telephone. However, the same components of display device 40 or slight variations thereof are also illustrative of various types of display devices such as televisions and portable media players.

[0047] The display device 40 includes a housing 41, a display 30, an antenna 43, a speaker 44, an input device 48, and a microphone 46. The housing 41 is generally formed from any of a variety of manufacturing processes as are well known to those of skill in the art, including injection molding, and vacuum forming. In addition, the housing 41 may be made from any of a variety of materials, including but not limited to plastic, metal, glass, rubber, and ceramic, or a combination thereof. In one embodiment the housing 41 includes removable portions (not shown) that may be interchanged with other removable portions of different color, or containing different logos, pictures, or symbols.

[0048] The display 30 of exemplary display device 40 may be any of a variety of displays, including a bi-stable display, as described herein. In other embodiments, the display 30 includes a flat-panel display, such as plasma, EL, OLED, STN LCD, or TFT LCD as described above, or a non-flat-panel display, such as a CRT or other tube device, as is well known to those of skill in the art. However, for purposes of describing the present embodiment, the display 30 includes an interferometric modulator display, as described herein.

[0049] The components of one embodiment of exemplary display device 40 are schematically illustrated in Figure 6B. The illustrated exemplary display device 40 includes a housing 41 and can include additional components at least partially enclosed therein. For example, in one embodiment, the exemplary display device 40 includes a

network interface 27 that includes an antenna 43 which is coupled to a transceiver 47. The transceiver 47 is connected to a processor 21, which is connected to conditioning hardware 52. The conditioning hardware 52 may be configured to condition a signal (e.g. filter a signal). The conditioning hardware 52 is connected to a speaker 45 and a microphone 46. The processor 21 is also connected to an input device 48 and a driver controller 29. The driver controller 29 is coupled to a frame buffer 28, and to an array driver 22, which in turn is coupled to a display array 30. A power supply 50 provides power to all components as required by the particular exemplary display device 40 design.

[0050] The network interface 27 includes the antenna 43 and the transceiver 47 so that the exemplary display device 40 can communicate with one ore more devices over a network. In one embodiment the network interface 27 may also have some processing capabilities to relieve requirements of the processor 21. The antenna 43 is any antenna known to those of skill in the art for transmitting and receiving signals. In one embodiment, the antenna transmits and receives RF signals according to the IEEE 802.11 standard, including IEEE 802.11(a), (b), or (g). In another embodiment, the antenna transmits and receives RF signals according to the BLUETOOTH standard. In the case of a cellular telephone, the antenna is designed to receive CDMA, GSM, AMPS or other known signals that are used to communicate within a wireless cell phone network. The transceiver 47 pre-processes the signals received from the antenna 43 so that they may be received by and further manipulated by the processor 21. The transceiver 47 also processes signals received from the processor 21 so that they may be transmitted from the exemplary display device 40 via the antenna 43.

[0051] In an alternative embodiment, the transceiver 47 can be replaced by a receiver. In yet another alternative embodiment, network interface 27 can be replaced by an image source, which can store or generate image data to be sent to the processor 21. For example, the image source can be a digital video disc (DVD) or a hard-disc drive that contains image data, or a software module that generates image data.

[0052] Processor 21 generally controls the overall operation of the exemplary display device 40. The processor 21 receives data, such as compressed image data from the network interface 27 or an image source, and processes the data into raw image data or into a format that is readily processed into raw image data. The processor 21 then sends the processed data to the driver controller 29 or to frame buffer 28 for storage. Raw data typically refers to the information that identifies the image characteristics at each location

within an image. For example, such image characteristics can include color, saturation, and greyscale level.

[0053] In one embodiment, the processor 21 includes a microcontroller, CPU, or logic unit to control operation of the exemplary display device 40. Conditioning hardware 52 generally includes amplifiers and filters for transmitting signals to the speaker 45, and for receiving signals from the microphone 46. Conditioning hardware 52 may be discrete components within the exemplary display device 40, or may be incorporated within the processor 21 or other components.

[0054] The driver controller 29 takes the raw image data generated by the processor 21 either directly from the processor 21 or from the frame buffer 28 and reformats the raw image data appropriately for high speed transmission to the array driver 22. Specifically, the driver controller 29 reformats the raw image data into a data flow having a raster-like format, such that it has a time order suitable for scanning across the display array 30. Then the driver controller 29 sends the formatted information to the array driver 22. Although a driver controller 29, such as a LCD controller, is often associated with the system processor 21 as a stand-alone Integrated Circuit (IC), such controllers may be implemented in many ways. They may be embedded in the processor 21 as hardware, embedded in the processor 21 as software, or fully integrated in hardware with the array driver 22. Embodiments as set forth above thus include computer readable media storing instructions that implement the methods described herein.

[0055] Typically, the array driver 22 receives the formatted information from the driver controller 29 and reformats the video data into a parallel set of waveforms that are applied many times per second to the hundreds and sometimes thousands of leads coming from the display's x-y matrix of pixels.

[0056] In one embodiment, the driver controller 29, array driver 22, and display array 30 are appropriate for any of the types of displays described herein. For example, in one embodiment, driver controller 29 is a conventional display controller or a bi-stable display controller (e.g., an interferometric modulator controller). In another embodiment, array driver 22 is a conventional driver or a bi-stable display driver (e.g., an interferometric modulator display). In one embodiment, a driver controller 29 is integrated with the array driver 22. Such an embodiment is common in highly integrated systems such as cellular phones, watches, and other small area displays. In yet another embodiment, display array

30 is a typical display array or a bi-stable display array (e.g., a display including an array of interferometric modulators).

[0057] The input device 48 allows a user to control the operation of the exemplary display device 40. In one embodiment, input device 48 includes a keypad, such as a QWERTY keyboard or a telephone keypad, a button, a switch, a touch-sensitive screen, a pressure- or heat-sensitive membrane. In one embodiment, the microphone 46 is an input device for the exemplary display device 40. When the microphone 46 is used to input data to the device, voice commands may be provided by a user for controlling operations of the exemplary display device 40.

[0058] Power supply 50 can include a variety of energy storage devices as are well known in the art. For example, in one embodiment, power supply 50 is a rechargeable battery, such as a nickel-cadmium battery or a lithium ion battery. In another embodiment, power supply 50 is a renewable energy source, a capacitor, or a solar cell, including a plastic solar cell, and solar-cell paint. In another embodiment, power supply 50 is configured to receive power from a wall outlet.

[0059] In some implementations control programmability resides, as described above, in a driver controller which can be located in several places in the electronic display system. In some cases control programmability resides in the array driver 22. Those of skill in the art will recognize that the above-described optimization may be implemented in any number of hardware and/or software components and in various configurations.

[0060] The details of the structure of interferometric modulators that operate in accordance with the principles set forth above may vary widely. For example, Figures 7A-7E illustrate five different embodiments of the movable reflective layer 14 and its supporting structures. Figure 7A is a cross section of the embodiment of Figure 1, where a strip of metal material 14 is deposited on orthogonally extending supports 18. In Figure 7B, the moveable reflective layer 14 is attached to supports at the corners only, on tethers 32. In Figure 7C, the moveable reflective layer 14 is suspended from a deformable layer 34, which may comprise a flexible metal. The deformable layer 34 connects, directly or indirectly, to the substrate 20 around the perimeter of the deformable layer 34. These connections are herein referred to as support posts. The embodiment illustrated in Figure 7D has support post plugs 42 upon which the deformable layer 34 rests. The movable reflective layer 14 remains suspended over the cavity, as in Figures 7A-7C, but the deformable layer 34 does not form the support posts by filling holes between the

deformable layer 34 and the optical stack 16. Rather, the support posts are formed of a planarization material, which is used to form support post plugs 42. The embodiment illustrated in Figure 7E is based on the embodiment shown in Figure 7D, but may also be adapted to work with any of the embodiments illustrated in Figures 7A-7C as well as additional embodiments not shown. In the embodiment shown in Figure 7E, an extra layer of metal or other conductive material has been used to form a bus structure 44. This allows signal routing along the back of the interferometric modulators, eliminating a number of electrodes that may otherwise have had to be formed on the substrate 20.

[0061] In embodiments such as those shown in Figure 7, the interferometric modulators function as direct-view devices, in which images are viewed from the front side of the transparent substrate 20, the side opposite to that upon which the modulator is arranged. In these embodiments, the reflective layer 14 optically shields the portions of the interferometric modulator on the side of the reflective layer opposite the substrate 20, including the deformable layer 34. This allows the shielded areas to be configured and operated upon without negatively affecting the image quality. Such shielding allows the bus structure 44 in Figure 7E, which provides the ability to separate the optical properties of the modulator from the electromechanical properties of the modulator, such as addressing and the movements that result from that addressing. This separable modulator architecture allows the structural design and materials used for the electromechanical aspects and the optical aspects of the modulator to be selected and to function independently of each other. Moreover, the embodiments shown in Figures 7C-7E have additional benefits deriving from the decoupling of the optical properties of the reflective layer 14 from its mechanical properties, which are carried out by the deformable layer 34. This allows the structural design and materials used for the reflective layer 14 to be optimized with respect to the optical properties, and the structural design and materials used for the deformable layer 34 to be optimized with respect to desired mechanical properties.

[0062] A major factor determining the power consumed by driving an interferometric modulator display is the charging and discharging the line capacitance for the columns receiving the image data. This is due to the fact that the column voltages are switched at a very high frequency (up to the number of rows in the array minus one per column for each frame update period), compared to the relatively low frequency of the row pulses (one pulse per row per frame update period). In fact, the power consumed by the

row pulses generated by row driver circuit may be ignored when estimating the power consumed in driving a display without sacrificing an accurate estimate of total power consumed. Accordingly, the term "column" as used herein is defined as the set of display inputs that receive image data at a relatively high signal transition frequency. The term "rows" is defined as the set of display inputs that receive a periodic applied signal that is independent of the display data and is applied at a relatively low frequency to each row, such as the row strobes described above. The terms "row" and "column" do not therefore imply any geometric position or relationship.

[0063] The basic equation for estimating the energy consumed by writing to an entire column, ignoring row pulse energy, is:

$$(\text{Energy/col}) = 1/2 * \text{count} * C_{line} * | V_{CH}^2 - V_{CL}^2 | \quad (1)$$

[0064] The power consumed in driving an entire array is simply the energy required for writing to every column divided by time or:

$$\text{Power} = \sum [\text{Energy/col}] * f \quad (2)$$

where:

count	=	number of transitions from V_{CH} to V_{CL} (and vice versa) required on a given column to display data for all rows
V_{CH}	=	the greater of two voltages applied to a column
V_{CL}	=	the lesser of the voltages applied to a column
C_{line}	=	capacitance of a column line
f	=	the frame update frequency (Hz)

[0065] It should be noted that these equations are applicable to driving voltages such as those shown in Figure 4B. Similar equations apply when negative voltages are used.

[0066] For a given frame update frequency (f) and frame size (number of columns), the power required to write to the display is linearly dependent on the frequency of the data being written. Of particular interest is the "count" variable in (1), which depends on the frequency of changes in pixel states (actuated or relaxed) in a given column. Thus, by reducing the number of column voltage transitions involved in writing to the

display, the amount of power consumed by the display is reduced. Currently, displays are addressed row-by-row, usually in a top-to-bottom order as described above with respect to Figures 5A and 5B. Addressing rows top-to-bottom may require many column voltage transitions to write a frame of image data to the display because the image data down a column may flip back and forth between "on" and "off" states a large number of times as the system proceeds through the set of rows in a linear top-down fashion.

[0067] Some embodiments of the invention involve utilizing a row-addressing order based on attributes of image data in order to update a display array using a reduced number of column voltage transitions. In order to reduce the number of column charge transitions, the system can create a row-addressing order based on the content of the image data. By ordering the row addressing with image content in mind, similar rows can be strobed one after the other, thereby reducing the total number of column transitions needed to write an image to the display.

[0068] Figure 8 illustrates an example of a prior art top-to-bottom implementation of column charge transitions and row addressing in a 5x5 array of display elements 12. The 5x5 array 50 may comprise a portion or all of display array 30 as described above. Figure 8A provides an example image being written to the 5x5 array 50. In this example, the entire first, third, and fifth rows have display elements in the non-reflective state. As used herein, a pixel element (or sub-element) in the non-reflective state may also be referred to as being "dark" or in an actuated state such as pixel 12b in Figure 1. The second and fourth rows are in a released state, also referred to as a reflective, "white," or non-actuated state such as pixel or display element 12a in Figure 1.

[0069] Figures 8B through 8F illustrate the column transitions necessary to display the pixel actuation scheme shown in Figure 8A using a conventional addressing ordering scheme. As discussed previously, the row-addressing order will proceed from top to bottom, with the necessary column charge transitions being performed to achieve the pixel image shown in Figure 8A. Referring now to Figure 8B, five column charge transitions, T1..T5 are shown. Because the image data indicates that each display element 12 in the first row should be actuated, each column charge transition sets the column voltage to the actuation voltage. If the row strobe goes from 6 to 10 (e.g., in accordance with Figure 4B), then this voltage would be 2 as illustrated in Figure 8B. Thus, when the first row is strobed, each of the display elements in row 1 is actuated.

[0070] Now referring to Figure 8C, the second row is addressed. Because the image data provides for five non-actuated display elements in the second row, the column voltage for each column is transitioned from the actuation voltage (e.g., 2V) to the release voltage (e.g., 10V) in transitions T6..T10. After transitioning the column voltage for each column, each of the display elements 12 in the second row is strobed so that each display element in the second row is released.

[0071] Like the first row, the image data indicates that the display elements in the third row should be actuated. Figure 8D shows five additional column voltage transitions T11..T15 that set the column voltage to the actuation voltage. The row is strobed, and each display element 12 is actuated by the strobing pulse. Figure 8E illustrates how each of the display elements 12 in the fourth row is released. Because the previous row's display elements were each actuated, in order to release the display elements in the fourth row, the column voltage must be transitioned for each column by transitions T16..T20. Upon completion of the column voltage transitions, the fourth row is strobed, resulting in the release of each display element in the row.

[0072] In Figure 8F, the fifth row in display array 30 is addressed. Each column is again transitioned from the release voltage to the actuation voltage because the previous row was white, and the current (fifth) row is dark. Thus, column charge transitions T21 through T25 set the column charge to the actuation voltage, and a row strobe actuates the appropriate display elements 12 in display array 30.

[0073] In the conventional process shown in Figure 8, twenty-five column voltage transitions were used to create the pixel actuation pattern. Because each column voltage transition consumes power, it is desirable to reduce the number of column voltage transitions when creating the display.

[0074] In one embodiment of the invention, the number of column charge transitions are reduced by setting a row-addressing order based on an attribute of the display data. Referring now to Figure 9A and 9B another 5x5 display array 60 is provided which has an identical actuation pattern to the display array previously discussed in Figure 8. By predetermining a row-addressing order based on an attribute of the image data, the number of column charge transitions is reduced significantly. In the case of Figure 9, the attribute upon which the row-addressing order is based is the "whiteness" of each row. Thus, those rows with the most white (or released) pixels are addressed first, and those with the fewest are addressed last.

[0075] Figure 9A illustrates column charge transitions T1..T5, which set each column to the release voltage. Once the columns have been charged, each of the white rows (rows 2 and 4 in this instance) is sequentially strobed to cause each display element 12 in the row to be released. Thus, two of the five rows of display elements have been created with only a total of five column charging transitions. Next, in Figure 9B, the column potentials are transitioned in each column by transitions T6..T10. After the transition, rows 1, 3, and 5 are sequentially strobed, causing the actuation of each display element 12 situated in the strobed rows. Thus, image is written to display array 60 using only ten column charging transitions, instead of 25, a 60% savings in power over the top to bottom addressing order of Figure 8.

[0076] This data dependent row addressing order can be performed on any set of image data to reduce column transitions. Tables 1 and 2 below also illustrate this row-addressing scheme as it can be applied to the actuation pattern shown in Figure 9. Image data analysis may, for example, involve first counting and tabulating the number of released pixels in each row. Table 1 shows for each row, how many of the pixels are released for the image of Figure 9. For rows 1, 3, and 5, 0 out of the 5 pixels in the row are white pixels. In rows 2 and 4, each of the pixels (i.e., 5 out of 5) is white. It will be appreciated that this counting could be performed for a display of any size, and with any variation of display data.

Table 1

Row #	1	2	3	4	5
# White Pixels	0	5	0	5	0

[0077] Given the pixel patterns described in Table 1, a row-addressing order may be derived by placing the rows in order from the most number of released pixels to the least, as shown in Table 2. For rows with the same number of released pixels, a random order or numerical order could be used to create an order within groups of rows having the same number of released pixels. Table 2 illustrates this sorting for the image of Figure 9.

Table 2

Address Order	Row #	White Pixels
1	2	5
2	4	5
3	1	0
4	3	0
5	5	0

[0078] In the examples provided in Figures 8 and 9 and Tables 1 and 2, each row was uniform in its actuation pattern. Each display element 12 in the first, third, and fifth rows was actuated, while each display element 12 in the second and fourth rows was released.

[0079] Basing the row-addressing order on the "whiteness" of the row was very effective for the image of Figure 9 because of the row uniformity. For other images with a narrower distribution of row whiteness the effectiveness will vary. In general, however, significant power reductions can be expected, especially when displaying images having regions of uniformity within them.

[0080] Furthermore, if the rows containing predominantly released pixels are written first, the line capacitance of the columns will decrease as the image is written, providing additional power reduction benefits.

[0081] For images or portions of images having rows with similar overall whiteness, more complicated row analysis can be performed to produce significant power reduction. Figure 10 provides an example of an image where ordering based on row whiteness alone provides no real advantage. In this image, because the rows each have three white pixels and three dark pixels, setting the row-addressing order based on the "whiteness" of the rows would not result in a change in the default top-to-bottom addressing order that was shown in Figure 8, as each row is similar in whiteness. Thus, fully writing this image to a display array would require a total of 30 column charging transitions using the process described in either Figure 8 or Figure 9.

[0082] To resolve this problem with images such as illustrated in Figure 10, rather than determining the row-addressing order based on an attribute of the entire row, a row-addressing order is created based on attributes of each half of each row. Tables 3-5 (shown below) provide an example of how the row addressing order may be based on the

left and right halves of a row (left sub-row 50 and right sub-row 52) to reduce column charging transitions necessary to create an image.

[0083] In this embodiment, the row is split into sub-rows 50 and 52 and the "whiteness" value is determined for each. Those rows in which both of sub-rows 50 and 52 are predominantly white are placed at the top of the row-addressing order. Rows in which left sub-row 50 is predominantly white and right sub-row 52 is not predominantly white are placed next in the addressing order. Rows in which right sub-row 52 is predominantly white and left sub-row 50 is not predominantly white are addressed next. Rows in which both sub-rows are not predominantly white are addressed last. Tables 3-5 show how this scheme may be applied to the to the actuation pattern of Figure 10.

[0084] Table 3 shows the number of "white" pixels in left sub-row 50 in each of the rows of the pixel array. In rows 1, 3, and 5, three out of three of the pixels on the left are white. In rows 2 and 4, none of the three pixels on the left are white.

Table 3 (Left Sub-Row)

Row #	1	2	3	4	5
# White Pixels	3	0	3	0	3

[0085] Table 4 shows the number of "white" pixels in right sub-row 52 of each row of the pixel array. Rows 1, 3, and 5 each have no white pixels on the right half, while in rows 2 and 4, each of the pixels is white on the right half.

Table 4 (Right Sub-Row)

Row #	1	2	3	4	5
# White Pixels	0	3	0	3	0

Because there are no rows in which both the left sub-row 50 and the right sub-row 52 are predominantly white, the row-addressing order in Table 5 begins with those rows in which left sub-row 50 is predominantly white and right sub-row 52 is not predominantly white. Thus, rows 1, 3, and 5 are placed at the top of the order. Rows 2 and 4 are then placed next in the order because they have predominantly white right sub-rows 52 and predominantly dark left sub-rows 50. Although there are no rows in which both the left sub-row and right sub-row are not predominantly white, if there were, they would be placed last in the row-addressing order.

Table 5 (Row-Addressing Order)

Address Order	Row #	White Pixels Left	White Pixels Right
1	1	3	0
2	3	3	0
3	5	3	0
4	2	0	3
5	4	0	3

[0086] This dramatically reduces the number of column transitions necessary to write the frame of Figure 10 over a top down addressing order. It will be appreciated that this same procedure could be applied to row quarters, eights, sixteenths, etc. with the benefit of more accurate row order determination and lower power, but at the cost of additional computational complexity.

[0087] A general method is shown in Figure 11 in which a display image may be created on display array 30. Display array 30 may advantageously comprise a MEMS display or other type of bi-stable display that includes pixels having actuated and unactuated states. At block 56, image data is received by the system. The image data may be received into display device 40 by way of user input interface 48, network interface 27, or it may be created by system processor 21 in response to a system event.

[0088] At block 58, display device 40 derives a row-addressing order based at least in part on part on attributes of the image data. The row addressing order may be stored in a register bank which is accessed by array driver 22 or driver controller 29 prior to writing image data to display array 30.

[0089] Depending upon the embodiment, the row-addressing order may be derived from various sources. In one embodiment, the row-addressing order is derived from an attribute of one or more rows of the image data. For example, the attribute might be the number of actuated pixels in the row and/or the number of unactuated pixels in the row. In yet another embodiment, the attribute may consider the "sameness" of various rows, i.e., the similarities between groups of rows. For example, in processing the image, the system processor 22 may determine that a number of non-adjacent rows have very similar or identical pixel actuation patterns. The row-addressing order may take this similarity into account, and place these rows together in the row-addressing order because

few column charge transitions would be required to write the display data to the identical or similar rows.

[0090] Lastly, at block 60, a display image is written to display array 30 by addressing rows in display array 30 according to the derived addressing order.

[0091] Although these embodiments have been described in terms of a row addressing order in which columns are charged to actuation and release voltages, one of skill in the art will readily appreciate that the invention may be easily implemented in a display device in which columns are strobed and rows are charged to actuation voltages and release voltages.

[0092] It will be appreciated that a row addressing order suitable for power reduction for a given frame need not be computed or derived in the array driver or processor local to the display itself. In some advantageous embodiments, a content provider can derive a suitable row addressing order and transmit the order to the display device along with the image data itself.

[0093] An example method of this type is provided in Figure 12. At state 62, a row addressing order is determined based at least in part on the image data. As described above, this may involve determining one or more row attributes for one or more rows of image data. For example, the row attributes may be determined by calculating the ratio of pixels or display elements in an actuated state to pixels or display elements in a non-actuated (i.e., released) state. The image data may not be in a format that directly indicates actuated and released pixels. In this case, it is possible to use substitute image information indicating the lightness or darkness of an image region or differences between image frames or regions of image frames. A variety of analyses can be performed that provide an indication of pixel actuation states along a row and that can be used to determine a row addressing order that will reduce energy consumption of the display device when the frame is written.

[0094] After determining the row-addressing order, at state 64, the row-addressing order is embedded in the image file itself. In some embodiments, these steps may take place when the image data is created. In other embodiments, the row-addressing order for the image may be determined by a networked computer or system such as a content server or headend server 106 in a network 104 as shown in Figure 6B. It will further be appreciated that the addressing order for an image need not be made part of the

image data itself. It can be transferred as part of an image header, or transmitted separately from the image data over the same or a different communications path.

[0095] Figure 13 illustrates a method implemented in the display device for receiving and displaying an image when a row-addressing order is included in the image file. At state 66, the display device may receive an image file which has a row-addressing order included with the image data. As described above, the row addressing order need not be in the image data itself, but may be received separately in some embodiments. In one embodiment, the image file may be received via the network interface 27, or it may be received via some other external data source such as a memory, a digital camera, or any other image data source that is external to display device.

[0096] At state 68, the display device writes the display image on the display array by addressing the rows in the order set forth by the row-addressing order. Thus, a display device may be configured to display image data according to an image dependent row-addressing order without having to perform computationally expensive calculations in determining that order.

[0097] In would also be possible to look at the row pixel patterns on a small scale, and perform minor modifications to the image data to reduce the number of column transitions when the proper row addressing order is utilized. In general, this may involve taking rows that are nearly identical in actuation pattern, and making them exactly identical. If this is performed for rows that are relatively widely separated from each other in the image, this will not affect the visual appearance, but will reduce the power required to write the image. These changes could be made close together while using an algorithm that holds local image values constant. This technique would be similar to stochastic dithering where pixels are modified to increase dynamic range.

[0098] Some displays can be addressed pixel-by-pixel instead of row-by-row. In these embodiments, essentially complete freedom with respect to which pixels to write to in what order is provided. In some such embodiments, all the white pixels in a column can be written to, and then all the black. This could be continued through the set of columns, producing one column transition per frame. In this embodiment, the rows become the high frequency modulated input and row transitions will dominate the power consumption. In this case, columns could be written to in order of whiteness to reduce the row capacitance as the display is written.

[0099] It will be understood by those of skill in the art that numerous and various modifications can be made without departing from the spirit of the present invention. Therefore, it should be clearly understood that the forms of the present invention are illustrative only and are not intended to limit the scope of the present invention.

WHAT IS CLAIMED IS:

1. A method of writing a display image to a display having an array of pixels, the method comprising:

receiving image data;

deriving a row-addressing order based at least in part on at least some of the stored image data; and

writing the display image to the display by addressing rows in the array of pixels according to the row-addressing order.

2. The method of Claim 1, wherein the received image data is stored in a frame buffer, and wherein the row-addressing order is derived from an attribute of one or more rows of the image data stored in the frame buffer.

3. The method of Claim 2, wherein the display is a bi-stable display comprising an array of pixels, said pixels having an actuated state and an un-actuated state.

4. The method of Claim 3, wherein the pixels in the array comprise interferometric modulator pixels.

5. The method of Claim 3, wherein one or more row attributes for the one or more rows is derived from a count of actuated pixels and a count of un-actuated pixels in that row.

6. The method of Claim 3, wherein one or more row attributes for the one or more rows is derived from a ratio of actuated pixels to un-actuated pixels in a sub-row of the row.

7. The method of Claim 2, further comprising:

prior to creating the display image on the display, sorting the one or more attributes into a numerical order.

8. The method of Claim 7, wherein creating the display image on the display comprises addressing the rows in the display according to the numerical order.

9. A method of determining a row-addressing order for an image comprising:

determining one or more row attributes for one or more rows of the data in the image; and

determining, based one or more row attributes, the row-addressing order.

10. The method of Claim 9, further comprising:

embedding the row-addressing order in an image file.

11. The method of Claim 10, wherein determining the row attributes comprises calculating a ratio of pixels in a first display state to pixels in a second display state for each of the one or more rows of data in the image.

12. The method of Claim 11, wherein determining the row-addressing order comprises sorting the determined row attributes.

13. The method of Claim 12, wherein the image is displayed on a bi-stable display comprising an array of pixels, said pixels having an actuated state and an un-actuated state.

14. The method of Claim 13, wherein the pixels in the array comprise interferometric modulators.

15. A method of displaying an image on a display comprising:

receiving an image data file, the image data file including a row-addressing order; and

creating the display image on the display by addressing the rows on the display according to the row-addressing order.

16. A display apparatus comprising:

a memory storing image data;

a processor configured to receive said image data and calculate a row-addressing order based on a row attribute for one or more rows of the image data; and

a controller configured to present the image data to a display on a row-by-row basis according to the calculated row-addressing order.

17. The display apparatus of Claim 16, wherein the memory is a frame buffer.

18. The display apparatus of Claim 16, wherein the row attribute is the number of released pixels in the rows of the image data.

19. The display apparatus of Claim 16, wherein the row attribute comprises a first value for a first part of the row and a second value for a second part of the row.

20. The display apparatus of Claim 16, wherein the first part of the row is a left half of the row, and the second part of the row is a right half of the row.

21. The display apparatus of Claim 16, wherein the processor is further configured to store the calculated row-addressing order in the memory.

22. The display apparatus of Claim 16, further comprising:

a processor that is configured to communicate with said display, said processor being configured to process image data; and

a memory device that is configured to communicate with said processor.

23. The display apparatus as recited in Claim 22, further comprising a driver circuit configured to send at least one signal to said display. .

24. The apparatus as recited in Claim 22, further comprising a controller configured to send at least a portion of said image data to said driver circuit.

25. The apparatus as recited in Claim 22, further comprising an image source module configured to send said image data to said processor.

26. The apparatus as recited in Claim 25, wherein said image source module comprises at least one of a receiver, transceiver, and transmitter.

27. The apparatus as recited in Claim 22, further comprising an input device configured to receive input data and to communicate said input data to said processor.

28. A display apparatus comprising:

means for receiving image data;

means for deriving an addressing order based at least in part on one or more attributes of the image data; and

means for presenting the processed image data to a display in accordance with the derived addressing order.

29. The display apparatus of Claim 28, wherein the storing means is a frame buffer.

30. The display apparatus of Claim 28, wherein the processing means comprises a system processor.

31. The display apparatus of Claim 28, wherein the processing means comprises a driver controller.

32. The display apparatus of Claim 28, wherein the presenting means comprises an array driver.

33. A system for displaying data on an array of interferometric modulators comprising:

a server configured to calculate an addressing order for image data,; and

a client device comprising a display and configured to receive the image data and the calculated addressing order from the server, and to display the image data on the array by addressing the array according to the addressing order.

34. The system of Claim 33, wherein the addressing order is a row-addressing order.

35. The system of Claim 33, wherein the addressing order is a pixel-addressing order.

36. The system of Claim 33, wherein the server if further configured to embed the calculated addressing order in the image data.

37. The system of Claim 36, wherein the calculated addressing order is embedded in an image header for the image data.

38. The system of Claim 36, wherein the calculated addressing order is embedded in a body of the image data.

39. The system of Claim 33, wherein the server is a headend system in a telecommunications network.

40. A computer-readable medium having computer-executable instructions stored thereon which, when executed cause a computing device to perform a method of displaying an image on a display comprising:

receiving an image data file, the image data file including a row-addressing order; and

creating the display image on the display by addressing the rows on the display according to the row-addressing order.

41. A computer-readable medium having computer-executable instructions stored thereon which, when executed cause a computing device to perform a method of writing a display image to a display having an array of pixels, the method comprising:

receiving image data;

deriving a row-addressing order based at least in part on at least some of the stored image data; and

writing the display image to the display by addressing rows in the array of pixels according to the row-addressing order.

42. The computer-readable medium of Claim 41, wherein the received image data is stored in a frame buffer, and wherein the row-addressing order is derived from an attribute of one or more rows of the image data stored in the frame buffer.

43. The computer-readable medium of Claim 42, wherein the display is a bi-stable display comprising an array of pixels, said pixels having an actuated state and an un-actuated state.

44. The computer-readable medium of Claim 43, wherein the pixels in the array comprise interferometric modulator pixels.

45. The computer-readable medium of Claim 43, wherein one or more row attributes for the one or more rows is derived from a count of actuated pixels and a count of un-actuated pixels in that row.

46. The computer-readable medium of Claim 43, wherein one or more row attributes for the one or more rows is derived from a ratio of actuated pixels to un-actuated pixels in a sub-row of the row.

47. The computer-readable medium of Claim 42, further comprising:

prior to creating the display image on the display, sorting the one or more attributes into a numerical order.

48. The computer-readable medium of Claim 47, wherein creating the display image on the display comprises addressing the rows in the display according to the numerical order.

49. A computer-readable medium having computer-executable instructions stored thereon, which when executed cause a computing device to perform a method of determining a row-addressing order for an image comprising:

determining one or more row attributes for one or more rows of the data in the image; and

determining, based one or more row attributes, the row-addressing order.

50. The computer-readable medium of Claim 49, further comprising:

embedding the row-addressing order in an image file.

51. The computer-readable medium of Claim 50, wherein determining the row attributes comprises calculating a ratio of pixels in a first display state to pixels in a second display state for each of the one or more rows of data in the image.

52. The computer-readable medium of Claim 51, wherein determining the row-addressing order comprises sorting the determined row attributes.

53. The computer-readable medium of Claim 53, wherein the image is displayed on a bi-stable display comprising an array of pixels, said pixels having an actuated state and an un-actuated state.

54. The computer-readable medium of Claim 53, wherein the pixels in the array comprise interferometric modulators.

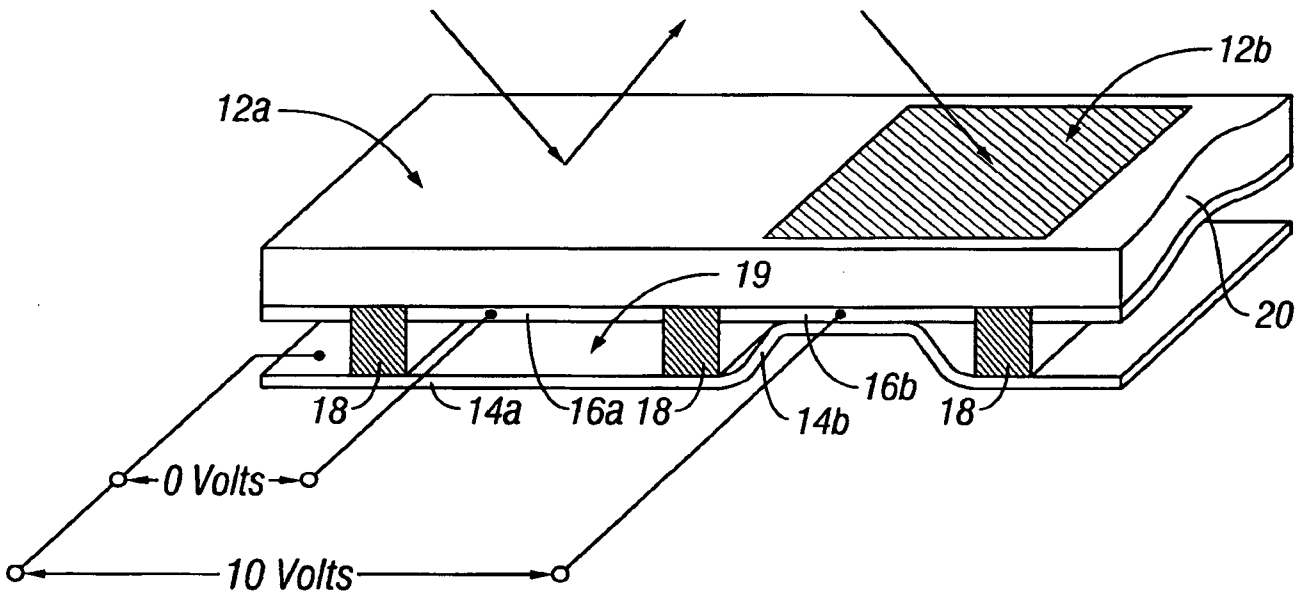


FIG. 1

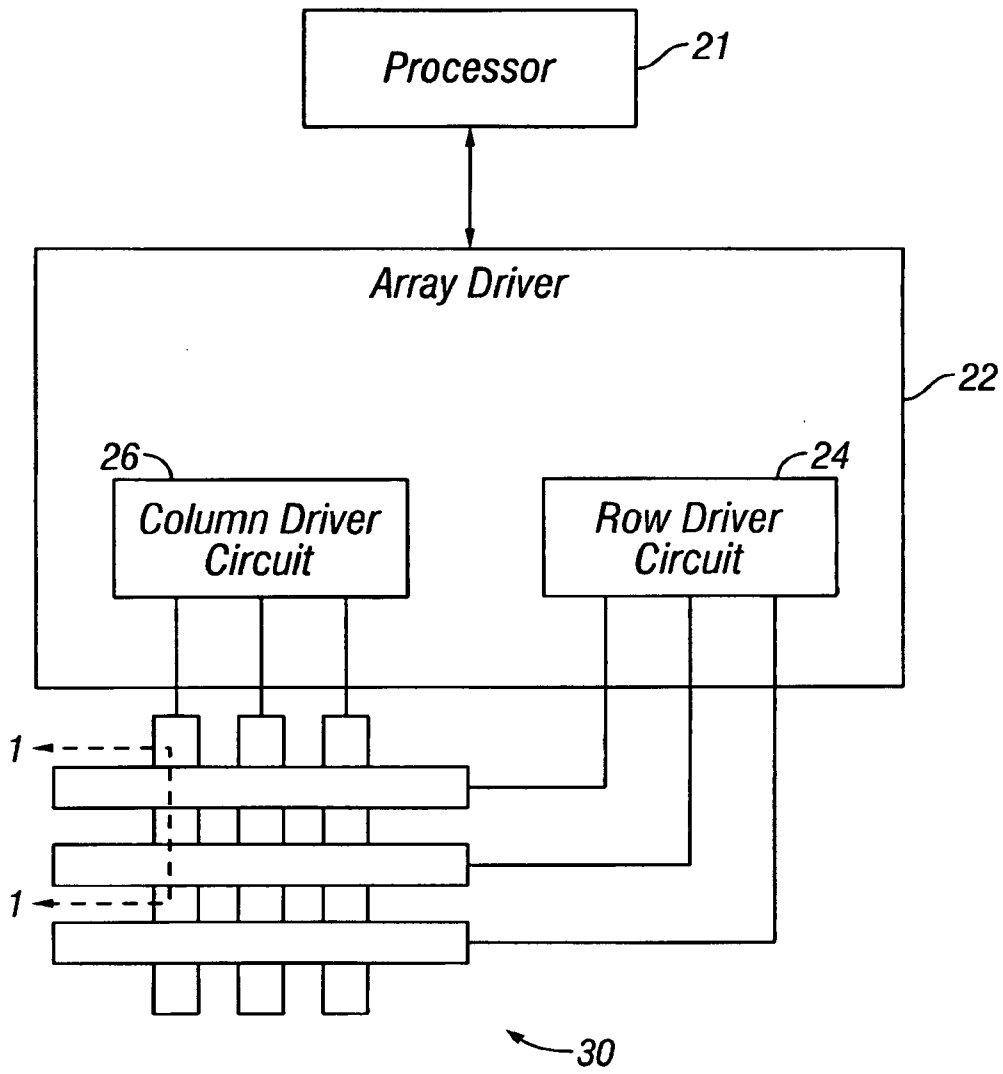

Processor
21
Array Driver
22
26
Column Driver Circuit
24
Row Driver Circuit
1
1
30

FIG. 2

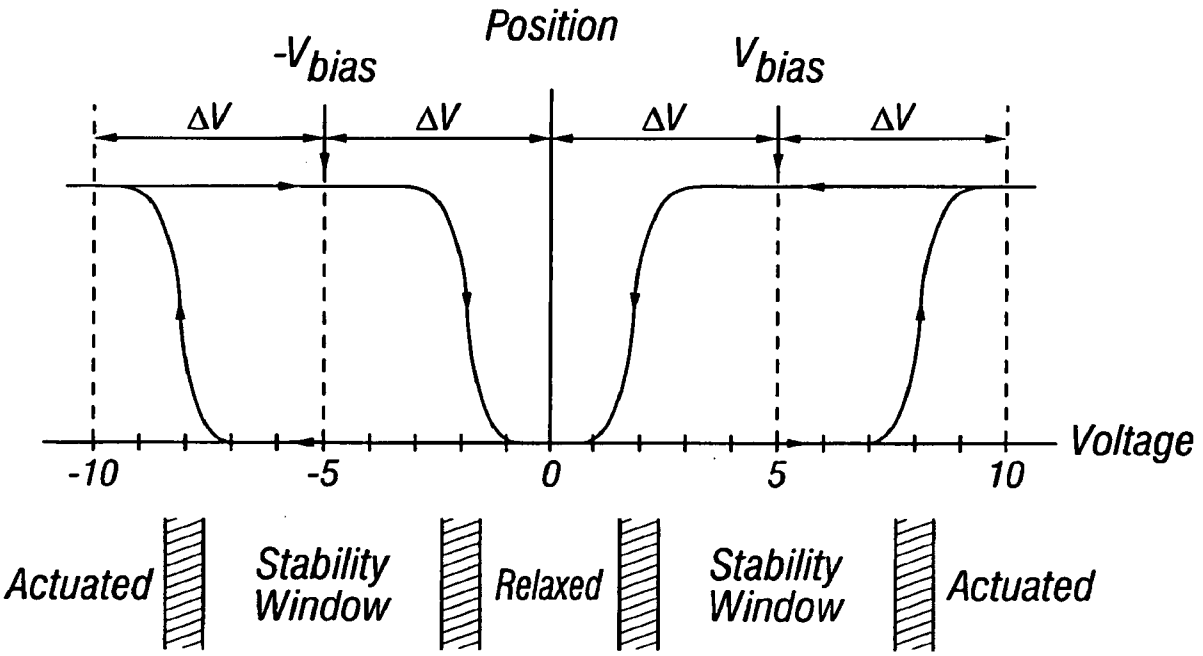


FIG. 3

Row Output Signals	Column Output Signals: $+V_{bias}$	Column Output Signals: $-V_{bias}$
0	Stable	Stable
$+\Delta V$	Relax	Actuate
$-\Delta V$	Actuate	Relax

FIG. 4

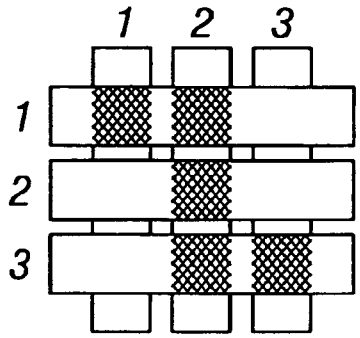

1
2
3
1
2
3

FIG. 5A

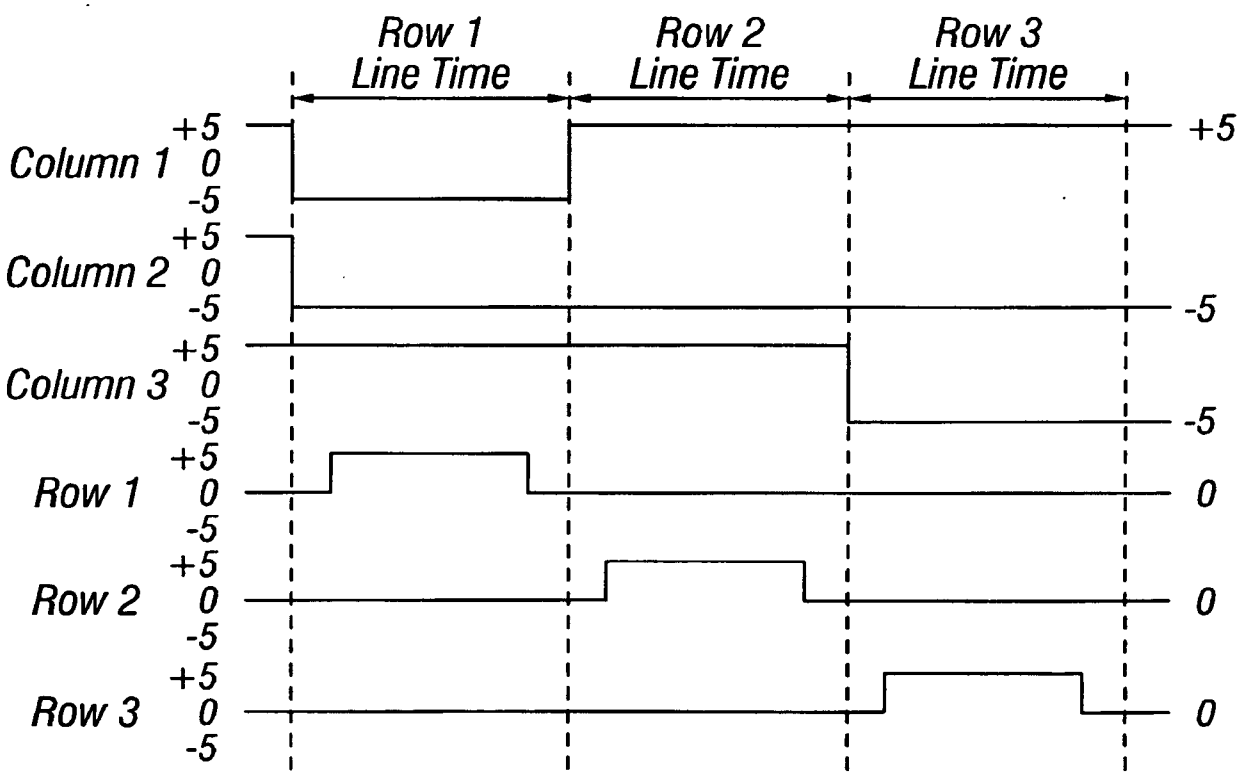

Row 1 Line Time
Row 2 Line Time
Row 3 Line Time
Column 1
Column 2
Column 3
Row 1
Row 2
Row 3
+5
0
-5
+5
-5
-5
0
0
0

FIG. 5B

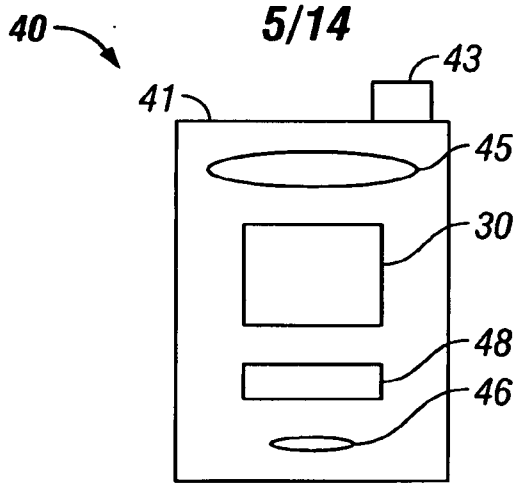

40
41
43
45
30
48
46

FIG. 6A

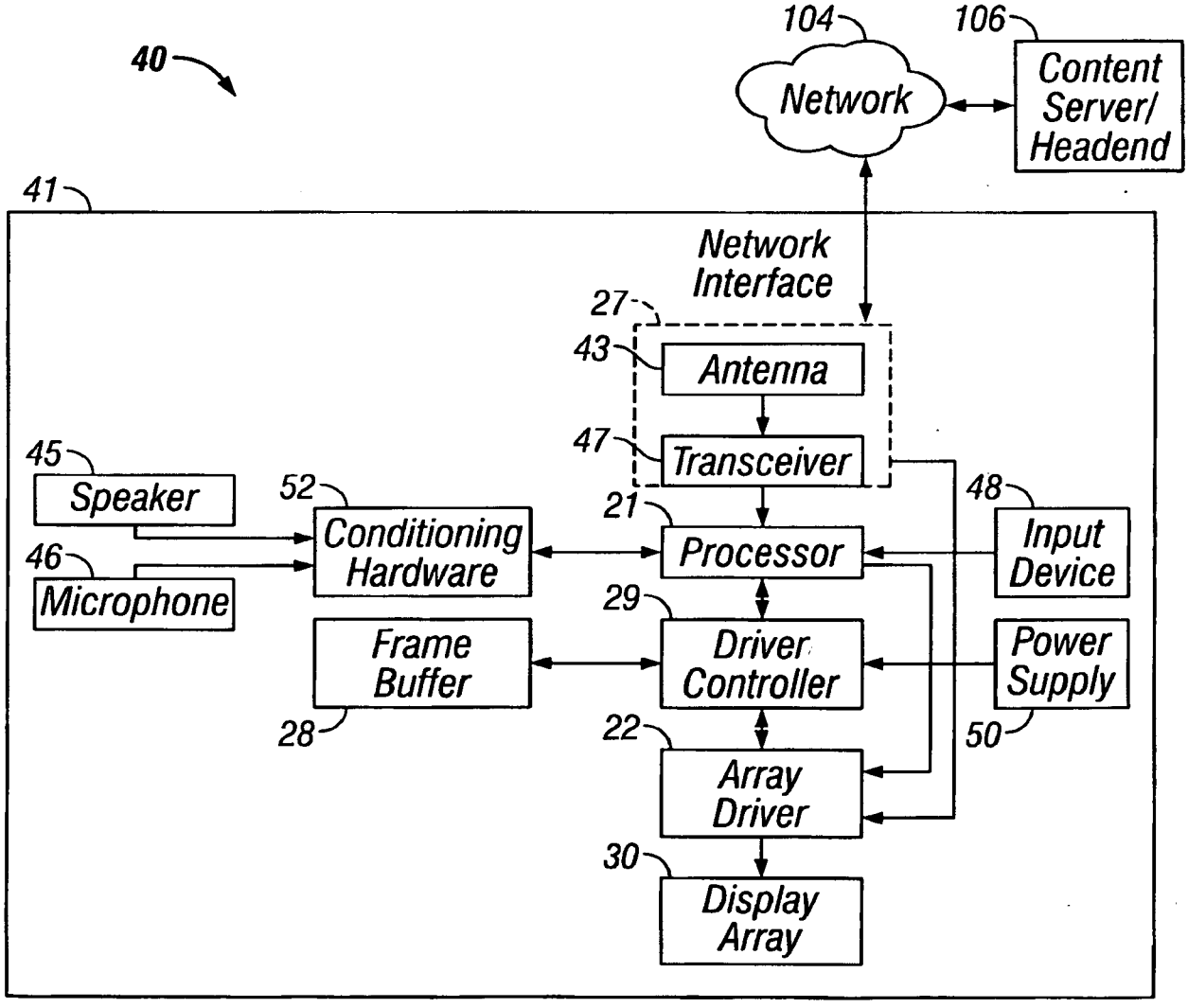

40
104
106
Network
Content Server/ Headend
41
Network Interface
27
43
Antenna
47
Transceiver
45
Speaker
52
Conditioning Hardware
21
48
Input Device
46
Microphone
Processor
29
Frame Buffer
Driver Controller
Power Supply
28
22
50
Array Driver
30
Display Array

FIG. 6B

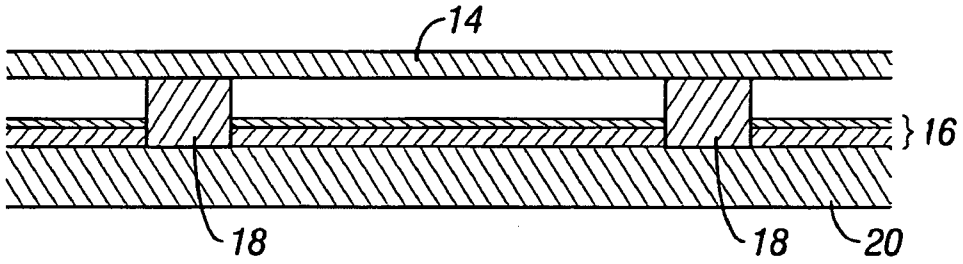


FIG. 7A

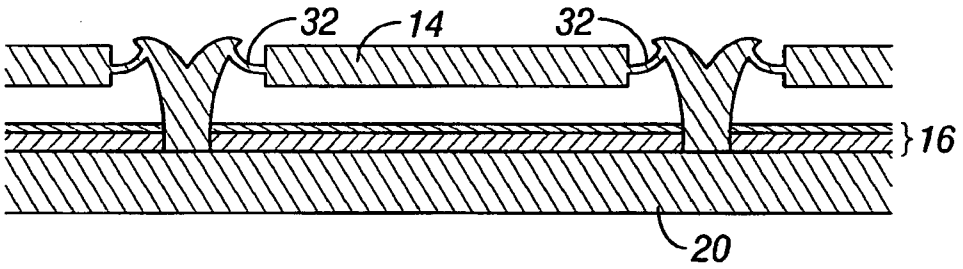


FIG. 7B

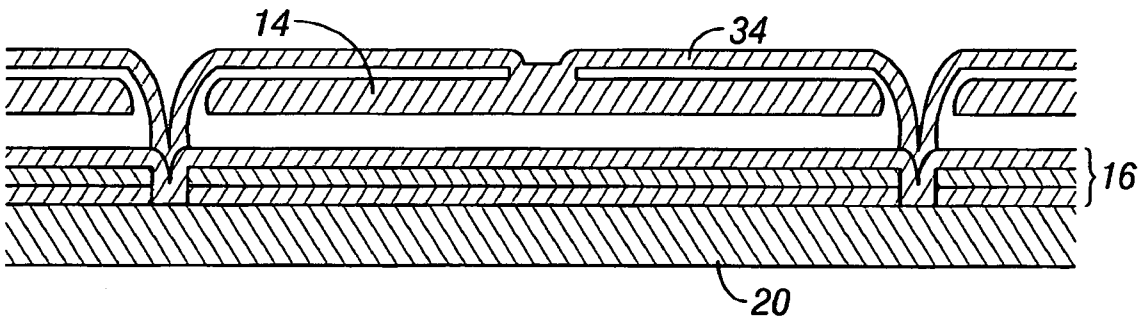


FIG. 7C

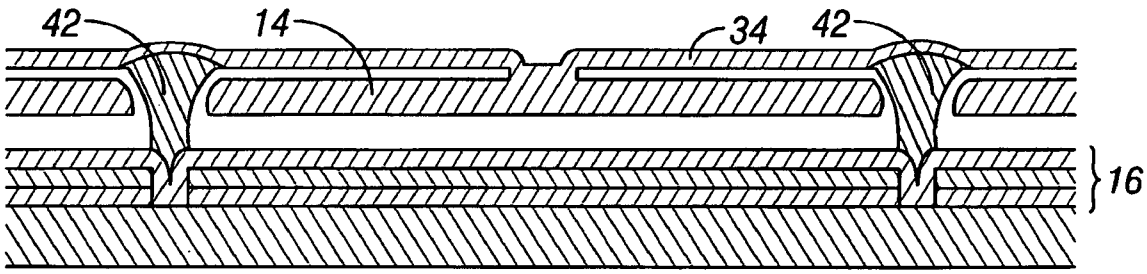


FIG. 7D

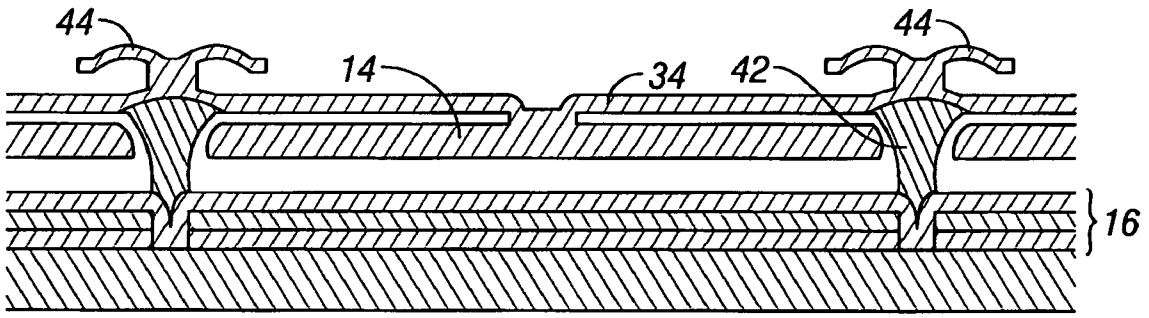


FIG. 7E

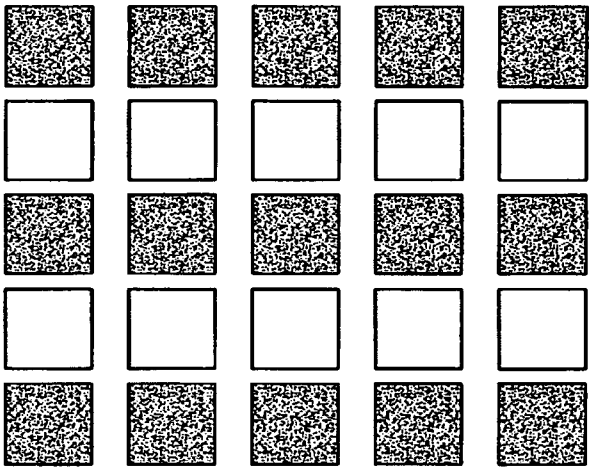


FIG. 8A

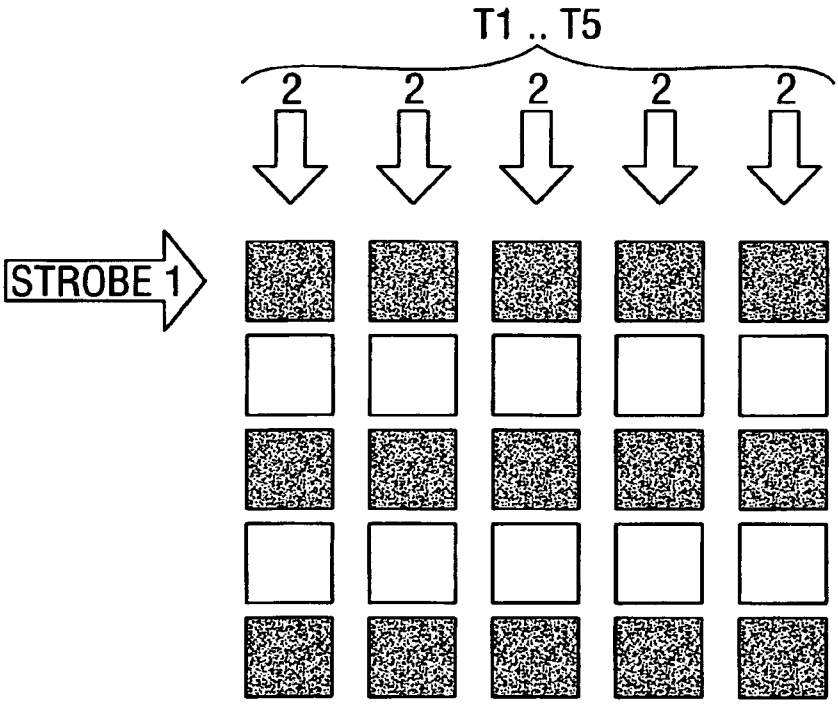


FIG. 8B
(Prior Art)

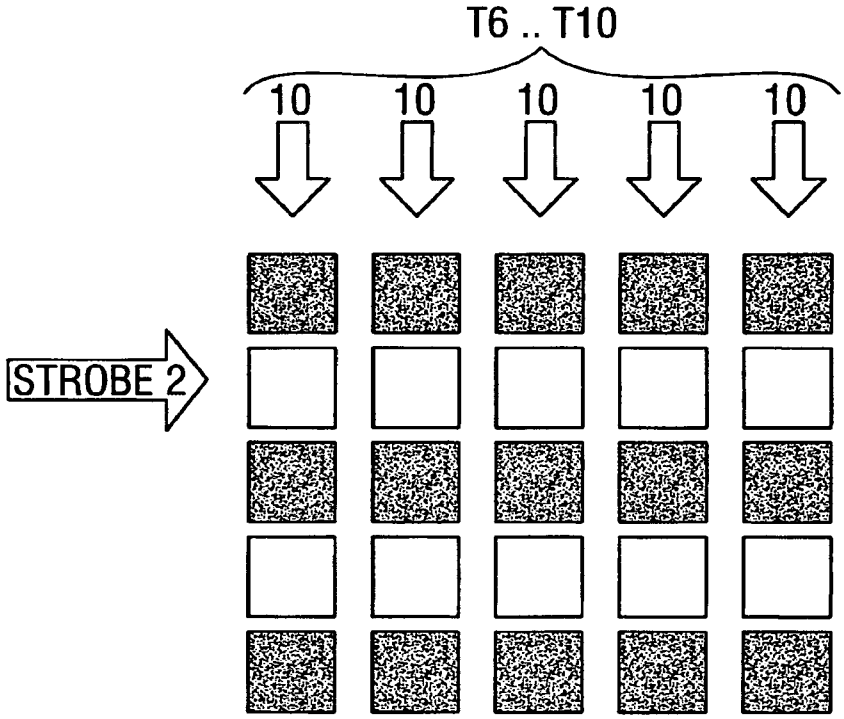


FIG. 8C
(Prior Art)

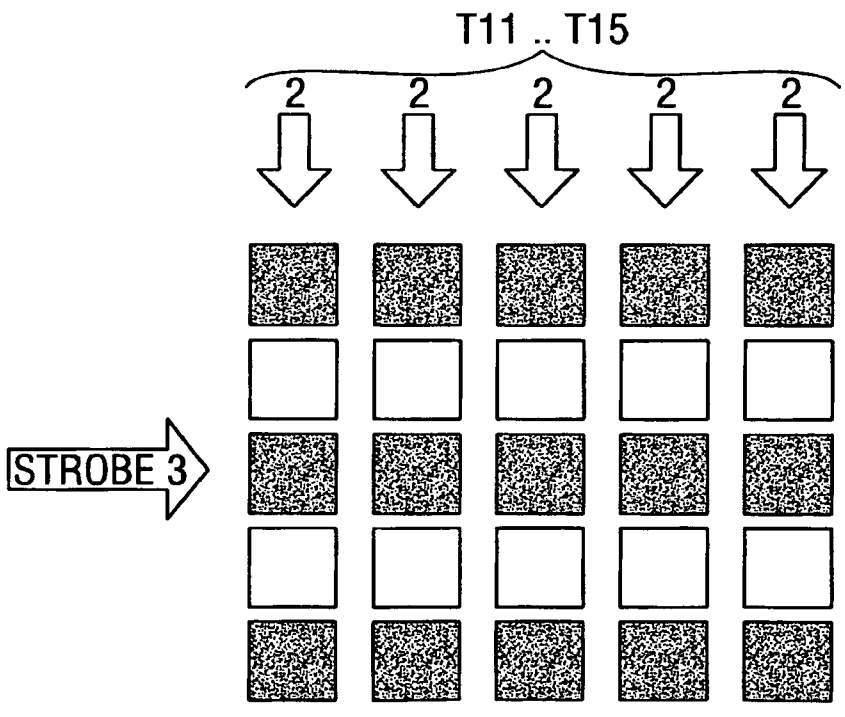


FIG. 8D
(Prior Art)

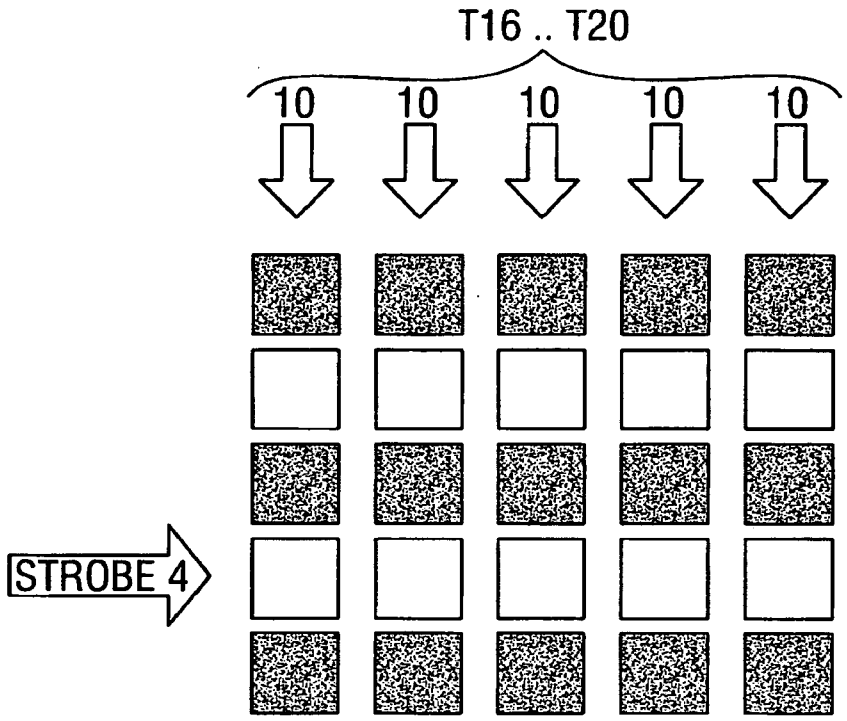


FIG. 8E
(Prior Art)

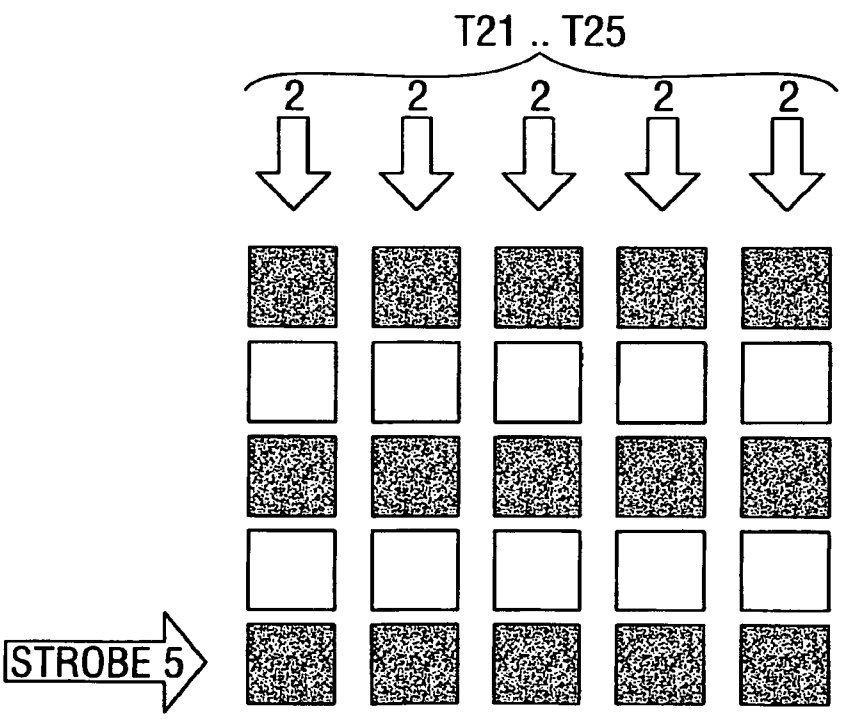


FIG. 8F
(Prior Art)

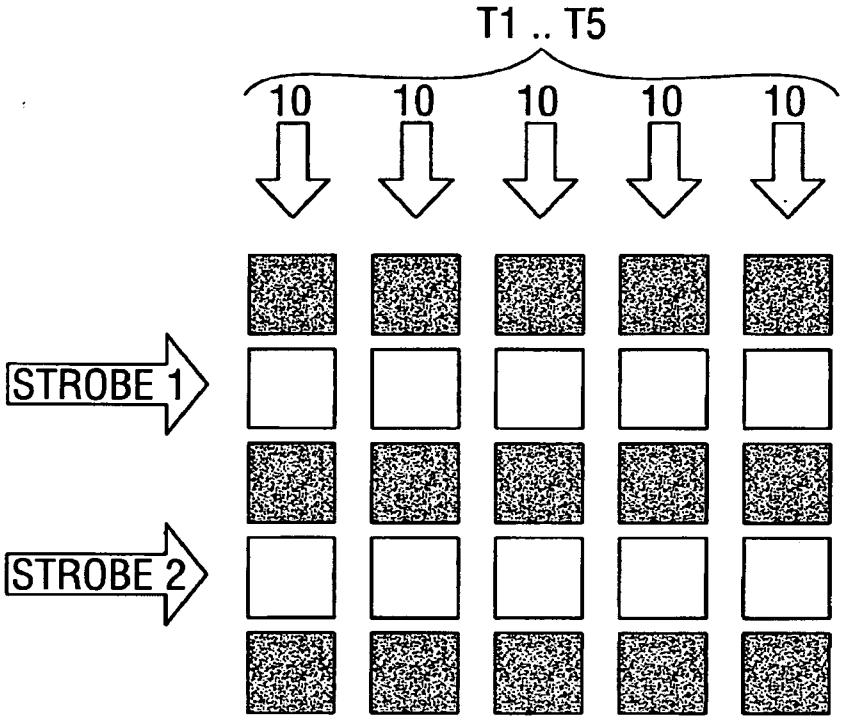

T1 .. T5
10
10
10
10
10
STROBE 1
STROBE 2

FIG. 9A

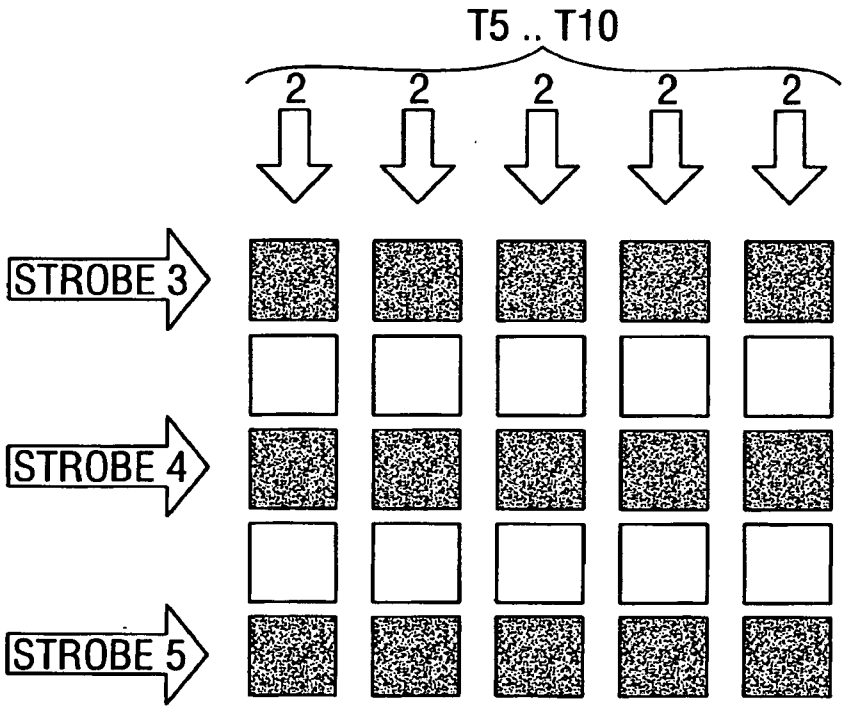

T5 .. T10
2
2
2
2
2
STROBE 3
STROBE 4
STROBE 5

FIG. 9B

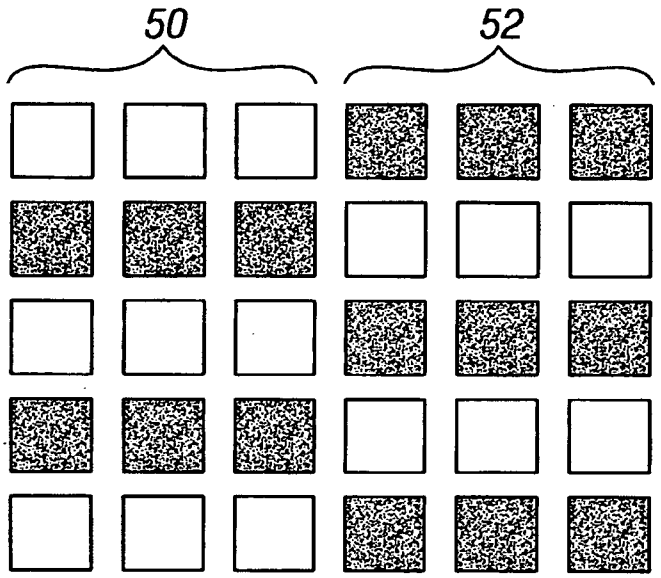


FIG. 10A

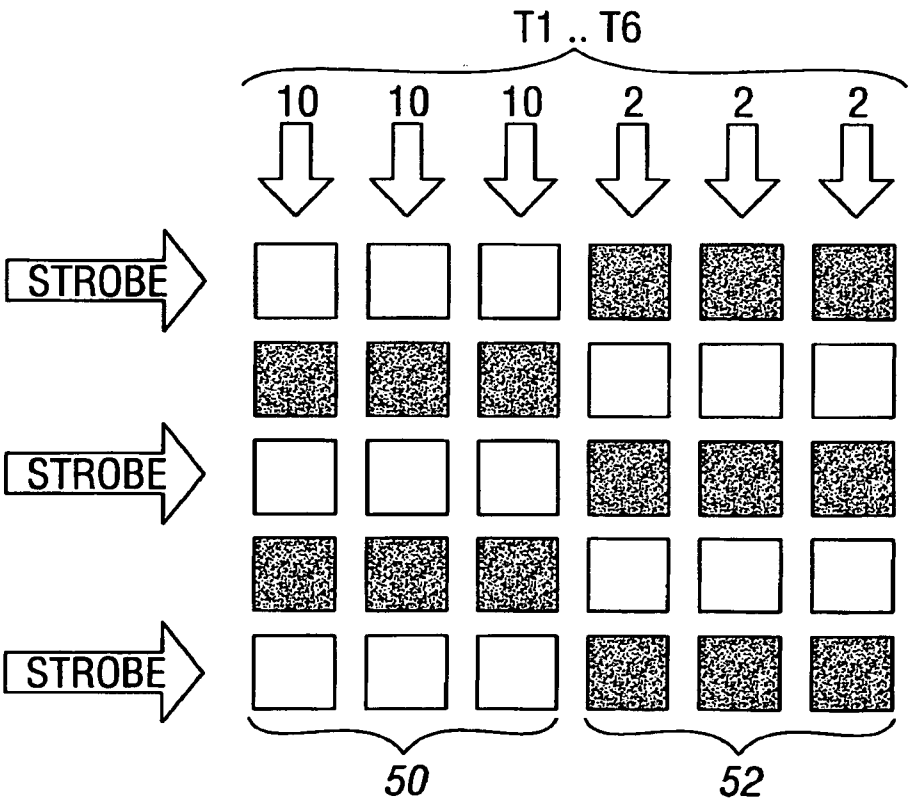


FIG. 10B

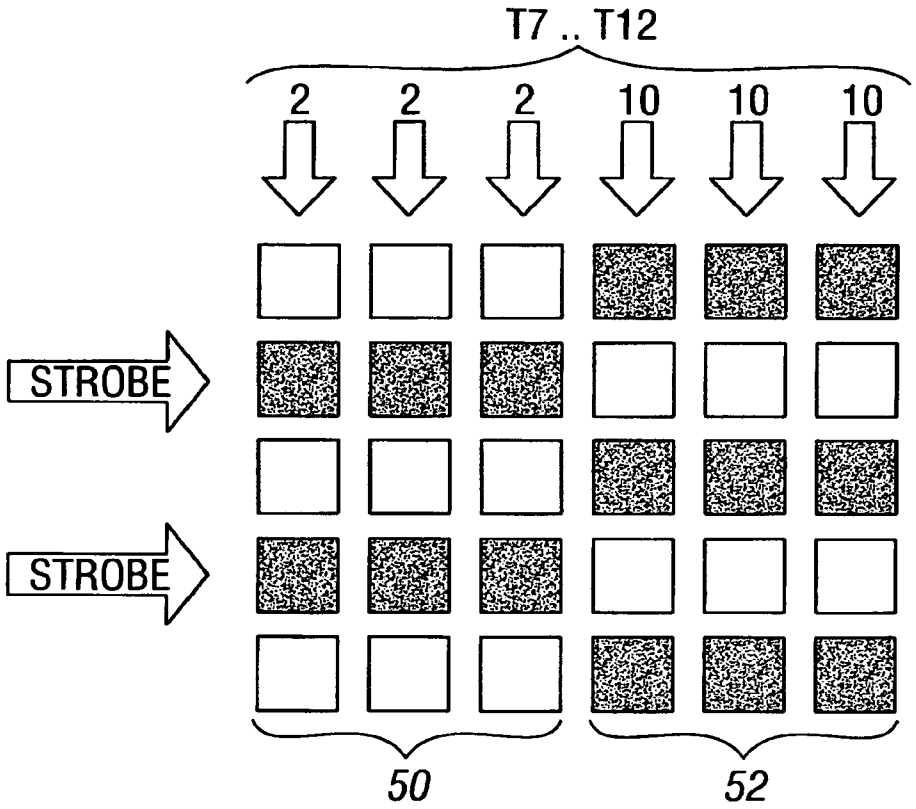


FIG. 10C

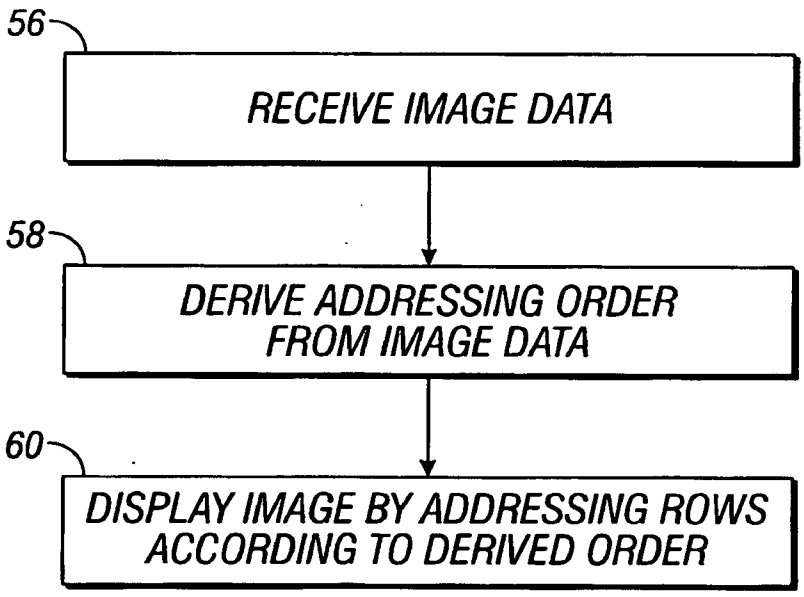


FIG. 11

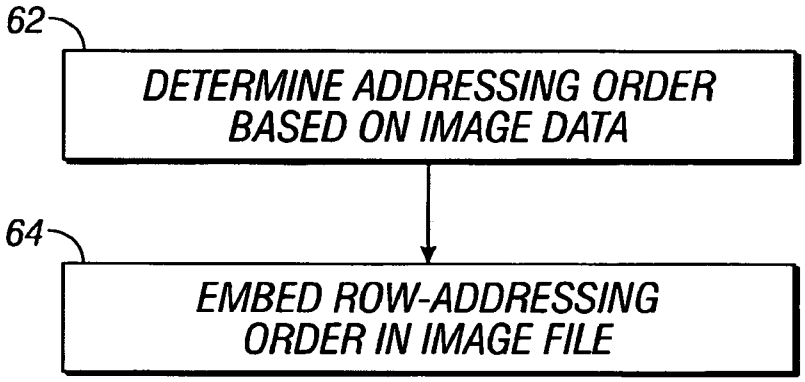

62
DETERMINE ADDRESSING ORDER BASED ON IMAGE DATA
64
EMBED ROW-ADDRESSING ORDER IN IMAGE FILE

FIG. 12

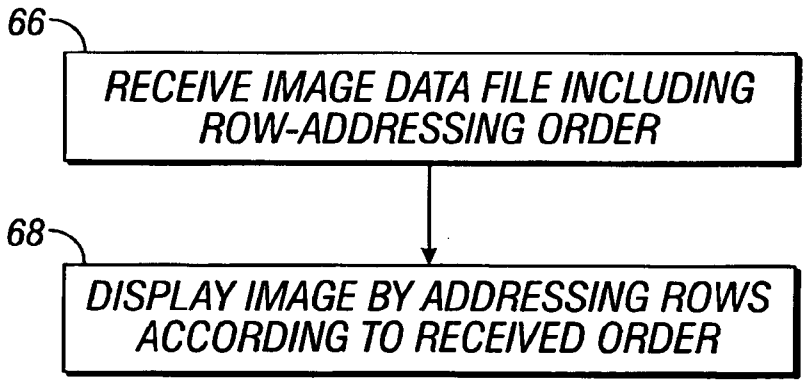

66
RECEIVE IMAGE DATA FILE INCLUDING ROW-ADDRESSING ORDER
68
DISPLAY IMAGE BY ADDRESSING ROWS ACCORDING TO RECEIVED ORDER

FIG. 13

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2007/009333

A. CLASSIFICATION OF SUBJECT MATTER
INV. G09G3/34 G09G3/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 01/82284 A (ULTRACHIP INC [US]; LIANG JEMM YUE [US]; XIAO PETER [US]) 1 November 2001 (2001-11-01)	1-9, 16-18, 21-35, 40-49
Y	abstract; figures 2,3 page 2, line 13 - page 2, line 28 page 5, lines 10-14 page 8, line 6 - page 13, line 32	39
X	EP 1 414 011 A (ST MICROELECTRONICS SRL [IT]; DORA S P A [IT]) 28 April 2004 (2004-04-28)	1-9, 16-18, 21-35, 40-49
Y	abstract; figures 1,2 paragraphs [0003], [0006], [0007], [0009] - [0011], [0013] - [0016], [0029] - [0031]	39

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 September 2007	27/09/2007

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Fulcheri, Alessandro

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2007/009333

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 07 064512 A (SHARP KK) 10 March 1995 (1995-03-10) abstract -----	1-9, 16-18, 21-35, 40-49
Y	EP 1 640 953 A (IDC LLC [US]) 29 March 2006 (2006-03-29) abstract; figure 7 -----	39

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2007/009333

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