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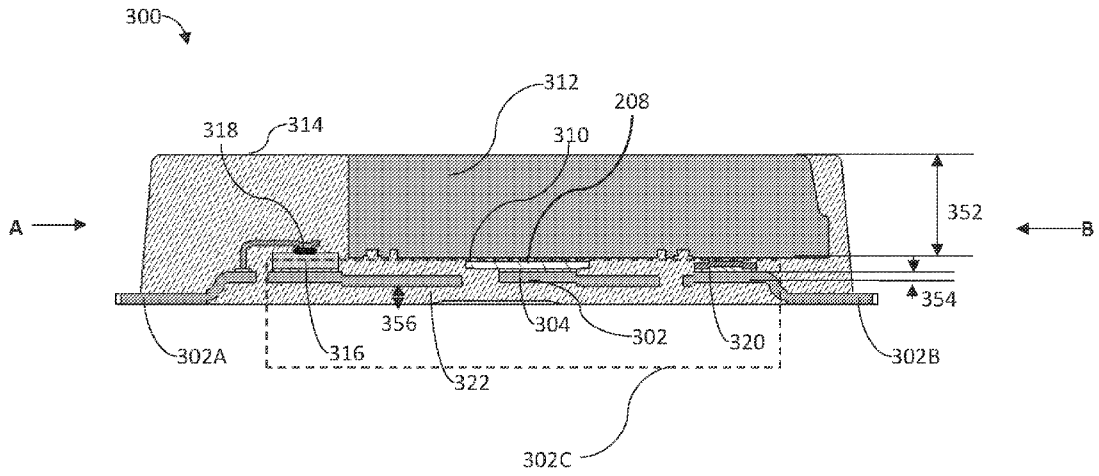

FIG. 3A

(57) Abstract: The present disclosure relates to a semiconductor package. The semiconductor package includes a semiconductor die having a first side and a second side, the second side being opposite to the first side, a lead frame one the first side of the semiconductor die, and a heat spreader on the second side of the semiconductor die. The lead frame is embedded in a molding material. The heat spreader has a thickness greater than a thickness of the lead frame to dissipate heat associated with a power surge through the heat spreader.

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SEMICONDUCTOR DEVICE PACKAGE WITH IMPROVED COOLING

[0001] This application claims the benefit of U.S. Provisional Patent Application No. 63/511,826, entitled "SEMICONDUCTOR DEVICE PACKAGE WITH IMPROVED COOLING," filed on July 3, 2023, the disclosure of which is hereby incorporated by reference in its entirety and for all purposes.

BACKGROUND

Technical Field

[0002] This application relates to semiconductor device packages. In particular, some embodiments relate to a semiconductor package with a cooling structure on one side of a semiconductor die and a molding material filled within the semiconductor package.

Description of Related Technology

[0003] Semiconductor devices are used in a wide variety of applications. In some applications, semiconductor devices can experience high electrical loads that can result in significant heating of the semiconductor device. There may be technical problems associated with high electrical loads, such as detrimental heating of the semiconductor device from the high load. In addition, such significant heating generated from the semiconductor die can cause thermal stress on a carrier, such as a printed circuit board, which integrates the semiconductor device.

SUMMARY

[0004] The innovations described in the claims each have several aspects, no single one of which is solely responsible for its desirable attributes. Without limiting the scope of the claims, some prominent features of this disclosure will now be briefly described.

[0005] One aspect of the present disclosure is a packaged integrated circuit device with power surge heat dissipation. The packaged integrated circuit device includes a semiconductor die having a first side and a second side that the second side is being opposite to the first side, a lead frame on the first side of the semiconductor die that the lead frame is

embedded in a molding material, and a heat spreader on the second side of the semiconductor die that the heat spreader has a thickness of at least 2.5 millimeters.

[0006] In one embodiment, the heat spreader and the lead frame can be configured to maintain the semiconductor die at a temperature of less than 200 degrees Celsius when subjected to a surge load of up to 160 Watts for 1 second from a steady state.

[0007] In one embodiment, the thickness of the heat spreader can be at least four times a thickness of the semiconductor die. An area of the heat spreader can be greater than an area of the semiconductor die, and the heat spreader can be extended beyond the semiconductor die. In addition, the thickness of the heat spreader can be between four and twenty times the thickness of the semiconductor die.

[0008] In one embodiment, the thickness of the heat spreader can be at least 2.5 times a thickness of the lead frame.

[0009] In one embodiment, the packaged integrated circuit device can have a recess in the molding material on a side of the packaged integrated circuit device that is opposite to the heat spreader.

[0010] In one embodiment, the lead frame and the heat spreader can both be joined to the semiconductor die.

[0011] In one embodiment, the semiconductor die can include a field effect transistor. In addition, the field effect transistor can be a gallium nitride field effect transistor.

[0012] In one embodiment, the lead frame can include a main frame, and a plurality of leads can be extended from the main frame. In addition, each lead of the plurality of leads can be flat outside of the molding material. In addition, each lead of the plurality of leads can include a wettable flank.

[0013] In one embodiment, the heat spreader can be a solid layer that can include a copper.

[0014] In one embodiment, the heat spreader can be a multi-layer structure that can include a first metal layer, a second metal layer, and a ceramic layer positioned between the first metal layer and the second metal layer.

[0015] Another aspect of the present disclosure is an integrated circuit assembly with power surge heat dissipation. The integrated circuit assembly includes a printed circuit board, a packaged integrated circuit device on the printed circuit board that includes a

semiconductor die, a lead frame positioned between the semiconductor die and the printed circuit board, and a heat spreader positioned on an opposite side of the semiconductor die than the lead frame, and a cooling structure in thermal contact with the heat spreader. The heat spreader has a thickness of at least 2.5 millimeters.

[0016] In one embodiment, the packaged integrated circuit device can include molding material or other separator to provide electrical and/or thermal insulation between the printed circuit board and the lead frame. In addition, the packaged integrated circuit device can have a recess in the molding material on a side facing the printed circuit board.

[0017] In one embodiment, the packaged integrated circuit device can further include a second packaged integrated circuit device on the printed circuit board, and the second packaged integrated circuit device can include a second heat spreader in thermal contact with the cooling structure.

[0018] In one embodiment, the cooling structure can include a heatsink and/or a cold plate.

[0019] Another aspect of the present disclosure is a packaged integrated circuit device with power surge heat dissipation. The packaged integrated circuit device includes a semiconductor die having a first side and a second side that the second side is being opposite to the first side, a lead frame on the first side of the semiconductor die that the lead frame is embedded in a molding material, and a cooling structure on the second side of the semiconductor die that the cooling structure includes two metal layers and a ceramic layer positioned between the two metal layers. The semiconductor die includes a field effect transistor. In addition, a thickness of the cooling structure is greater than 2.5 millimeters.

[0020] For purposes of summarizing the disclosure, certain aspects, advantages, and novel features of the innovations have been described herein. It is to be understood that not necessarily all such advantages may be achieved in accordance with any particular embodiment. Thus, the innovations may be embodied or carried out in a manner that achieves or optimizes one advantage or group of advantages as taught herein without necessarily achieving other advantages as may be taught or suggested herein.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] Some features, aspects, and advantages of the disclosure are described with reference to drawings of certain embodiments, which are intended to illustrate, but not to limit, the present disclosure. It is to be understood that the accompanying drawings, which are incorporated in and constitute a part of this specification, are for the purpose of illustrating concepts disclosed herein and may not be to scale.

[0022] FIG. 1A is a plot of temperature versus time for a packaged integrated circuit (IC) device according to some embodiments.

[0023] FIG. 1B includes heat maps of temperature distributions in a conventional packaged IC device and in a packaged device according to some embodiments.

[0024] FIG. 2 is a schematic cross-sectional diagram of an example of a packaged IC device that utilizes dual-sided cooling according to some embodiments.

[0025] FIG. 3A is a schematic cross-sectional diagram of an example of a packaged IC device that uses single-sided cooling according to some embodiments.

[0026] FIG. 3B is a schematic plan view of an example of electrical paths through the packaged IC device of FIG. 3A.

[0027] FIG. 4 is a schematic cross-sectional diagram of a semiconductor die connected on a first side to a heat slug with solder and connected to a printed circuit board (PCB) facing lead frame with solder on a second side opposite the first side.

[0028] FIG. 5 is a schematic cross-sectional diagram of an example of a surface mount device that is mounted on a printed circuit board according to some embodiments.

[0029] FIG. 6 is a schematic cross-sectional diagram of an example embodiment of a packaged IC device that includes a local recess.

[0030] FIG. 7 shows a bottom perspective view of a packaged IC device that includes a local recess according to some embodiments.

[0031] FIG. 8 is a schematic cross-sectional diagram of an example embodiment of an IC assembly that includes multiple packaged IC devices according to some embodiments.

[0032] FIGS. 9A, 9B, and 9C are schematic cross-sectional diagrams of different cross-sections of an example embodiment of a packaged IC device that includes a multi-layer cooling structure according to some embodiments.

[0033] FIG. 10A is a schematic diagram of an example of three dimensional view of the packaged IC device of FIG. 9A.

[0034] FIG. 10B is an exploded view of the packaged IC device of FIG. 10A.

[0035] FIG. 11A is a schematic cross-sectional diagram of an example embodiment of a packaged IC device that includes an example cooling structure according to some embodiments.

[0036] FIG. 11B is a schematic cross-sectional diagram of an example embodiment of a packaged IC device that includes an example cooling structure according to some other embodiments.

[0037] FIG. 12 is a schematic diagram of an example exploded view of the packaged IC device of FIG. 11B.

[0038] FIG. 13 is a schematic cross-sectional diagram of an example embodiment of a packaged IC device that includes an example cooling structure and lead frame according to some other embodiments.

[0039] FIG. 14 is a schematic cross-sectional diagram of an example embodiment of a packaged IC device that includes an example cooling structure and lead frame according to some other embodiments.

[0040] FIGS. 15A, 15B, and 15C illustrate various examples of cooling structures according to some other embodiments.

DETAILED DESCRIPTION OF CERTAIN EMBODIMENTS

[0041] The following detailed description of certain embodiments presents various descriptions of specific embodiments. However, the innovations described herein can be embodied in a multitude of different ways, for example, as defined and covered by the claims. In this description, reference is made to the drawings where like reference numerals and/or terms can indicate identical or functionally similar elements. It will be understood that elements illustrated in the figures are not necessarily drawn to scale. Moreover, it will be understood that certain embodiments can include more elements than illustrated in a drawing and/or a subset of the elements illustrated in a drawing. Further, some embodiments can incorporate any suitable combination of features from two or more drawings. The headings

provided herein are for convenience only and do not necessarily affect the scope or meaning of the claims.

Introduction

[0042] Electronic components containing one or more integrated circuit (IC) dies can be deployed in a wide variety of applications. For example, such components may form part of a power electronics system. In some cases, such power electronics systems may be used for providing power for heating, ventilation, and air conditioning (HVAC) systems, an electric vehicle, or as part of a stationary energy storage system, such as a system for storing solar energy, or for other applications where there is a need for power delivery. For example, in an electric vehicle, such systems can be used to convert alternating current to direct current for charging or from direct current to alternating current to provide power output. A power electronics system can be used, for example, to convert direct current from a solar panel or battery to alternating current. In some cases, such power electronics systems can be used in utility applications, such as a grid-tie inverter that converts direct current to alternating current for insertion into an electrical power grid. There are many other applications for such systems. In some cases, components may comprise diode switches, field effect transistors (FETs) such as metal-oxide-semiconductor field effect transistors (MOSFETs) (e.g., gallium nitride (GaN) MOSFETs), insulated-gate bipolar transistors (IGBTs), other bipolar transistors, the like, or any suitable combination thereof. In certain applications, such switches can be included in an inverter that converts a direct current (DC) voltage to an alternating current (AC) voltage. These components may have significant heat output when operational.

[0043] Electronics systems, such as power electronic systems, can produce significant amounts of heat under both steady state load conditions and under surge conditions. Such heat can present significant problems. For example, excess heat can lead to one or more of component damage, reduced lifetime, lower reliability, decreased performance, or the like. For example, heat can cause excessive thermal stresses on one or more components of electronic systems, causing weakened solder joints and/or damaged semiconductor components. In some applications, power surge loads may result in rapid temperature rises. High power surge loads may be encountered in various applications, for example, when

starting portable compressors, HVAC systems, refrigeration systems, electric motors, power converters, or the like.

[0044] Even short power surge loads of about one half to one second can cause significant changes in the temperature of the electronic systems. Conventional cooling solutions may pose technical limitations to manage such rapid temperature rises (e.g., rapid heat generation) due to the power surge loads. Illustratively, a semiconductor die under steady-state operation can consume 18 Watts (W) and reach approximately 100°C when cooled using a traditional top-side heatsink. When a power surge load of 100 W is applied for one-half second, the die temperature can rise significantly. For example, after about 1 second, a die temperature can increase by about 100°C. In some implementations, a smaller die (e.g., a die with an area of about 9 squared millimeters (mm^2)) can experience a greater temperature increase than a larger die (e.g., a die with an area of about 24 mm^2). For example, after one second of the power surge, the die temperature can rise to about 200°C , about 220°C, or more, depending on the particular cooling solution provided in the conventional cooling solutions and also including additional factors, such as the die size, the package size, the package design, and so forth. In some cases, the semiconductor dies are attached directly to a lead frame or die paddle (which can operate as a heat spreader within a molded package). The package may be affixed with heatsinks, heat spreaders, cold plates, or the like to aid in dissipating heat. However, adding mass to a heat slug (e.g., by adding a pedestal on top of the heat slug or otherwise increasing the mass of the heat slug) and/or adding external heat spreaders may not significantly help to manage the semiconductor die temperatures during power surge conditions. Such semiconductor die package may lack good thermal contact with the added mass and thus may be unable to take advantage of the added thermal capacity in a short period of time. For example, in response to the power surge, the heat may not reach the heat slug, such that the heat may travel through a thermal interface material before reaching the heatsink, which may limit the rate of heat transfer, which can play a significant role in managing die temperatures during power surge loads.

[0045] In some cases, electronic components may be designed to operate under steady state conditions. For example, heat transfer materials inside an electronic component may be sized to manage heat dissipation under common load conditions. Such an approach can offer many advantages, such as minimizing size and reducing cost as less material may be

used. However, such approaches may not be suitable for certain types of use cases, such as managing large and/or power surge loads.

[0046] The electronic components may be designed to cool from one side, such as bottom cooled through a printed circuit board (PCB). However, heat conduction through the PCB may be inadequate for certain applications. In some cases of the heat conduction through the PCB, a coin comprising copper or another thermally conductive material may be embedded within the PCB under an electronic component to facilitate cooling. However, such an approach can add additional cost and complexity to the PCB and may reduce the density of components on the PCB. Moreover, power electronic systems can raise the temperature of the PCB assembly to temperatures in excess of 100°C, which can limit the flow of heat away from the electronic component via the PCB. Alternatively, in some cases, a PCB may be configured with holes that expose the bottom side of the IC and a heat sink or other thermal transfer apparatus may be in thermal contact with the bottom side of the IC through the hole. In some cases, top-sided cooling may be used to cool ICs, for example, as described in U.S. Patent No. 10,658,276, entitled "Device with top-side base plate," the disclosure of which is hereby incorporated by reference in its entirety and for all purposes.

[0047] Aspects of this disclosure relate to semiconductor packages with a cooling solution designed to effectively dissipate heat in various operational environments, such as large and/or sustained loads and also relatively short power surge loads. Thus, the cooling solutions disclosed herein are designed with a large thermal capacity and rapid heat transport (e.g., dissipation) capabilities. This disclosure describes examples of systems and techniques for providing solutions for effectively dissipating the heat in various operational environments, including power surges of relatively short durations. Such examples of the systems and techniques can be used without further modification or complicating the PCB design or component assembly processes. In some cases, such a cooling solution may be manufactured using established, efficient manufacturing methods.

[0048] In some embodiments of this disclosure, the PCB is used as a carrier of the semiconductor package. For example, various semiconductor components, including packaged IC devices can be mounted on the PCB. In some embodiments, applying the various cooling solutions and techniques of this disclosure can result in the PCB having a lower temperature than an integrated circuit (IC) package mounted to the PCB. In some embodiments, the PCB

can be utilized to aid the heat dissipation from the packaged IC device. In some embodiments, a lead frame can be affixed near the bottom surface of the packaged IC device. The lead frame can be used to provide electrical connections to a die and/or other components of the packaged IC device. The lead frame can, in some embodiments, be exposed or partially exposed, which can facilitate heat transfer from the packaged IC device to the PCB.

Packaged IC Devices with Power Surge Heat Dissipation

[0049] **FIG. 1A** illustrates temperature changes of a semiconductor die included in a packaged IC device, having heat dissipation structure (e.g., cooling structure) in accordance with embodiments disclosed herein. The heat dissipation structure or cooling structure, for example, can include a top side heat slug (also referred to herein as a die paddle or heat spreader) and an encapsulated lead frame in accordance with embodiments disclosed herein. A die paddle of in one or more embodiments of this disclosure can also be referred to as a heavy clip, a heat spreader, a heat slugger, a cooling solution, etc. Thus, any of the die paddles disclosed herein can be referred to as a heat spreader, heavy clip, heat slugger, or cooling solution. For embodiments of this disclosure, packaged IC devices can be manufactured with the die paddle mounted on a semiconductor die as a last or close to last step. This may be referred to as flipped die assembly. A front side of the semiconductor die can face downward to electrically bond to a lead frame and then the heavy clip can be assembled on the semiconductor die. As shown in FIG. 1A, a packaged IC device operating at a steady state at state region 102 and consuming about 35 W of power, can have the semiconductor die, operating at a temperature of about 116°C. When exposed to a surge load of about 160 W for a duration of about one second in a surge load region 104, the temperature of the semiconductor die can rise to about 212°C as indicated in FIG. 1A. When exposed to a surge load of about 160 W for a duration of about one second in a surge load region 104, the temperature of the semiconductor die can rise to about 188°C in some other applications. Either of these temperatures in both the steady state condition and the power surge condition provide significant heat management compared to the conventional methods.

[0050] **FIG. 1B** illustrates an example of the temperature distribution of a packaged IC device. A heat map 112 shows the temperature distribution of a packaged IC device disclosed in some embodiments of this disclosure, for example, by using a clip-bonded die

package with a thin lead frame of about 0.9 millimeter (mm) and a heat slug of about 2.5 mm according to some embodiments of the present disclosure. A heat map 114 shows an example of the temperature distribution of a conventional packaged IC device. Such conventional packaged IC devices can use traditional wire bonding and mounting structures with a thickness of about 1.27 mm.

[0051] The heat maps 112, 114 represent the temperature of the semiconductor device after applying a surge load of 160W power for a duration of 1 second after a steady state condition with 30W of power. As shown in the heat map 112, the packaged IC device (e.g., having a heat dissipation structure according to embodiments of the present disclosure), temperatures in the region 112A of the packaged IC device can remain below about 200°C, as shown in the temperature range 112B. In a conventional packaged IC device, the heat map 114 shows that the temperature in an outer region 114A of the packaged IC device is above 240°C, corresponding to the temperature range 114B. In addition, the semiconductor die region 114C of the conventional packaged IC device has a temperature of about 300°C. Such high temperatures can cause thermal stress on the component of the packaged IC device resulting in damage to the packaged IC device and/or can risk exceeding the melting temperature of die attach solder (e.g., high-melting point solder such as $Pb_{93.5}Sn_5Ag_{1.5}$, which can have a melting point of from about 296°C to about 301°C, or $Pb_{95.5}Sn_{2.5}Ag_{2.5}$, which can have a melting point of from about 299°C to about 304°C).

[0052] **FIG. 2** illustrates an example of a packaged IC device 200 that utilizes dual-sided cooling according to some embodiments. The packaged IC device 200 can include a lead frame 202, die clip 204, a semiconductor die 208, die paddle 212, and housing 214. The die paddle 212 can comprise thermally conductive material, such as one or more copper, lead, steel, etc. The die paddle 212 can be referred to as a heat dissipation structure (e.g., cooling structure). As shown in FIG. 2, a bottom surface of the lead frame 202 can be partially or fully exposed. In some embodiments, the lead frame 202 can be brought into contact (e.g., direct contact) with a PCB. In some embodiments, a thermal compound or solder joint can be included between the lead frame 202 and the PCB to improve thermal conduction into the PCB. Thus, the lead frame 202 can be in thermal contact with the PCB. The housing 214 can include or consist essentially of molding material. For example, molding material can form the housing 214.

[0053] In some embodiments, the die paddle 212 includes thermally conductive material and can dissipate heat generated from the semiconductor die 208. For example, one side of the semiconductor die 208 (e.g., the top side of the semiconductor die 208, as illustrated in FIG. 2) is bonded with the die paddle 212 by a thermal compound or solder joint. The heat generated from the semiconductor die 208 can flow to the die paddle 212. In some embodiments, the die paddle 212 and the lead frame 202 can be sufficiently thick to dissipate heat associated with a power surge. Such thicknesses can be significantly greater than conventional thicknesses sufficient to only achieve steady state heat dissipation for a stable maximum die temperature. A thickness 252 of the die paddle 212 can be 2 times or greater than 2 times a thickness 256 of the lead frame 202. The lead frame 202 can be shaped to function as a thin die paddle 212. In some embodiments, a thickness 252 of the die paddle 212 can be in a range from 4 times to 20 times a thickness of 254 of the semiconductor die 208. In some embodiments, a thickness 252 of the die paddle 212 can be 2 times or greater than 2 times a thickness of 259 of the die clip 204. The die paddle 212 and the lead frame 202 can each have an area that is greater than the area of the die 208. The die paddle 212 and the lead frame 202 can each extend beyond the die 208.

[0054] The heat capacity and thermal conductivity of the die paddle 212 and the lead frame 202 can dampen an increase in the temperature of the semiconductor die 208 in the presence of a momentary power surge. Accordingly, packaged IC device 200 can keep the die 208 and package within thermal specifications, including during power surges. In certain embodiments, the die paddle 212 and the lead frame 202 can together have a thermal mass sufficient to maintain the die at a temperature of less than 200°C, 190°C, 180°C, 170°C, 160°C, or 150°C when the die 208 is subjected to a surge load of up to 100 W or up to 160 W from steady state for 0.5 seconds. In some embodiments, the die paddle 212 and the lead frame 202 can together have a thermal mass sufficient to maintain a die at a temperature of less than 200°C, less than 190°C, or less than about 180°C when the die 208 is subjected to a surge load of up to 100 W or up to 160 W from steady state for 1 second.

[0055] In some embodiments, a thickness 252 of the die paddle 212 and a thickness 256 of the lead frame 202 can be designed to meet various technical specifications. In some cases, the thicknesses 252, 256 of the die paddle 212 and the lead frame 202, respectively, can preferentially remove heat from the bottom side of the packaged IC device or the top side of

the packaged IC device. For example, in an application directed to absorbing the heat at the die 208 and dissipating more heat via the top side of the packaged IC device 200 may involve a thinner thickness 256 of lead frame 202 and a thicker thickness 252 of die paddle 212. In this example, the thickness 252 of the die paddle 212 can be at least 4 times thicker than the thickness 256 of the lead frame 202. Further, in this example, more heat is desired to be absorbed from the semiconductor die 208 and removed via the top side of the packaged IC device, while a thicker lead frame 202 and thinner die paddle 212 can result in more heat being absorbed from the die and removed via the bottom side of the package. In some examples, more heat can be dissipated via the bottom side of the packaged IC device 200 than the previous example. This application may involve a thicker lead frame 202. In this example, the thickness 252 of the die paddle 212 can be between a 2-3.5 times thicker than the thickness 256 of the lead frame 202. Further, in this example, more heat is desired to be absorbed from the semiconductor die 208 and removed via the top side of the packaged IC device, such that a thicker lead frame 202 and thinner die paddle 212 can result in more heat being absorbed from the semiconductor die 208 and removed via the bottom side of the package. The proportion of thickness between 252 and 256 may be adjusted such as to maximize heat absorption with least die temperature rise.

[0056] While FIG. 2 depicts a lead frame 202 that is at least partially exposed, in some embodiments, the lead frame 202 may not be exposed. For example, in some applications, the lead frame 202 may not be exposed to avoid electrical connections between the electrical contact points of the PCB and the exposed lead frame 202. For example, a PCB can have exposed features such as one or more of high voltage vias, low voltage vias, traces, or the like. With an exposed lead frame 202, it can be desirable to route around a packaged IC device instead of passing under the packaged IC device to avoid making electrical contact with the lead frame 202. For example, the exposed lead frame 202 can pose electrical interference between the packaged IC device and any signals passing under the packaged IC device 200.

[0057] In some cases, a PCB may be at a similar temperature or a higher temperature than a die that is mounted to the PCB (e.g., a die disposed in an integrated circuit (IC) package that is affixed to the PCB). Thus, cooling from the bottom (e.g., PCB-facing) side of a packaged IC device may be of limited effectiveness in such cases. In some other cases, thermal transfer through the bottom of a packaged IC device may result in an increase in the

temperature of a semiconductor die inside the package, for example if the PCB is hotter than the die. Accordingly, in some embodiments, the thickness of any metal components near the bottom of a packaged IC device can preferably be relatively thin, while any metal components near the outward-facing side of the packaged IC device can be made thicker to provide greater thermal mass, thereby increasing thermal transfer towards an outward surface of the packaged IC device that is opposite to the PCB. For example, the thickness 252 of the die paddle 212 can be greater than the thickness 256 of the lead frame 202, such that the thickness 252 of the die paddle 212 can be at least 5 times thicker than the thickness 252 of the die paddle 212.

[0058] In some embodiments, thermally insulating a lead frame of a packaged IC device from a PCB (e.g., a high temperature PCB) can reduce the temperature of the lead frame relative to the PCB and also increase the combined heat absorption of the lead frame and die paddle. For example, thermally insulating the lead frame 202 to isolate the lead frame 202 from the contact with the PCB (having the high temperature) can prevent the lead frame 202 from further increasing the temperature via heat dissipations from the semiconductor die 208 and also the PCB.

[0059] In some embodiments, the molding material of the packaged IC device can provide such thermal insulation between the lead frame and the PCB. In some embodiments without limitation, molding material may not be used and/or another separator may be used. In some embodiments, separation from the PCB can be provided by an air gap between the PCB and the packaged IC device.

[0060] **FIG. 3A** illustrates an example packaged IC device 300 that uses single-sided cooling according to some embodiments. The packaged IC device 300 can include a lead frame 302, lead attach solder 304, semiconductor die 208, paddle attach solder 310, die paddle 312, and housing 314. The die paddle 312 can be composed of thermally conductive material, such as copper, lead, steel, etc. The die paddle 312 can be referred to as a heat dissipation structure (e.g., cooling structure). The packaged IC device 300 can include an electrically conductive spacer 316, which can duplicate the thickness of the semiconductor die 208 for keeping coplanar the interfacing surfaces of other components engaging the semiconductor die 208. In some embodiments, the housing 314 can include or consist essentially of molding material. For example, molding material can form the housing 314.

[0061] In some embodiments, the packaged IC device 300 can include additional circuitry. In some embodiments, the packaged IC device 300 can include a thermistor die 318. The thermistor die 318 can be configured to sense the temperature of the components, such as the packaged IC device 300, semiconductor die 208, lead frame 302, and/or any other components included in the packaged IC device 300. In some embodiments, the lead frame 302 can include a group of leads 302A (for example, a group of leads extended on A side of the lead frame 302) to electrically connect to the terminal(s) of the semiconductor die 208 and the thermistor die 318. For the purpose of illustration, FIG. 3A shows one lead 302A connected to the thermistor die 318, however, the group of leads 302A can include additional leads connected to terminals of the semiconductor die 208, for example as illustrated in FIG. 3B.

[0062] In some embodiments, the lead frame 302 can include a main frame 302C and a plurality of leads extended from the main frame 302C. In some examples, as further described in FIG. 3B, a plurality of leads is extended on the A side of the packaged IC device 300, for example, the leads extended on the A side can include a group of leads 302A, including two source leads and a gate lead. In some cases, the group of leads 302A can further include at least one of a kelvin source lead, a thermistor lead (e.g., one lead of the leads 302A connected to the thermistor die), or a sensing lead (configured to monitor voltage and/or current of the lead frame 302). In some embodiments, each lead is positioned on an outward side of the housing 314, and each lead of the plurality of leads is a flat lead. Additionally, the end of each lead (e.g., an outward side of the housing 314) of the plurality of leads can include a wettable flank. Additionally, the wettable flank can be soldered on a corresponding contact point of the PCB.

[0063] In some embodiments, the lead frame 302 can be embedded within the housing 314, with only electrical contacts exposed. The housing 314 can comprise molding material 322. In certain applications, a group of leads 302B can also extend from the lead frame 302. In some examples, the group of leads 302B can be electrically coupled with the drain terminal of the semiconductor die 208 via the die paddle 312. For example, two leads 302B (only shown one lead 302B in FIG. 3A) can be exposed outside of the housing 314 by providing electrical contact with a terminal of the semiconductor die 208, such as a drain terminal of the semiconductor die 208. For example, the drain terminal of the semiconductor die 208 is electrically coupled with the die paddle 312, and the die paddle 312 is connected to the leads

302B. In some examples, the die paddle 312 and the leads 302B are connected via a passive electronic component 320, such as a capacitor. In some embodiments, a molding material 322 can be embedded inside the housing 314. As illustrated in FIG. 3A, the molding material 322 can be included between the lead frame 302 and the bottom surface of the packaged IC device 300.

[0064] As shown in FIG. 3A, the die paddle 312 can extend to the top surface of the packaged IC device 300. The die paddle 312 can be exposed at least partially on the top surface of the packaged IC device 300. In some embodiments, the die paddle 312 can be referred to as a heat slug, a heat spreader, or the like.

[0065] In some embodiments, by using a thick die paddle 312 that extends to the top of the packaged IC device 300, heat transfer via the top of the packaged IC device 300 can be achieved without the use of a separate heat spreader. If a separate heat spreader is used, for example, because the die paddle 312 does not extend to the top of the packaged IC device 300, a thermal interface material can be applied between the die paddle 312 and the heat spreader. However, typical thermal interface materials can act as thermal bottlenecks as they can have thermal conductivities that are smaller than the thermal conductivities of the metals used to form the lead frame, heat spreader, heat slug, or die paddle.

[0066] In certain applications, the die paddle 312 can include copper and/or be mostly copper. The lead frame 302 can include copper and/or be mostly copper.

[0067] The semiconductor die 208 and other dies disclosed herein can be integrated circuit dies. These dies can include power switching devices that can generate significant heat.

[0068] The die paddle 312 can be sufficiently thick to dissipate heat associated with a power surge. The die paddle 312 can dampen an increase in temperature of the semiconductor die 208 in the presence of a power surge. Accordingly, the packaged IC device 300 can keep the semiconductor die 208 and package within temperature specification during power surge conditions. A thickness of 352 of the die paddle 312 can be at least 2.5 mm. For example, the thickness 352 of the die paddle 312 can be in a range from 2.5 mm to 5 mm. In certain instances, the thickness 352 of the die paddle 312 can be in a range from 2.5 mm to 3 mm. In some examples, the thickness 352 of the die paddle 312 is at least 3 times of a thickness 354 of the lead frame 302. In some embodiments, a separation 356 between the lead frame 302 and the bottom surface of the packaged IC device 300 can be thicker than the thickness 354 of the lead

frame. In some cases, the molding material 322 is included between the lead frame 302 and the bottom surface of the packaged IC device 300. In some cases, the main frame 302C of the lead frame 302 is separated from the bottom surface of the packaged IC device 300 by the separation 356. In some examples, the molding material 322 provides the separation between the main frame 302C of the lead frame 302 and the bottom surface of the packaged IC device 300.

[0069] In some configurations of the packaged IC device 300, where the PCB runs hotter than the packaged IC device 300, the lead frame 302 can be relocated relatively farther away from the PCB (e.g., from the bottom of the packaged IC device 300). For example, moving the lead frame 302 upward and away from the PCB can reduce the transfer of heat from the PCB to the lead frame 302. However, there can be limits to how far the lead frame 302 can be positioned above the PCB. For example, a large separation can result in undesirably large inductance loops. In some cases, a large separation can result in undesirable voltage losses as signals, power, etc., flow to and from the packaged IC device. In some embodiments, long leads used to make connections when there is a relatively large separation can impact performance, such as when operating at higher switching frequencies.

[0070] In these embodiments, the separation 356 can further be increased by reducing the thickness 352 of the die paddle 312 for a given overall packaged IC device height. Thus, in some cases, a greater separation from the PCB can result in less thermal mass above the die. The lower thermal mass profile of the die paddle 312 may cause degradation in heat dissipation. To enhance and/or optimize the thermal mass profile of the die paddle 312 and the heat dissipation, the thickness 352 of the die paddle 312 can be at least 1.25mm. In various applications, the thickness 352 of the die paddle 312 can also be determined based on various surge load conditions, such as in various power levels ranging between 60W to 160W. In these applications, the thickness 352 of the die paddle 312 can be increased as the power level increases. For example, the 1.25mm of thickness 352 of the die paddle 312 can effectively dissipate the heat when the power surge load is about 60W.

[0071] In some embodiments, the thickness 354 of the lead frame 302 can be reduced, thereby increasing the separation 356 between the lead frame 302 and the bottom surface of the packaged IC device 300. For example, the thickness 354 of the lead frame 302 can be 0.5mm. While a thinner lead frame 302 can be advantageous because it can enable

greater separation between the lead frame 302 and the PCB, electrical considerations can limit the thinness of the lead frame. For example, if the lead frame 302 is too thin, voltage drops due to the resistance of the electrical connection between the PCB, and the die may fall outside of design specifications and/or acceptable limits.

[0072] Thus, for some implementations, the thickness 354 of the lead frame 302, the thickness 352 of the die paddle 312, the separation 356 between the lead frame 302 and the PCB, and the overall device height can be considered. For example, these parameters can be modified based on the operating environment or specification of the packaged IC device 300, such as one or more switching speeds, cooling needs, power demands, resistive losses, or one or more other suitable parameters.

[0073] **FIG. 3B** shows an example of electrical paths through the packaged IC device 300 of FIG. 3A. The lead frame 302 (e.g., included inside the packaged IC device 300, as illustrated in FIG. 3A) can include a plurality of leads connected to terminals of the semiconductor die 208 and a thermistor die 318 (e.g., included inside the packaged IC device 300, as illustrated in FIG. 3A). In FIG. 3B, sides A and B of the bottom view can correspond to the sides A and B, respectively, of the packaged IC device 300 illustrated in FIG. 3A. In some examples, source leads 302AA, 302AB are electrically connected to a source terminal of the semiconductor die 208. A gate lead 302AD of the plurality of leads is connected to the gate terminal of the semiconductor die 208. In addition, a Kelvin source lead 302AE of the plurality of leads is connected to the Kelvin source terminal of the semiconductor die 208. In some examples, the lead frame 302 can include an additional sensing circuitry (or die) to sense the electrical characteristics of the semiconductor die, such as voltage, current, power, and the like. In these examples, a sense lead 302AC of the plurality of leads is connected to the sense terminal of the sensing circuitry. In some cases, the lead frame 302 can also be connected to an additional die, such as the thermistor die 318. The thermistor die 318 is an example of a sensor die. The thermistor die 318 can sense the temperature of the die and can be electrically coupled with the lead 302AF. The number and type of additional die and leads are merely illustrated as examples, and more than one additional die and lead can be used in certain applications.

[0074] The drain leads 302B can include leads 302BA and 302BB. The leads 302BA and 302BB can be electrically connected to a drain terminal of the semiconductor die

208. For example, the die paddle 312 can be a conductive material structure and provide an electrical connection between the drain terminal of the semiconductor die 208 and the two drain leads 302BA and 302BB.

[0075] **FIG. 4** schematically illustrates an example of a block diagram of a packaged IC device. In some examples, a semiconductor die 208 is connected on a first side to a die paddle 312 (e.g., also generally referred to as heat sink, heat slug, die paddle, thermal conductor, or the like) with solder 410 and connected to a PCB-facing lead frame 302 with solder 420 on a second side opposite the first side. In some embodiments, the thickness of the die paddle 312 can be maximized to extract heat from the semiconductor die 208 (e.g., having high temperature) via the die paddle 312. For example, in some embodiments, the PCB-facing lead frame 302 can be isolated by embedding the lead frame 302 in molding material to achieve electrical isolation, thermal insulation, and so forth from the PCB. In some embodiments, the PCB-facing lead frame 302 can be maintained at a temperature of less than about 120°C, for example, about 85°C. In some embodiments, contact between a packaged IC device and a PCB can be minimized.

[0076] While reference above is made to soldering lead frames 302, die paddle 312, and so forth to a semiconductor die 208, it will be appreciated that other approaches are possible. For example, in some embodiments, components can be bonded, sintered, or otherwise generally joined to the semiconductor die.

Surface Mount Epoxy Recess

[0077] Packaged IC devices can be subjected to a variety of non-ideal conditions. For example, they may be subjected to significant heat, vibration, and so forth. In some cases, a packaged IC device may be installed in a vehicle such as an automobile or a plane, heavy machinery, and so forth, where it is subject to significant vibrations or thermal cycling between cold and hot temperatures. Such conditions can result in premature failure of a device. For example, a packaged IC device that is under significant thermal stress, vibrational stress, and so forth may become detached from a PCB due to over stress of fatigue failure. Internal stresses can result in delamination or other failures of a packaged IC device.

[0078] In some embodiments, a packaged IC device can be a soldered surface mount device. In some embodiments, a surface mount device can have one or more recess

areas into which epoxy, or other materials, can be distributed. The use of epoxy in such recesses can aid in securing the surface mount device to a PCB and can provide stress relief. In some embodiments, such recesses can be used to achieve multi-device co-planarity. Multi-device co-planarity can be advantageous by enabling the use of a single flat heatsink to cool multiple devices. While surface mount devices are considered in this description, it will be appreciated that similar approaches can be used for packaged IC devices that use through-hole mounting and/or another suitable technology.

[0079] In some embodiments, epoxy can be more viscous than solder paste used to attach the surface mount device to electrical contacts on a PCB. The use of epoxy can offer several benefits, such as preventing or mitigating high centering of the package body, lifting of soldered leads, or both. Epoxy can prevent or mitigate tilting of the package body with respect to the PCB or hold SMD components at their designed seating plane with the PCB. Epoxy can prevent or mitigate height inconsistency or variation occurring during assembly processes. For example, height consistency can enable co-planarity of two or more devices. Thus, a heat spreader or heatsink with a flat bottom surface can be used to provide thermal management of more than one surface mount device. Because the two or more surface mount devices are coplanar, there can be a reduced thickness of thermal gap filler material on top of the devices between the devices and the heatsink or heat spreader, which can improve thermal performance. This approach can provide significant benefits, as a thermal gap filler material can be a large source of thermal resistance. Accordingly, thermal performance can be improved by reducing or eliminating the need to use thick thermal gap filler material that may otherwise be needed if the surface mount devices are not co-planar.

[0080] **FIG. 5** illustrates an example of a surface mount device 502 that is mounted to a printed circuit board 504 according to some embodiments. In FIG. 5, the surface mount device 502 is mounted to the PCB 504. The PCB 504 can include a solder mask 506 and solder pads 508 on a side that is facing the surface mount device 502. The surface mount device 502 can be electrically connected to the PCB 504 via the solder pads 508. For example, the surface mount device 502 can be mounted to the solder pads 508 of the PCB 504 using solder 510. As discussed above, the use of solder alone can result in the surface mount device 502 being tilted with respect to the PCB 504 as the solder 510 may not distribute evenly on all the solder pads 508. The epoxy 512 can be used to affix the surface mount device 502 to the PCB 504. The

height of the epoxy 512 can define a separation distance between the bottom surface of the surface mount device 502 and the top surface of the PCB 504.

[0081] In some embodiments, a surface mount device can have a relatively large recess, for example as depicted in FIG. 5. However, other configurations are possible. For example, a surface mount device can have one or more well-defined local recesses for receiving epoxy. Such an approach can, in some embodiments, improve co-planarity of multiple surface mount devices by partially restricting the flow of epoxy. The use of local recesses can have one or more other advantages. For example, a local recess can be advantageous during manufacturing processes in which suction is used to hold a device package during a topside grinding operation. Recesses may be positioned for epoxy 512 to be close to solder 510 to allow strain relief to reduce stresses on solder 510.

[0082] **FIG. 6** illustrates an example embodiment of a packaged IC device 600 that includes a local recess 610. As shown in FIG. 6, a packaged IC device 600 can include a die paddle 602, lead frame 604, a semiconductor die 208, and housing 608. The housing 608 can have a local recess 610 disposed on a bottom surface of the housing 608. The packaged IC device 600 is a packaged IC device. In some embodiments, the local recess 610 can have a recess depth of from about 50 micrometers to about 500 micrometers, for example about 100 micrometers. The recess depth of the local recess 610 can be any suitable depth for a particular application. For example, the recess depth of the local recess 610 can be any suitable value, constrained by the overall height of the packaged IC device 600 and the space for other components of the packaged IC device 600, such as the die paddle 602, lead frame 604, semiconductor die 606, solders used to make electrical connection between the components of the packaged IC device 600, any cooling embedded in the packaged IC device 600 (for example, if a separate heat spreader is used instead of a thick die paddle), and so forth.

[0083] Further in FIG. 6, in some examples, the thickness 652 of the die paddle 602 is at least 5 times the thickness 654 of the lead frame 604. In some embodiments, the separation 656 between the lead frame 604 and the bottom surface of the packaged IC device 600 (in some examples, the thickness of the molding material filled between the lead frame 604 and the bottom surface of the packaged IC device 600) can be at least 2 times the thickness 654 of the lead frame. In some embodiments, the distance of the separation 656 can be determined based on molding resin flowability, viscosity. The shape of the separation 656 from

the bottom surface facing the printed-circuit board may contain shapes such as the local recess 610, illustrated in FIG. 6. In some examples, the separation 656 can be equal or thinner than the thickness 654 of the semiconductor die 606.

[0084] **FIG. 7** shows a bottom perspective view of a packaged IC device 600 that includes a local recess 610 according to some embodiments. In FIG. 7, the packaged IC device 600 can include a housing 608 with a local recess 610 disposed on the bottom surface of the housing 608. The packaged IC device 600 can include source leads 612, additional leads 614 (e.g., gate leads, sense leads, Kelvin source leads, thermistor leads, and so forth), and drain leads 616. The structure depicted in FIG. 7 can be used, for example, in a power integrated circuit.

[0085] FIG. 7 is one example. The number and type of leads is not necessarily limited. For example, a device package can include more leads, fewer leads, and/or different leads than those shown in FIG. 7. While FIG. 7 shows that the source and drain leads are larger than other leads, this is not necessarily the case in all applications. In some embodiments, leads can all be the same size. According to some other embodiments, some leads can have sizes that are different from one or more other leads.

[0086] **FIG. 8** illustrates an example embodiment of an IC assembly that includes multiple packaged IC devices 802, 804, according to some embodiments. The packaged IC devices 802, 804 can be, for example, surface mount devices. In FIG. 8, a first packaged IC device 802 and a second packaged IC device 804 are mounted to a PCB 806. The PCB 806 can have a solder mask 808 and contact pads 810. The first packaged IC device 802 and second packaged IC device 804 can be electrically connected to the PCB 806 (e.g., to the contact pads 810 of the PCB 806) using solder 812. Epoxy 814 can be used to attach the first packaged IC device 802 and the second packaged IC device 804 to the PCB 806. The first packaged IC device 802 can be implemented in accordance with any suitable principles and advantages disclosed herein. The second packaged IC device 804 can be implemented in accordance with any suitable principles and advantages disclosed herein. For example, the first packaged IC device 802 and the second packaged IC device 804 can each include a lead frame and a relatively thick die paddle configured to dissipate heat associated with a power surge. As discussed above, the epoxy 814 can help to maintain a consistent vertical placement of the packaged IC devices.

[0087] The top surfaces of the first packaged IC device 802 and second packaged IC device 804 can be co-planar. A heatsink 816 having a flat bottom surface can be in contact with top surfaces of the first packaged IC device 802 and the second packaged IC device 804. In some embodiments, a thermal interface material 818 may be placed between the heatsink 816 and the top surfaces of the packaged IC devices 802 and 804. The thermal interface material 818 can be relatively thin (e.g., as compared to the thickness of thermal interface that would be needed if the packaged IC devices were not co-planar), enabling more efficient heat transfer from the first packaged IC device 802 and second packaged IC device 804 to the heatsink 816. The heatsink 816 is an example of a cooling structure. Any other suitable cooling structure, such as a cold plate, can be implemented in place of or in addition to the heatsink 816.

[0088] **FIG. 9A** illustrates an example of a packaged IC device 900. In some embodiments, the packaged IC device can have various configurations of the heat dissipation structure or the cooling structure. For example, the packaged IC device 300 of FIG. 3A includes the die paddle 312, as a cooling structure of the packaged IC device 300. The packaged IC device 900 includes a die paddle 912 comprising a multi-layer cooling structure. As illustrated, the packaged IC device 900 and the packaged IC device 300 can have the same components, except that (1) these two packaged IC devices have different die paddles and (2) the IC device 900 includes a recess in which epoxy can be distributed. For example, the packaged IC device 300 includes the die paddle 312 and the packaged IC device 900 includes the die paddle 912, which is a multi-layer cooling structure.

[0089] As illustrated in FIG. 9A, the die paddle 912 includes three layers, a top layer 912A, a middle layer 912B, and a bottom layer 912C. In some embodiments, the top layer 912A can be comprised of copper active metal brazing (Cu AMB) and the bottom layer 912C can comprise or consist essentially of copper (Cu). In some embodiments, the top layer 912A and the bottom layer 912C can include a same material, such as copper, Cu AMB, or the like, etc. The middle layer 912B can comprise a ceramic, such as silicon nitride, or any other suitable material.

[0090] A thickness of 952 of the die paddle 912 can be at least 2.5 mm. For example, the thickness 952 of the die paddle 912 can be in a range from 2.5 mm to 5 mm. In certain instances, the thickness 952 of the die paddle 912 can be in a range from 2.5 mm to 3 mm. As

one example, the thickness 952 of the die paddle 912 can be about 2.75 mm. In some examples, the thickness 952 of the die paddle 912 is at least 2.5 times a thickness 954 of the lead frame 302. For example, the die paddle 912 can be in a range from 2.5 times to 10 times a thickness 954 of the lead frame 302. As another example, the die paddle 912 can be in a range from 4 times to 10 times a thickness 954 of the lead frame 302.

[0091] In some embodiments, thicknesses 952A, 952C of the top and bottom layers 912A, 912C, respectively, are at least two times a thickness 952B of the middle layer 912B. In these embodiments, the thickness 952A and the thickness 952C can be the same. In some examples, the thickness 952A and the thickness 952C can be different, such that the thickness 952A can be thicker or thinner than the thickness 952C.

[0092] In some examples, an area 962B of the middle layer 912B can be larger than areas 962A, 962C of the top and bottom layers 912A, 912C, respectively. In these examples, the area 962C can be larger than the area 962A. In addition, the top, middle, and bottom layers 912A, 912B, and 912C are included within the housing 314.

[0093] In some cases, the lead frame 302 is separated from the bottom surface of the packaged IC device 300 by the separation 956 distance. In some embodiments, a separation 956 between the lead frame 302 and the bottom surface of the packaged IC device 900A can be thicker than the thickness 354 of the lead frame. In some cases, the molding material can be filled between the lead frame 302 and the bottom surface of the packaged IC device 900A.

[0094] **FIGS. 9B and 9C** illustrate other cross-sectional views of the packaged IC device 900. The cross-sectional view of FIG. 9B can be generally parallel to the cross-sectional view of FIG. 9A. In the cross-sectional view of FIG. 9A, the two illustrated leads include a source lead 302A and a drain lead 302B. In the cross-sectional view of FIG. 9B, the illustrated lead 302A1 can be located between two source leads and the packaged IC device 900 is free from leads opposite to the lead 302A1 illustrated in FIG. 9B. The lead 302A1 illustrated in FIG. 9B can be a gate lead, a sensing lead, or a Kelvin source lead, for example. The cross-sectional view of FIG. 9C can be generally perpendicular to the cross-sectional view of FIG. 9A and extend through a central portion of the packaged IC device 900.

[0095] **FIG. 10A** illustrates a three-dimensional assembly view of the packaged IC device 900 of FIGS. 9A-9C. As shown in FIG. 10A, the packaged IC device 900 includes the die paddle 912, having the top, middle, and bottom layers 912A, 912B, 912C, respectively.

[0096] As illustrated, the lead frame 302 can include a plurality of leads to terminals of the semiconductor die 208 (shown in FIG. 9A). In some examples, source leads 302AA, 302AB are electrically connected to a source terminal of the semiconductor die 208. A gate lead 302AD of the plurality of leads is connected to the gate terminal of the semiconductor die 208. In addition, a Kelvin source lead 302AE of the plurality of leads is connected to the Kelvin source terminal of the semiconductor die 208. In some examples, the lead frame 302 can include one or more leads connected to sensing circuitry (or die) to sense the electrical characteristics of the semiconductor die, such as voltage, current, power, and the like. In these examples, a sense lead (not shown in FIG. 10A) is connected to the sense terminal of the sensing circuitry. The number and type of additional die and lead are merely illustrated as examples, and more than one additional die and lead can be used in certain applications.

[0097] The drain leads 302B can be electrically connected to a drain terminal of the semiconductor die 208. For example, the die paddle 912 can be a conductive material structure and provide an electrical connection between the drain terminal of the semiconductor die 208 and the two drain leads 302B.

[0098] In some embodiments, each lead (e.g., an outward side of the housing 314) of the plurality of leads is a flat lead. Additionally, the end of each lead (e.g., an outward side of the housing 314) of the plurality of leads includes a wettable flank. Additionally, the wettable flank can be soldered on a corresponding contact point of the PCB.

[0099] **FIG. 10B** illustrates an exploded view of parts of an example of a packaged IC device 900 according to some embodiments. As shown in FIG. 10B, a packaged semiconductor component 1100 can be mounted on a lead frame 302. In some embodiments, the lead frame 302 can provide electrical contacts for electrical connections with terminals of the semiconductor die 208, such as drain, source, gate, and/or Kelvin source terminals.

[0100] As shown in FIG. 10B, the packaged semiconductor component 1100 can include a die paddle 912, a bonding layer 1004 (e.g., a die back and spacer solder), a spacer 1006, a semiconductor die 208, a bonding layer 1010 (e.g., a die back and spacer solder). In some examples, the bonding layers 1004, 1010 can be formed based on a pattern that can include multiple areas to provide electrical connections with corresponding die connection terminals (e.g., contact terminals), such as source, Kelvin source, drain, and gate of the semiconductor die 208. In some examples, the bonding layers 1004, 1010 can be formed of a

conductive material, such as, without limitation, solder, conductive epoxy, or the like. The lead frame 302 can include any suitable configuration disclosed herein.

[0101] **FIGS. 11A and 11B** illustrate packaged IC devices with examples of heat spreader 1112 (shown in FIG. 11A) and 1122 (shown in FIG. 11B) according to embodiments of this disclosure.

[0102] Referring to FIG. 11A, the heat spreader 1112 can be formed of a solid conductive material. The heat spreader 1112 can include or consist essentially of copper. As illustrated in FIG. 11A, a packaged IC device 1100A can include the heat spreader 1112 having a first portion 1112A and a second portion 1112B. The first and second portions 1112A, 1112B can be formed by using a same material, such as a copper. In some embodiments, the first and second portions 1112A, 1112B can have an electrically insulating material 1113 therebetween that is securely bonded such as an active metal brazed (AMB) construction whereby a silicon nitride ceramic sheet can be used to produce a copper AMB. The electrically insulating material 1113 can be a ceramic. In some examples, the thickness 1152A of the first portion 1112A and 1152B of the second portion 1112B can be between two and five times the thickness electrically insulating material 1113. In some embodiments, the AMB can be used as a substrate for mounting a semiconductor die.

[0103] As illustrated in FIG. 11B, a packaged IC device 1100B can include the heat spreader 1122 having a first portion 1122A and a second portion 1122B. In some embodiments, the first and second portions 1122A, 1122B can be formed by using a same material, such as a copper. In some embodiments, the first and second portions 1122A, 1122B can be formed by using a different material, such that the first portion 1122A can be formed with copper, and the second portion 1122B can be formed with copper AMB. In some examples, the thickness 1162A of the first portion 1122A can be between two to five times the thickness 1162B of the second portion 1122B.

[0104] **FIG. 12** illustrates an exploded view of parts of an example of a packaged IC device 1100B of FIG. 11B according to some embodiments. As shown in FIG. 12, a packaged semiconductor component 1200 can be mounted on a lead frame 302. In some embodiments, the lead frame 302 can provide electrical contacts for electrical connections with terminals of the semiconductor die 208, such as drain, source, gate, and/or Kelvin source terminals.

[0105] As shown in FIG. 12, the packaged semiconductor component 1200 can include a heat spreader 1122, a bonding layer 1004 (e.g., a die back and spacer solder), a spacer 1006, a semiconductor die 208, a bonding layer 1010 (e.g., a die back and spacer solder). The heat spreader 1122 can be a die paddle. In some examples, the bonding layers 1004, 1010 can be formed based on a pattern that can include multiple areas to provide electrical connections with corresponding die connection terminals (e.g., contact terminals), such as source, Kelvin source, drain, and gate of the semiconductor die 208. In some examples, the bonding layers 1004, 1010 can be formed by a conductive material, such as, without limitation, solder, conductive epoxy, or the like. The lead frame 302 can include any suitable configuration disclosed herein.

[0106] **FIG. 13** illustrates an example of a packaged IC device 1300 having a top layer 912A, a middle layer 912B, and a bottom layer 912C. An example of a top layer 912A, a middle layer 912B, and a bottom layer 912C configuration and their respective thicknesses and compositions are described with respect to FIG. 9A. In some embodiments, the bottom layer 912C can include one or more notches, such as notches 912CA and 912CB. The lead frame 302D can include a plurality of leads that the leads 302D1 can extend directly from one or more terminals (e.g., one or more of source terminal, gate terminal, or Kelvin source terminal) external to the housing 314. In some embodiments, the lead 302D1 can be a flat lead.

[0107] **FIG. 14** illustrates an example of a packaged IC device 1400 having the heat spreader 1112 (e.g., heat spreader) of FIG. 11A and lead frame 302D of FIG. 13.

[0108] **FIGS. 15A-15C** illustrate various examples of a heat spreader (e.g., heat spreader) having various shapes. For example, as shown in FIG. 15A, a heat spreader 1512A can have a notch 1512AA. FIGS. 15B and 15C illustrate that a solid copper clip can be replaced by an AMB with an underside notch. FIG. 15B illustrates one side of the AMB clip, and FIG. 15C illustrates an opposite side of the AMB clip. As illustrated in FIG. 15B, on a top side, a thickness of a heat spreader 1512B can be gradually decreased toward the middle section of the heat spreader 1512B and increased from the middle section to an outer section of the heat spreader 1512B. As shown in FIG. 15C, a bottom side 1512C of the heat spreader 1512B can have a notch 1512CA and a secondary square notch 1512CB.

Additional Embodiments

[0109] In the foregoing specification, the disclosure has been described with reference to specific embodiments. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the disclosure. The specification and drawings are, accordingly, to be regarded in an illustrative rather than restrictive sense.

[0110] Indeed, although this disclosure is in the context of certain embodiments and examples, it will be understood by those skilled in the art that the inventions extend beyond the specifically disclosed embodiments to other alternative embodiments and/or uses of the inventions and equivalents thereof. In addition, while several variations of the embodiments have been shown and described in detail, other modifications, which are within the scope of this disclosure, will be readily apparent to those of skill in the art based upon this disclosure. It is also contemplated that various combinations or sub-combinations of the specific features and aspects of the embodiments may be made and still fall within the scope of the disclosure. It should be understood that various features and aspects of the disclosed embodiments can be combined with, or substituted for, one another in order to form varying modes of the embodiments disclosed herein. Any methods disclosed herein need not be performed in the order recited. Thus, it is intended that the scope of the disclosure should not be limited by the particular embodiments described above.

[0111] It will be appreciated that the systems and methods of the disclosure each have several innovative aspects, no single one of which is solely responsible or required for the desirable attributes disclosed herein. The various features and processes described above may be used independently of one another or may be combined in various ways. All possible combinations and subcombinations are intended to fall within the scope of this disclosure.

[0112] Certain features that are described in this specification in the context of separate embodiments also may be implemented in combination in a single embodiment. Conversely, various features that are described in the context of a single embodiment also may be implemented in multiple embodiments separately or in any suitable subcombination. Moreover, although features may be described above as acting in certain combinations and even initially claimed as such, one or more features from a claimed combination may in some cases be excised from the combination, and the claimed combination may be directed to a

subcombination or variation of a subcombination. No single feature or group of features is necessary or indispensable to each and every embodiment.

[0113] It will also be appreciated that conditional language used herein, such as, among others, "can," "could," "might," "may," "e.g.," and the like, unless specifically stated otherwise, or otherwise understood within the context as used, is generally intended to convey that certain embodiments include, while other embodiments do not include, certain features, elements and/or steps. Thus, such conditional language is not generally intended to imply that features, elements and/or steps are in any way required for one or more embodiments or that one or more embodiments necessarily include logic for deciding, with or without author input or prompting, whether these features, elements and/or steps are included or are to be performed in any particular embodiment. The terms "comprising," "including," "having," and the like are synonymous and are used inclusively, in an open- ended fashion, and do not exclude additional elements, features, acts, operations, and so forth. In addition, the term "or" is used in its inclusive sense (and not in its exclusive sense) so that when used, for example, to connect a list of elements, the term "or" means one, some, or all of the elements in the list. In addition, the articles "a," "an," and "the" as used in this application and the appended claims are to be construed to mean "one or more" or "at least one" unless specified otherwise. Similarly, while operations may be depicted in the drawings in a particular order, it is to be recognized that such operations need not be performed in the particular order shown or in sequential order, or that all illustrated operations be performed, to achieve desirable results. Further, the drawings may schematically depict one more example processes in the form of a flowchart. However, other operations that are not depicted may be incorporated in the example methods and processes that are schematically illustrated. For example, one or more additional operations may be performed before, after, simultaneously, or between any of the illustrated operations. Additionally, the operations may be rearranged or reordered in other embodiments. In certain circumstances, multitasking and parallel processing may be advantageous. Moreover, the separation of various system components in the embodiments described above should not be understood as requiring such separation in all embodiments, and it should be understood that the described program components and systems may generally be integrated together in a single software product or packaged into multiple software products. Additionally, other

embodiments are within the scope of the following claims. In some cases, the actions recited in the claims may be performed in a different order and still achieve desirable results.

[0114] Further, while the methods and devices described herein may be susceptible to various modifications and alternative forms, specific examples thereof have been shown in the drawings and are herein described in detail. It should be understood, however, that the disclosure is not to be limited to the particular forms or methods disclosed, but, to the contrary, the disclosure is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the various implementations described and the appended claims. Further, the disclosure herein of any particular feature, aspect, method, property, characteristic, quality, attribute, element, or the like in connection with an implementation or embodiment can be used in all other implementations or embodiments set forth herein. Any methods disclosed herein need not be performed in the order recited. The methods disclosed herein may include certain actions taken by a practitioner; however, the methods can also include any third-party instruction of those actions, either expressly or by implication. The ranges disclosed herein also encompass any and all overlap, sub-ranges, and combinations thereof. Language such as "up to," "at least," "greater than," "less than," "between," and the like includes the number recited. Numbers preceded by a term such as "about" or "approximately" include the recited numbers and should be interpreted based on the circumstances (e.g., as accurate as reasonably possible under the circumstances, for example ±5%, ±10%, ±15%, etc.). Phrases preceded by a term such as "substantially" include the recited phrase and should be interpreted based on the circumstances (e.g., as much as reasonably possible under the circumstances). For example, "substantially constant" includes "constant." Unless stated otherwise, all measurements are at standard conditions, including temperature and pressure.

[0115] As used herein, a phrase referring to "at least one of" a list of items refers to any combination of those items, including single members. As an example, "at least one of: A, B, or C" is intended to cover: A, B, C, A and B, A and C, B and C, and A, B, and C. Conjunctive language such as the phrase "at least one of X, Y and Z," unless specifically stated otherwise, is otherwise understood with the context as used in general to convey that an item, term, etc. may be at least one of X, Y or Z. Thus, such conjunctive language is not generally intended to imply that certain embodiments require at least one of X, at least one of Y, and at least one of Z to each be present. The headings provided herein, if any, are for convenience

only and do not necessarily affect the scope or meaning of the devices and methods disclosed herein.

[0116] Accordingly, the claims are not intended to be limited to the embodiments shown herein but are to be accorded the widest scope consistent with this disclosure, the principles and the novel features disclosed herein.

WHAT IS CLAIMED IS:

1. A packaged integrated circuit device with power surge heat dissipation, comprising:

a semiconductor die having a first side and a second side, the second side being opposite to the first side;

a lead frame on the first side of the semiconductor die, the lead frame being embedded in a molding material; and

a heat spreader on the second side of the semiconductor die, the heat spreader having a thickness of at least 2.5 millimeters.

2. The packaged integrated circuit device of claim 1, wherein the heat spreader and the lead frame are configured to maintain the semiconductor die at a temperature of less than 200 degrees Celsius when subjected to a surge load of up to 160 Watts for 1 second from a steady state.

3. The packaged integrated circuit device of claim 1 or claim 2, wherein the thickness of the heat spreader is at least four times a thickness of the semiconductor die, wherein an area of the heat spreader is greater than an area of the semiconductor die, and wherein the heat spreader extends beyond the semiconductor die.

4. The packaged integrated circuit device of claim 3, wherein the thickness of the heat spreader is between four and twenty times the thickness of the semiconductor die.

5. The packaged integrated circuit device of claim 1, wherein the thickness of the heat spreader is at least 2.5 times a thickness of the lead frame.

6. The packaged integrated circuit device of any of claims 1-5, wherein the packaged integrated circuit device has a recess in the molding material on a side of the packaged integrated circuit device that is opposite to the heat spreader.

7. The packaged integrated circuit device of any of claims 1-6, wherein the lead frame and the heat spreader are both joined to the semiconductor die.

8. The packaged integrated circuit device of any of claims 1-7, wherein the semiconductor die comprises a field effect transistor.

9. The packaged integrated circuit device of claim 8, wherein the field effect transistor is a gallium nitride field effect transistor.

10. The packaged integrated circuit device of any of claims 1-9, wherein the lead frame comprises a main frame and a plurality of leads extending from the main frame, and wherein each lead of the plurality of leads is flat outside of the molding material.

11. The packaged integrated circuit device of claim 10, wherein each lead of the plurality of leads comprises a wettable flank.

12. The packaged integrated circuit device of any of claims 1-11, wherein the heat spreader is a solid layer comprising copper.

13. The packaged integrated circuit device of any of claims 1-11, wherein the heat spreader is a multi-layer structure comprising a first metal layer, a second metal layer, and ceramic layer positioned between the first metal layer and the second metal layer.

14. An integrated circuit assembly with power surge heat dissipation, comprising:

a printed circuit board;

a packaged integrated circuit device on the printed circuit board, the packaged integrated circuit device comprising a semiconductor die, a lead frame positioned between the semiconductor die and the printed circuit board, and a heat spreader positioned on an opposite side of the semiconductor die than the lead frame, the heat spreader having a thickness of at least 2.5 millimeters; and

a cooling structure in thermal contact with the heat spreader.

15. The integrated circuit assembly of claim 14, wherein the packaged integrated circuit device comprises molding material or other separator to provide electrical and/or thermal insulation between the printed circuit board and the lead frame.

16. The integrated circuit assembly of claim 15, wherein the packaged integrated circuit device has a recess in the molding material on a side facing the printed circuit board.

17. The integrated circuit assembly of claim 14, further comprising a second packaged integrated circuit device on the printed circuit board, the second packaged integrated circuit device comprising a second heat spreader in thermal contact with the cooling structure.

18. The integrated circuit assembly of any of claims 14-17, wherein the cooling structure comprises a heatsink and/or a cold plate.

19. A packaged integrated circuit device with power surge heat dissipation, comprising:

a semiconductor die having a first side and a second side, the second side being opposite to the first side, the semiconductor die comprising a field effect transistor;

a lead frame on the first side of the semiconductor die, the lead frame being embedded in a molding material; and

a cooling structure on the second side of the semiconductor die, the cooling structure comprising two metal layers and a ceramic layer positioned between the two metal layers, wherein a thickness of the cooling structure is greater than 2.5 millimeters.

20. The packaged integrated circuit device of claim 19, wherein the thickness of the cooling structure is at least 2.5 times a thickness of the lead frame.

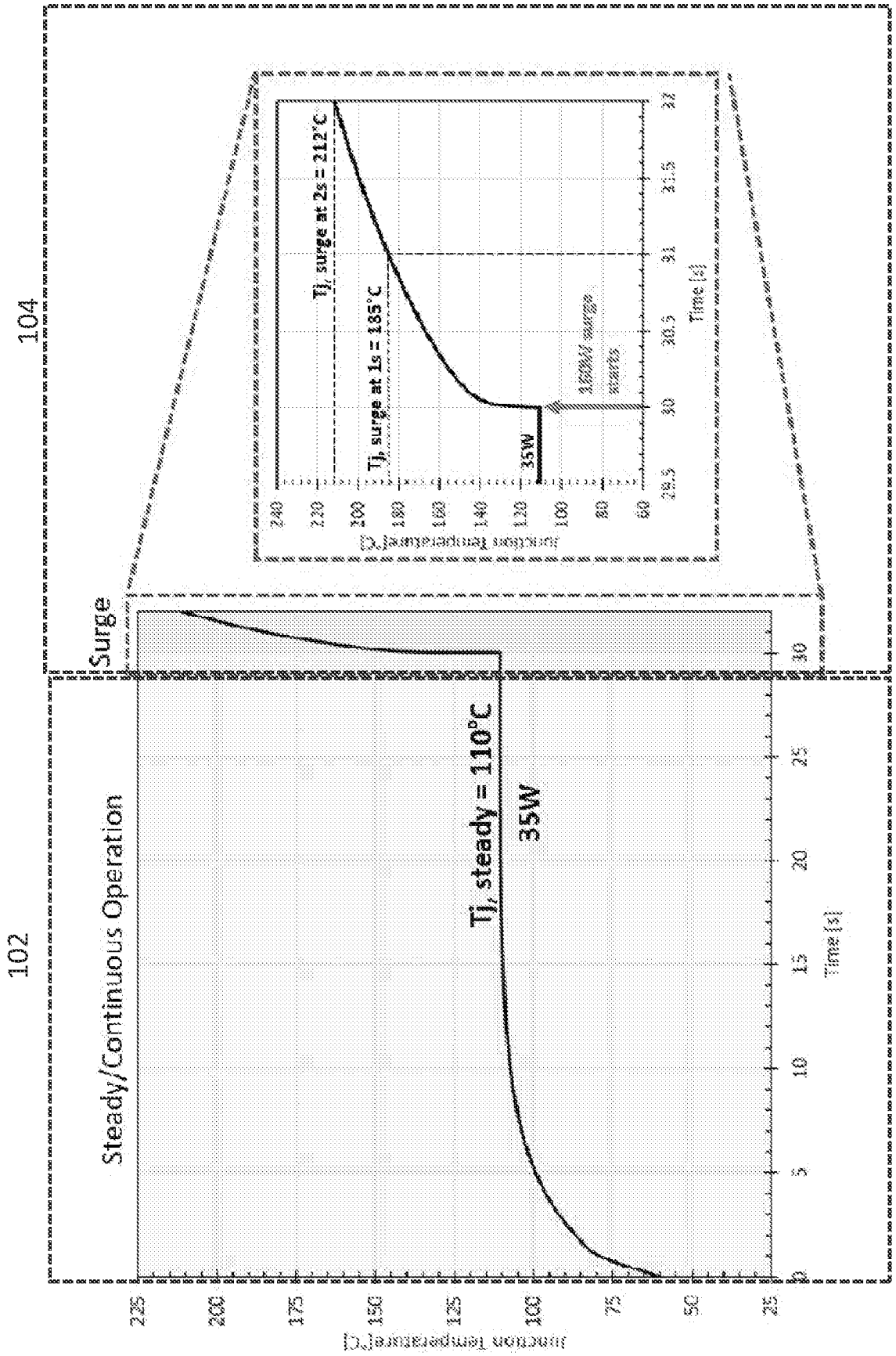
102
104
Steady/Continuous Operation
Surge
Tj, steady = 110°C
35W
Tj, surge at 1s = 185°C
Tj, surge at 2s = 212°C
35W
160W surge
Time [s]
Junction temperature [°C]

FIG. 1A

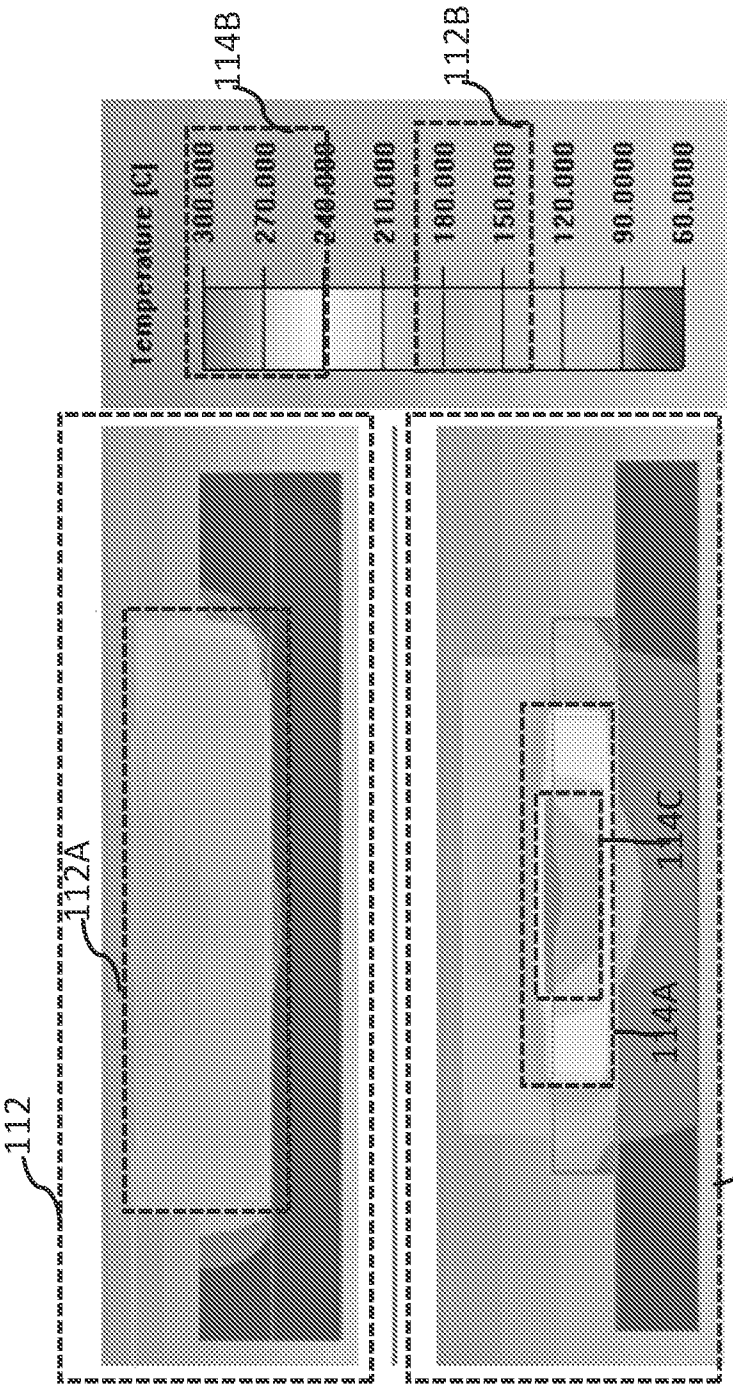
Temperature [C]
300.000
270.000
240.000
210.000
180.000
150.000
120.000
90.0000
60.0000
114B
112B
112
112A
114
114A
114C

FIG. 1B

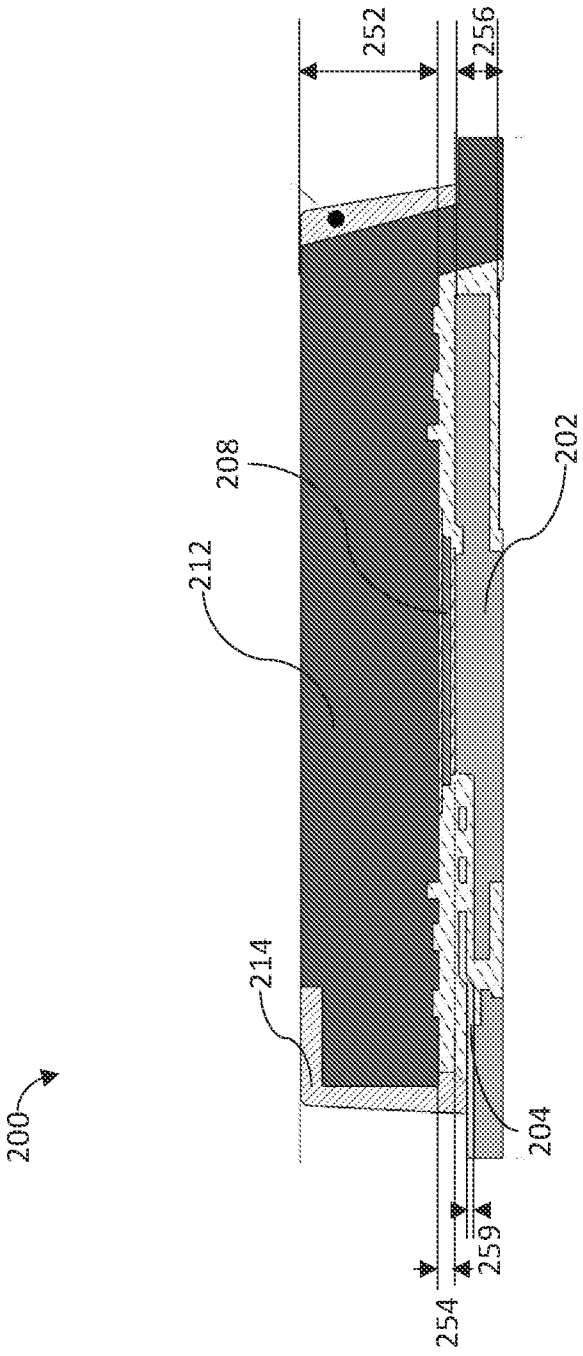

FIG. 2

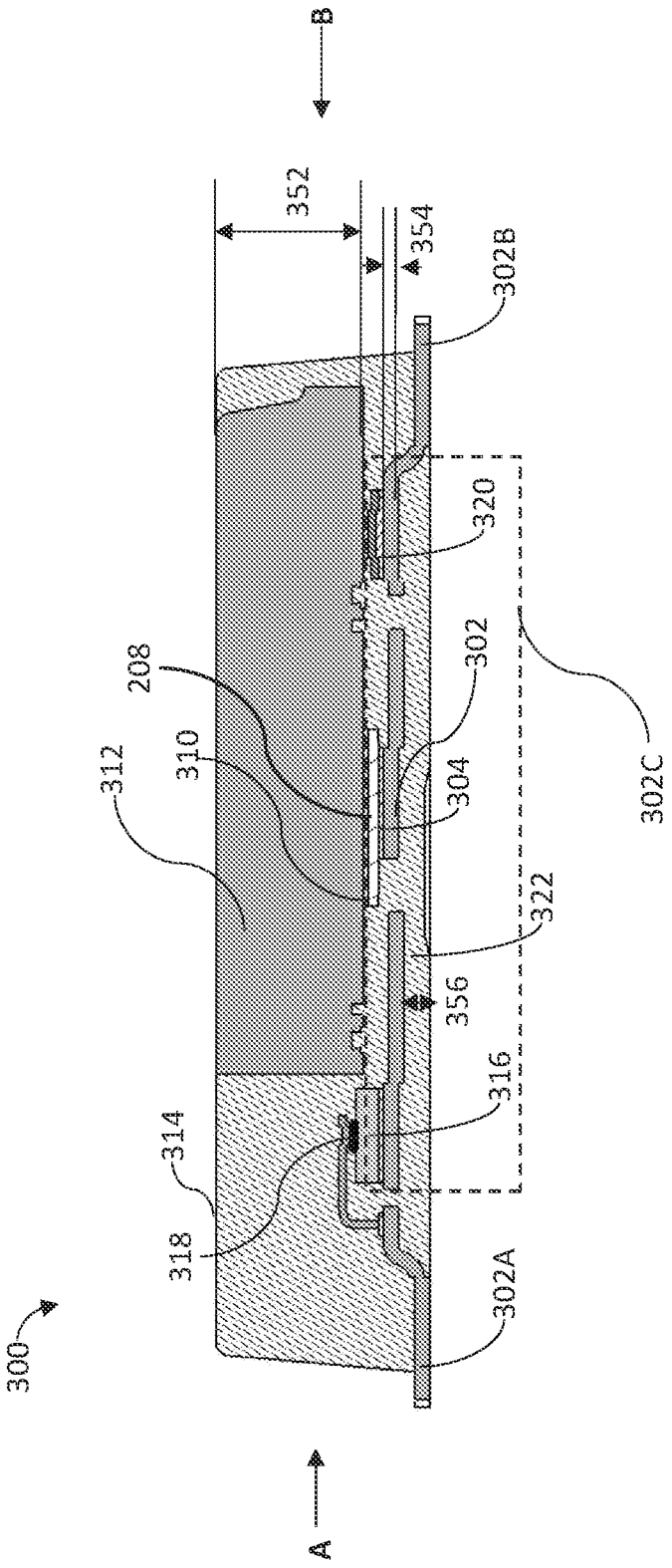
B
352
354
302B
320
208
302
310
304
312
302C
322
356
316
314
318
302A
300
A

FIG. 3A

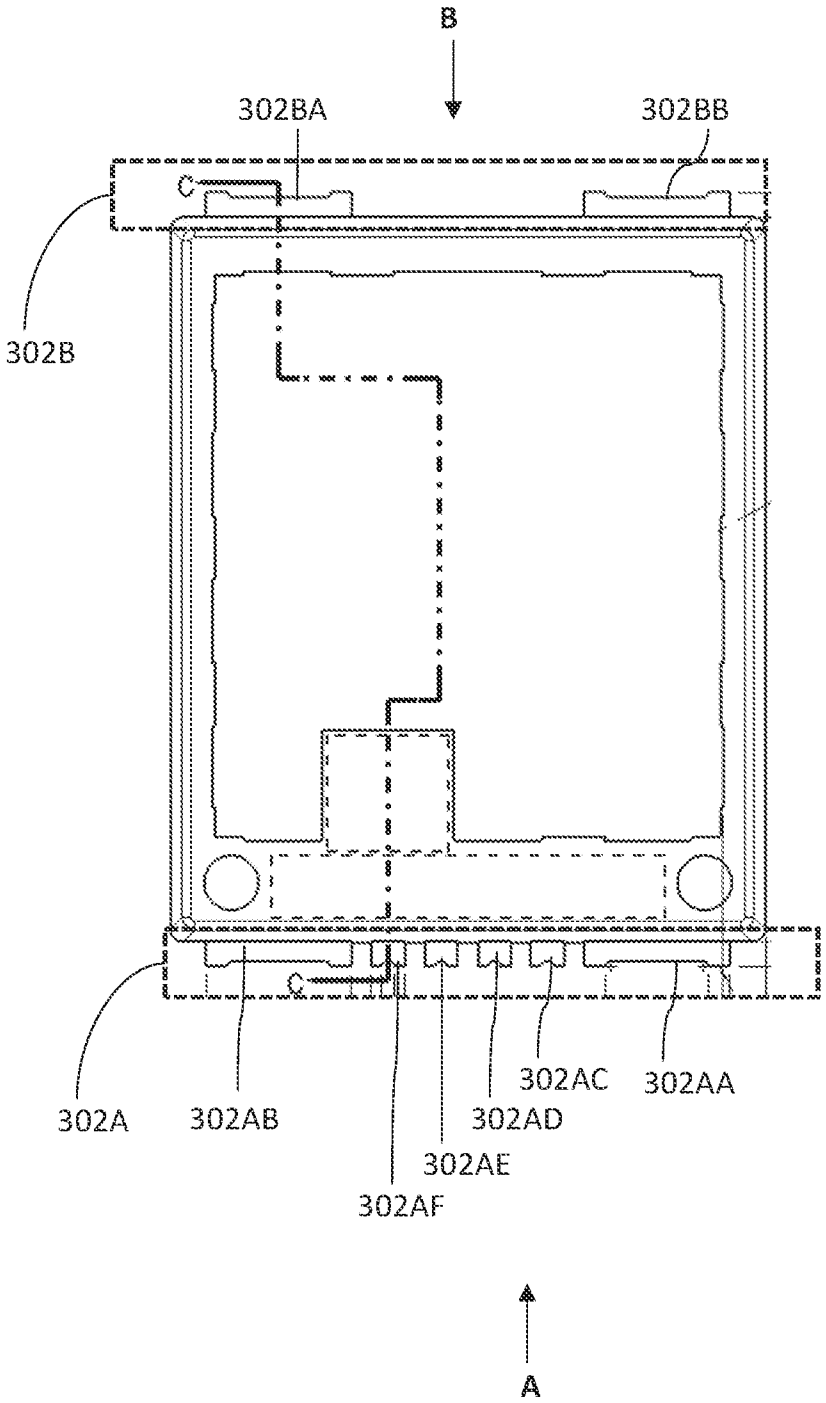
B
302BA
302BB
302B
302A
302AB
302AF
302AE
302AD
302AC
302AA
A

FIG. 3B

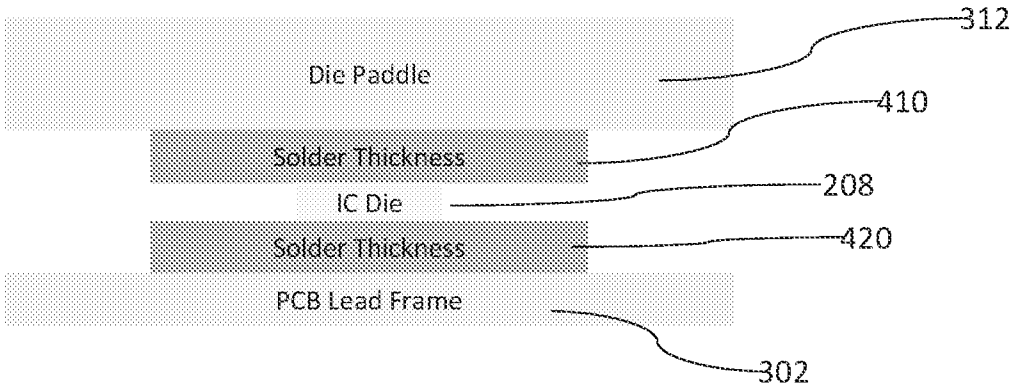
Die Paddle
312
Solder Thickness
410
IC Die
208
Solder Thickness
420
PCB Lead Frame
302

FIG. 4

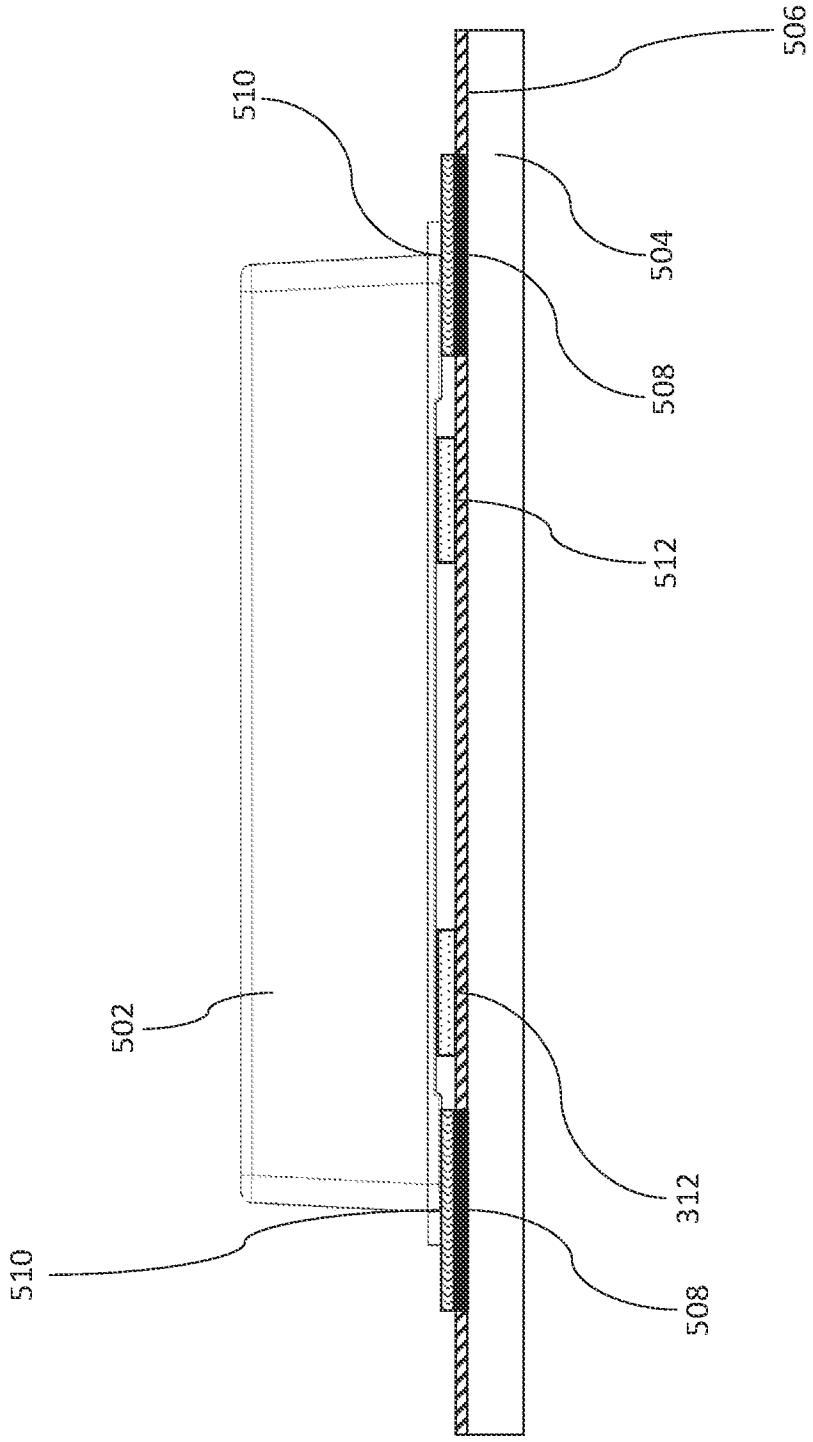

FIG. 5

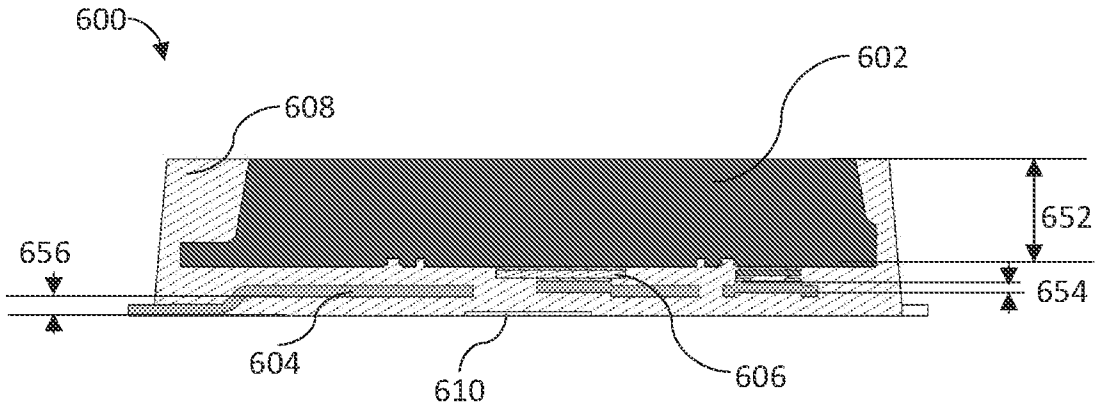
600
602
608
652
656
654
604
610
606

FIG. 6

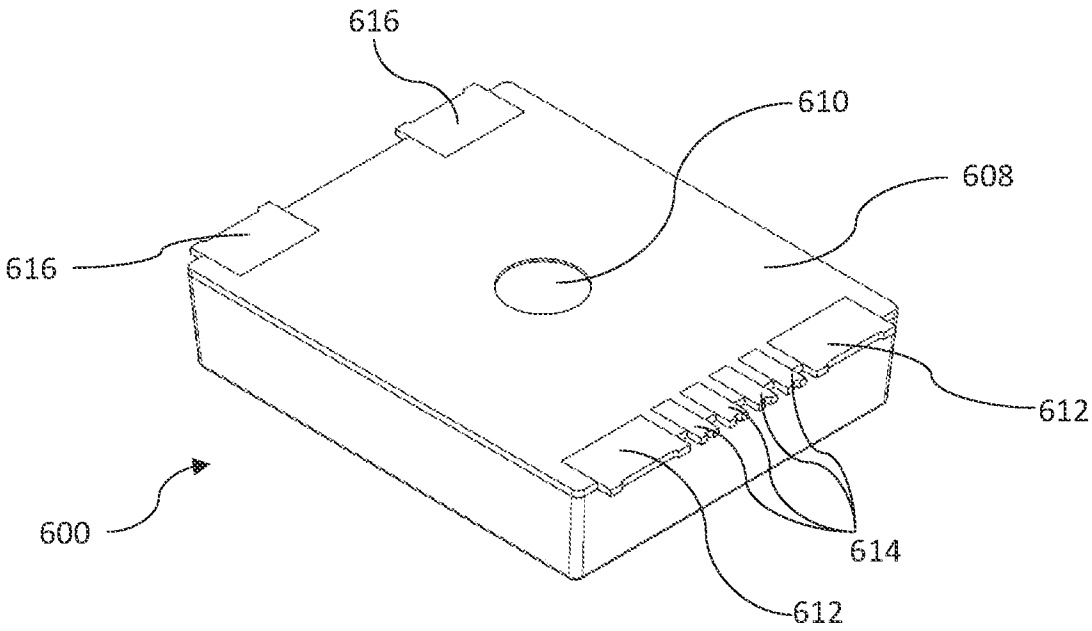
616
610
608
616
612
600
614
612

FIG. 7

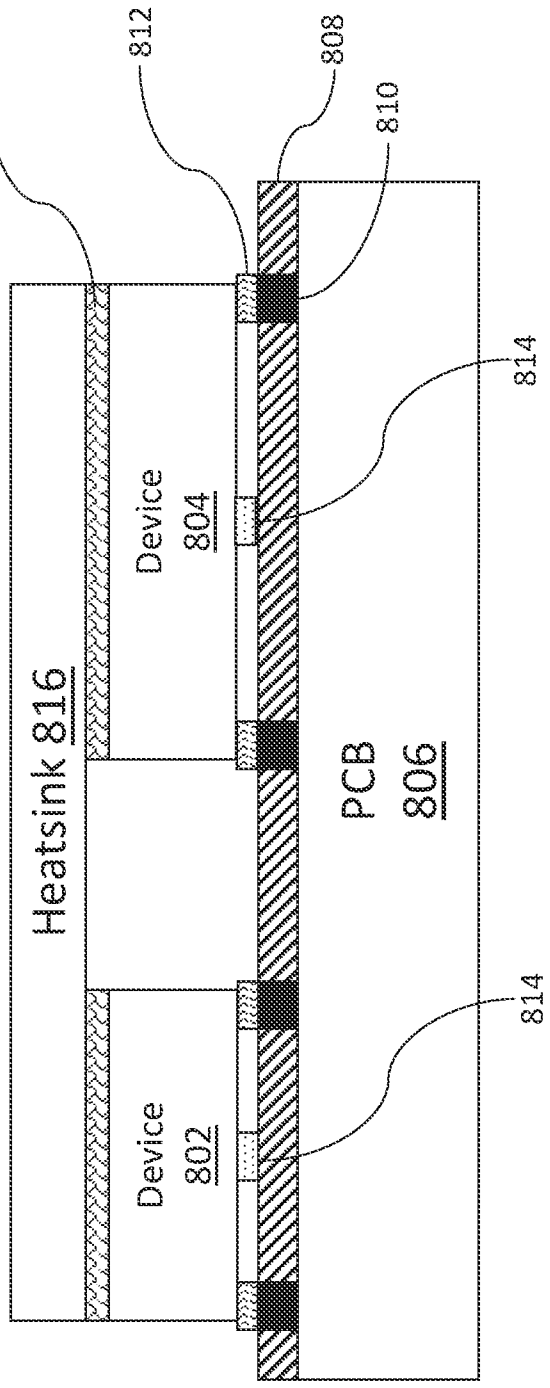
818
812
808
810
814
Device
804
Heatsink 816
PCB
806
814
Device
802

FIG. 8

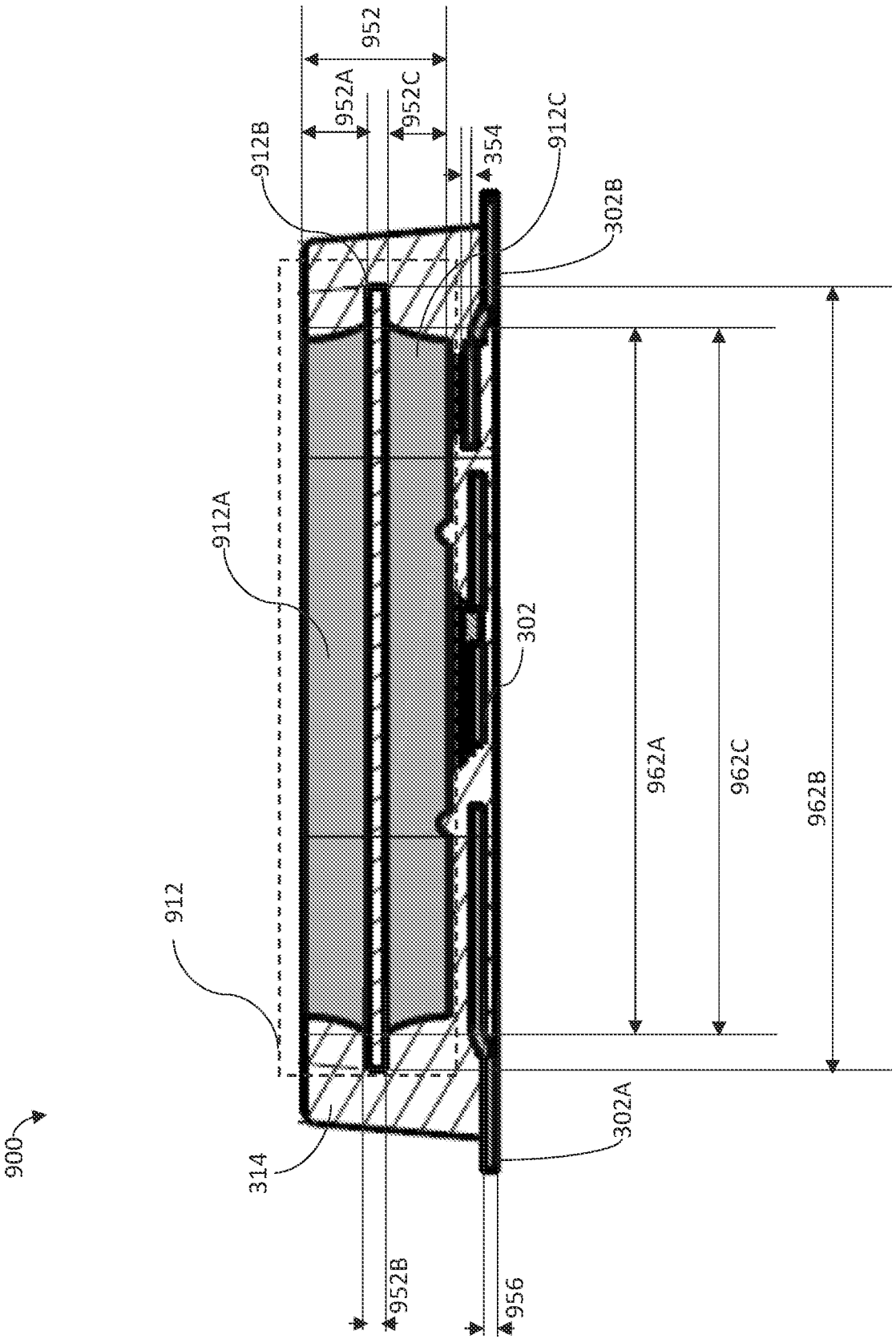
900
912
912A
912B
912C
314
302
302A
302B
354
952
952A
952B
952C
956
962A
962B
962C

FIG. 9A

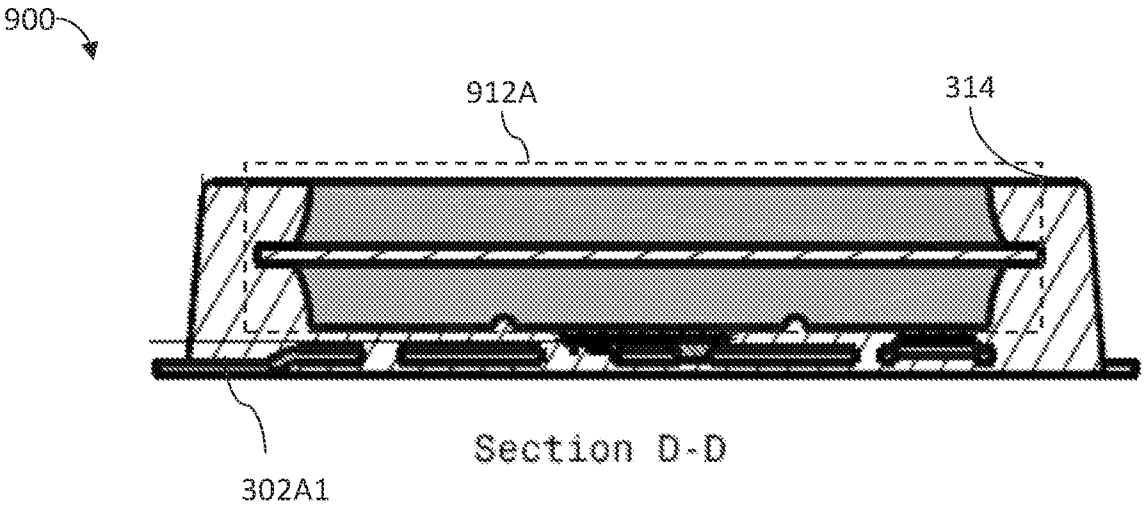

FIG. 9B

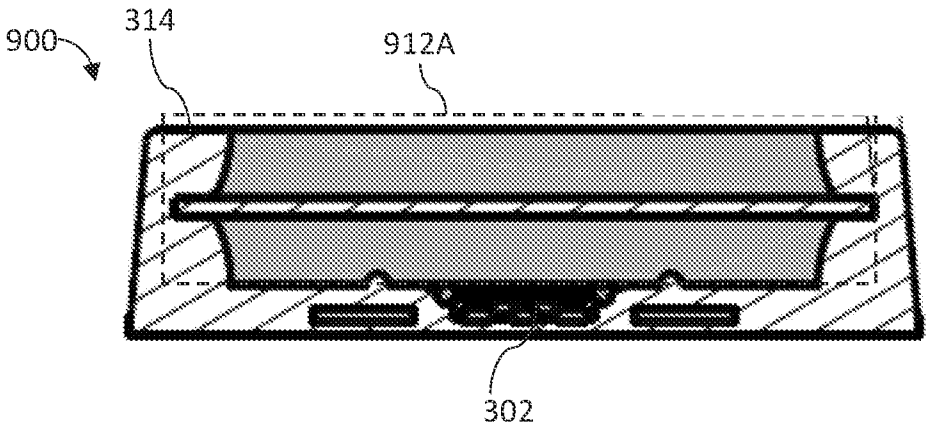

FIG. 9C

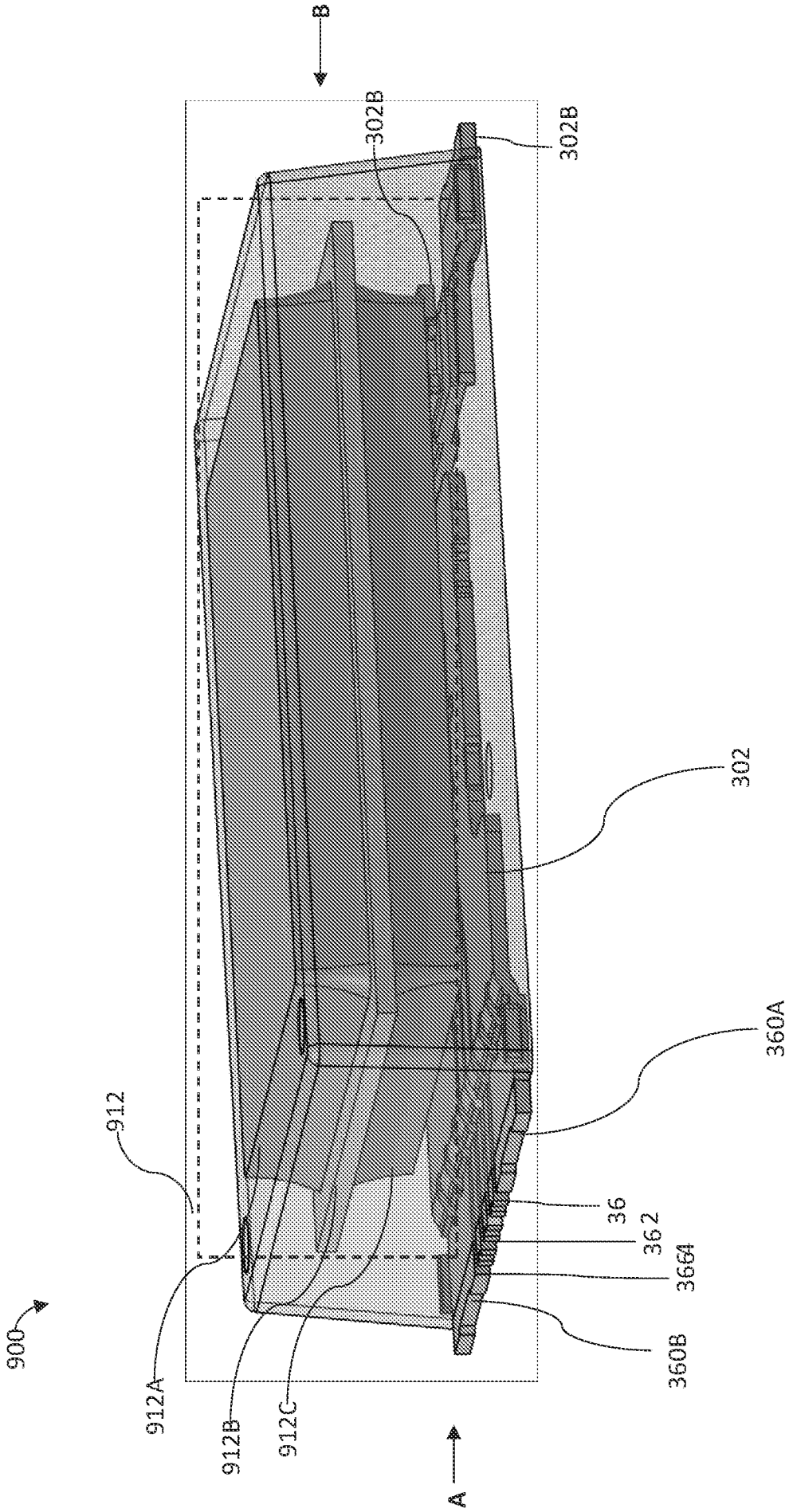

FIG. 10A

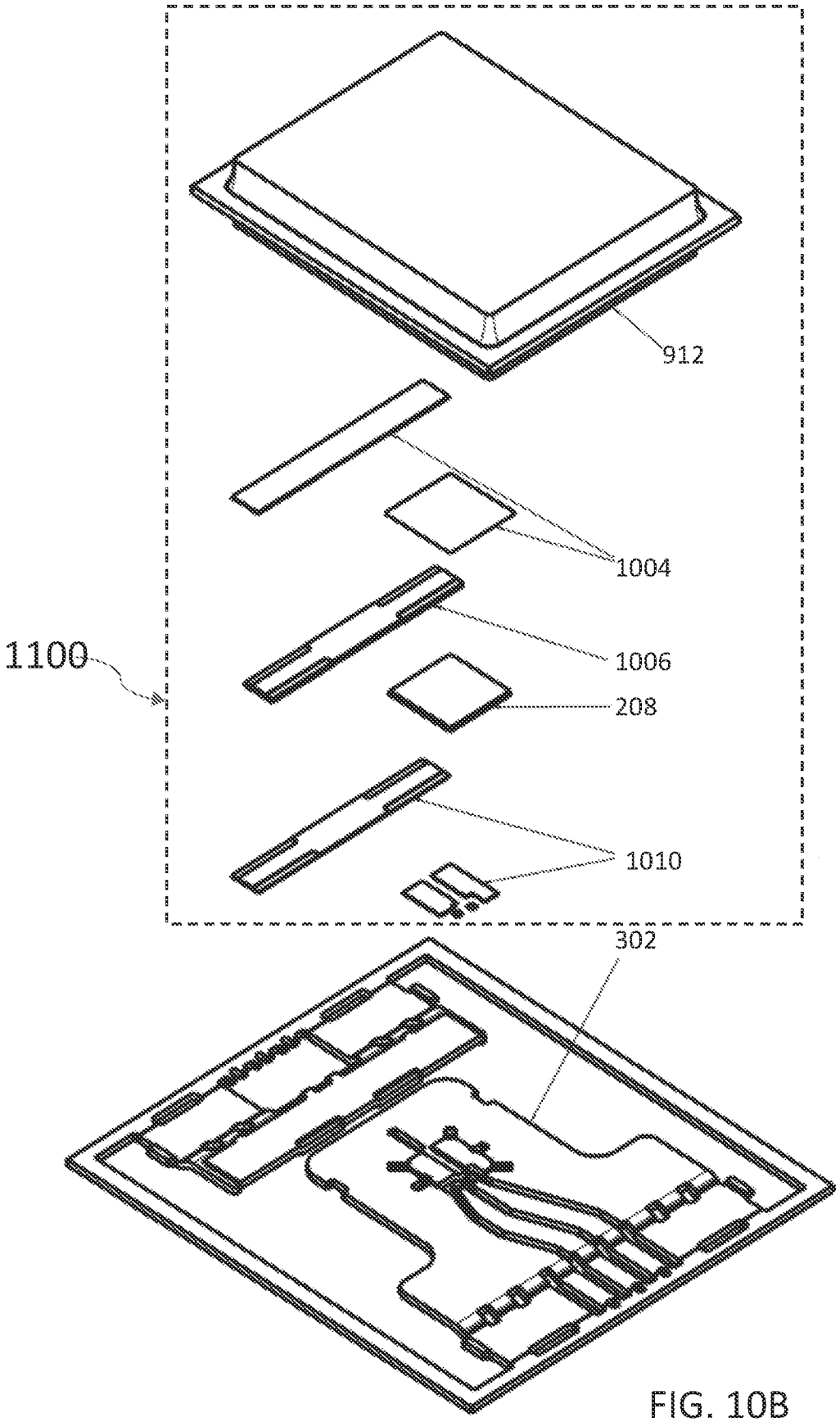

FIG. 10B

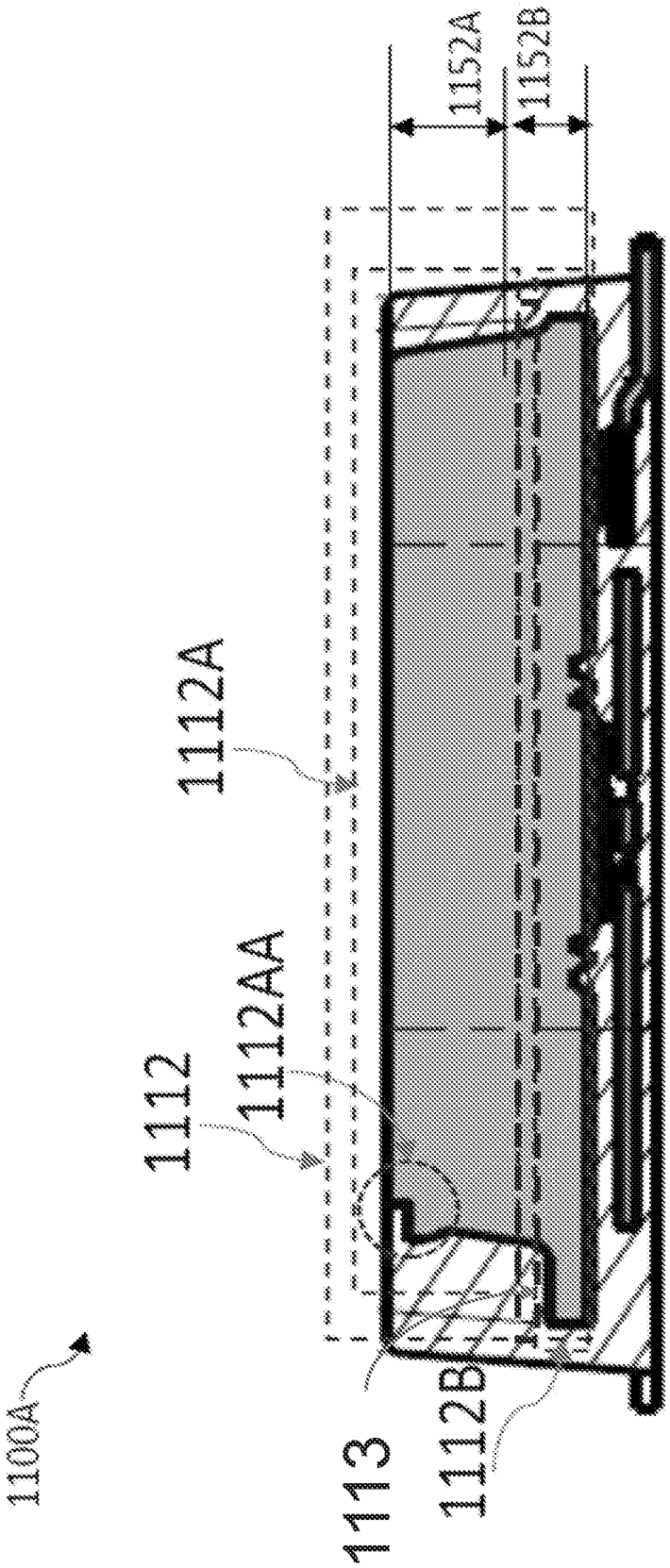

FIG. 11A

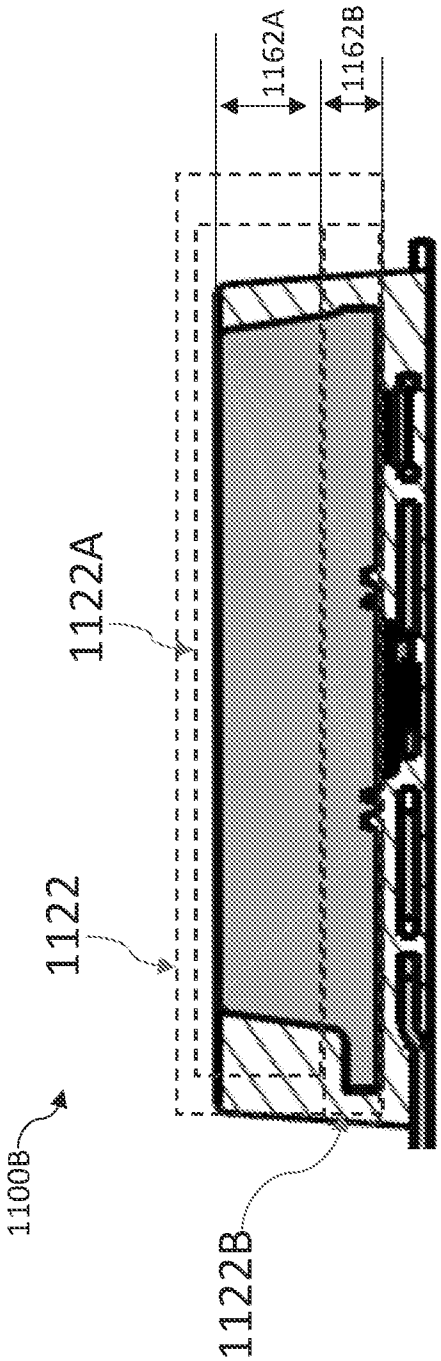

FIG. 11B

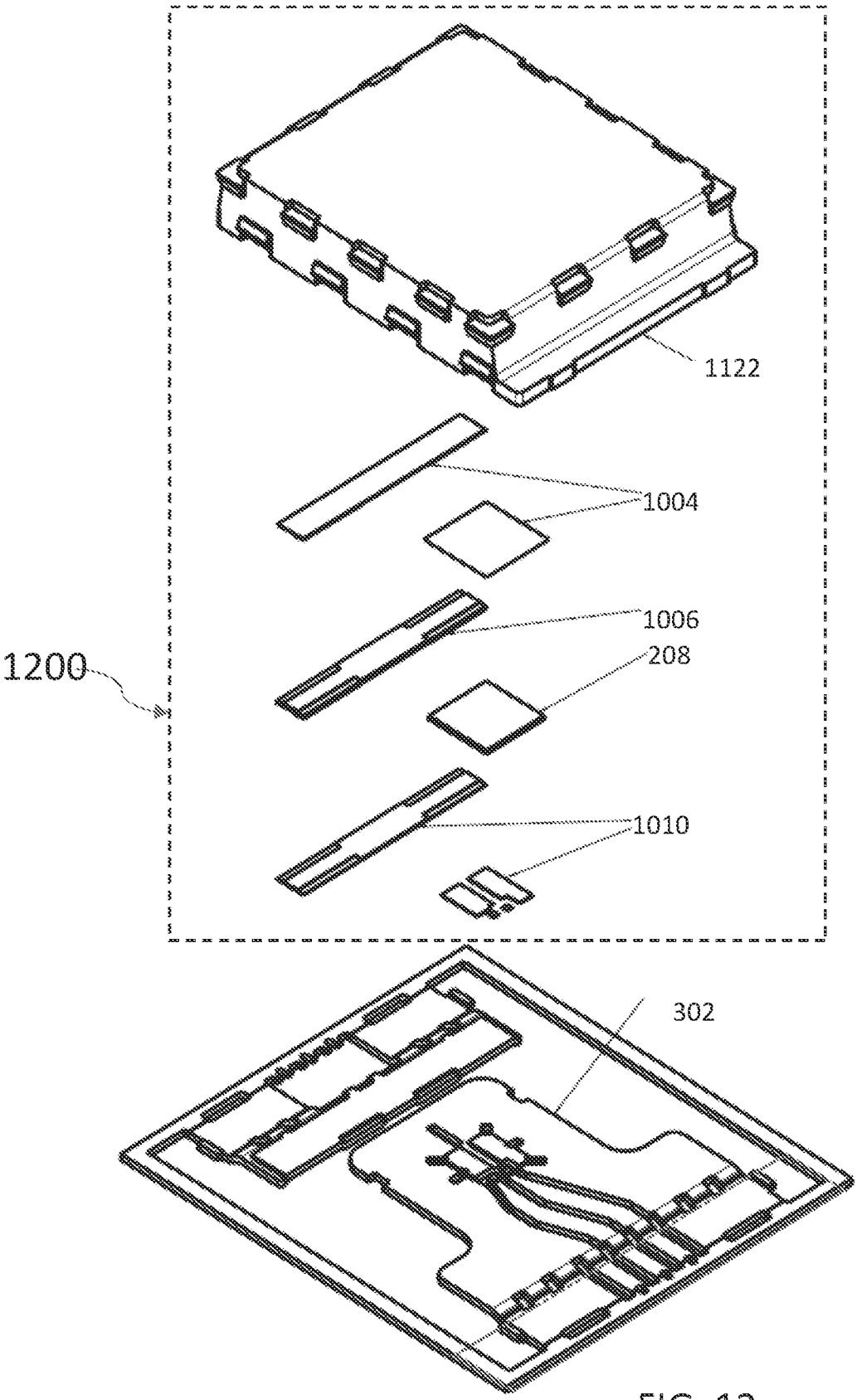

FIG. 12

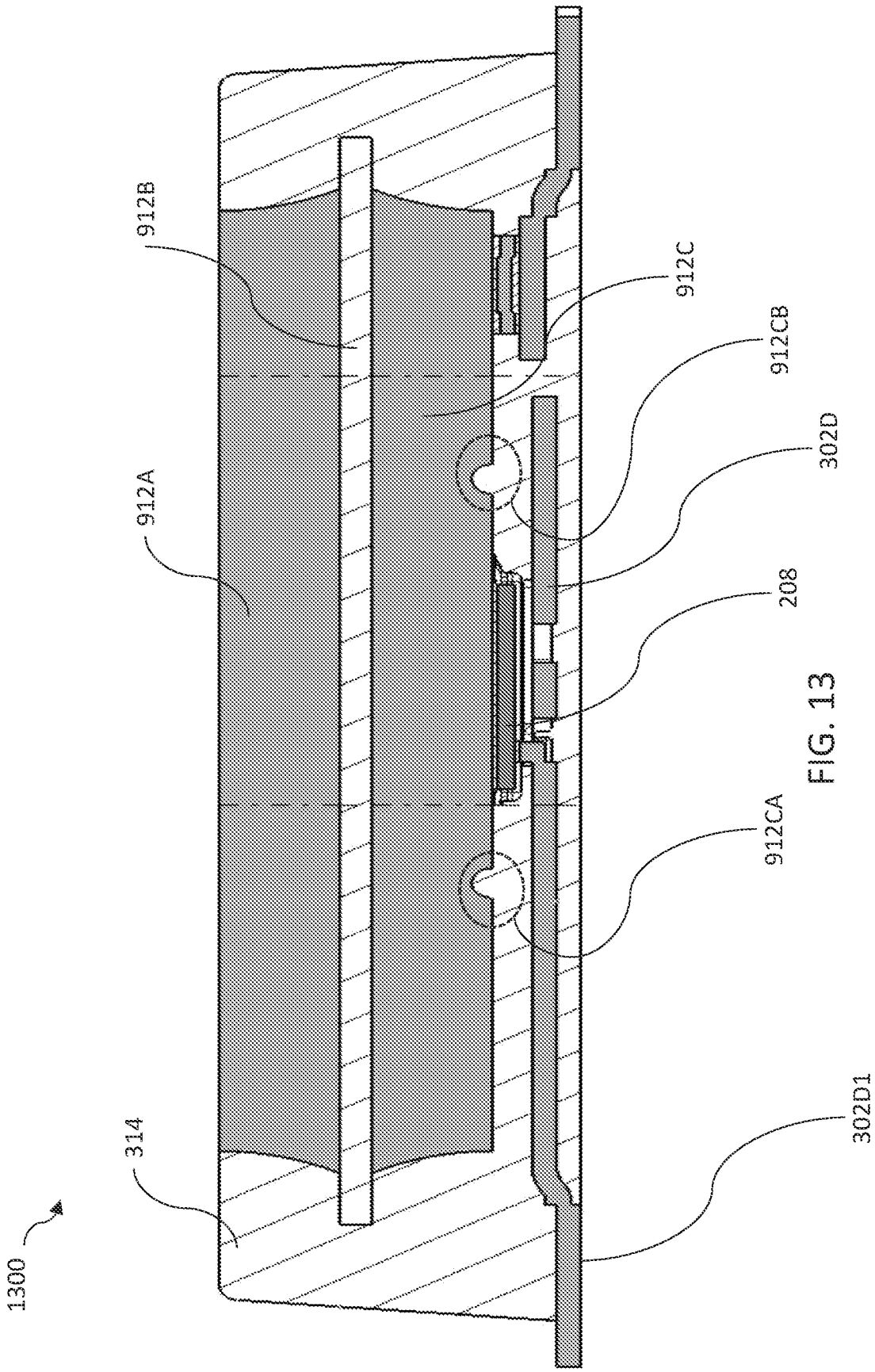

FIG. 13

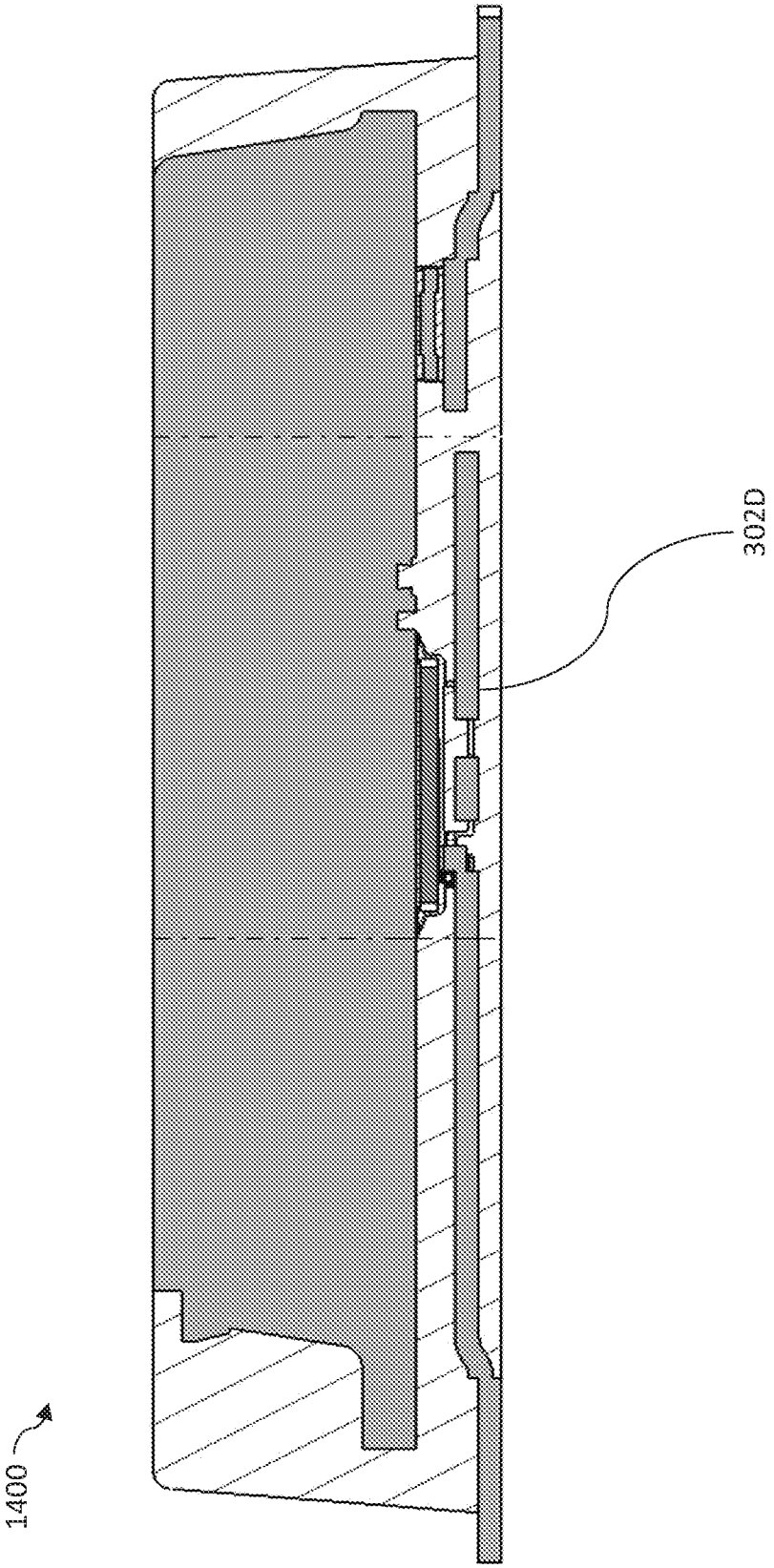

FIG. 14

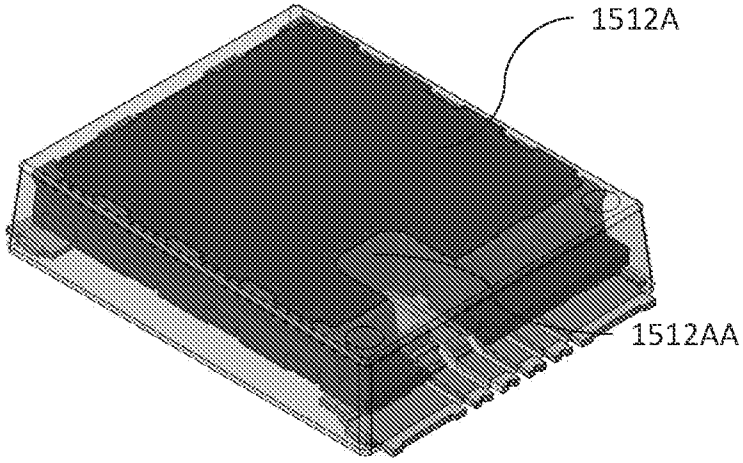

FIG. 15A

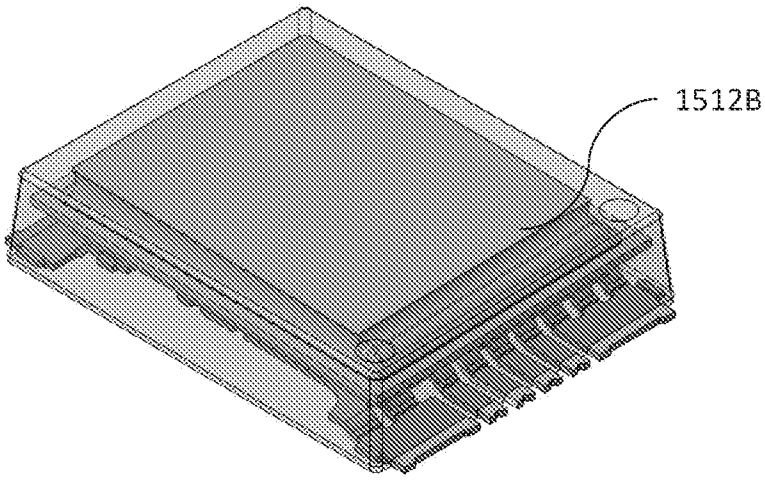

FIG. 15B

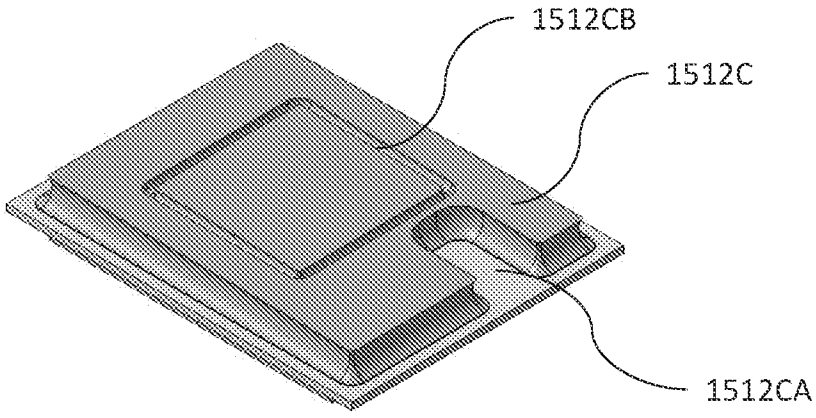

FIG. 15C

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2024/036356

A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L23/373 H01L23/31 H01L23/495
ADD. H01L23/433

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	JP 2015 211178 A (MITSUBISHI ELECTRIC CORP) 24 November 2015 (2015-11-24) paragraph [0013] paragraph [0023] paragraph [0028] paragraph [0035] - paragraph [0037] paragraph [0048] - paragraph [0049] figures 9-10	1,2,7,8, 10-13,19 6,14-18, 20

X Y	JP 2019 192877 A (DENSO CORP) 31 October 2019 (2019-10-31) paragraph [0019] paragraph [0023] paragraph [0025] paragraph [0027] - paragraph [0030] figure 1	1,7-13, 19 6,14-18, 20

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[x] Further documents are listed in the continuation of Box C.

[x] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance;; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance;; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 August 2024	12/09/2024

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Rodríguez San S., H

1

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2024/036356

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 2012 164697 A (MITSUBISHI ELECTRIC CORP) 30 August 2012 (2012-08-30)	1,3,7-12
Y	paragraph [0015] paragraph [0017] paragraph [0019] paragraph [0030] figures 6-7	4-6, 14-18

Y	US 2018/342438 A1 (CHEN LIU [DE] ET AL) 29 November 2018 (2018-11-29) paragraph [0045] - paragraph [0046] paragraph [0052] - paragraph [0053] paragraph [0066] - paragraph [0069] paragraph [0091] - paragraph [0094] figures 11-12	4,5, 14-18,20

Y	US 2022/157682 A1 (FUERGUT EDWARD [DE] ET AL) 19 May 2022 (2022-05-19) paragraph [0159] - paragraph [0160] figure 23	6,16

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2024/036356

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		US 2022157682 A1	19-05-2022
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