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GB 1394075
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EP A1 0067365

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G5C
G4A

(54) A series/parallel conversion circuit and display driver

(57) A series/parallel conversion circuit for use in a display driver circuit includes a plurality of first latch circuits (6) which latch a serial data signal, one bit or several bits at a time, the output of a counter (4) which counts a clock signal being decoded (5) to activate the first latch circuits (6) in succession to latch one bit or several bits of serial data simultaneously. After data has been latched into all of the first latch circuits, the data is output in parallel using second latch circuits (2). This reduces the number of gate circuits activated, and therefore reduces complexity and power consumption.

FIG. 2

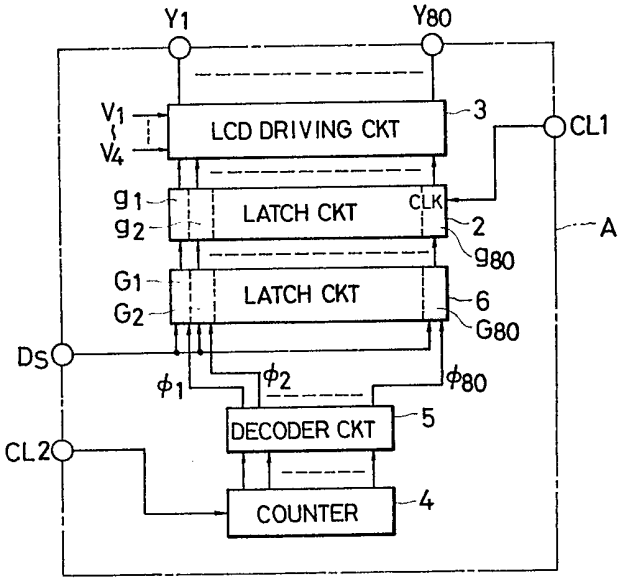

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FIG. 1

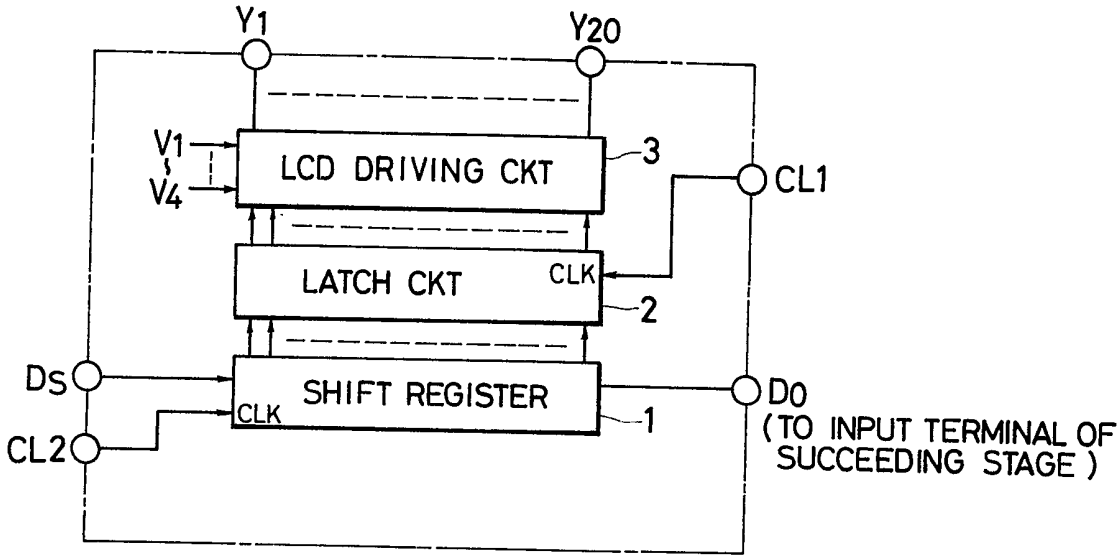

Y1
Y20
V1
V4
LCD DRIVING CKT
3
CL1
LATCH CKT
CLK
2
DS
SHIFT REGISTER
CLK
1
DO
(TO INPUT TERMINAL OF SUCCEEDING STAGE)
CL2

FIG. 2

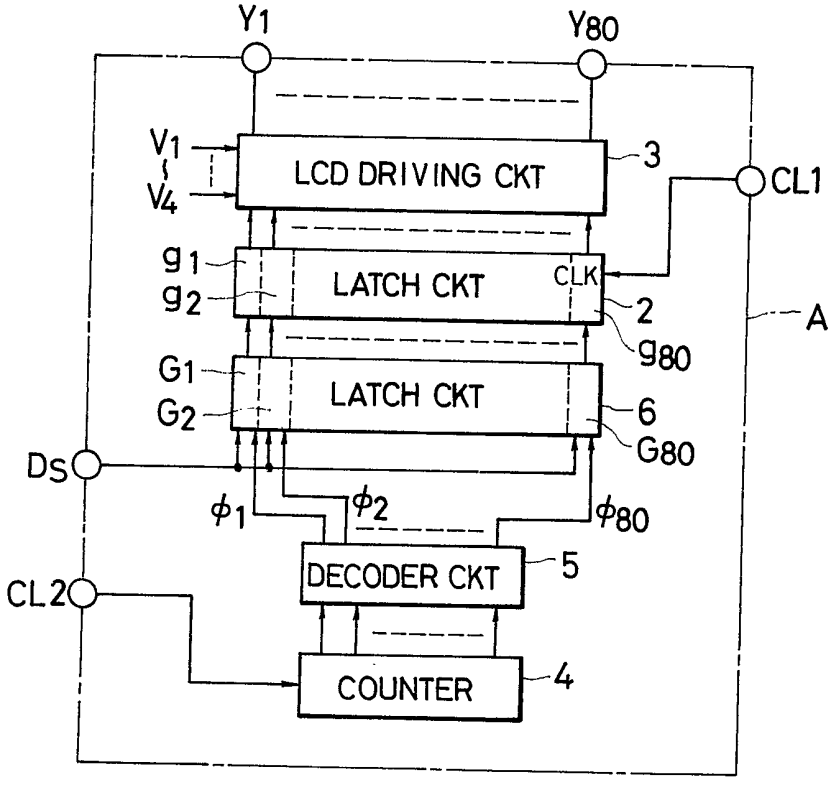

Y1
Y80
V1
V4
LCD DRIVING CKT
3
CL1
g1
g2
LATCH CKT
CLK
2
A
g80
G1
G2
LATCH CKT
6
G80
DS
φ1
φ2
φ80
DECODER CKT
5
CL2
COUNTER
4

FIG. 3

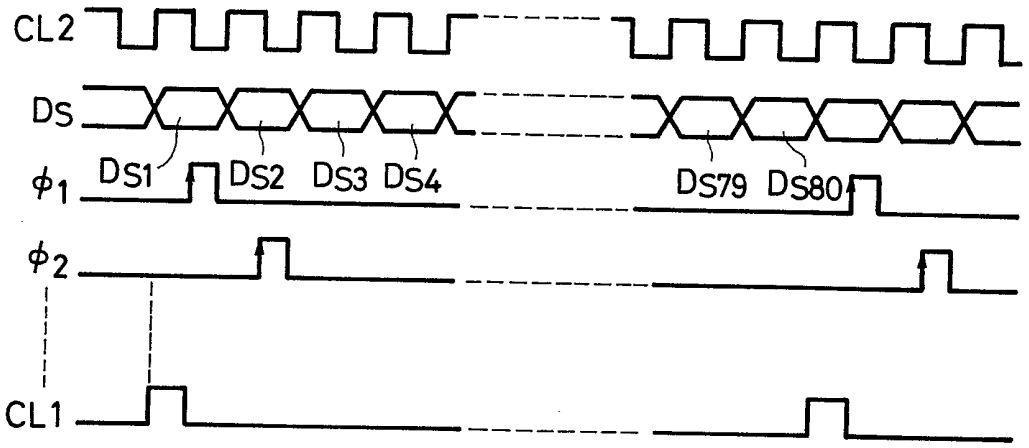

CL2
Ds
ϕ_1
DS1
DS2
DS3
DS4
DS79
DS80
ϕ_2
CL1

FIG. 4

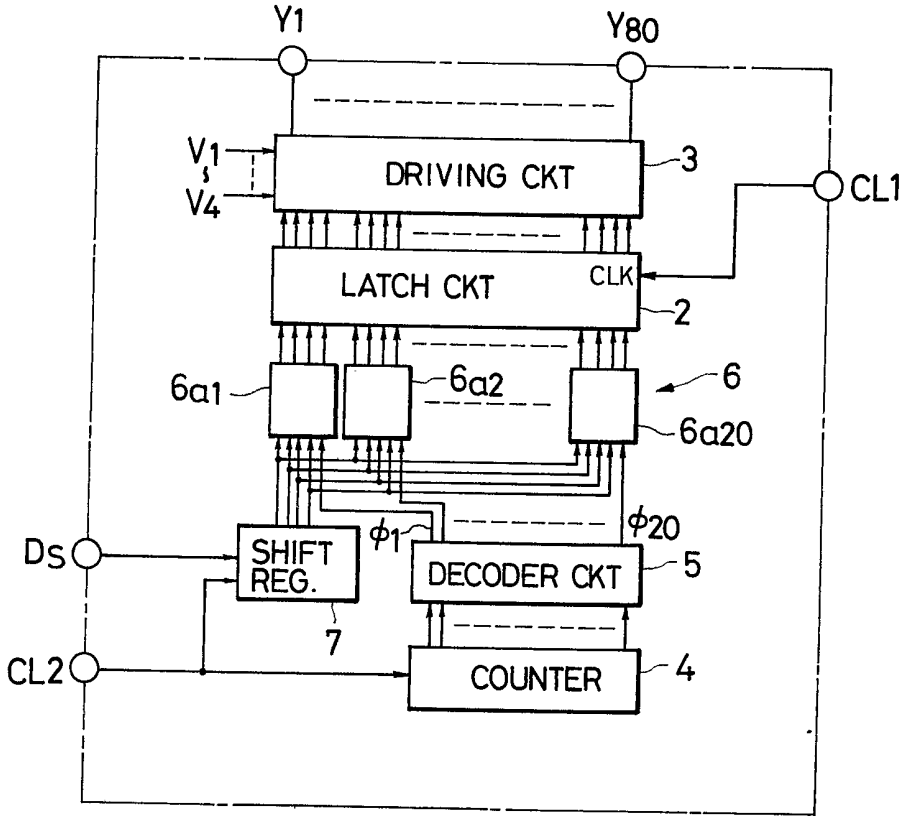

Y1
Y80
V_1
V_4
DRIVING CKT
3
CL1
LATCH CKT
CLK
2
6a1
6a2
6
6a20
ϕ_1
ϕ_{20}
Ds
SHIFT REG.
7
DECODER CKT
5
CL2
COUNTER
4

FIG. 5

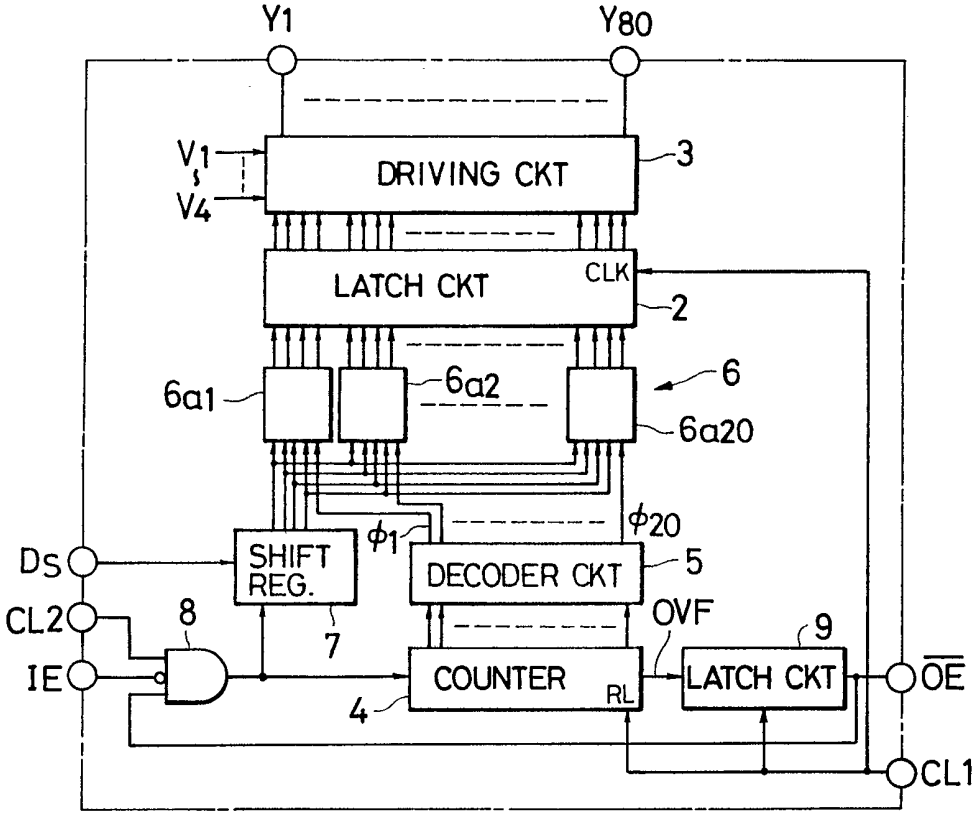

Y1
Y80
V1
V4
DRIVING CKT
3
LATCH CKT
CLK
2
6a1
6a2
6
6a20
Ds
SHIFT REG.
φ1
φ20
DECODER CKT
5
CL2
8
7
OVF
9
IE
COUNTER
RL
LATCH CKT
OE
4
CL1

FIG. 6

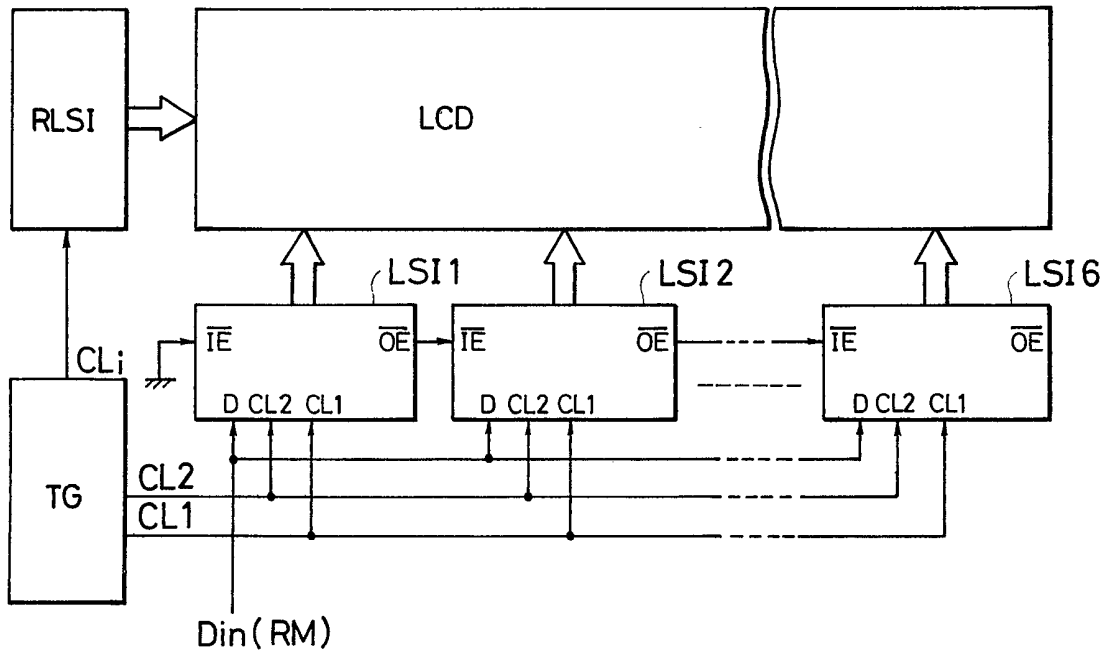

RLSI
LCD
LSI1
LSI2
LSI6
CLi
IE
OE
D CL2 CL1
TG
CL2
CL1
Din (RM)

FIG. 7

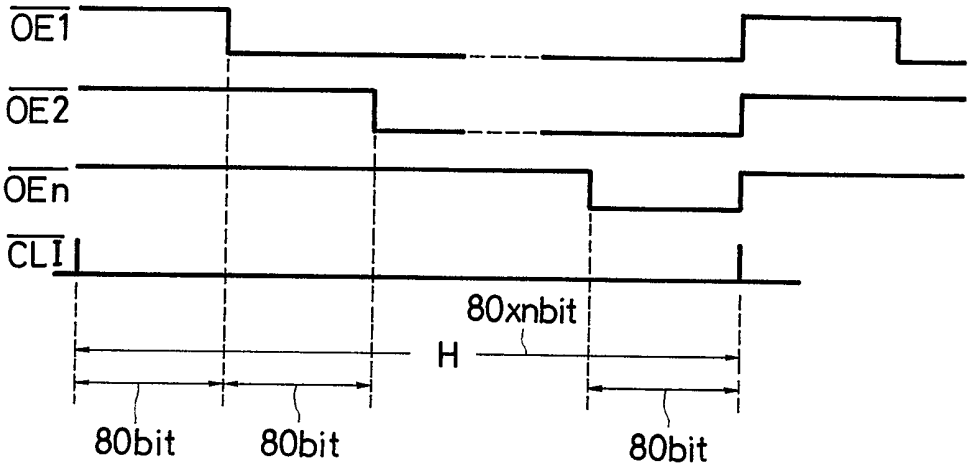

OE1
OE2
OEn
CLI
80xnbit
H
80bit
80bit
80bit

FIG. 8

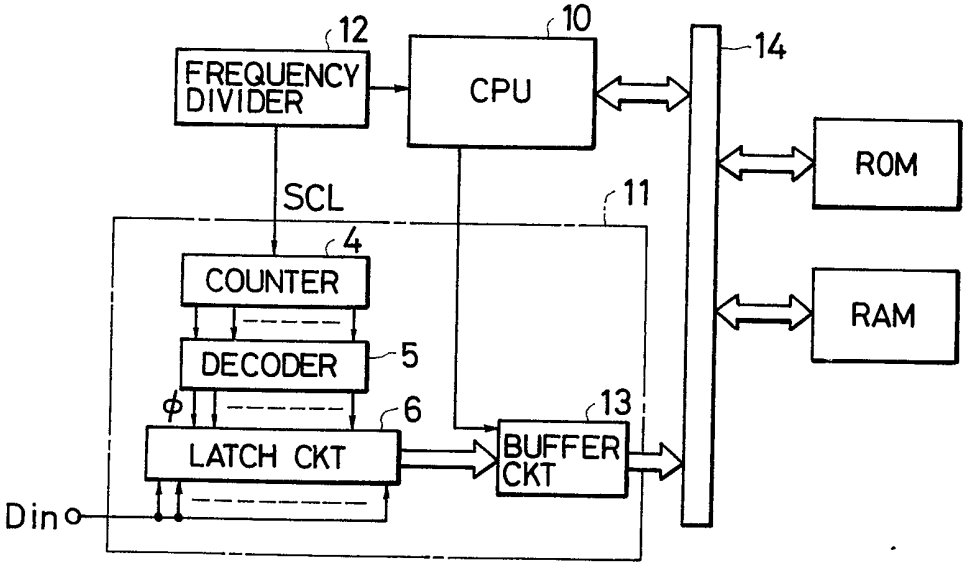

12
FREQUENCY DIVIDER
10
CPU
14
ROM
RAM
SCL
11
4
COUNTER
5
DECODER
φ
6
LATCH CKT
13
BUFFER CKT
Din

FIG. 9

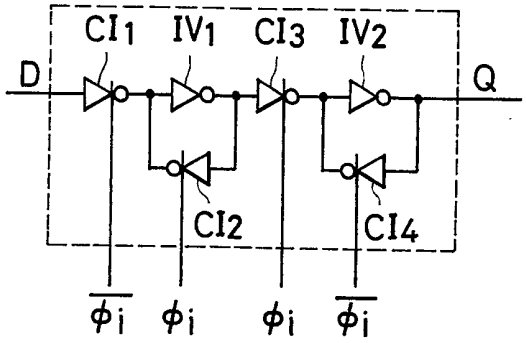
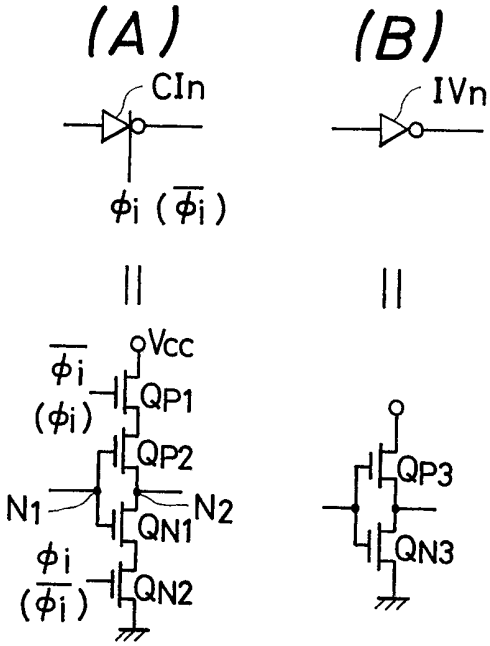

CI1
IV1
CI3
IV2
D
Q
CI2
CI4
$\overline{\phi i}$
ϕi
ϕi
$\overline{\phi i}$

FIG. 10


(A)
(B)
CIn
IVn
ϕi ($\overline{\phi i}$)
Vcc
$\overline{\phi i}$
(ϕi)
QP1
QP2
N1
N2
QN1
ϕi
($\overline{\phi i}$)
QN2
QP3
QN3

SPECIFICATION

A series/parallel conversion circuit and display driver device using this circuit

The present invention relates to semiconductor integrated circuit technology, and more specifically to a data transfer technique which is effective when used, for example, in a display driver which generates display drive signals for a serial input/output (I/O) device and a liquid-crystal display device (LCD), in a data processing system using a serial communication method.

When characters or figures are to be displayed on the display panel of a liquid-crystal device with a dot-matrix structure, image signals corresponding to the characters or figures to be displayed are supplied to the signal line electrodes according to a selection timing set by scanning line electrodes. A typical liquid-crystal drive LSI that generates drive signals for signal line electrodes is shown in Figure 1 of the accompanying drawings. For instance, reference may be made to page 34 of Hitachi MOS LSI Data Book LCD Driver LS2 published by Hitachi Ltd., March 1983.

In the liquid-crystal driver LSI, as seen in Figure 1, serial image signal data D_s (character patterns, etc.) read out from a refresh memory is supplied and shifted in synchronism with a clock signal CL2 into an internal shift register 1 and, all of the bits of the data in the shift register 1 are latched simultaneously into a latch circuit 2 in synchronism with a clock signal CL1 supplied at the selection timing of the scanning line electrodes. Thus, serial/parallel conversion of the image signal data is carried out. Depending on the data held in the latch circuits 2, an LCD driver circuit 3 forms and outputs a drive signal of an appropriate level for the signal line electrodes.

The liquid-crystal driver has a fixed number of output terminals, so that in order to drive a display panel which has more signal line electrodes than the number of the output terminals of one liquid-crystal driver, a plurality of liquid-crystal drivers must be connected to a longitudinal configuration.

With the liquid-crystal driver, however, since the serial/parallel conversion of data is performed by using a shift register, all the flip-flops making up the shift register are activated simultaneously when inputting image signal data.

The liquid-crystal driver is constituted by CMOS stages (complementary MOSFETs) in order to reduce the power consumption. However, since the current consumption of a CMOS LSI increases with the operating frequency, the current consumption of the entire liquid-crystal driver increases as the size of the display panel becomes larger.

When the liquid-crystal display device is driven at frequencies below 70Hz, the display seems to flicker when illuminated by conventional lighting, such as a fluorescent lamp powered by the mains power supply (50 Hz). Even when the dot structure of the display panel of a liquid-crystal display device is increased, and more liquid-crystal drivers are connected in series, the period during which a certain signal line electrode is driven becomes longer if the liquid-crystal drivers are activated by clock signals (CL1, CL2) of the same frequency as that used for a smaller number of drivers. This means that the drive frequency of the entire display panel decreases.

With a display panel with a large number of dots, to prevent the drive frequency dropping below 70 Hz, it is necessary to increase the frequency of the clock signals supplied to the liquid-crystal driver. As a result, the current consumption of the liquid-crystal driver increases. These are the problems with conventional liquid-crystal drivers.

It is an object of the present invention to provide a serial/parallel conversion circuit with a small current consumption, and a display driver using this circuit.

It is another object of the invention to provide a display driver which has a small current consumption and an operating function for providing a clear display.

According to one aspect of the present invention there is provided a series/parallel conversion circuit including: a counter circuit connected to receive and count clock signals; decoder means connected to said counter circuit for decoding the content of said counter circuit to produce successive output signals in synchronism with said clock signal; and a latch circuit made up of a plurality of gate circuits, each of said gate circuits having a latch function, said latch circuit being connected to receive a serial data signal at said gate circuits and to receive said output signals from said decoder means in synchronism with said clock signal so that respective serial data is latched in respective gate circuits; whereby all data input to said latch circuit as serial data may be transferred from said latch circuit in response to a control signal simultaneously as parallel data.

According to a second aspect of the present invention there is provided a display driver device including: a counter circuit connected to receive and count clock signals; decoder means connected to said counter circuit for decoding the content of said counter circuit to produce successive output signals in synchronism with said clock signal; a latch circuit made up of a plurality of gate circuits, each of said gate circuits having a latch function, said latch circuit being connected to receive a serial data signal at said gate circuits and to receive a serial data signal at said gate circuits and to receive said output signals from said decoder means in synchronism with said clock signal so that respective serial data is latched in respective gate circuits; and means including a display driver circuit connected to said latch circuit for receiving and holding all bits of said image signal data from said latch circuit simultaneously, whereby said image signal data may be output in parallel as line drive signals to an external display device.

The present invention will now be described in greater detail by way of example with reference to the remaining figures of the accompanying drawings, wherein:

Figure 2 is a block diagram of a first embodiment of a series/parallel conversion circuit, applied to a liquid-crystal driver;

Figure 3 is a waveform diagram of clock signals and image signal data used for the operation of the display device;

Figure 4 is a block diagram of a second embodiment of a series/parallel conversion circuit, applied to a liquid-crystal driver;

Figure 5 is a block diagram of a third embodiment of a series/parallel conversion circuit, applied to a liquid-crystal driver;

Figure 6 is a block diagram of one example of a display device using the liquid-crystal driver shown in Figure 5;

Figure 7 is a waveform diagram of one example of the display operation;

Figure 8 is a block diagram of one of the above embodiments of a series/parallel conversion circuit applied to a serial I/O device of a micro-computer system;

Figure 9 shows an example of a logic circuit of a static flip-flop; and

Figure 10(A) and *(B)* show examples of the circuits of a clocked inverter and an inverter, respectively.

Referring first to Figure 2, the circuit blocks contained within the one dotted chain line A are formed on a semiconductor substrate, such as single-crystal silicon, by known CMOS integrated circuit manufacturing technology. The liquid-crystal driver is formed of complementary MOSFETs, although it may not be restricted thereto. The liquid-crystal driver drives signal line electrodes of a liquid-crystal display panel of a dot-matrix construction which consists of scanning line electrodes and signal line electrodes. The driver generates drive signals for 80 signal line electrodes in this embodiment. In order to generate drive signals for the 80 signal line electrodes at the scanning line electrode selection timing, a counter 4, a decoder circuit 5, a latch circuit 6, a second latch circuit 2, and a drive circuit 3 are provided.

A clock signal C12 of the same period as the serial image signal data Ds supplied from external terminals is supplied to the counter 4 and is thereby counted. The counter 4 is preferably constructed so that it can count up to the same number (80) as the number of bits within the latch circuits 6 and 2. In other words, when the count reaches "79", the counter returns to "0" and continues counting the clock signal CL2.

The counter 4 consists of a plurality of gate circuits, connected in series, each of which is constructed for example as a static type flip-flop circuit. Each static flip-flop is formed of complementary MOSFETs. Output signals from the counter 4 are taken from output points of the gate circuit in each stage and are supplied to the decoder circuit 5.

The decoder circuit 5 comprises a plurality of unit decoders (gate circuits), in this embodiment 80 unit decoders. It accepts the output signals from the counter 4, and decodes and forms selection signals ø1 to ø80. Each unit decoder is preferably formed of a static NOR gate circuit consisting of complementary MOSFETs.

The selection signals ø1 to ø80 output from decoder circuit 5 are supplied to each gate circuit making up the latch circuit 6. The latch circuit 6 comprises gate circuits G1 to G80, each of which is formed of a static flip-flop consisting of complementary MOSFETs, for example. Each gate circuit is supplied with the corresponding selection signal. For example, the gate circuit G1 is supplied with selection signal ø1, and the gate circuit 80 with selection signal ø80. Input operation of the gate circuits is controlled by the supplied selection signal.

In this way, a gate circuit specified by the selection signals ϕ 1 to ϕ80 is selected among the gate circuits G1 to G80 in the latch circuit 6, and the image signal data Ds is inputted and held in the selected gate circuit. Namely, though the serial image signal data Ds supplied from external terminals is supplied in common to each gate circuit G1 to G80, each bit of the image signal data is supplied and held in the gate circuit specified by the selection signals ϕ1 to ϕ80 issued in synchronism with the clock signal CL2.

As the counter 4 counts up the clock signal CL2, the selection signals are outputted from the decoder circuit 5 in the order of ϕ1, ϕ2 ... ϕ80. According to these selection signals, the gate circuits G1 to G80 operate to input the data sequentially from one end of the latch circuit 6 to the other, in subindex order. According with this, a total of 80 bits of the image signal data Ds are successively applied to and held in the latch circuit 6. In the example shown in Figure 3, the data bit Dsl is inputted to gate circuit Gl and held there, and data bit Ds2 is inputted to gate circuit G2 and held there. Similarly, data bit Ds80 is inputted to gate circuit G80 and held there.

When all 80 bits of the image signal data Ds have been inputted to the latch circuit 6, a clock signal CL1 is supplied from external terminals to the second latch circuit 2. The second latch circuit 2, in the same way as the latch circuit 6, comprises a plurality of gate circuits, in this embodiment 80 gate circuits g1 to g80. Each gate circuit g1 to g80 is formed, for example, of a flip-flop which receives an output signal from the corresponding gate circuit G1 to G80. More specifically, the output signal from gate circuit G1 is supplied to the input terminal of gate circuit g1, and the output signal from gate circuit G80 is supplied to the input terminal of gate circuit g80. Each of the gate circuits g1 to g80 receives and holds the corresponding output signal from latch circuit 6 supplied to its input terminal in synchronism with the clock signal CL1. Thus, the latch circuit 2 receives and holds all the 80 bits of image signal data which are held in and outputted from the latch circuit 6 simultaneously in synchronism with the clock signal CL1. In this way, serial image signal data is converted into parallel signals.

The driver circuit 3 processes, according to an appropriate timing signal (not shown), the image signal data held in and outputted from the latch circuit 2, and forms drive signals Y1 to Y80, each of which consist of multi-value pulses for AC-driving the corresponding liquid crystals. Voltages V1 to V4 are supply voltages used to generate the multi-value pulses, and are supplied from external sources. The method of AC-driving the liquid crystals is known and so a detailed description thereof is omitted.

As described above, in this embodiment, the clock signal CL2 of the same period as the serial image signal data Ds is counted by the counter 4. The count is decoded by the decoder circuit 5, and the stages of the first latch circuit 6 are successively enabled by

the output signals (selection signals) of the decoder circuit 5. So, compared with the circuitry of Figure 1, the number of gates to be operated when converting an 80-bit group of serial image signal data Ds into parallel signals is considerably reduced.

Namely, in the circuitry shown in Figure 1, in order to convert the n bits of serial data into parallel signals, it is necessary to operate both of the gate circuits (flip-flops) of n stages which form the shift register 1 and the gate circuits (flip-flops) of n stages which form the latch circuit 2. Thus, if the frequency of the clock signal CL1 (latch clock) supplied to the latch circuit 2 is assumed to be f, the clock signal CL2 (shift clock) supplied to the shift register 1 will have to have a frequency of nf. In a static CMOS circuit composed of complementary MOSFETs, current consumption is proportional to the operating frequency.

In the case where each gate circuit is composed of a static CMOS circuit with the circuit form of Figure 1, in order to reduce the current consumption of the liquid-crystal driver, the current consumption of the shift register 1 is proportional to $n \times nf = n^2f$, because the n gate circuits (static CMOS flip-flops) operate at a frequency of nf. In addition, in the latch circuit 2, n gate circuits (static CMOS flip-flops) operate at a frequency f, so that its current consumption is proportional to $n \times f = nf$. If it is assumed that the current consumed when the gate circuits of the shift register 1 are activated is equal to the current consumed by the operation of the gate circuits making up the latch circuit 2, then the total current consumption will be approximately proportional to the sum of these current consumption, i.e., proportional to $n^2f + nf = (n^2 + n)f$.

In accordance with the present invention, on the other hand, the clock signal CL2 can be counted from 0 to $(n - 1)$ if the smallest integer m that satisfies $2^m > n$ is selected, and the counter 4 is constructed of that number of bits. The current consumed when an m-bit counter 4 counts the clock signal CL2 of a frequency nf is as follows. Namely, the current consumption at the least significant bit portion of the counter 4 is proportional to nf, the current consumption at the next bit portion is proportional to nf/2, and that at the next bit portion is proportional to nf/4. In this way, the current consumption is reduced sequentially by a factor of 1/2, so that the current consumption of the most significant bit is proportional to $nf/2^m$. Therefore, the total current consumption of the counter is proportional to $nf \times (1 + 1/2 + 1/4 + ... + 1/2^m)$. Since the sum of the serial $1 + 1/2 + 1/4 + ... + 1/2^m$ does not exceed 2, the current consumption of counter 4 is less than a value proportional to 2nf. In this embodiment, when the decoder circuit 5 drives an n-bit latch circuit, only two of the n gate circuits (unit decoders) of the decoder circuit 5 operate at the same time, including the one which resets the original state. The number of gate circuits which are activated within the latch circuit 6 by the output signals (selection signals) from the decoder circuit is one. Thus, 2n gate circuits in the decoder circuits operate at frequency f, and, n gate circuits in the latch circuit 6 operate at frequency f. Therefore the current consumption of the decoder 5 is proportional to 2nf, and that of latch circuit 6 is proportional to nf. The latch circuit 2, which is operated by the clock signal CL1, has the same current consumption as that of Figure 1.

If it is assumed that the current consumption of each of the gate circuits of the counter 4, the current consumption of each of the gate circuits of the decoder circuit 5, and the current consumptions of each of the gate circuits of the latch circuits 6 and 2 are equal to each other, that is, if the current consumption per bit is the same for the counter 4, the decoder circuit 5, and the latch circuits 6 and 2, then the current consumption of this embodiment is approximately proportional to $6nf = (2nf + 2nf + nf + nf)$.

If the current consumption of the gate circuits of the circuitry of Figure 1 is virtually equal to that of the gate circuits of this embodiment, and if there are 6 or more bits, the relationship $6nf < (n^2 + n)f$ holds. In other words, when converting serial data made up of 6 or more bits into parallel signals, the number of gate circuits to work in this embodiment is $6/(n + 1)$, less than that of Figure 1, and the total current consumption is also reduced. Taking $n = 80$ as an example, as in this embodiment, the number of gates working is about 1/13 that of Figure 1 and a substantial reduction in current consumption is achieved.

Figure 9 shows an example of a logic circuit used for the gate circuits that make up the latch circuits 2, 6 and the counter 4. In the Figure, C11 to C14 are clocked inverters, and IVI and IV2 are inverters. These inverters make up a static flip-flop used as gate circuit.

This flip-flop takes in a signal supplied to an input terminal D when a control signal $\overline{\phi i}$ goes high. When a control signal i ϕ goes high, the flip-flop holds that signal, and at the same time outputs the signal through an output terminal Q. When control signal $\overline{\phi i}$ goes high again, a signal supplied to the input terminal D at that time is accepted. During this time, the previous signal is still output from the output terminal Q.

Thus, when the control signal $\overline{\phi i}$ goes high, the clocked inverter CI1 operates and supplies the inverter IV1 with an inverted version of the signal supplied the input terminal D. Next, when the control signal ϕi goes high again, the clocked inverters CI2, CI3 operate. According with this, a latch circuit is formed by the inverter IV1 and the clocked inverter CI2, and the signal is held in the latch circuit. The held signal is then outputted through the clocked inverter CI3 and the inverter IV2 from the output terminal Q. After this, when control signal $\overline{\phi i}$ goes high again, the clocked inverter CI4 operates. According to this operation, the inverter IV2 and the clocked inverter CI4 from a latch circuit when holds the signal being outputted from the output terminal Q, and therefore the signal continues to be outputted.

Control signal $\overline{\phi i}$ and control signal ϕi are inverted in phase with respect to each other. Accordingly, when clocked inverters CI1, CI4 are given a high-level control signal $\overline{\phi i}$ and are operational, then the clocked inverters CI2, CI3 are given a low-level

control signal ϕi, making them non-operational. Similarly, when the clocked inverters CI2, CI3 are operational, clocked inverters CI1, CI4 are made non-operational.

In this embodiment, the clocked inverter CIn and the inverter IVn are formed of CMOS circuits, as shown in Figure 19(A) and Figure 10(B), respectively, although this is not essential to the invention.

The clocked inverter shown in Figure 10(A) is made operational when a low-level control signal $\overline{\phi i}$ (or ϕi) is supplied to a p-channel MOSFET QP1 and a high-level control signal ϕi (or $\overline{\phi i}$) to an n-channel MOSFET QN2, so that the clocked inverter outputs to a node N2 a signal according to a signal supplied to a node N1. On the other hand, this clocked inverter is made non-operational when a high-level control signal $\overline{\varnothing i}$ (or $\varnothing i$) is supplied to p-channel MOSFET PQ1 and a low-level control signal $\varnothing i$ ($\overline{\varnothing i}$)to n-channel MOSFET QN2. For example, if the signal supplied the clocked inverter when it is operational changes, MOSFETs QP1, QP2 and QN1, QN2 all turn on temporarily so that a through current and charging and discharging current for a capacitive load consisting of a stray capacitance and an input capacitance to a succeeding stage, pass to the clocked inverter. Similarly, in the CMOS inverter, when the input signal changes, MOSFETs QP3, QN3 making up the inverter turn on temporarily so that a through current and charging and discharging current for a capacitive load consisting of a stray capacitance and an input capacitance to a succeeding stage, pass to the inverter.

Therefore, in the flip-flop shown in Figure 9, when the control signal $\overline{\varnothing i}$ is made to go high so that a signal is inputted, and for instance, the input signals to the clocked inverter CI1 and the inverter IV1 are changed, through currents flow to the circuits. Moreover, when the control signal $\varnothing i$ is made to go high in order to hold and output the held signal, and the input signal to the clocked inverters C12, C13 and inverter IV2 are changed, through currents flow to these inverters.

In this embodiment, the number of flip-flop gate circuits working is smaller than that of the circuitry of Figure 1. Namely, the number of flip-flops that input and hold signals is reduced. This means that the through currents of the clocked inverters and the inverters of the flip-flops are reduced, and therefore the total current consumption is reduced. For instance, the latch circuit 6 made up of the flip-flops is considered, selection signals from a selection circuit (in this embodiment, it is formed by the decoder circuit 5 and the counter 4) are used as control signals for the flip-flops. The image signal data is applied to the input terminal D and signals from the output terminal D are supplied to the latch circuit 2. Namely, for example, the selection signal $\varnothing 1$ is supplied to the flip-flop of the gate circuit G1 as its control signal $\overline{\phi i}$. Thus, the selection signal $\overline{\phi i}$ which is an inversion of the selection signal $\phi 1$ is supplied to the flip-flop. The flip-flop which forms the gate circuit G1 operates only when the selection signal $\phi 1$ is issued from the decoder circuit 5. That is, it takes in the image signal data Ds and holds the data. After this, the flip-flop holds the image signal data Ds until the selection signal $\varnothing$ 1 is output again. While the data is being held in the inverters IV1, IV2 and the clocked inverters CI2, CI3, since only the MOSFETs (QP3 or QN3, and QP2 or QN1) which correspond to the input signal are held at the on state, through current will not flow to the flip-flop. As a result, the total current consumption can be reduced.

Incidentally, if the counter 4 is formed of these flip-flops, a plurality of flip-flops are connected in series. In addition, if the latch circuit 2 is formed of these flip-flops, a signal is supplied from the output terminal of gate ciruit Gn to the corresponding input terminal D of the flip-flop, and a signal from the output terminal Q is supplied to the LCD driver circuit 3. This control signal CL1 is used as its control signal $\overline{\phi i}$, and an inversion of the control signal CL1 is used as control signal ϕi.

As can be seen from the above description, as the size of the liquid-crystal display panel being driven increases, and the number of its signal line electrodes increases, and also the number of bits in the image signal data Ds, i.e., the number of bits of the latch circuit 2, increases, the reduction in the number of operating gates and the current consumption of this embodiment becomes conspicuous.

Though, in this embodiment, the counter 4 is previously constructed with hardware so that it can count up to the same number as that of the bits in the latch circuits 2 and 6, the counter can be constructed otherwise. For example, the externally-supplied clock signal CL1 can be used as a reset signal for the counter. In this case, the counter is constructed so that when it has counted the clock signal CL2 from 0 to (n − 1), it is reset by the reset signal and starts counting again.

Furthermore, although in the above embodiment the display driver circuit is made up of the latch circuit 2 and the driver circuit, it is not restricted to that construction. For instance, the driver circuit 3 itself can be provided with a latch function.

Next, a second embodiment of this invention applied to a liquid-crystal driver will be described with reference to Figure 4. In this embodiment, twenty unit latch circuits 6a each of which includes a 4 bit unit, make up the first latch circuit 6.

Each unit latch circuit 6a in the first latch circuit 6 is composed of four status flip-flops, each being formed of the CMOS circuit described with reference to Figure 9. The four static flip-flops receive in common a selection signal outputted from the decoder circuit 5, as will be described later. When the common selection signal is supplied, the four flip-flops take in and hold signals from a shift register (described later). The flip-flops hold the held signals until the selection signal is supplied again, that is, they remain in a hold condition.

In this embodiment, a common shift register 7 is provided for the plural unit latch circuits 6a. The shift register 7 is made up of, for instance, four of the static flip-flops described with reference to Figure 9. The shift register 7 is driven by the clock signal CL2 to take in serial image signal data Ds four bits at a time, and shift them. The four signals outputted in parallel from the shift register 7 are supplied to each unit latch circuit 6a1 to 6a20. That is, the data

contained in the shift register 7 is transferred in parallel to the unit latch circuits 6a1 to 6a20 which make up the latch circuit 6.

In Figure 4, a counter 4 has a similar construction to that of the embodiment of Figure 2. The counter 4 counts the clock signal CL2. Unlike the first embodiment, the decoder circuit 5 does not form 80 different selection signals, but decodes appropriate signals at each stage of the counter 4, and thereby forms and outputs selection signals $\phi 1$ to $\phi 20$ for each four pulses of the clock signal CL2.

The selection signals $\phi 1$ to $\phi 20$ are successively supplied to the unit latch circuits 6a1 to 6a20 of the latch circuit 6. The four bits of data inputted to the shift register 7 at first are latched into the first unit latch circuit 6a1 in synchronism with the timing of selection signal $\phi 1$, and are held there. The next four bits of data inputted to the shift register 7 are latched into the second unit latch circuit 6a2, in synchronism with the timing of selection signal $\phi 2$, and are held there.

After 80 bits of image signal data Ds have been divided into 4-bit data sections and each 4-bit data section has been transferred to one of the unit latch circuits 6a1 to 6a20, the clock signal CL1 is applied to the second latch circuit 2, and the 80 bits of data held in the first latch circuit 6 are transferred to the second latch circuit 2 simultaneously. This converts the serial image signal data Ds into parallel signals. After this, in the same way as in the first embodiment, the signal lines of the liquid-crystal display device are driven by the operation of the driver circuit 3.

In this second embodiment, although the number of the gates of the shift register 7 increases, the number of gates in the decoder circuit 5 decreases from 80 to 20, compared with the first embodiment. Thus, the counter circuit and the decoder circuit for shaping the selection signals to activate the unit latch circuits 6a1 to 6a20 are simplified, making the circuit design on the counter circuit said easier.

Next, a third embodiment of this invention applied to a liquid-crystal driver will be described. In this embodiment, a new circuit is added to ensure the desired operation of the LSI liquid-crystal drivers which are connected in series so as to increase the number of drive signals to cope with the situation in which a large display panel is used and the number of signal line electrodes of the liquid-crystal display device is greater than the number of outputs of drive signals Y1 to Y80 of liquid-crystal drivers.

With this embodiment, as shown in Figure 5, the clock signal CL2, which in the embodiment of Figure 4 is supplied to the shift register 7 and the counter 4, is supplied to an AND gate circuit 8. An inverted control signal supplied from an external terminal $\overline{IE}$ and an output signal Q of a third latch circuit 9 are used as control signals for the AND circuit 8. The third latch circuit 9 is formed of flip-flops.

This latch circuit 9 makes the output signal Q fall from high level to low level, when it receives an overflow signal OVF from the counter 4 which counts the clock signal CL2. The output signal Q of the latch circuit 9 is outputted from an external terminal $\overline{OE}$. Here, the counter circuit is formed of the counter 4 and the latch circuit 9. The clock signal CL1 supplied from an external terminal is supplied to a clear terminal RL of the counter 4 and the latch circuit 9, and to a clock terminal CLK of the latch circuit 2.

With the liquid-crystal driver of this embodiment, when the external terminal $\overline{IE}$ is made to go low with the reset state of the latch circuit 9 (when its output signal Q is at high level), and AND gate circuit 8 opens, supplying the clock signal CL2 to the shift register 7 and the counter 4. As described with reference to Figure 4, the serial image signal data Ds is successively inputted and held in the latch circuit 6 in synchronism with the tming of clock signal CL2. When 80 clock signals C12 have been supplied and 80 bits of image signal data have been inputted, the counter 4 overflows, making the output signal Q of latch circuit 9 go low, thereby closing the AND gate circuit 8. Therefore, the image signal data is held in the latch circuit 6, even when the succeeding clock signal CL2 occurs.

If the clock signal CL1 is generated when scanning line electrodes have been switched, the contents of the latch circuit 6 are transferred to the second latch circuit to provide a display according to the image signal data received. At the time, since the counter 4 and latch circuit 9 are reset by the clock signal CL1, the AND gate circuit 8 is opened again. This enables the input of the image signal data corresponding to the next scanning line electrode.

Figure 6 shows a block diagram of one example of a display device using a plurality of the liquid-crystal drivers shown in Figure 5.

The display device of this embodiment uses a large size liquid-crystal display panel LCD, which has, for instance, 480 signal line electrodes in lateral direction (480 dots) and 64 scanning line electrodes in the vertical direction (64 dots). In order to cope with this expansion of the display area, six of the liquid-crystal drivers of Figure 5 are used to form drive signals for the 480 signal line electrode. To provide control signals $\overline{IE}$ and $\overline{OE}$ in this case, the six liquid-crystal drivers LSI1 to LS16 are connected in a cascade configuration. Namely, the control signal terminal $\overline{IE}$ of the first-stage liquid-crystal driver LSI1 is constantly supplied with a low level such as the earth potential of the circuit. Its control signal terminal $\overline{OE}$ is connected to the control signal terminal $\overline{IE}$ of the liquid-crystal driver LSI2 in the next stage, and all the control signal terminals $\overline{OE}$ and $\overline{IE}$ are connected successively in this way.

The input data terminal D and the clock terminals CL1 and CL2 of the liquid-crystal drivers LSI1 to LSI6 are each connected in common. A clock signal generated by a timing generator circuit TG is supplied to the clock terminals CL1 and CL2. Although not especially restricted thereto, image signal data which was serially read out, for example, from a refresh memory according to the scan timing of the scanning electrode is supplied to all the input data terminals D.

The scanning line electrodes of the liquid-crystal display panel LCD are activated, although not especially restricted thereto, by the liquid-crystal driver LSIs which form drive signals for the scanning line

electrodes according to the clock signal CL1 supplied from the timing generator circuit TG.

Next, an example of the display operation of this embodiment will now be described with reference to the waveform diagram of Figure 7. When all the liquid-crystal drivers LSI1 to LSI6 are reset by the clock signal CL1, the latch circuit 9 of each driver is also reset, making the control signal terminal $\overline{OE}$ go high. This closes the AND gate circuit 8 of the drivers LSI2 to LSI6 in the second and subsequent stages, so that the clock signal CL2 is not supplied to the shift registers 7 in those liquid-crystal drivers. On the other hand, since the liquid-crystal driver LSI1 in the first stage is maintained to the low-level signal at its control terminal $\overline{IE}$, its internal AND gate circuit 8 is opened to supply the clock signal CL2 to its shift register 7 and counter 4. Therefore, the first 80 bits of the image signal data are inputted to the latch circuit 6 in the driver LSI1.

In the liquid-crystal driver LSI1, when the 80 bits of image signal data have been inputted, the counter 4 overflows, making the output signal Q of the latch circuit 9 go low. This closes the internal AND gate circuit 8, stopping the action of the shift register 7 and counter 4 and, on the other hand, causes the output of a low-level signal from the control signal terminal $\overline{OE}$, making the control signal terminal of the next driver LS12 go low.

As a result, the AND gate circuit 8 in the driver LSI2 opens, so that the clock signal CL2 is supplied to its shift register 7 and counter 4. The next 80 bits of image signal data are then inputted to the latch circuit 6 of the driver LSI2. In the same way, the image signal data is divided into 80-bit data sections, and each 80-bit data section is input to the drivers LSI3 to LSI6 in sequence.

In this way, 480 bits of image signal data are all inputted within a display period H of one scanning line electrode. The contents of the first latch circuit 6 are transferred to the second latch circuit 2 according to the clock signal CL1 which is generated at the electrode switching timing.

Therefore, brightness is displayed along the switched scanning line electrode according to the image signal data transferred to the latch circuit 2. In other words, the image signal data supplied to all the liquid-crystal drivers LSI1 to LSI6 corresponds to the scanning line electrode next to the one currently displaying. Since the clock signal CL1 resets the counters 4 and latch circuits 9 of all the liquid-crystal drivers LSI1 to LSI6, image signal data corresponding to the next scanning line electrode is inputted in the same way as described above.

In the liquid-crystal drivers of the three disclosed embodiments, the first and second latch circuits 6 and 2 are composed of 80 bits so that the number of drive signals that can be output is 80. However, it is also possible to divide each of the latch circuits 6 and 2 into two circuits so that each divided latch circuit has 40 bits, and to provide a switching circuit which is switched by an appropriate control signal to supply the image signal data input to one of the latch circuits.

In these embodiments, the present invention has been applied to an LSI for driving a liquid-crystal display device. Any desired LSI for driving a display device consisting of LEDs (light-emitting diodes) can easily be formed by changing the construction of the driver circuit 3, without having to modify the main part of the circuit.

In addition, the essential part of the first embodiment, i.e., the serial/parallel conversion circuit (consisting of the counter 4, decoder circuit 5 and first latch circuit 6), can be applied to the main part of another device, such as a serial I/O device, as shown in Figure 8, of a microcomputer system using a serial communication system. In this case, the counter 4 of the serial I/O device 11 counts a sampling clock SCL supplied from a frequency divider 12, and the count is decoded by the decoder 5 to shape a selection signal ϕ. The latch circuit 6 is activated by the selection signal to sequentially take in the transferred serial data. After the data transfer is completed, a read signal Pr outputted from a microprocessor 10 causes the data held in the latch circuit 6 to be sent in parallel to a buffer circuit 13, from which it is sent onto an internal bus 14.

Instead of a shift register which shifts its contents when it receives a serial data signal supplied from external equipment, as provided in the prior art, the present invention utilizes a plurality of first latch circuits which latch a serial data signal one bit unit or units of several bits at a time, a counter which counts a clock signal indicating the latch timing, and a decoder circuit which decodes the counter content and forms a control signal to activate one of the first latch circuits according to the counter content. The first latch circuits are activated in succession one circuit in synchronism with the timing of the clock signal to latch one bit or several bits of serial data simultaneously. After data has been latched into all of the first latch circuits, the data is output in parallel from the first latch circuits. Because of this construction, the first latch circuits used to provide series/parallel conversion are activated by the decoder circuit only when necessary. This reduces the number of gate circuits activated during the series/parallel conversion. Therefore, it is possible to obtain a series/parallel conversion circuit, and a display driver using the same, having a substantially reduced current consumption and a low power consumption.

The counter circuit may be also be provided with a latch circuit which holds a counter-overflow signal and outputs this signal to external equipment. This construction has the following advantages when applied to a display device which has an expended display area which exceeds the number of drive signal lines available. The timing activating the circuit to convert serial image signal data into parallel signals can be controlled externally. Since the operation of each series/parallel circuit can be stopped by a counter-overflow signal, a plurality of series/parallel conversion circuits for driving the signal lines can be activated in succession on a time-division basis. This adds a rational display operation function to the display driver device, and thereby prevents excessive current consumption.

Whilst the invention has been described with reference to various embodiments thereof, many

modifications of the above described circuits are possible. For example, the number of drive electrodes can be changed in various numbers as necessary. In this case, the number of bits in the latch circuit and the count of the counter need only be set according to the number of electrodes. The drive circuit can be formed of separate semiconductor integrated circuit devices. In addition, the circuit which selectively supplies the clock signal indicating the timing for inputting the serial data can have various modifications. The flip-flops making up the latch circuits 2, 6 and the counter 4 are not limited to the ones described above, various other types can be used.

In a display device using a plurality of semiconductor integrated circuit devices (liquid-crystal drivers) for driving plural signal lines, a device for driving scanning line electrodes can be replaced by a plurality of such devices. The timing generating circuit TG can be made to form a timing signal for AC-driving the liquid crystals, and supply that timing signal to the device driving signal line electrodes, and also to the device driving scanning line electrodes.

Although the above description is mainly concerned embodiments of the present invention as applied to a display driver driving a display device of a dot matrix structure, this invention can be applied to other types of display devices, such as those of a segment type consisting of common electrodes and segment electrodes. This invention can also be widely applied to any data processing system in which serial/parallel conversion is necessary.

CLAIMS

1. A series/parallel conversion circuit including: a counter circuit connected to receive and count clock signals; decoder means connected to said counter circuit for decoding the content of said counter circuit to produce successive output signals in synchronism with said clock signal; and a latch circuit made up of a plurality of gate circuits, each of said gate circuits having a latch function, said latch circuit being connected to receive a serial data signal at said gate circuits and to receive said output signals from said decoder means in synchronism with said clock signal so that respective serial data is latched in respective gate circuits; whereby all data input to said latch circuit as serial data may be transferred from said latch circuit in response to a control signal simultaneously as parallel data.

2. A series/parallel conversion circuit according to claim 1, wherein said counter circuit includes a counter and a circuit connected to receive and hold a counter-overflow signal from said counter so as to output an inhibit signal indicating that said counter has overflowed, and means for inhibiting application of said serial data signal to said latch circuit in response to said inhibit signal.

3. A series/parallel conversion circuit according to claim 1, wherein said latch circuit is made up of a plurality of unit latch circuits, each unit latch circuit including a number of gate circuits; and further including a shift register having at least the same number of stages as the number of gate circuits in each of said unit latch circuits, said shift register being connected to receive and shift said serial signal data in synchronism with said clock signal and being connected to each of said unit latch circuits, so that said image signal data inputted to said shift register is periodically latched into said unit latch circuits in sequence under control of the output signals from said decoder means.

4. A series/parallel conversion circuit according to claim 3, wherein said counter circuit includes a counter and a circuit connected to receive and hold a counter-overflow signal from said counter so as to output an inhibit signal indicating that said counter has overflowed, and means for inhibiting application of said serial data signal to said latch circuit in response to said inhibit signal.

5. A display driver device including: a counter circuit connected to receive and count clock signals; decoder means connected to said counter circuit for decoding the content of said counter circuit to produce successive output signals in synchronism with said clock signal; a latch circuit made up of a plurality of gate circuits, each of said gate circuits having a latch function, said latch circuit being connected to receive a serial data signal at said gate circuits and to receive said output signals from said decoder means in synchronism with said clock signal so that respective serial data is latched in respective gate circuits; and means including a display driver circuit connected to said latch circuit for receiving and holding all bits of said image signal data from said latch circuit simultaneously, whereby said image signal data may be output in parallel as line drive signals to an external display device.

6. A display driver device according to claim 5, wherein said counter circuit includes a counter and a circuit connected to receive and hold a counter-overflow signal from said counter so as to output an inhibit signal indicating that said counter has overflowed, and means for inhibiting application of said serial data signal to said latch circuit in response to said inhibit signal.

7. A display driver device according to claim 5, wherein said latch circuit is made up of a plurality of unit latch circuits, each unit latch circuit including a number of gate circuits; and further including a shift register having at least the same number of gate circuits in each of said unit latch circuits, said shift register being connected to receive and shift said serial signal data in synchronism with said clock signal and being connected to each of said unit latch circuits, so that said image signal data inputted to said shift register is periodically latched into said unit latch circuits in sequence under control of the output signals from said decoder means.

8. A display driver device according to claim 7, wherein said counter circuit includes a counter and a circuit connected to receive and hold a counter-overflow signal from said counter so as to output an inhibit signal indicating that said counter has overflowed, and means for inhibiting application of said serial data signal to said latch circuit in response to said inhibit signal.

9. A display driver device according to claim 5,

wherein said display driver circuit includes means for shaping said drive signals and for applying said shaped drive signals to the signal lines of a liquid-crystal device of a dot matrix structure.

10. A series/parallel conversion circuit constructed and arranged to operate substantially as herein described with reference to and as illustrated in Figures 2, 4 or 5 of the accompanying drawings.

11. A display driver device constructed and arranged to operate substantially as herein described with reference to and as illustrated in Figures 2, 4 or 5 of the accompanying drawings.

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