United States Patent [19]

Gutleber

[11] **3,917,999**

[45] **Nov. 4, 1975**

[54] **MULTIPLEXED PSEUDO NOIE PULSE BURST CODES WITH SPACE TAPER**

[76] Inventor: **Frank S. Gutleber**, 24 Carriage House Lane, Little Silver, N.J. 07739

[22] Filed: **June 18, 1974**

[21] Appl. No.: **480,451**

[52] **U.S. Cl.** **325/40**; 325/56

[51] **Int. Cl.²** **H04B 7/02**

[58] **Field of Search**... 179/15 AP, 15 AW; 340/348; 325/38 A, 40, 41, 42, 44, 56; 178/69 R, 68

[56] **References Cited**

UNITED STATES PATENTS

3,388,330	6/1968	Kretzmer	325/42
3,492,578	1/1970	Gerrish et al.	325/42
3,681,579	8/1972	Schweitzer	178/69 R

Primary Examiner—Benedict U. Safrourek

Attorney, Agent, or Firm—Nathan Edelberg; Robert P. Gibson; Daniel D. Sharp

[57] **ABSTRACT**

A pulse signalling system combining a multiplexed pseudo-noise code expansion theory with a space-coded array antenna synthesis technique to produce a high resolution waveform. The antenna space coding technique enables the clearing of any desired area in the frequency portion of the ambiguity surface. The multiplexed code expansion process simultaneously controls the side lobes in the time domain by utilizing a pair of code signals which, upon detection, provide an impulse autocorrelation function.

5 Claims, 5 Drawing Figures

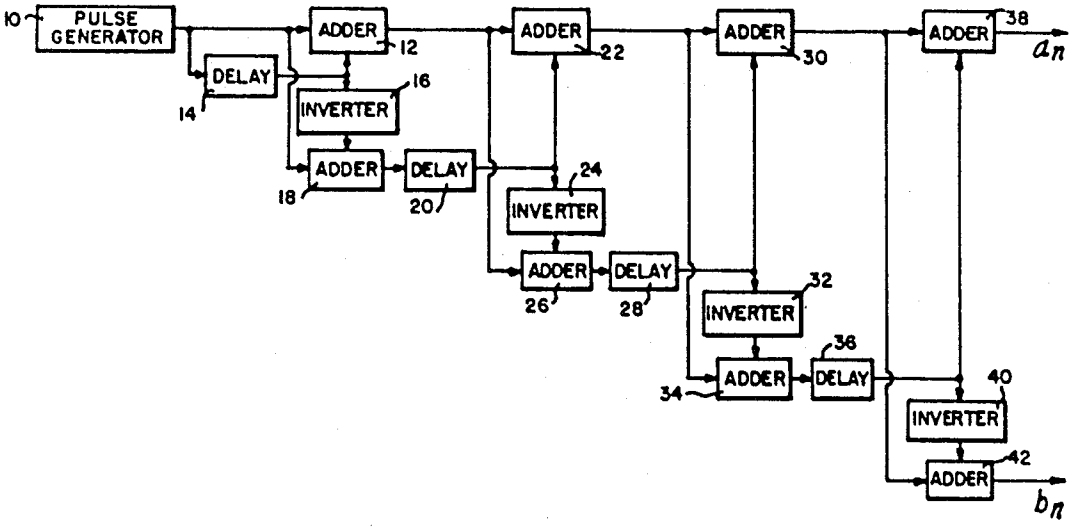


Fig. 1.

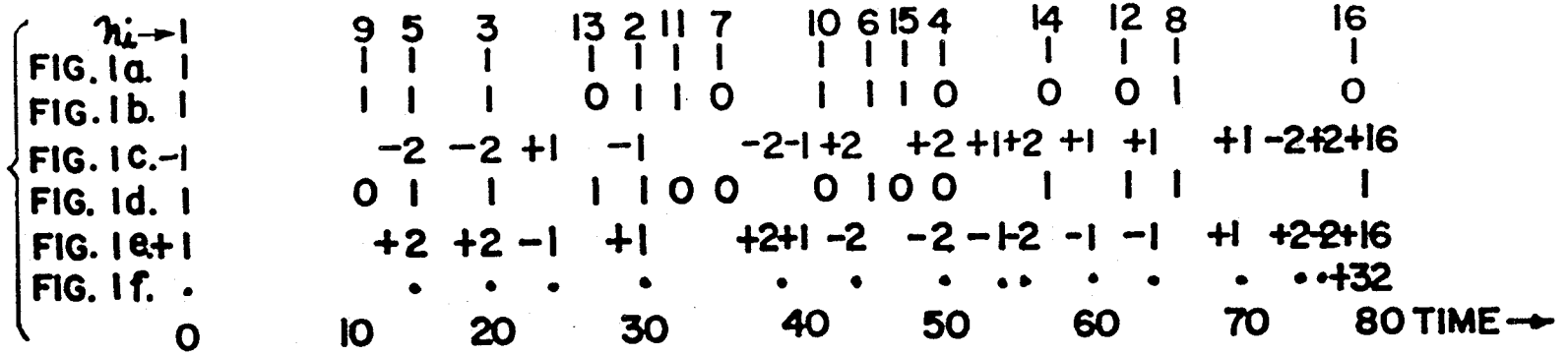
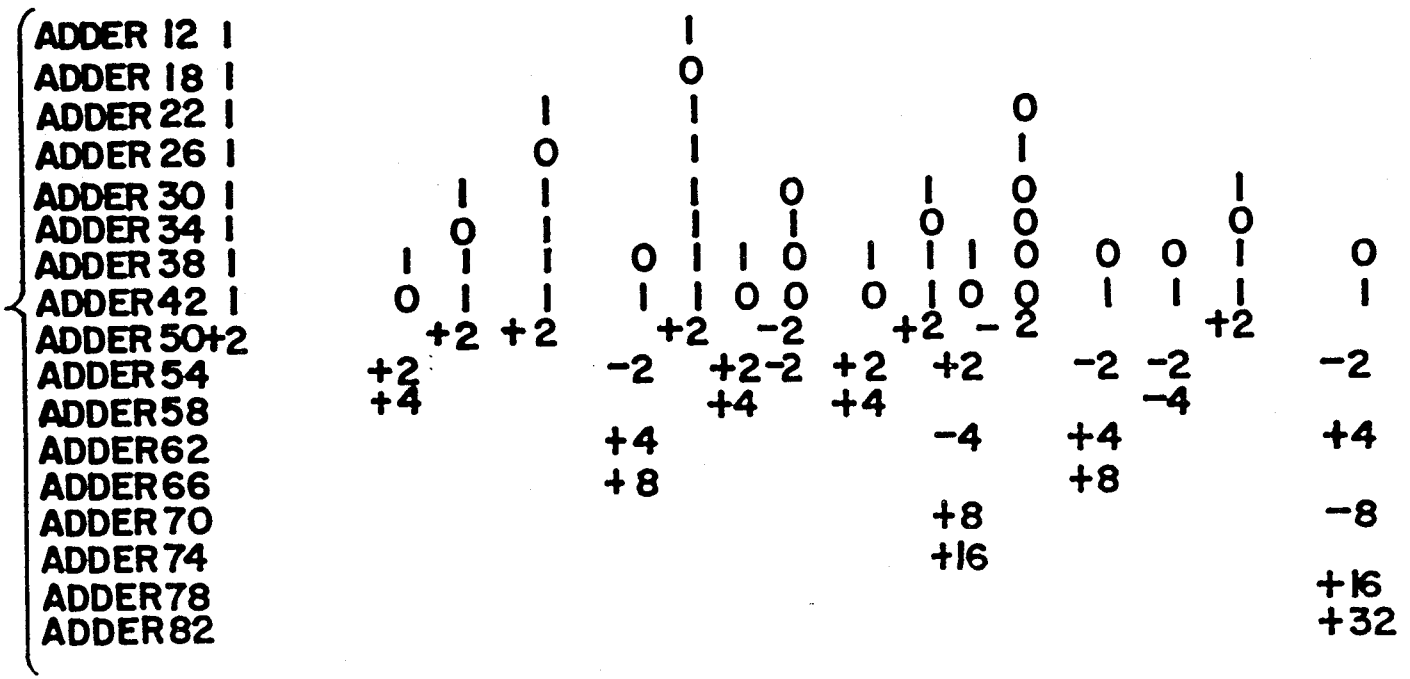

$n_i \rightarrow$ 1
FIG. 1a.
FIG. 1b.
FIG. 1c.-1
FIG. 1d.
FIG. 1e.+1
FIG. 1f.
0
9 5 3 13 2 11 7 10 6 15 4 14 12 8 16
-2 -2 +1 -1 -2-1 +2 +2 +1 +2 +1 +1 +1 -2 +2 +16
+2 +2 -1 +1 +2+1 -2 -2 -1 -2 -1 -1 +1 +2 +2 +16
• • • • • • • • • • • • • • +32
10 20 30 40 50 60 70 80 TIME

Fig. 4.


ADDER 12
ADDER 18
ADDER 22
ADDER 26
ADDER 30
ADDER 34
ADDER 38
ADDER 42
ADDER 50+2
ADDER 54
ADDER 58
ADDER 62
ADDER 66
ADDER 70
ADDER 74
ADDER 78
ADDER 82

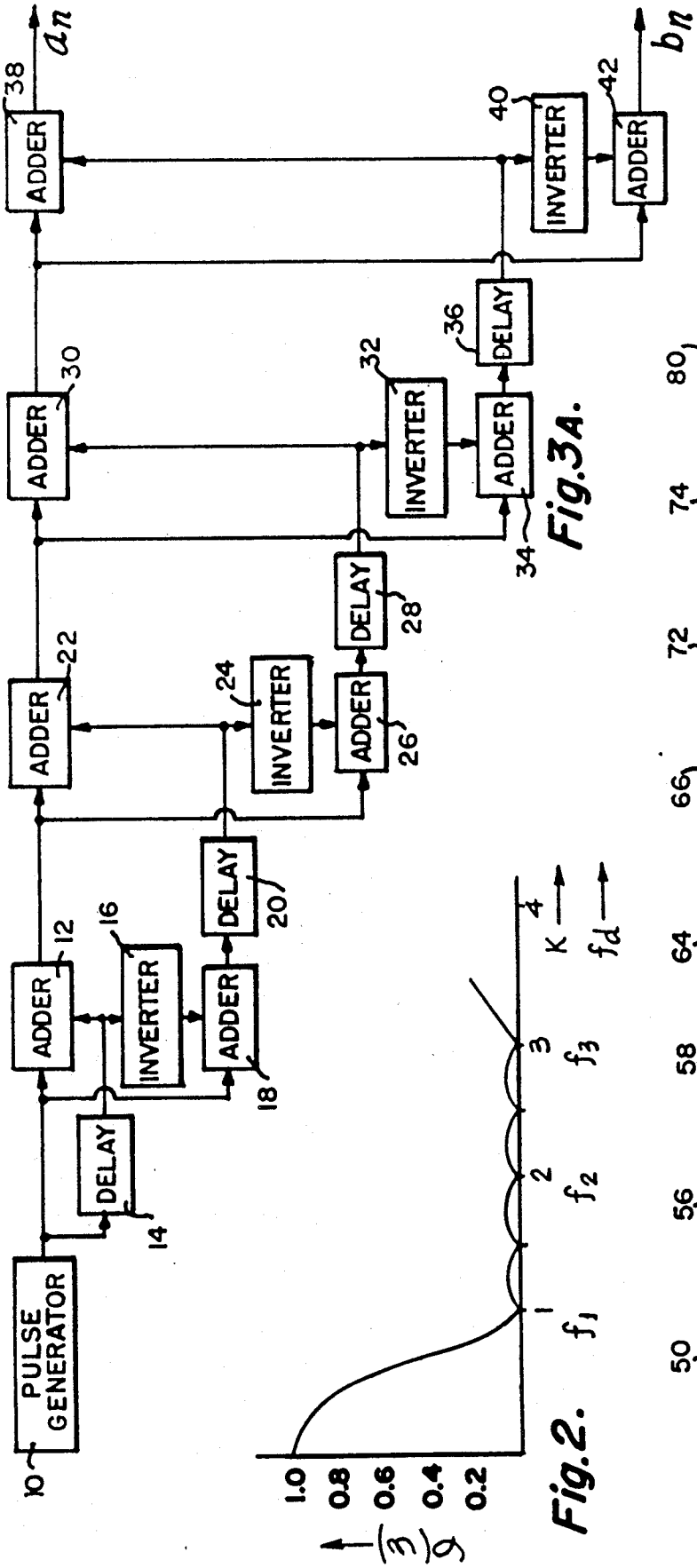


Fig.3A.

Fig.2.

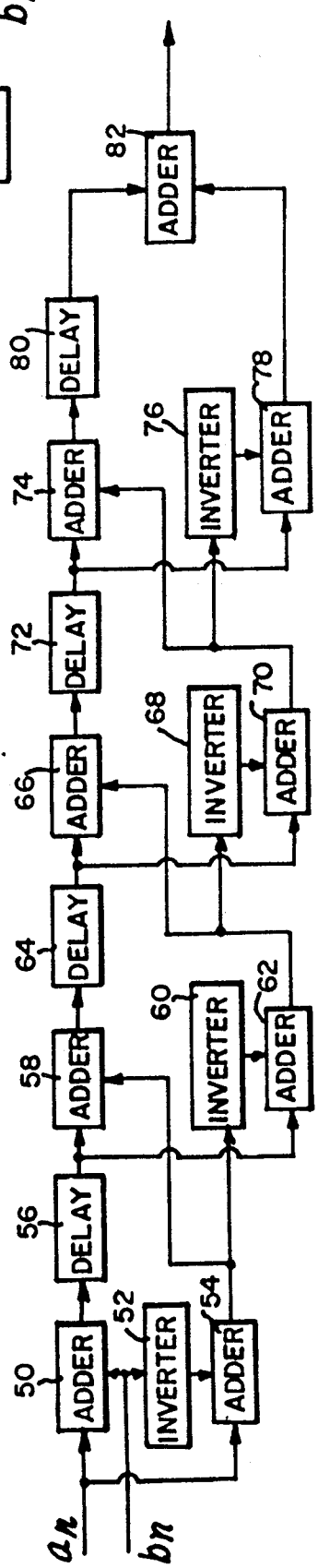


Fig.3B.

MULTIPLEXED PSEUDO NOISE PULSE BURST CODES WITH SPACE TAPER

The invention described herein may be manufactured and used by or for the Government for governmental purposes without the payment of any royalties thereon or therefor.

FIELD OF THE INVENTION

This invention relates to pulse signalling systems and, more particularly, to such a system in which a high degree of resolution is simultaneously obtainable in both frequency and range. As will be understood, such characteristics are especially attractive in radar and navigation systems, altimeter and fuze applications, moving target indicators, and in communications systems, in general.

SUMMARY OF THE INVENTION

The pulse signalling system of the present invention incorporates a multiplexed pseudo-noise code expansion theory, together with a space-coded array antenna synthesis technique similar to that described in my issued U.S. Pat. No. 3,130,410. The antenna space coding technique is formulated to surpress side lobes in the frequency domain of an ambiguity surface, whereas the multiplexed pseudo-noise code expansion theory is formulated to surpress side lobes in the time domain.

As will be seen below, a composite signal code structure is employed, consisting of a pair of signals termed code mates, having amplitudes and autocorrelation functions which provide a peak output at a given time and a zero output (or outputs having the same magnitude but opposite polarity) at all other times. The individual bits, or elements, of the composite structure, furthermore, are controllably time spaced in position to clear a desired frequency area. The signal waveform recovered upon detection of such a radiated code structure will be seen to be an impulse function at the principal axis substantially simultaneously both in the time domain and in the frequency domain, independent of any doppler shift.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features of the present invention will be more clearly understood from a consideration of the following description taken in connection with the accompanying drawings in which:

FIGS. 1*a*–1*f* illustrate space coding and multiplexed pseudo-noise coding expansion theories helpful in an understanding of the present invention;

FIG. 2 shows a frequency response plot also helpful in an understanding of the invention.

FIGS. 3*a* and 3*b* are functional block diagrams of code generator and code pulse compression apparatus illustrating the invention; and

FIG. 4 is a series of pulse code representations as exist at various points within the block diagrams of FIG. 3.

DETAILED DESCRIPTION OF THE DRAWINGS

As will be readily apparent to one skilled in the art, a consecutive series of code bits received from a radar response, for example, may be expressed as:

$$a_0 e^{j\Psi_0},\ a_1 e^{j\Psi_1},\ a_2 e^{j\Psi_2},\ \ldots\ a_{n-1} e^{j\Psi_{n-1}} \qquad (1)$$

where the phase of the ith bit consists of:

$\Psi_i = \Psi_{ic} - 2\pi n_{(i+1)}\tau f_d$;

Ψ_{ic} = phase of the code;

f_d = doppler frequency;

$n_{(i+1)}\tau$ = time displacement from the first code bit; and

$2\pi n_{(i+1)}\tau f_d$ = phase change introduced due to the doppler effect. If this code of expression (1) were applied to a matched filter of the type described in my issued U.S. Pat. Nos. 3,461,451, 3,519,746 or 3,634,765, for example, the phases of the code bits along the zero time axis would line up. The phase contribution of the doppler frequency in controlling the ambiguity function of a return along the frequency axis, therefore, is all that need be considered. In such case, the phases of the code bits become:

$$\Psi_0 = n_1 2\pi\tau f_d = n_1\Psi = 0$$
$$\Psi_1 = n_2 2\pi\tau f_d = n_2\Psi$$
$$\Psi_2 = n_3 2\pi\tau f_d = n_3\Psi$$
$$\vdots$$
$$\Psi_{n-1} = n_m 2\pi\tau f_d = n_m\Psi$$

These expressions may be more generally written as:

$$n'\Psi = n\Psi + \pi \qquad (3)$$

Where:

n = existing code bit to be affected by the doppler shift;

and

n' = new code bit position needed to produce a desired lobe pattern.

Because

$$\Psi = 2\pi\tau f_d \qquad (4)$$

these last two expressions can be combined to

$$n' = n + \frac{1}{n\tau f_d} \qquad (5)$$

Letting $\tau f_d = K$, expression (5) reduces to

$$n' = n + \frac{1}{2K} \qquad (6)$$

As will be seen, equation (6) is identical in form to equation (12) of my U.S. Pat. No. 3,130,410 and may be utilized in like manner to completely synthesize the time code structure for any desired lobe pattern along the frequency axis of the ambiguity surface. As with equation (12) there, equation (6) states that to form a new code bit position n', we add the quantity $\frac{1}{2}K$ to the previous code bit position n. Equation (6) thus indicates the basic method for building up the space-coded bit positions of this invention. Each time it is desired to extend the code, the number of bits will be doubled. Each added bit, furthermore, will be the distance $\frac{1}{2}K$ from its own corresponding previous existent bit.

However, the quantity k can still be chosen in such a manner as to facilitate design procedures and to make as simple as possible the computations involved. For this reason, f_{d0} is defined as the doppler frequency where the first null in the frequency domain occurs. By making K_1 equal to 1 at the first null, i.e. f_d equals f_{d0}, the entire design can be "normalized". For $K = f_d/f_{d0}$, and by repeating equation (6) to find the time coded delays to produce forced nulls in the frequency domain for $K_1 = 1$, $K_2 = 3/2$, $K_3 = 2$, $K_4 = 5/2$, the following 16 time code positions will be produced:

$n_1 = 0$
$n_2 = 1/2 = \Delta\tau_1/\tau$
$n_3 = 1/3 = \Delta\tau_2/\tau$
$n_9 = 1/5 = \Delta\tau_4/\tau$
$n_{10} = 1/2 + 1/5 = 7/10$
$n_{11} = 1/3 + 1/5 = 8/15$

-continued

$n_4 = 1/2 + 1/3 = 5/6$	$n_{12} = 5/6 + 1/5 = 31/30$
$n_5 = 1/4 = \Delta\tau_3/\tau$	$n_{13} = 1/4 + 1/5 = 9/20$
$n_6 = 1/2 + 1/4 = 3/4$	$n_{14} = 3/4 + 1/5 = 19/20$
$n_7 = 1/3 + 1/4 = 7/12$	$n_{15} = 7/12 + 1/5 = 47/60$
$n_8 = 5/6 + 1/4 = 13/12$	$n_{16} = 13/12 + 1/5 = 77/60$

In order to normalize these code positions along the time axes, the values in the above table are multiplied by 60 with the result being shown in FIG. 1*a* as the space-coded time positions for the code bits. As will be appreciated, this time position coding illustrates that forced nulls will appear in the frequency domain of the ambiguity surface when the first code bit is positioned at time 0, the second code bit is positioned at time 30, the third code bit is positioned at time 20, the fourth code bit is positioned at time 50, etc. This is also illustrated by the coded time position frequency response plot of FIG. 2 for different design values of *K*. The desired frequency area cleared of side lobes will be appreciated to extend from f_1 to f_3.

In general, because $K = f_d/f_{d0}$, it can be shown that the maximum value of K of physical significance can be expressed as B/f_{d0}, where B is the signal bandwidth of the system. For f_{d0} equal to 100 Hz, the desired frequency area cleared of side lobes in FIG. 2 will be seen to extend to 300 Hz, and τ, the reciprocal of f_{d0} at $K =$ 1, will be seen to be 10,000 micro-seconds. a single, a — the

FIGS. 1*b* and 1*d* show a pair of code signals termed code mates, having amplitudes and autocorrelation functions to compress to a single impulse lobelessly. As is described in my aforementioned U.S. Pat. Nos. 3,461,451, 3,519,746 or 3,634,765, when code mates of this type are detected and the resultant detected outputs are linearly added, there is provided an impulse output of high amplitude at a given time in a waveform and a zero output at all other times. Following the techniques described in such patents, the impulse autocorrelation functions for such code signals may be obtained, and are of the type respectively shown in FIGS. 1*c* and 1*e*. The linear output for these detected code signals is shown in FIG. 1*f* as having asingle, high amplitude peak, completely free from spurious peaks of lower amplitude elsewhere in the waveform. As will be seen, the individual bits of these two code signals are inserted within the space-coded time positions of FIG. 1*a*—the high amplitude impulse output being developed at "normalized" time position 77.

FIGS. 3*a* and 3*b* are functional block digarams showing the generation of these code signal bits within the space-coded time positions, and the resulting detection and linear addition to provide the impulse output. In the discussion that follows, it will be understood that FIG. 3*a* illustrates the apparatus for generating the code signal bits for transmission, while FIG. 3*b* illustrates the apparatus for compressing the code signal bits received.

Thus, referring to FIG. 3*a*, a pulse generator 10 provides a digital "1" signal to one input terminal of an adder 12 and to a delay circuit 14, which imparts a delay of $\Delta\tau_1$, or 30, time positions to the generator output. The output of delay circuit 14 is coupled to a second input terminal of adder 12, and to an inverter 16. The signal from generator 10 and the output of inverter 16 are in turn coupled to another adder 18, whose output signal is applied to a second delay circuit 20. This circuit 20 imparts a delay of $\Delta\tau_2$, or 20, time positions to the input code bits.

The output from delay circuit 20 is also seen to be applied to one input terminal of an adder 22 — the other terminal of which is provided with the output from adder 12 — and to a further inverter 24. The signal from the inverter 24 is applied to one input of yet another adder stage 26, also along with the output signal from adder 12. The otuput from adder 26 will then be seen to be applied to a third delay circuit 28, which imparts a delay of $\Delta\tau_3$, or 15, code time positions. From delay circuit 28, the developed signal is applied both to an input terminal of a further adder stage 30 and to an inverter 32, the second input terminal of adder 30 being applied the output from adder 22.

The output signal from adder 22 is then applied to one input terminal of another adder 34, along with the output from inverter 32. The output signal from adder 34 is applied via a fourth delay circuit 36 — first, to one input terminal of an adder 38 and second, to an inverter circuit 40. Also provided at the second input of adder 38 is the output signal from adder 30, the delay circuit 36 in this instant providing a delay of $\Delta\tau_4$, or 12, time code positions. The output from adder 38 is indicated by the reference notation a_n, whereas the output from inverter 40 is applied to an adder 42 along with the output from adder 30 to provide an output signal indicated as b_n.

The pulse code output signals developed by the adder stages 12, 18, 22, 26, 30, 34, 38 and 42 are shown in FIG. 4. The identities between the time spaced, pulse code signal from adder 38 and the time spaced signal code of FIG. 1*b* — as well as similar identities between the time spaced pulse code from adder 42 and the time spaced signal of FIG. 1*d* — will be apparent.

The block diagram of FIG. 3*b* also includes a plurality of adder, delay and inverter circuits. As illustrated, the code signal represented by the notation a_n is radiated, for example, received with a doppler frequency shift, and applied as such to one input terminal of an adder 50, to another input of which the received, frequency shifted b_n code signal is applied. That b_n signal code is also applied to an inverter 52, the output therefrom being applied to an adder 54 along with the a_n code.

The output signal from adder 50 is applied to a delay circuit 56, the imparted delay of which is equivalent to the $\Delta\tau_4$, or 12, time code position delay of circuit 36 in the upper portion of the drawing. The output from delay circuit 56 is applied both to an input terminal of a further adder 58 and to an input terminal of another adder 62. The otuput signal from adder 54 is also applied first, to a second terminal of adder 58 and second, via an inverter 60 to the other input terminal of adder 62. The output signal from adder 58 is applied to a delay circuit 64, similar to the delay circuit 28, in imparting a delay of $\Delta\tau_3$, or 15, time code positions to the input pulse signal. As with the delay circuit 56, the output of circuit 64 is applied to a pair of adders, 66 and 70. The second input terminal of these two adders are respectively supplied with the output signal from adder 62 and with that signal inverted, as supplied from adder 62 via an intermediate inverter stage 68.

The output signal from adder 66 is, in turn, applied to a further delay circuit 72, similar to the delay circuit 20, in imparting a delay of $\Delta\tau_2$, or 20, time code positions to the individual pulse bits. The output of delay circuit 72 is applied both to an adder 74 and to an

adder **78**, other input terminals of which are respectively provided with the output pulse from the adder **70** and with an inverted pulse signal from that stage by means of an inverter **76**. As shown, the output signal from adder **74** is finally applied via a delay circuit **80** to one input terminal of a last adder **82**, to a signal input terminal of which is applied the output signal from adder **78**. Delay circuit **80**, in this regard, is similar to the delay circuit **14**, in providing a delay of $\Delta\tau_1$, or 30, time code positions to the input pulse signal.

The pulse code output signals developed by the adder stages **50, 54, 58, 62, 66, 70, 74, 78** and **82** are also shown in FIG. **4**. The output from adder **82** will be seen identical to the pulse code representation of FIG. **1f**.

This illustrative example of FIGS. **1–4** thus shows that by transmitting a pair of coded signals, termed code mates, an impulse function can be obtained in the time domain of the ambiguity surface upon receipt and detection. By controlling the positions of a timing sequence into which the individual pulse bits are inserted, an impulse function can be obtained in the frequency domain substantially simultaneously therewith. Although a specific pair of code signals have been utilized, others of the type noted in my referenced patents may be employed as well, necessitating only a rearrangement of the adder and inverter positionings of FIGS. 3*a* and 3*b* to provide the continued impulse output in the time domain. With the same values selected for the design parameter *K*, the same doppler frequency area will continue to be cleared of side lobes in providing the high resolution return waveform. If a greater doppler frequency area were desired to be cleared, *K* can simply be increased from 5/2, to 3, to 7/2, etc., with the number of pulse bit positions in the timing sequence doubling for each increase. As such will be seen to correspondingly increase the complexity of the block diagram of FIG. **3**, some compromise between resolution and construction would most likely be needed.

While there has been described what is considered to be a preferred embodiment of the present invention, it will be readily apparent to those skilled in the art that modifications may be made without departing from the scope of the teachings herein. It is therefore contemplated that the invention be read in light of the claims appended hereto.

I claim:

1. A pulse doppler frequency signalling system for generating a code mate pair of asymmetrically interleaved code bits for transmission and for reception after undergoing a doppler frequency shift which provides for code compression to a lobeless impulse function in the time domain and for controllable minimization of lobes in the frequency domain of the ambiguity diagram comprising a pulse generator for providing a single input pulse, and a code pair expander responsive to said input pulse and including a plurality of *m* cascaded code pair expansion circuits each doubling the number of code bits and thereby forming a new code mate pair, each of said code expansion circuits having circuit means for delaying the code bits of one of said previous code mate pairs and for adding the delayed previous code mate pair with the undelayed previous code mate pair to form a first expanded code, and each of said code expansion circuits having circuit element means for delaying and for inverting one of said previous code mate pairs and for adding the inverted delayed previous code mate pair to the undelayed previous code mate pair to form a second expanded code, the delay introduced into the delaying means of a given xth one of the m circuit means and circuit element means is given by $\frac{1}{2}f_{d_{xx}}$ where $f_{d_{xx}}$ is the selected frequency of the xth null in the frequency domain.

2. The system of claim **1** further comprising a code pair compression means responsive to said generated first and second expanded codes, and including a plurality of m cascaded code pair compression circuits each halving the number of code bits and thereby forming a new code mate pair, said compression circuits each having delay means identical to the delaying means of the corresponding code pair expansion circuit and code inversion means for inverting one of the previous code mate pairs, and summing means for adding the code bits of the mth compression circuit to obtain a single output pulse.

3. The system of claim **1** wherein the xth code pair expander circuit includes a first portion for deriving the bits of the first code a_x and a second portion for deriving the corresponding bits of the second code b_x, said first portion including means for delaying the previous code b_{x-1} and adding the latter to the previous code a_{x-1}, and said second portion including means for inverting the delayed code b_{x-1} and adding said delayed inverted code to the previous code a_{x-1}.

4. The system of claim **2** wherein the xth code pair expander circuit includes a first portion for deriving the bits of the first code a_x and a second portion for deriving the corresponding bits of the second code b_x, said first portion including means for delaying the previous code b_{x-1} and adding the latter to the previous code a_{x-1}, and said second portion including means for inverting the delayed code b_{x-1} and adding said delayed inverted code to the previous code a_{x-1}.

5. The system of claim **2** wherein the yth code pair compression circuit includes a first portion for deriving the bits of the first code a_y and second portion for deriving the corresponding bits of the second code b_y, said first portion including means for delaying the bits of the previous code a_{y-1} and adding these delayed bits to the bits of previous code b_{y-1}, and said second portion including means for inverting the bits of the previous code b_{y-1}, and said second portion including means for inverting the bits of the previous code b_{y-1} and adding these inverted bits to the delayed bits of previous code a_{y-1}.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 3,917,999
DATED : 4 November 1975
INVENTOR(S) : Frank S. Gutleber

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

The correct title is: "Multiplexed Pseudo Noise Pulse Burst Codes with Space Taper"

Column 3, lines 28 and 29, delete "a single, a - the".

Signed and Sealed this

thirteenth Day of April 1976

[SEAL]

Attest:

RUTH C. MASON
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents and Trademarks

UNITED STATES PATENT AND TRADEMARK OFFICE

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