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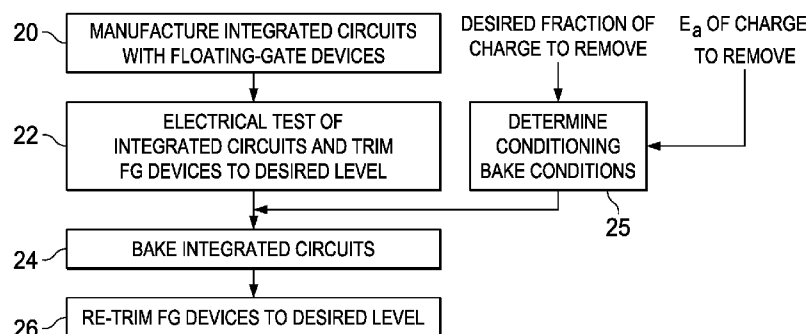


FIG. 4

(57) Abstract: A conditioning process is performed for integrated circuits including floating-gate devices, such as floating-gate capacitors or transistors in analog or other circuits in which the devices are to be programmed to a specific level. Following initial programming (22) of the floating-gate devices to a specific programmed level, the integrated circuits are subjected to a conditioning bake (24), followed by re-trim (26) back to the initial programmed level. That portion of the charge at the floating-gate device that was weakly held is removed by the conditioning bake, while the re-trim replaces that charge with more strongly held (higher activation energy) programmed charge.

REDUCING RETENTION LOSS IN ANALOG FLOATING GATE MEMORY

[0001] This relates generally to integrated circuit electrical manufacture, and more particularly to post-fabrication processing of integrated circuits including analog floating gate memory cells to improve data retention capability.

BACKGROUND

[0002] An increasingly important type of semiconductor integrated circuits implement analog circuit functions, in which input and output signals and information are communicated and processed in the analog domain. Typically, analog integrated circuit functions rely on reference levels (voltages and currents) that are established and regulated on-chip. Proper functioning of the analog integrated circuit, and particularly such functioning over variations in power supply voltage, temperature, and other operating conditions, often critically depends on the stability of reference voltages and currents over such variations. However, manufacturing variations reflected in physical parameters of the integrated circuits can affect the reference levels as generated in these integrated circuits. Accordingly, many analog integrated circuits include some ability to “trim” or adjust the on-chip precision reference circuits, as well as other circuit functions within those integrated circuits. Trimming is typically performed at manufacture, after electrical measurement or other evaluation of the performance of the raw circuit as manufactured.

[0003] Recently, programmable non-volatile memory elements have been considered for use as trimming elements, such as in replacement of fuses or antifuses. Examples of these non-volatile memory elements include floating-gate metal-oxide-semiconductor (MOS) transistors, in which the state of the transistor is defined by charge trapped at a floating gate electrode, such as a floating capacitor plate. Programming of the device is accomplished through such mechanisms as Fowler-Nordheim tunneling and hot carrier injection. Programming of floating-gate structures is attractive as a trimming technique, because of the precision to modern programming methods can set the charge, and because this programming operation is a purely electrical process. An example of such a programmable voltage reference circuit is described in Roman, et al., “A 1 μ A Bandgap-Less Programmable Voltage Regulator”, 56th International

Midwest Symposium on Circuits and Systems, (IEEE, 2013), pp. 5–8, incorporated herein by this reference.

[0004] However, trimming of circuit parameters by floating-gate elements relies on retention of the trapped charge at the floating gate for the life of the device, considering that the trimming may only be available at the time of manufacture (e.g., before packaging). But conventional floating-gate structures in analog integrated circuits have been observed to exhibit some degree of charge leakage over time, which results in degradation of trimmed levels in the circuits relying on those structures. Accordingly, while the small chip area required by analog floating-gate technology for certain analog circuits (such as bandgap reference circuits) is attractive, the charge retention capability of these devices is often not sufficiently reliable for use in certain applications, particularly those intended for use in high-temperature environments, such as remote sensors and systems (e.g., in machine-to-machine networks).

[0005] This data retention vulnerability has been addressed by the use of specific dielectric films for those analog floating-gate capacitors. But this specific construction necessarily increases the manufacturing cost of the integrated circuits by requiring additional dielectric deposition processes, among other additional process steps, such as the deposition and patterning of an additional conductor layer for those capacitors. For example, it is known to construct the analog floating-gate device as a double-level polysilicon device, in which a dedicated dielectric film that defines tunneling regions is formed between the two polysilicon levels. This approach requires an additional deposition process for the separate tunneling dielectric film and, because this film is relatively thick, presents a relatively small capacitance per unit area.

[0006] As further background, the phenomenon of stress-induced leakage current (SILC) in dielectric films, such as silicon dioxide, has been observed. According to the conventional model for SILC, defects in the silicon dioxide structure are created by electrical stress across the film. These defects serve as charge traps, such that electrons or holes can be trapped within the dielectric film. Floating-gate devices that are programmed by Fowler-Nordheim or other tunneling across a thin dielectric film are known to be vulnerable to this mechanism, because a portion of the programming charge crossing the dielectric film can become trapped at the stress-induced sites.

SUMMARY

[0007] Described examples provide a method of improving the as-manufactured data retention

capability of floating-gate memory devices.

[0008] Described examples provide such a method that can be efficiently implemented with little additional manufacturing cost.

[0009] Described examples provide such a method that provides such improved data retention performance without requiring additional deposition processes.

[0010] Described examples provide such a method that enables the use of analog floating-gate devices in precision reference circuits, such as replacement for bandgap reference circuits.

[0011] According to described examples, an integrated circuit including a floating-gate capacitor that is to be programmed to a desired analog level is manufactured according to the desired process technology, and the floating-gate capacitor is electrically programmed to the desired analog level. Following that programming, or trimming, the integrated circuit is subjected to a conditioning bake at an elevated temperature for a selected duration. The integrated circuit is then again electrically programmed to restore the desired analog level.

[0012] According to some described examples, multiple integrated circuits, each including at least one circuit including a programmable floating-gate device, are fabricated in wafer form. In a first electrical test of the integrated circuits, the floating-gate devices in the integrated circuits are programmably trimmed to a selected analog level. Following the first electrical test, the integrated circuits are conditioned by a bake at a time and temperature selected according to an activation energy of a charge leakage mechanism. Following the bake, the devices are re-trimmed to a selected level.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] FIG. 1 is an electrical diagram, in schematic form, of a programmable floating gate device with which example embodiments may be used.

[0014] FIGS. 2a and 2b are plan and cross-sectional views, respectively, of the physical construction of the device of FIG. 1.

[0015] FIGS. 3a and 3b are plots of data retention performance of a sample of analog floating-gate integrated circuits.

[0016] FIG. 4 is a flow diagram of a method of fabricating floating-gate devices with improved data retention, according to embodiments.

[0017] FIG. 5 is a series of plots of time versus temperature used in selection of parameters for the conditioning bake.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0018] The one or more embodiments described in this specification are implemented into an integrated circuit, including a programmable circuit of a type known as an analog floating-gate circuit, and such implementation is particularly advantageous in that context. However, the example embodiments may be beneficially applied to in other applications, such as floating-gate digital memory cells, particularly those intended to store more than one digital bit per cell.

[0019] FIG. 1 is an electrical schematic of the arrangement of a conventional analog floating-gate circuit, in connection with which example embodiments may be used. This analog floating-gate circuit includes an electrically floating electrode serving multiple functions. Specifically, analog floating-gate electrode 2 in this circuit of FIG. 1 serves as the gate electrode for metal-oxide-semiconductor (MOS) transistor 4, and as a first plate of storage capacitor 6. Transistor 4 may be at an input of an analog circuit or other function, such as an amplifier. A second plate of storage capacitor 6 is coupled to a reference voltage, namely ground in this example. In operation, the voltage stored across storage capacitor 6 determines the voltage at the gate of MOS transistor 4, and thus the extent to which transistor 4 conducts between drain D and source S, for a given drain-to-source bias.

[0020] In this arrangement, analog floating-gate electrode 2 is programmable to a particular analog state by tunnel capacitors 8p, 8n. Analog floating-gate electrode 2 serves also as a first plate of each of these tunnel capacitors 8p, 8n. In this example, a second plate of tunnel capacitor 8p is connected to a terminal TP, while a second plate of tunnel capacitor 8n is connected to a terminal TN. The capacitor dielectric for tunnel capacitors 8p, 8n is contemplated to be relatively thin, to allow mechanisms such as Fowler-Nordheim tunneling to transfer charge between terminals TP, TN and analog floating-gate electrode 2, depending on the bias. Tunnel capacitors 8p, 8n permit both the programming of stored charge onto floating-gate electrode 2, and also removal of that stored charge (“erase”). In many implementations in which erase is not necessary or desirable, only one of these tunnel capacitors 8p, 8n is implemented.

[0021] In operation, the programming of analog floating-gate electrode 2 by electrons tunneling through tunnel capacitor 8n is performed by applying a pulse of an appropriate negative voltage to terminal TN, relative to the voltage at terminal TP and to the ground reference voltage at the opposite plate of storage capacitor 6. An example of such a “programming” pulse, for a fully programmed level, is a voltage of about -11 volts at terminal

TN relative to terminal TP and ground, for on the order of 20 msec. The voltage divider of capacitors 8n, 8p, 6 will result in most of that voltage appearing across tunnel capacitor 8n, enabling electrons to tunnel through its capacitor dielectric to analog floating-gate electrode 2. Those electrons will then be trapped at analog floating-gate electrode 2, considering that direct (e.g., DC) connection is absent between analog floating-gate electrode 2 and any other circuit element. Conversely, electrons can be removed from analog floating-gate electrode 2 by applying an appropriate positive voltage at terminal TP relative to terminal TN and to the ground reference voltage at the opposite plate of storage capacitor 6. The voltage divider of capacitors 8n, 8p, 6 will result in most of that voltage appearing across tunnel capacitor 8p, causing electrons that are trapped on analog floating-gate electrode 2 to tunnel through its capacitor dielectric to terminal TP. An example of such a “erase” pulse, to remove a fully programmed level, is a voltage of about +11 volts at terminal TP relative to terminal TN and ground, for a duration on the order of 20 msec. The duration of the program and erase pulses can be adjusted to precisely set the charge state at analog floating-gate electrode 2. Following programming, the trapped charge on analog floating-gate electrode 2 will establish a voltage across storage capacitor 6, and thus a gate voltage for MOS transistor 4 that controls its conduction. Tunnel capacitors 8n, 8p thus enable precise setting of the charge at analog floating-gate electrode 2, and thus precise adjustment of the analog state of the circuit including MOS transistor 4.

[0022] The analog floating gate circuit of FIG. 1 is useful in various circuit environments, including voltage and current reference circuits, programmable gate array structures, trim capability for analog circuits and reference circuits in digital circuits, level shift circuits, and multi-bit EEPROM memory cells (e.g., in which each floating gate memory cell is capable of storing intermediate levels). Alternative embodiments are possible.

[0023] FIG. 2a illustrates, in plan view, the construction of an analog floating-gate structure, such as that electrically shown in FIG. 1, and in connection with which embodiments may be used. FIG. 2b illustrates, in cross-section, the construction of capacitor 6. The sizes of elements shown in FIGS. 2a and 2b are not necessarily to scale, relative to one another. For example, the widths of elements shown in FIG. 2a may in actuality be substantially narrower, relative to the length of the same element, than that shown. Similarly, the relative thicknesses of elements in the cross-sectional views of FIG. 2b may not correspond to that in actual devices. In any case, these structures may be fabricated by conventional manufacturing technology, including at those

process nodes extending into the sub-micron regime. The structures of FIGS. 2a and 2b are adaptable to the desired manufacturing technology.

[0024] As shown in FIG. 2a, analog floating-gate electrode 2 is constructed of polycrystalline silicon (polysilicon) element 16, which extends over the surface of a semiconductor wafer (or over a semiconductor surface layer, in the silicon-on-insulator context) in forming multiple devices or components. Polysilicon element 16 is typically doped to a desired conductivity type and concentration, to be conductive to the desired extent, such as by n-type doping for this example in which MOS transistor 4 is n-channel. Polysilicon element 16 has a widened portion at its end, serving as a lower plate of storage capacitor 6, and is otherwise narrower, such as at a minimum feature size for the manufacturing technology. As shown in FIG. 2b for storage capacitor 6, the lower plate portion of polysilicon element 16 overlies trench isolation dielectric structure 13. Gate dielectric 17 (e.g., formed of deposited or thermal silicon dioxide) is disposed between the surface of isolation dielectric structure 13 and polysilicon element 16, and will also underlie polysilicon element 16 at those locations at which it overlies active regions (e.g., at transistor 4 and tunnel capacitors 8p, 8n). In this example, the surface into which isolation dielectric structure 13 is formed is the top surface of p-type silicon substrate 10. Upper plate 12 of storage capacitor 6 is formed of a metal such as tantalum nitride, and overlies the widened portion of polysilicon element 16 at this location. In this embodiment, capacitor dielectric 18 is formed of one or more dielectric layers, such as silicon nitride, silicon dioxide, or a combination of these or other dielectric materials.

[0025] Referring again to FIG. 2a, transistor 4 and tunnel capacitors 8p, 8n are constructed along the portion of polysilicon element 16 defining analog floating-gate electrode 2 overlying active regions (e.g., semiconductor portions not underlying isolation dielectric structures 13). MOS transistor 4 is defined where polysilicon element 16 overlies an active region of p-type substrate 10, separated therefrom by gate dielectric 17. Heavily-doped n-type source/drain regions 15_n are formed into the p-type active region on opposite sides of polysilicon element 16 in the conventional self-aligned fashion. Top side contacts from an overlying metal conductor, and corresponding to terminals D, S as in the circuit of FIG. 1, are made through an interlevel dielectric layer to source/drain regions 15_n.

[0026] Tunnel capacitor 8n is constructed essentially similarly as n-channel MOS transistor 4, where polysilicon element 16 overlies an instance of a p-type active region (separated by gate

dielectric 17). Heavily-doped n-type source/drain regions 15_n are formed at that location similarly as for transistor 4. Because top side contacts to source/drain regions 15_n are both connected to terminal TN, tunnel capacitor 8n operates as a capacitor rather than a transistor. Tunnel capacitor 8p is constructed essentially similarly as tunnel capacitor 8n, but at a location at which polysilicon element 16 overlies an n-type active region, such as the surface of an n-well formed into substrate 10. Top side contacts to p-type source/drain regions 15_p on either side of polysilicon element 16 are connected to terminal TP, so that tunnel capacitor 8p operates as a capacitor.

[0027] In the example shown in FIG. 2a, the difference in relative area between tunneling capacitors 8p, 8n, on a first hand, and storage capacitor 6, on a second hand, along with any differences in the capacitor dielectric materials and thicknesses, will be reflected in the relative capacitances between these elements. Because the capacitance of storage capacitor 6 is substantially larger than the capacitances of tunnel capacitors 8n, 8p (and also the parasitic gate-to-active capacitance of transistor 4), tunneling of electrons can be achieved at reasonable bias voltages to avoid damage or breakdown. This disparity in capacitive coupling is contemplated to provide excellent programming and erase performance.

[0028] Many variations in the electrical and physical construction of an analog floating-gate circuit in an integrated circuit, relative to that described above, are possible. From an electrical standpoint, such variations include circuits, such as a reference circuit arranged as a conventional dual floating-gate differential amplifier circuit. Examples of other analog floating-gate circuits include analog memory devices and digital electrically programmable memory cells (including cells that may be set into one of more than two possible states, reflecting a multiple-bit data value). From a construction standpoint, such variations include other arrangements of the floating-gate device, including polysilicon-to-polysilicon floating-gate capacitors and polysilicon-to-active capacitors, and including floating-gate devices that are programmable by other mechanisms besides Fowler-Nordheim tunneling. Examples of such alternative structures are described in Patent Application Publication No. US 2013/0221418 and Patent No. US 8,779,550, both commonly assigned herewith, and in Ahuja et al., "A Very High Precision 500-nA CMOS Floating-Gate Analog Voltage Reference", J. Solid-State Circ., Vol. 40, No. 12 (IEEE, December 2005), pp. 2364–72, all such references incorporated herein by reference.

[0029] Data retention is a significant vulnerability in floating-gate devices, particularly in

analog and other precision applications in which degradation of the trapped charge at the floating-gate device is reflected at the output of the circuit that includes such device, sometimes to such an extent that detectable loss of charge at the floating-gate device occurs over the operating life of the integrated circuit. The mechanism of this loss of charge is temperature accelerated, and thus can be accelerated by exposing the integrated circuit to high temperature. Accordingly, a common accelerated life test for integrated circuits including analog floating gate devices is an unbiased bake at a temperature of at least 125 degC for on the order of 1000 hours.

[0030] For example, FIG. 3a illustrates an example of data retention loss in a sample of analog floating-gate circuits. Specifically, the circuits in this sample are voltage reference circuits that have been trimmed to provide a desired output voltage V_{out} , by electrically programming a floating-gate capacitor. The sample analyzed in FIG. 3a includes over 150 individual circuits in wafer form, from multiple wafers over three different wafer lots. In FIG. 3a, the spread labeled “Initial” shows the output voltages of the reference circuits after initial trimming of their floating-gate devices to provide a nominal output voltage V_{out} of 3.00 volts. The horizontal lines indicate the standard deviation of the output voltage spreads for two of the wafer lots. After this initial trimming, the sample exhibited a mean output voltage V_{out} essentially at 3.00 volts, with a standard deviation of around 10 mV.

[0031] FIG. 3a also illustrates the output voltages of this same sample of integrated circuits following a 24 hour bake at 250 degC, in its spread labeled “Post Bake”. As evident from these results, this bake caused significant and detectable retention loss, shifting the mean output voltage V_{out} to about 2.90 volts, with wide variation among the sample as evident by a standard deviation of about 50 mV. This experiment indicated that the charge loss varied both within wafer lots and also among wafer lots. The retention loss from this high temperature bake foreshadows a drift of the output voltage V_{out} in the overall population of these circuits over system life. This data retention loss renders analog floating-gate circuits and devices unsuitable for many precision applications.

[0032] According to example embodiments, the nature of the trapped charge that is lost from a floating-gate device in a data retention bake (as shown in FIG. 3a) or in system use differs from the charge that is programmed into and trapped at the floating-gate device. The difference in the nature of these types of trapped charge is useful to condition the floating-gate devices, in the manufacturing process flow, so that their data retention performance over operating life is

dramatically improved.

[0033] Based on experiments, it is believed that the charge lost from a programmed floating-gate device over time and temperature is the most weakly-bound charge in the device, namely that trapped charge that is at lower energy levels. These types of trapped charge in a floating-gate device are believed to include charge in dielectric material surrounding the floating-gate device due to processing (e.g., plasma charging during deposition and etch processes), and also charge trapped in the capacitor (or transistor gate) dielectric at defects caused by the electrical stress of programming and other operations that apply an electric field across the dielectric material (e.g., akin to stress-induced leakage). More specifically, the trapped charge resulting from processing amounts to charge that already exists on the device as manufactured, and does not depend on the programming operation. By comparison, the electrical stress-induced trapped charge largely results from the high electric fields and significant programming current involved in programming the floating-gate from its native, as-manufactured, state to the nominal trim level. In each of these cases, the trapped charge that is lost in the data retention bake is contemplated to be the same charge that would be lost from the floating-gate device over time during normal operation in its system use via Frankel-Poole conduction and other mechanisms.

[0034] In contrast, the programmed charge trapped on the floating-gate element itself (e.g., polysilicon element 16 of capacitor 6 in FIGS. 2a and 2b) is believed to be at higher energy levels than that of the processing charge and charge at stress-induced defects in the dielectric film. These energy levels are commonly expressed as activation energies. In this regard, it is believed that the programmed charge trapped on the floating-gate element has an activation energy of at least 1.0 eV. Conversely, it is believed that a significant amount of the bulk oxide charge (which is trapped charge from the manufacturing processes) and electrical stress-induced charge has an activation energy below 1.0 eV. For example, the activation energies of silicon/dielectric interface traps ranges from mid-gap (0.0 eV) to the edges of the valance and conduction bands (about 0.6 eV). To the extent that this and other unintentional (e.g., not on the floating-gate electrode) trapped charge is at an activation energy above 1.0 eV, such high energy level charge is not contemplated to affect the data retention performance of the device over normal operating lifetimes.

[0035] It has been discovered, in connection with example embodiments, that these differences

in activation energy are advantageous in conditioning the floating-gate devices during manufacturing test. Generally, example embodiments carry out this conditioning by essentially removing low activation energy trapped charge, which can affect long-term data retention, and replacing that charge with high activation energy trapped charge, which is much more stable over system life. As a result, the trimmed floating-gate devices, such as in an analog circuit (e.g., a voltage or current reference circuit), can be conditioned to ensure the long-term stability and reliability of that trim level.

[0036] Referring to FIG. 4, example embodiments are described for a method of manufacturing integrated circuits, including analog or other circuits that include a floating-gate device to be programmed to a relatively precise trim level.

[0037] As illustrated in FIG. 4, this method begins with process 20, in which integrated circuits including programmable floating-gate devices, in particular such floating-gate devices that are to be programmed to a particular level such as used in analog and other precision circuits, are manufactured. Manufacturing process 20 may be carried out in the conventional manner for the particular technology with which the integrated circuits are to be fabricated. Examples of suitable process flows suitable for use as process 20 according to example embodiments are described in the above-incorporated Patent Application Publication No. US 2013/0221418, Patent No. US 8,779,550, and the above-cited Ahuja et al. article. The programmable floating-gate devices resulting from process 20 may be in the form of capacitors such as capacitor 6 of FIGS. 2a and 2b in which one plate is electrically isolated (e.g. “floating”), or in the form of transistors in which a gate electrode is electrically isolated or floating. For the case of floating-gate capacitors, various types of capacitor construction may be used, including metal-to-polysilicon capacitors such as shown in FIG. 2a and 2b, poly-to-poly capacitors, and poly-to-active capacitors. Floating-gate transistors may be constructed with a single gate electrode that is electrically floating, or in transistors including multiple gate electrodes including the floating gate electrode and one or more control electrodes. Also, the various circuits including the floating-gate devices can vary widely, including analog or digital memory functions, voltage reference and regulator circuits such as low drop-out regulators (LDOs). Accordingly, the types of floating-gate devices and circuits fabricated in the integrated circuits manufactured by process 20 can vary in construction.

[0038] In process 22, initial trimming of the floating-gate devices in the integrated circuits

manufactured in process 20 is performed. This trimming will typically be performed as part of a more extensive electrical test of the integrated circuits including the floating-gate devices, where such electrical test includes those functional and parametric tests suitable for the particular integrated circuits. Typically, electrical test and trim process 22 in example embodiments will be performed with the manufactured integrated circuits in wafer form, such as using automated test equipment at a conventional “multiprobe” test station. Such testing and trimming of the integrated circuits while in wafer form can permit direct access by a probe to the programming circuitry for the floating-gate devices, or to the output of the circuit including the floating-gate device, or both. Alternatively, electrical test and trim process 22 may be performed after dicing and packaging of the integrated circuits manufactured in process 20, particularly if the circuit including the floating-gate device can be accessed directly or indirectly from an external pin.

[0039] As part of electrical test and trim process 22, the floating-gate devices that are to be conditioned according to this embodiment are programmed to a desired analog level. This programming of the floating-gate device, or “trimming” of the circuit including the device, is performed by the application of programming voltages to terminals of the floating-gate device to effect the desired charge transfer to or from the floating gate or plate element. This trimming may be performed by applying the programming bias as a series of pulses, with the output of the circuit sensed periodically to control the programming to stop at the desired circuit output level. Alternatively, the trimming operation may be performed in a separate electrical operation from the electrical test, with the test and trim operations performed at a different time or using different equipment from one another.

[0040] The programming involved in this trimming of the floating-gate devices in process 22 operates to develop a net charge on the floating electrode, through the operation of a mechanism such as Fowler-Nordheim tunneling. In general, the programming involves the movement of electrons through the dielectric film adjacent to the floating-gate electrode such that either electrons or holes, depending on the programming bias applied and the operative mechanism, remain trapped on the floating-gate electrode after removal of the programming bias. In the initial programming performed in electrical test and trim process 22, this trimming brings each floating-gate electrode from its native, as-manufactured, state to the desired programmed level, as reflected at the output of a circuit including the floating-gate electrode. An example of this programmed state is shown in FIG. 3a by the output voltage V_{out} of 3.00 volts to which the

sample of devices was initially programmed (“Initial”).

[0041] According to example embodiments, following electrical test and trim process 22, the trimmed integrated circuits are subjected to a conditioning bake in process 24. Conditioning bake process 24 may be performed on the integrated circuits in the same form as in electrical test and trim process 22, such as in wafer form, or alternatively may be performed following other processing including packaging. As described in further detail below, conditioning bake process 24 is intended to cause the loss of some charge from the floating-gate devices programmed in process 22, specifically that charge that is relatively weakly held in the device and that would be vulnerable to loss during the system life of the integrated circuit.

[0042] In this regard, according to the embodiment shown in FIG. 4, the particular conditions of conditioning bake process 24 are determined in process 25. It has been discovered, according to example embodiments, that the types of charge that is most vulnerable to loss over the operating life of the floating-gate device are those that are held by a temperature-activated mechanism, and that have relatively low activation energies. According to some embodiments, the conditions of conditioning bake process 24 are selected, in process 25, to remove a desired fraction of charge that is at a particular activation energy and lower. Accordingly, inputs into determining process 25 include an estimate of an activation energy E_a of the charge to be removed, and the desired fraction of that charge to be removed from the floating-gate devices.

[0043] According to one approach, process 25 is performed based on knowledge of the temperature acceleration of charge loss. FIG. 5 illustrates time vs. temperature plots corresponding to the removal of at least 90% of charge from a floating-gate device, for charge types of various activation energies ranging from 0.5 eV to 0.9 eV. It is believed, in connection with this embodiment, that trapped charge having an activation energy greater than 1.0 eV is at a sufficiently high energy level as to be unlikely to be lost over the operating life of the integrated circuit at expected temperature and operating conditions. Accordingly, conditioning bake process 24 in this embodiment is directed to that charge at activation energies below 1.0 eV, as shown in FIG. 5.

[0044] The plots of FIG. 5 are based on the well-known Arrhenius equation:

$$n(t) = n(0) \exp \left[vt \cdot \exp \left(-\frac{E_a}{kT} \right) \right]$$

where $n(t)$ is the number of charges (electron charge) at time t , E_a is the activation energy (eV), v

is the collision frequency (sec^{-1}), T is the temperature (deg K), and k is Boltzmann's constant. For the plots of FIG. 5, collision frequency ν is estimated at $1.2\text{E}+03 \text{ sec}^{-1}$ from data corresponding to an activation energy E_a of 1.0 eV at 150 degC. The plots of FIG. 5 are thus calculated by solving the Arrhenius equation for the value of time t at which $n(t) = 0.90n(0)$, at bake temperatures ranging from 150 degC to 250 degC in 25 degree steps, and for each of the activation energies $E_a = [0.5 \text{ eV}, 0.6 \text{ eV}, 0.7 \text{ eV}, 0.8 \text{ eV}, 0.9 \text{ eV}]$.

[0045] According to this embodiment, process 25 is determined by selecting a combination of bake time and bake temperature that is predicted by the Arrhenius equation, or by another approach, to remove a selected fraction of trapped charge, at a selected activation energy or lower, from a floating-gate device such as that in the integrated circuits manufactured in process 20. The selected activation energy of the charge to be removed may be estimated by experiment, or may be based on prior analyses. Referring to FIG. 5, a bake of about 100 hours at about 175 degC would be predicted to remove at least about 90% of trapped charge at activation energies E_a of 0.7 eV and lower. Similarly, a bake of about 24 hours at a temperature of about 250 degC would be predicted to remove at least about 90% of trapped charge at activation energies E_a of 0.8 eV and lower. In any case, conditioning bake process 24 will typically have a duration of at least about four hours, and will typically be at a temperature of at least 125 degC.

[0046] Other approaches for determining the conditions of conditioning bake process 24 may alternatively be used. Such other approaches would consider factors, such as the nature of the trapped charges and the amount of charge to be removed. Also, whether the Arrhenius equation or other approaches are followed, other factors may also enter into the determination of process 25 in selecting the particular conditions of conditioning bake process 24. For example, the bake may need to be performed at or below a maximum temperature of the bake equipment or a maximum temperature that may be tolerated by the integrated circuits. Also, the time involved for the conditioning bake is necessarily limited by the desired manufacturing cycle time. For example, a bake of more than 24 hours would commonly be undesirable.

[0047] Following conditioning bake process 24 at the conditions determined in process 25, re-trim process 26 is then performed on the conditioned integrated circuits as shown in FIG. 5. According to example embodiments, re-trim process 26 again trims the floating-gate devices to replace charge that was lost in conditioning bake 24. As in process 22, the re-trim of process 26 will be performed by programming while monitoring an output voltage from the circuit including

the floating-gate devices being programmed, to ensure that the re-trim reaches but does not significantly exceed the desired level. The amount of charge programmed (e.g., crossing the dielectric film to be trapped at the floating-gate electrode) in re-trim process 26 will typically be much less than the amount of charge programmed in the initial trimming of process 22. This can be seen, by analogy, from FIG. 3a in which the loss of charge shown in the “Post Bake” column, following a 24 hour bake at 250 degC, amounts to a shift of output voltage V_{out} by an average of 100 mV, at a standard deviation of about 50 mV. The change in output voltage effected by the original trimming of process 22 is typically much larger, on the order of volts for the example of FIG. 3a.

[0048] The level to which re-trim process 26 programs the floating-gate devices need not necessarily match the level initially programmed in process 22. The re-trim level should be at least as heavily programmed as in initial programming process 22 (so the magnitude of charge at the floating-gate electrode after re-trim is equal to or greater than that after the initial programming, whether referring to trapped electrons or holes), given the variability of charge loss among a population of devices caused by conditioning bake process 24. If the desired re-trim level is less than that of the originally-programmed level, some devices that exhibit little or no data retention loss may have a programmed level following conditioning bake 24 greater than the ultimate desired level of re-trim process 26.

[0049] Furthermore, according to some embodiments, it is desirable that the level to which re-trim process 26 programs the floating-gate devices is the same to which the initial programming of process 22 trimmed those devices. It is believed that one of the types of charge vulnerable to data retention loss is that charge which is trapped in electrical stress-induced sites in the dielectric of the floating-gate device. It is further believed that the charge that becomes trapped in those electrical stress-induced sites correlates with the amount of programming charge passing through the dielectric in the trimming operation, so it increases with the magnitude of the programming charge. Assuming that stress-induced trapped charge is essentially removed by conditioning bake 24 (e.g., if that charge type has relatively low activation energy), minimizing the extent of the programming in re-trim step 26 would result in less trapped charge at these stress-induced trap sites. This minimization would be accomplished by re-trim process 26 programming the floating-gate devices to no more than about the same level than that originally programmed in the trimming of process 22.

[0050] Similarly as for processes 22, 24, re-trim process 26 may be performed with the integrated circuits still in wafer form (for those implementations in which processes 22, 24 are performed at the wafer level, of course), or alternatively after the packaging or other processing of those integrated circuits. However, if re-trim process 26 is performed after packaging, some provision for direct or indirect access to the circuit including the floating-gate devices must be provided, in order to ensure that the re-trim of those devices is performed to the desired programming level.

[0051] It has been observed from experiment, in connection with example embodiments, that the process described above according to those embodiments significantly improves the data retention performance of floating-gate devices. FIG. 3b illustrates the post re-trim performance of the same sample as shown in FIG. 3a, for which the output voltage V_{out} degraded by about 100 mV on average, from a 24 hour bake at 250 degC. As shown in FIG. 3b by the column indicated "Re-Trim", re-trim process 26 restored the nominal output voltage V_{out} to 3.00 volts to the sample. But following this re-trim, the data retention performance of this sample improved significantly from that following the initial programming, with output voltage V_{out} remaining essentially flat after a 24 hour bake at 125 degC, and then again after 100 hours of the bake at 125 degC. Subsequent data has indicated that this excellent data retention continued for this sample out to 800 hours of the 125 degC bake, with less than 0.5% loss exhibited after that extended bake. Also, this minimal data retention loss over that extended bake also exhibited little variation among the sample, both from wafer-to-wafer within the same lot and among wafer lots. It is therefore contemplated that the excellent data retention of floating-gate devices conditioned by example embodiments will be exhibited over the expected life of the integrated circuits including these devices in system use.

[0052] Accordingly, it is believed, according to example embodiments, and has been borne out by experiment, that the charge lost from the floating-gate devices by conditioning bake process 24 is that of relatively low activation energies, and thus the easiest charge to remove by temperature activation, while the charge re-programmed in re-trim process 26 is that of relatively high activation energy (e.g., charge trapped on the floating-gate electrode), and thus much more difficult to remove by temperature activation. Because temperature-activated mechanisms tend to dominate data retention loss in floating-gate devices, example embodiments can provide significant improvement in the data retention performance of integrated circuits.

[0053] Also, example embodiments can be efficiently implemented into the overall manufacturing and test flow without undue cost or complexity. Equipment costs are minimized, in that only ovens for the conditioning bake and an additional electrical test operation for the re-trim are added to the process flow. Complex and costly additions to the fabrication test flow, such as are involved in the deposition and removal of dielectric films specific to the floating-gate devices, are avoided.

[0054] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A method of setting a trim level of an analog circuit in a semiconductor integrated circuit, the analog circuit including a floating-gate device, the method comprising:
 - electrically programming the floating-gate device to a first trim level;
 - then baking the integrated circuit at an elevated temperature for a selected duration; and
 - then again electrically programming the floating-gate device to a second trim level equal to or greater than about the first trim level.
2. The method of claim 1, wherein the second trim level is equal to about the first trim level.
3. The method of claim 1, wherein the electrically programming is performed with the integrated circuit in wafer form, and wherein the baking includes baking the wafer including the integrated circuit.
4. The method of claim 1, wherein the baking operates to remove charge from the programmed floating-gate device, and further comprising: estimating an activation energy of a type of charge removed by the baking; and based on the activation energy, selecting the elevated temperature and duration of the baking to remove a selected amount of the type of charge.
5. The method of claim 1, wherein the selected duration of the baking is at least about four hours.
6. The method of claim 5, wherein the elevated temperature is at least about 125 degC.
7. The method of claim 1, wherein the elevated temperature is at least about 150 degC, and wherein the selected duration is at least about 24 hours.
8. The method of claim 1, wherein the elevated temperature is at least about 200 degC, and wherein the selected duration is at least about 10 hours.
9. The method of claim 1, wherein the elevated temperature is about 250 degC, and wherein the selected duration is at least about 4 hours.
10. A method of manufacturing a semiconductor integrated circuit, the integrated circuit including a floating-gate device, the method comprising:
 - fabricating a floating-gate device at a semiconductor surface of a body;
 - applying programming voltages to the floating-gate device to store charge at the device corresponding to a first trim level;
 - then baking the integrated circuit at an elevated temperature for a selected duration; and

then applying programming voltages to the floating-gate device to store charge at the device corresponding to a second trim level equal to or greater than about the first trim level.

11. The method of claim 10, wherein the baking operates to remove stored charge from the floating-gate device, and further comprising: estimating an activation energy of a type of charge removed by the baking; and based on the activation energy, selecting the elevated temperature and duration of the baking to remove a selected amount of the type of charge.

12. The method of claim 10, wherein the second trim level is equal to about the first trim level.

13. The method of claim 10, wherein the fabricating fabricates a plurality of integrated circuits at the semiconductor surface of a wafer, each of the plurality of integrated circuits including a floating-gate device, wherein the applying programming voltages is performed for each of the integrated circuits on the wafer, and wherein the baking includes baking the wafer at the elevated temperature for the selected duration.

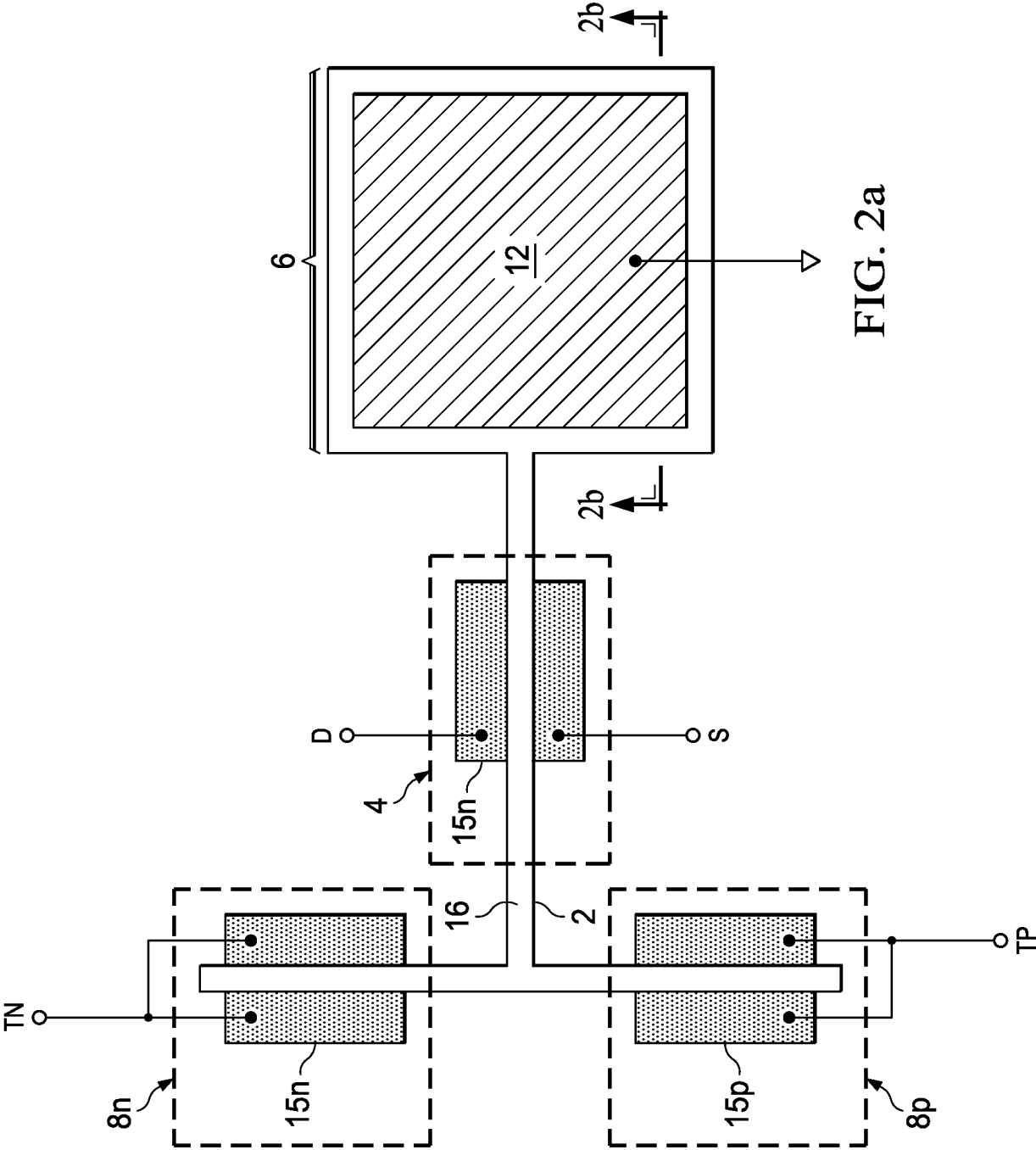
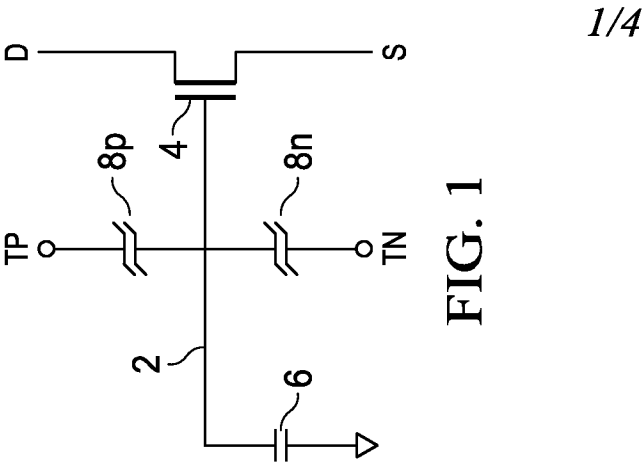
14. The method of claim 10, wherein the selected duration of the baking is at least about four hours.

15. The method of claim 14, wherein the elevated temperature is at least about 125 degC.

16. The method of claim 10, wherein the elevated temperature is at least about 150 degC, and wherein the selected duration is at least about 24 hours.

17. The method of claim 10, wherein the elevated temperature is at least about 200 degC, and wherein the selected duration is at least about 10 hours.

18. The method of claim 10, wherein the elevated temperature is about 250 degC, and wherein the selected duration is at least about 4 hours.



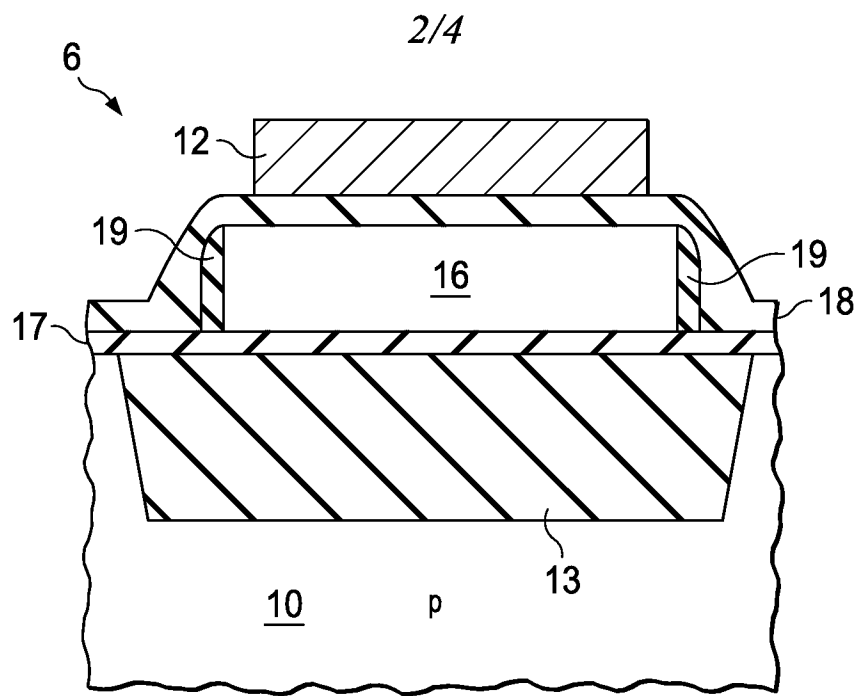


FIG. 2b

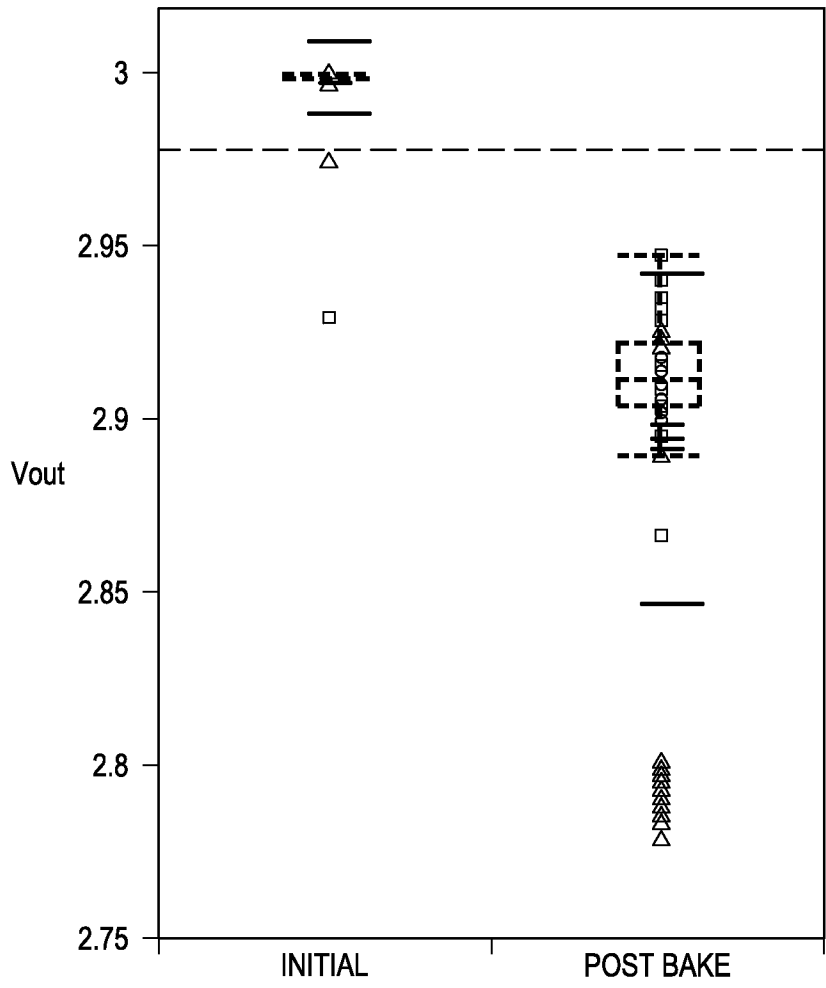
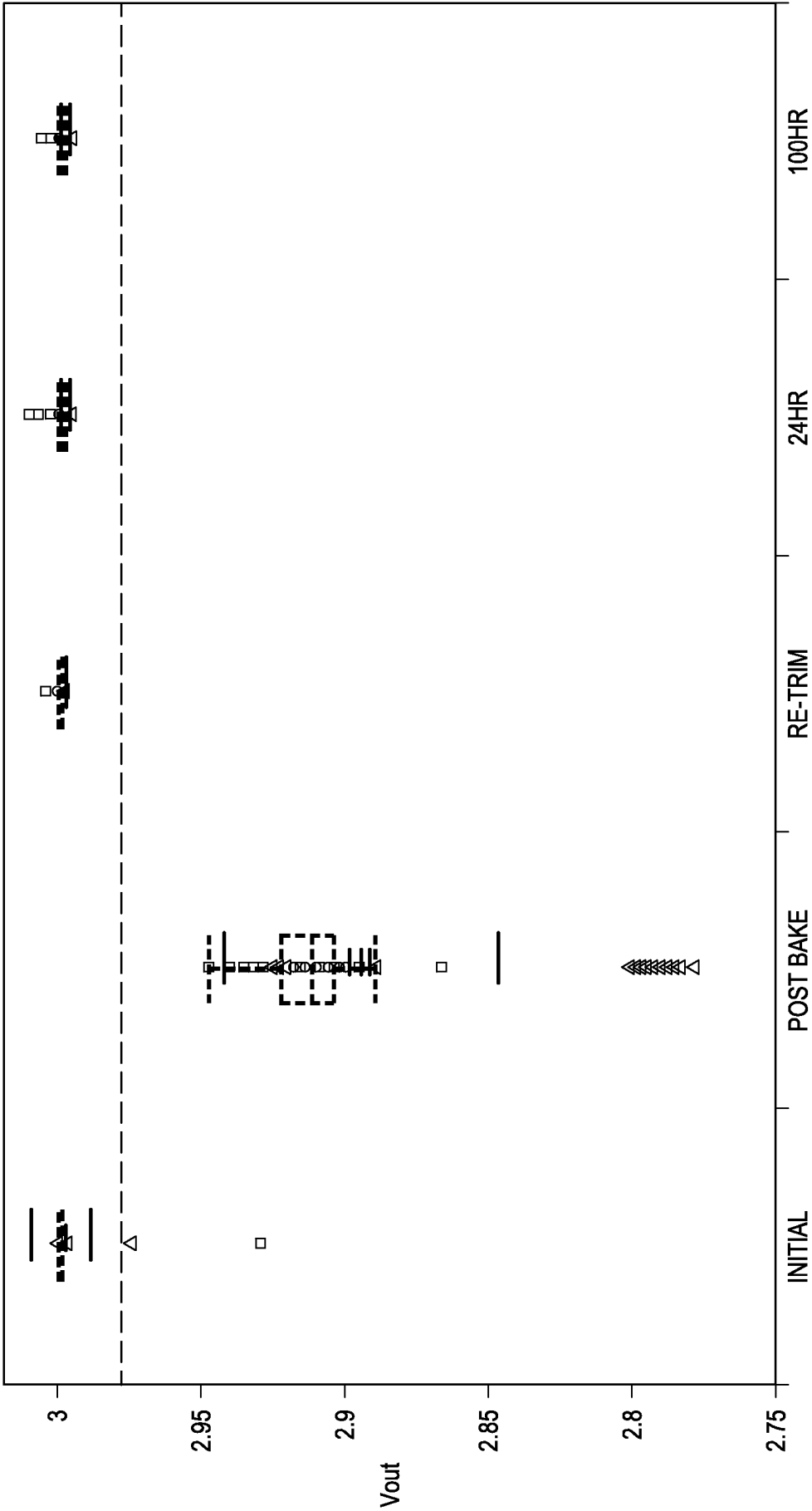


FIG. 3a

FIG. 3b



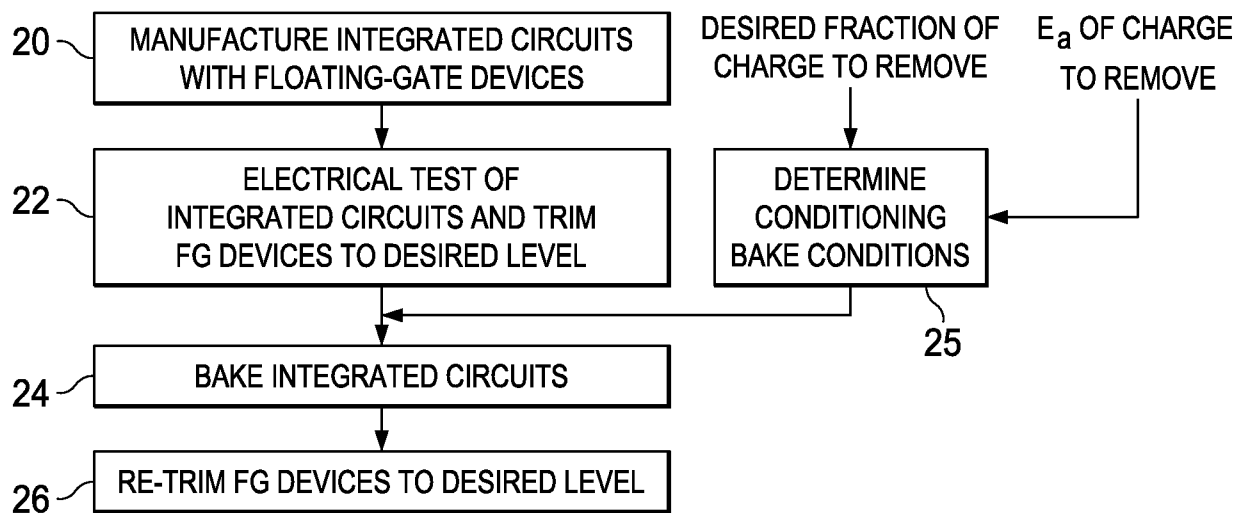


FIG. 4

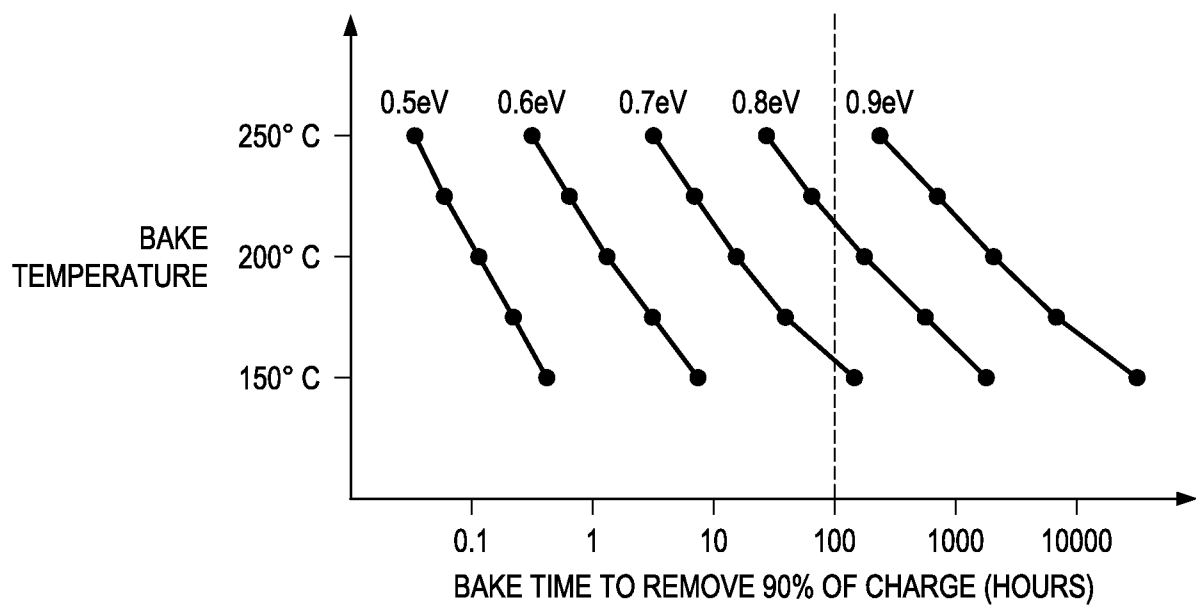


FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2015/035701

A. CLASSIFICATION OF SUBJECT MATTER		
H01L 27/115 (2006.01) G11C 16/04 (2006.01)		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols)		
H01L 21/00, 21/02, 21/04, 21/334, 21/335, 21/336, 21/78, 21/782, 21/824, 21/8247, 27/00, 27/02, 27/04, 27/10, 27/105, 27/108, 27/115, 29/00, 29/66, 29/70, 29/772, G11C 16/00, 16/04,		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 2014/004797 A1 (TEXAS INSTRUMENTS INCORPORATED et al.) 03.01.2014	1-18
A	US 2012/0074479 A1 (TEXAS INSTRUMENTS INCORPORATED) 29.03.2012	1-18
A	US 2012/0241829 A1 (TEXAS INSTRUMENTS INCORPORATED) 27.09.2012	1-18
A	US 2010/0165740 A1 (KABUSHIKI KAISHA TOSHIBA) 01.07.2010	1-18
☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.		
* Special categories of cited documents: “A” document defining the general state of the art which is not considered to be of particular relevance “E” earlier document but published on or after the international filing date “L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) “O” document referring to an oral disclosure, use, exhibition or other means “P” document published prior to the international filing date but later than the priority date claimed “T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention “X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone “Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art “&” document member of the same patent family		
Date of the actual completion of the international search		Date of mailing of the international search report
22 September 2015 (22.09.2015)		08 October 2015 (08.10.2015)
Name and mailing address of the ISA/RU: Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37		Authorized officer M. Bryleva Telephone No. 499-240-25-91