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Machanian et al.

[11] **3,815,720**

[45] **June 11, 1974**

[54] **MONEY RECEIVING AND CREDIT ACCUMULATOR SYSTEM**

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[73] Assignee: **The Wurlitzer Company**, Chicago, Ill.

[22] Filed: **Sept. 8, 1972**

[21] Appl. No.: **287,290**

[52] **U.S. Cl.** ..... **194/15**, 194/1 N

[51] **Int. Cl.** **G11b 19/08**

[58] **Field of Search** ..... 194/9, 1 N, 15, 12; 340/162; 274/10; 179/6.3

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Primary Examiner—Robert B. Reeves
Assistant Examiner—Joseph J. Rolla
Attorney, Agent, or Firm—Olson, Trexler, Wolters, Bushnell & Fosse, Ltd.

[57] **ABSTRACT**

A money receiving and credit accumulator system is disclosed herein which can continuously receive coins therein without the need of resetting a memory circuit or the like. The credit pulses and bonus credit pulses produced are stored until such time as a scanning signal transfers these pulses into an up-down counter. This allows a plurality of coin receiving and tune selection boxes to be positioned at remote locations and each coin receiving box can receive money and store credits and bonus credits independent of the other. The number of credits accumulated for each coin or bill is determined by the monetary value of the coin or bill and the number of bonus credits added to the circuit is determined by the total amount of money deposited. The bonus credits are automatically inserted into an up-down counter which forms part of the credit accumulator circuit. The entire credit accumulator circuit is designed to be formed as an integrated circuit on a single monolithic chip.

17 Claims, 12 Drawing Figures

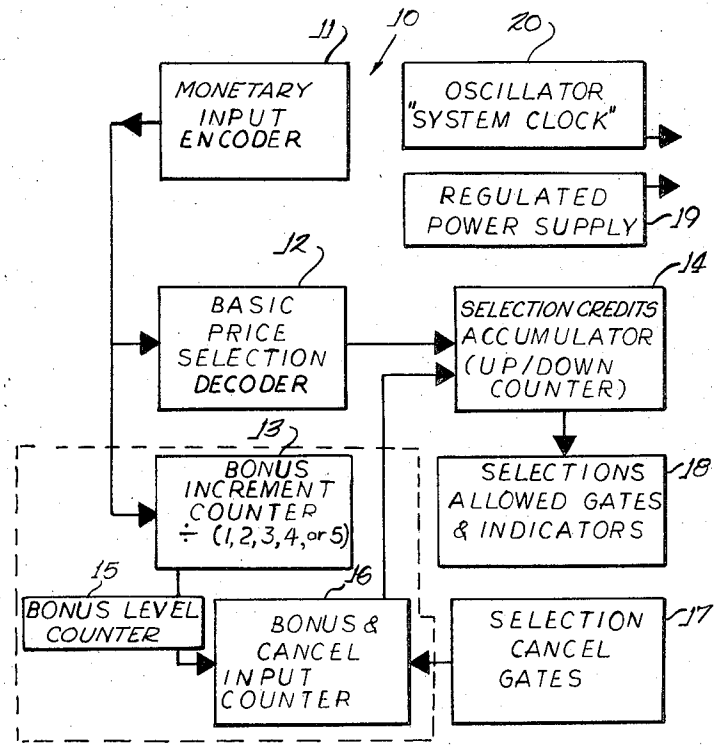


FIG. 1.

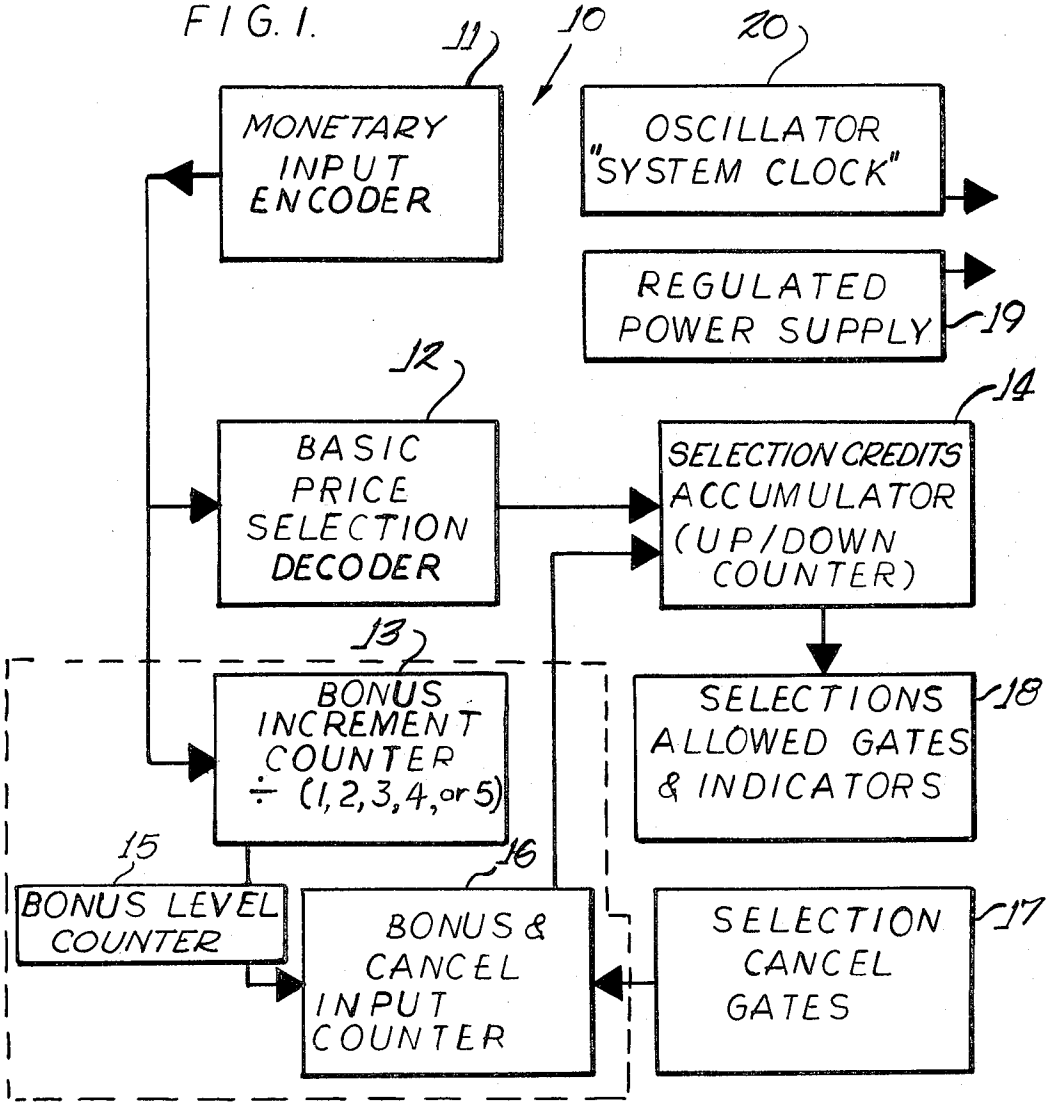
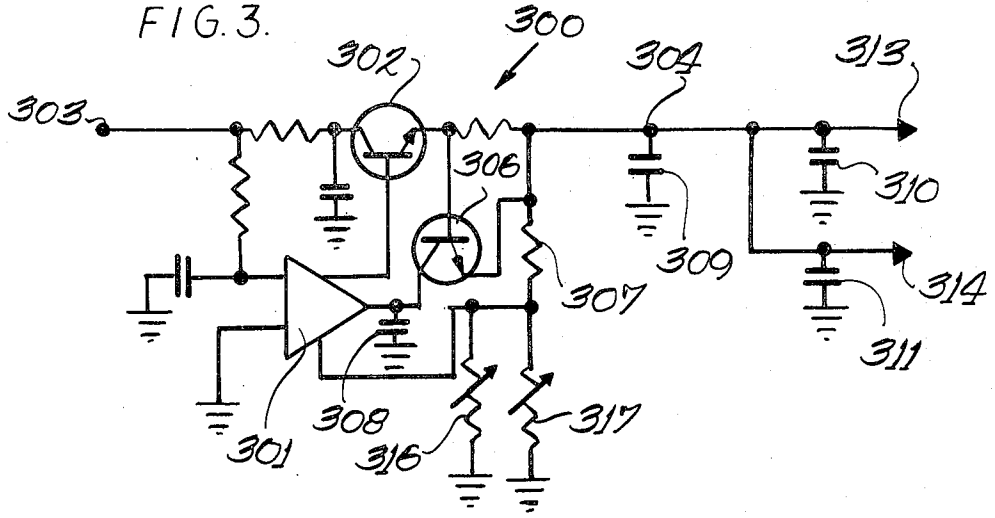

11
10
20
MONETARY INPUT ENCODER
OSCILLATOR "SYSTEM CLOCK"
REGULATED POWER SUPPLY
19
12
14
BASIC PRICE SELECTION DECODER
SELECTION CREDITS ACCUMULATOR (UP/DOWN COUNTER)
13
BONUS INCREMENT COUNTER ÷ (1,2,3,4, or 5)
SELECTIONS ALLOWED GATES & INDICATORS
18
15
16
BONUS LEVEL COUNTER
BONUS & CANCEL INPUT COUNTER
SELECTION CANCEL GATES
17

FIG. 3.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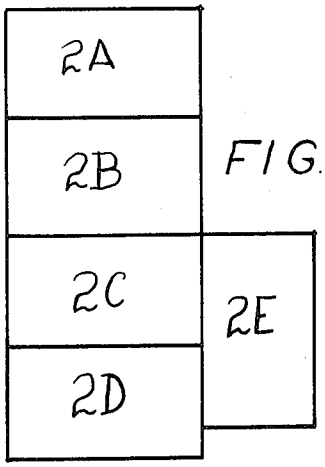


FIG. 2.

FIG. 4.

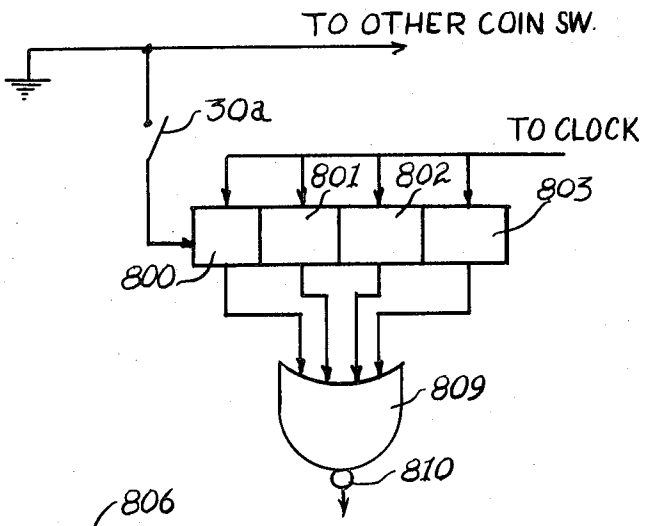


FIG. 5.

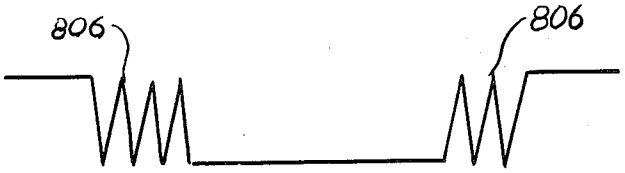


FIG 6

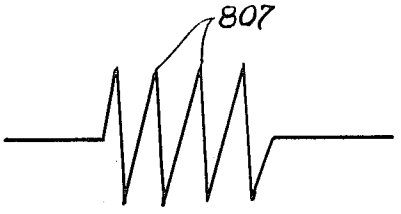
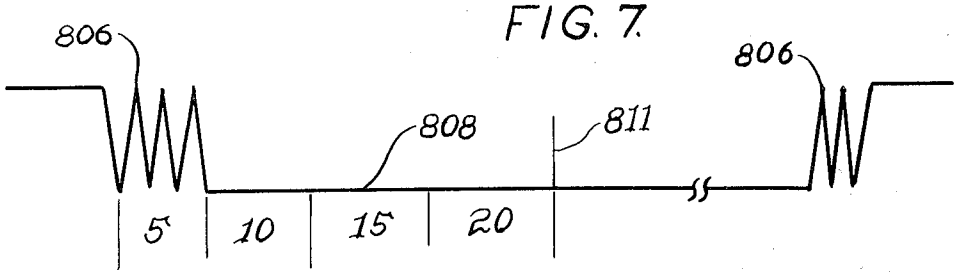


FIG. 7.



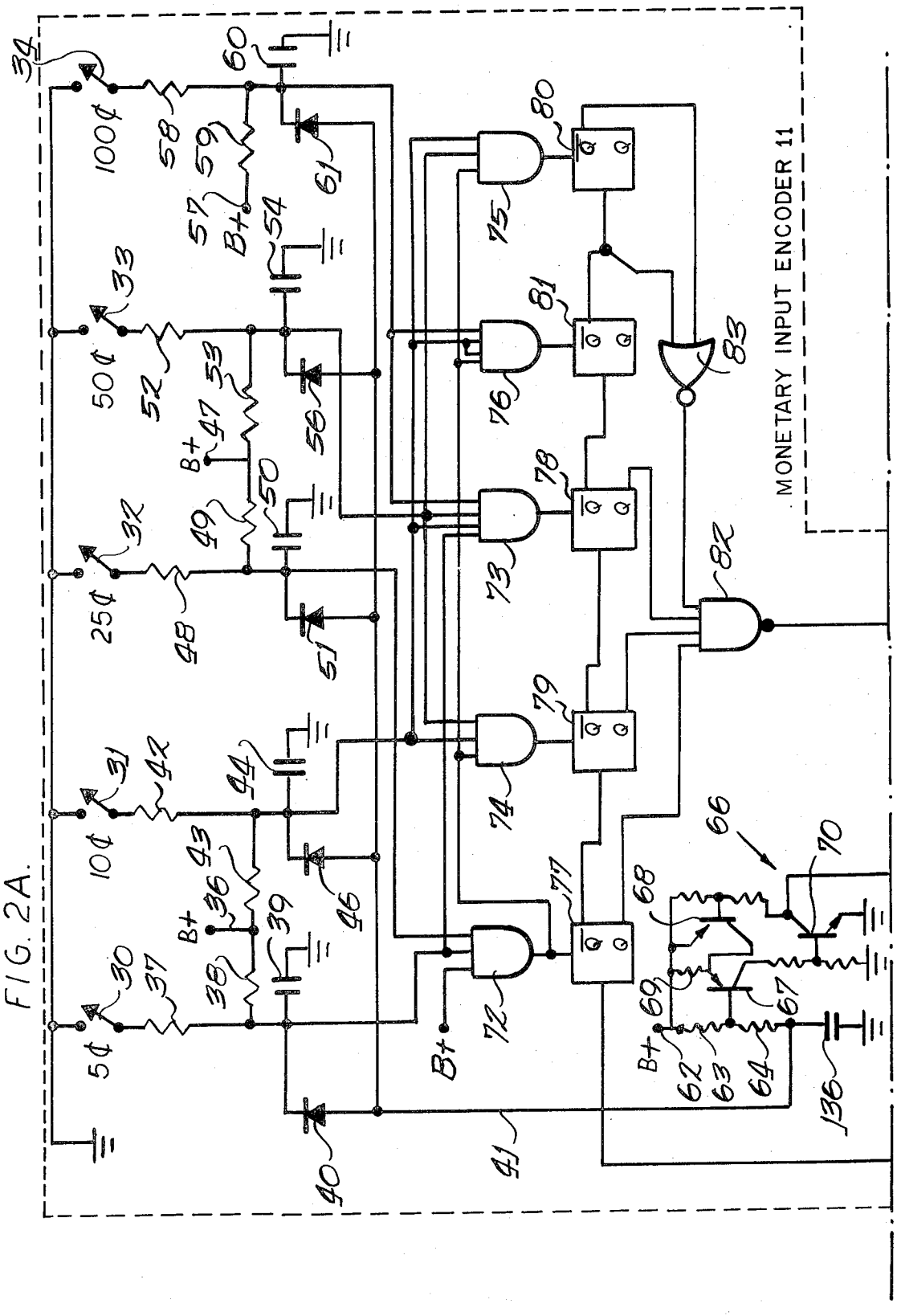


FIG. 2A.

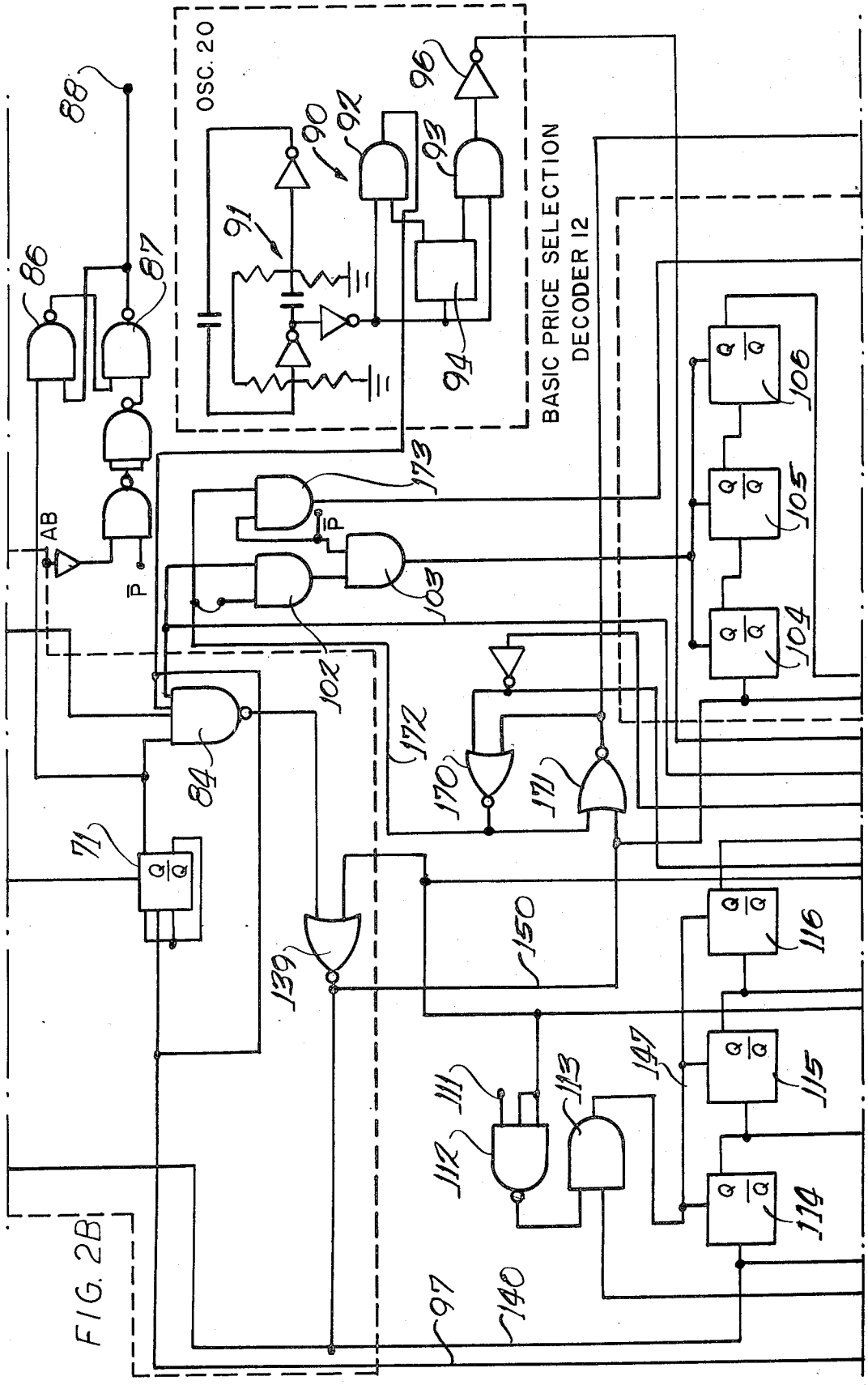

OSC. 20
BASIC PRICE SELECTION DECODER 12
88
86
87
91
90
92
93
96
94
AB
P
173
103
102
84
71
172
170
171
139
150
106
105
104
116
115
114
147
111
112
113
97
140

FIG. 2B

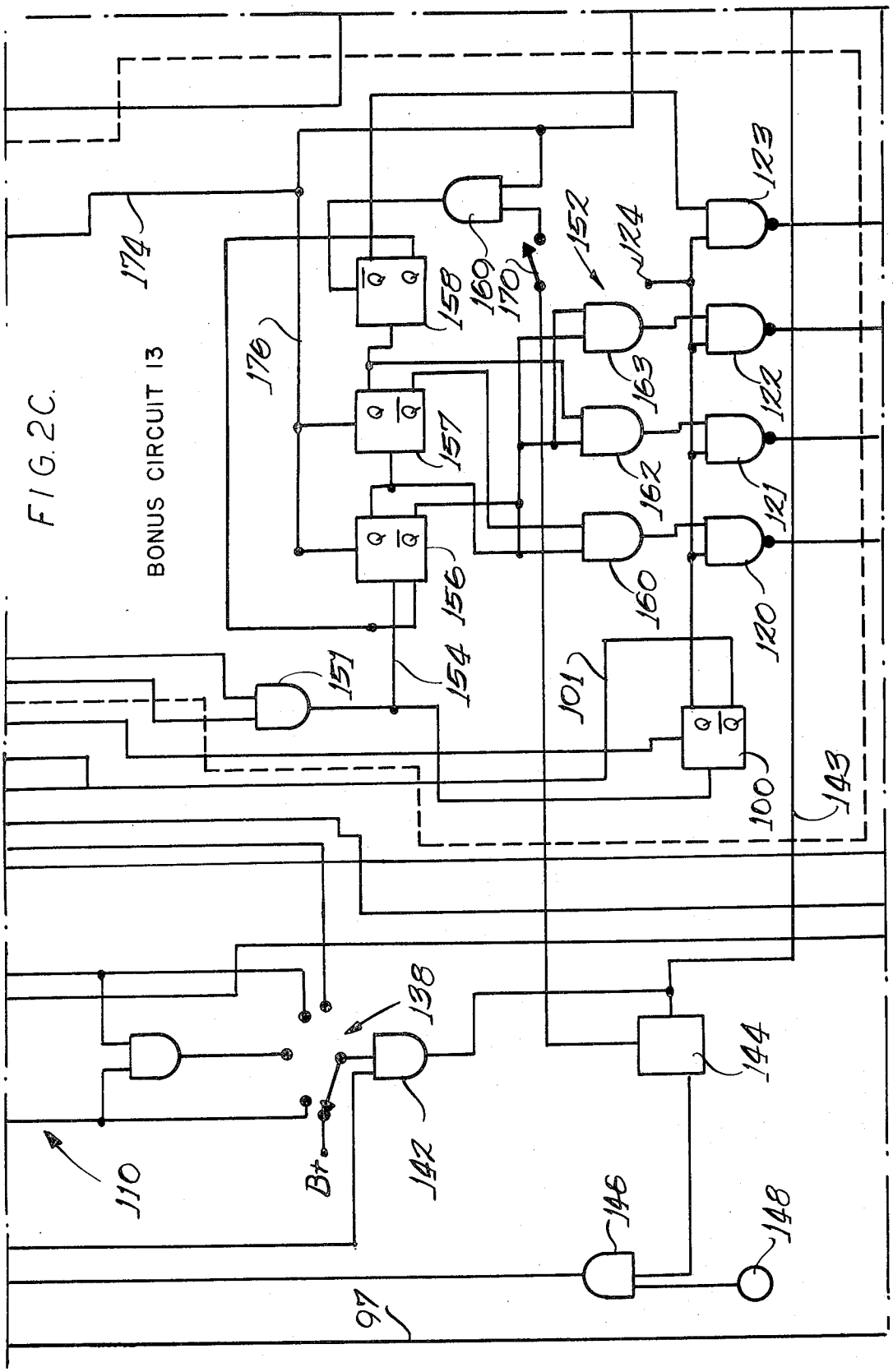

BONUS CIRCUIT 13
174
176
158
160
170
152
124
123
157
163
122
156
162
121
154
160
120
151
101
100
143
138
144
110
B+
142
146
148
97

FIG. 2C.

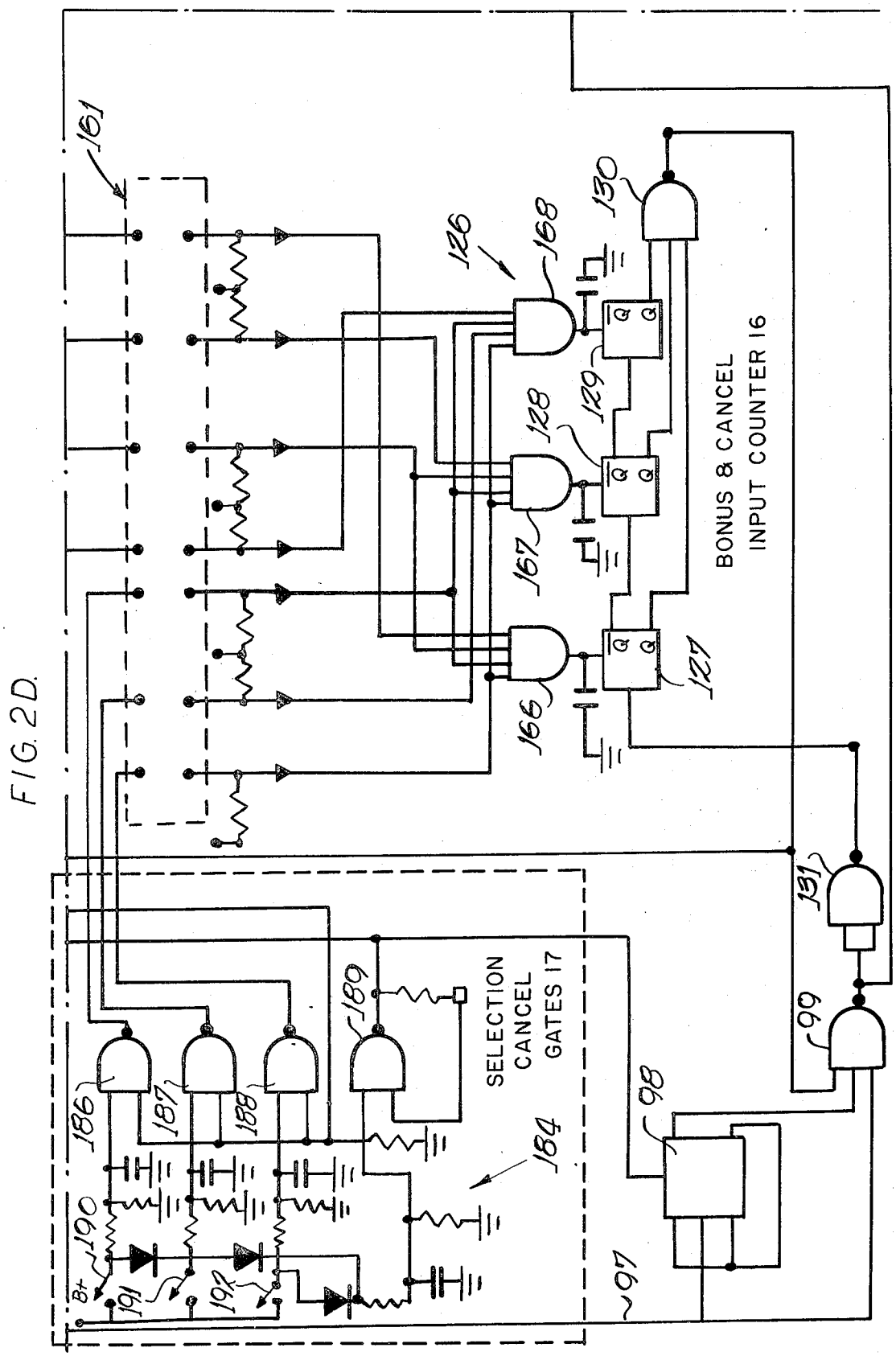
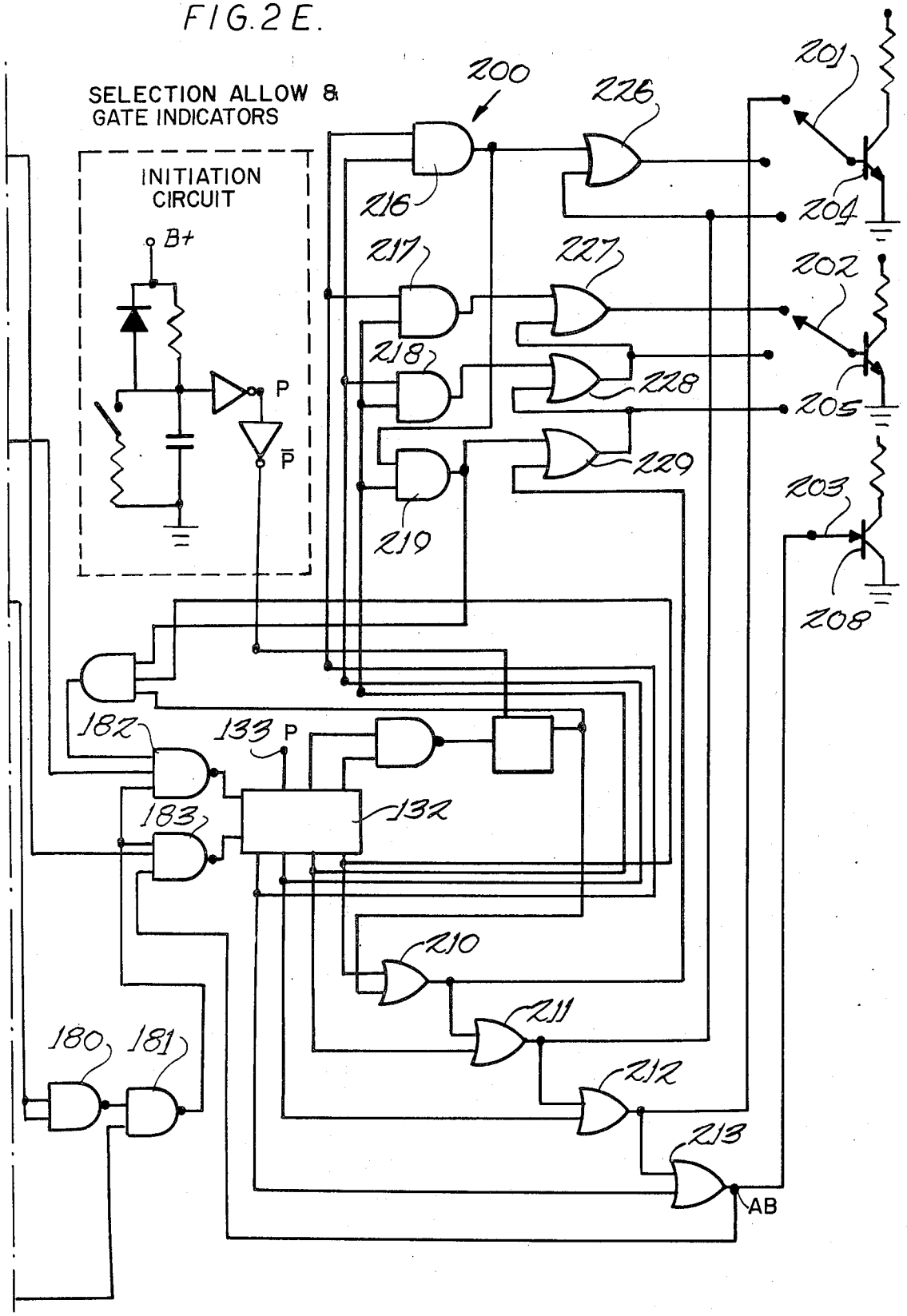

161
126
168
130
128
129
167
127
166
BONUS & CANCEL
INPUT COUNTER 16
131
99
98
97
189
SELECTION
CANCEL
GATES 17
184
186
187
188
190
191
192
B+

FIG. 2D.

FIG. 2E.


SELECTION ALLOW & GATE INDICATORS
INITIATION CIRCUIT
B+
P
P̄
200
201
202
203
204
205
208
216
217
218
219
226
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213
AB

MONEY RECEIVING AND CREDIT ACCUMULATOR SYSTEM

BACKGROUND OF THE INVENTION

This invention relates generally to a coin operated circuit arrangement used to register a number of unit credits corresponding to the value of the coin deposited therein for operating vending machines, or the like. More particularly, the circuit arrangement illustrated herein is directed to a coin accumulator circuit which produces bonus credit pulses to provide a bonus or discount credit when a predetermined minimum monetary value is accumulated in the circuit.

Coin accumulator apparatus are used in vending machines of all kinds and have found widespread popularity for use in situations where coin accumulation is necessary because of the cost of particular items may be more than can be obtained by a single coin, or bill. Several coins, or bills, are then necessary to actuate the necessary mechanisms to allow selection of a particular item from the vending machine or to select a musical selection from a juke box or the like. While vending machines in general are anticipated for use with the present invention the coin accumulator and bonus credit circuit arrangement illustrated herein has particular utility when used in conjunction with juke boxes which play record selections of both the 45 r.p.m. and LP types in a conventional and well-known manner.

Heretofore, the deposit of a particular coin denomination within a coin receiving receptacle of a juke box would allow the depositor to select a given number of records to be played. For example, deposit of a 10 cent and 5 cent coin might allow a single selection while the deposit of a quarter might allow two or three selections to be made, thereby providing bonus or discount credits for using coins of larger denomination. Some prior art units are equipped with coin receiving means capable of receiving 50 cent pieces to allow even a greater number of selections and further bonus or discount credits for coins of larger denomination. For example, five or more selections can be provided for a single 50 cent coin. Generally, coin accumulators allow only a given number of selections corresponding to the denomination of the single coin deposited, and therefore, penalize the vending machine user who happens to have the right amount of money but in smaller denomination coins.

SUMMARY OF THE INVENTION

Accordingly, it is an object of this invention to provide a coin accumulator and bonus credit circuit arrangement which will accumulate coins of all denominations and register credits for the amount of money received and insert bonus or discount credits into the credit accumulator upon sensing money insertion beyond predetermined amounts regardless of the denomination of the coins used to accumulate the credits.

Another object of this invention is to provide a new and improved coin accumulator and bonus credit circuit arrangement which is relatively simple, at least when compared with present day solid state technology, so that it can be formed as a single integrated circuit.

Briefly, the coin accumulator and bonus credit circuit of this invention includes a five stage binary counter and an input encoding network, which may be

a diode matrix or gate, connected to a plurality of movable switch contacts which are actuated by the insertion of coins of different denominations, and may further include a switch operated by sensing the value of a given bill. Each 5 cent input will produce a single clock pulse output from coin input counter which is then applied to a price setting circuit which sets the value of each credit and to a bonus level circuit which will produce discount credits upon sensing a predetermined number of previous regular price credits. Each coin input results in the number of credit pulses or counts which correspond to the number of nickels that can be divided into the coin, that is, a dollar will produce 20 clock pulses from the coin input counter. It will be noted that the coin input encoding network can be altered as desired to accommodate coin values of foreign countries as is necessary.

The price setting circuit is a pre-selected divider circuit used to set the basic price of each selection. In the particular circuit configuration shown the circuit can be manually set to divide the pulse count input by 1, 2, 3, 4 or 5 by the use of a single jumper wire connected in circuit with the divider. Thus, if the divider is set at 2, then two nickel pulses will produce a single selection output pulse at the accumulator and thus set the basic price for each selection to two nickels or one dime per play.

The output pulses from the coin actuated circuit are also delivered to a bonus level circuit which supplies additional credit pulses. This bonus credit circuit is formed by a decoder system which has a separate output for each of the quarter levels to be used for bonus levels. The bonus credits can be given in any preset manner desired. The coin accumulator and bonus credit circuit of this invention also includes an oscillator clock circuit which is the clock pulse generator that is common to all of the sections of the logic circuit and also includes a regulated power supply for applying power to all of the circuits in the system. The entire logic circuit can be formed on a single integrated chip to further cut cost and size.

The novel circuit arrangement of this invention provides for minimizing the number of discrete electronic logic circuits needed while also expanding the versatility of the system so that a multiplicity of coin receiving boxes can be positioned at remote locations at tables, counters or booths and are electrically tied into a single juke box control for making selections remotely therefrom. The circuit arrangement includes a divide-by-1, 2, 4 or 5 circuit which counts credits so that on every preselected bonus level a bonus credit pulse is produced so that additional selection credits are created upon registering the first bonus level (5 cents, 10 cents, 20 cents, 25 cents) in the system regardless of the order in which coins are deposited. The divide (1, 2, 4 or 5) circuit produces a bonus pulse which is stored temporarily in a time delay circuit before it is delivered to the credit and bonus credit accumulator circuit. While the bonus pulse is still in the time delay circuit, the (1, 2, 4 or 5) bonus increment counter will automatically recycle itself upon producing bonus pulse output to again start counting coins which are inserted into the coin receiving mechanism. A synchronized clock pulse is then delivered to the time delay circuit whereupon the bonus credit or credits stored therein are delivered to the credit and bonus credit accumulator. By storing the credit pulse for a predetermined time interval the

bonus increment counter can be actuated in immediate succession by using, for example, six or more successive nickels in a remote selector control box when the bonus increment level is set at 25 cents. Once the bonus pulse is stored in the time delay circuit it can be delivered therefrom to the credit and bonus credit accumulator at a later time corresponding to the scanning or clock pulse time interval. Therefore, the plurality of wall mounted coin receiving selector boxes remotely positioned from a coin operated juke box, or the like, can be scanned one at a time, electronically, and the credit and bonus credits stored therein delivered to the credit and bonus credit accumulator sequentially so that coins deposited in one of the remotely situated coin operated selector boxes will not affect credits in other coin operated selector boxes.

Accordingly, many other objects, features and advantages of this invention will be more fully realized and understood from the following detailed description when taken in conjunction with the accompanying drawings wherein like reference numerals throughout the various views of the drawings are intended to designate similar elements and components.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram showing the various circuit stages arranged in accordance with the principles of this invention;

FIG. **2** shows the arrangement of the sheets containing FIGS. **2A**, **2B**, **2C**, **2D** and **2E**;

FIGS. **2A**, **2B**, **2C**, **2D** and **2E** illustrate the logic circuit of this invention;

FIG. **3** is a schematic diagram showing one form of power supply that can be with this invention;

FIG. **4** is a block diagram illustrating a circuit arrangement whereby extraneous pulses are eliminated from the coin accumulator so that false credits are not given;

FIG. **5** illustrates a wave form showing extraneous pulses which may be produced due to switch bounce when a coin is inserted into the system;

FIG. **6** illustrates extraneous pulses which may be produced by static electricity to give unwanted credits; and

FIG. **7** illustrates the timed delay characteristic of the circuit of FIG. **4** to overcome the effects produced by the extraneous pulses shown in FIGS. **5** and **6**.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

Referring now to the drawings FIG. **1** is a simplified block diagram illustrating the various electronic components of this invention and is designated generally by reference numeral **10.** The electronic circuit **10** preferably is adapted for LSI (large scale integration) so that the entire circuit can be formed on a single chip or substrate using modern logic circuit technology. The components of the circuit **10** can be either bipolar logic (RTL, T^2L etc.) or MOS (*p*-channel, CMOS etc.) or any combination of these, as desired.

The credit and bonus credit accumulator circuit of FIG. **1** is particularly useful when used in conjunction with a juke box wherein the value of each selection may change in accordance with the number of credits registered which corresponds to the amount of money deposited into a coin receiving mechanism. If a single selection is to be made with the system programmed for 10 cents play, a deposit of two nickels, or one dime, will register two coin credits and 1 selection credit. Upon making the selection the selection credit is cleared from the credit accumulator. However, if 25 cents, in any combination ranging from nickels, dimes and quarters is deposited in the coin receiving mechanism, there will be one coin credit for every 5 cents so deposited plus none, one, or more bonus selection credits which, depending on the bonus program, may allow three or more record selections to be obtained. The number of bonus selections awarded any given user at a particular time will correspond to the total amount of money deposited in the coin receiving mechanism prior to making a first selection. By inserting bonus credit pulses into the circuit, the unit cost per selection decreases as the number of bonus credits afforded the user increases.

This is best illustrated by the block diagram of FIG. **1** wherein the coin input counter **11** includes a coin receiving mechanism, and/or a bill reader for detecting bills, which has an output thereof connected to a basic price selection divisor **12.** The basic price selection divisor **12** receives an input signal for each 5 cents of value deposited in the coin receiving mechanism. If the selection base price is 10 cents, as mentioned above, then a divide-by-two circuit will require two pulses from the coin input counter **11.** The output of the coin input counter **11** is also delivered to a bonus increment counter circuit **13,** and the normal credit pulses, after being converted to selection credits, are delivered to the selection accumulator **14** which comprises an up-down counter. After sensing a predetermined number of normal credit pulses a bonus pulse is generated in the bonus increment counter circuit **13** which, in turn, is delivered to the bonus level counter and the bonus and cancel input counter **16** whereupon this bonus pulse is delivered to the selection accumulator up-down counter **14.** The output of the circuit **14** is delivered to a circuit **18** which indicates the number of selections allowed while a circuit arrangement **17** is connected to the bonus and cancel input counter **16** for restarting the circuit thereby preventing a higher number of bonus credit pulses from being supplied after an initial selection has been made.

More specifically, the coin input counter **11** includes a plurality of coin sensing switches and a five stage binary counter circuit connected to an input encoder arrangement. This will allow a single nickel input to result in one clock pulse output to drive the circuits **12** and **13.** Each coin inserted into the coin receiving mechanism of the circuit **11** will result in a number of counts or clock pulses equivalent to the number of nickels that can be divided into the coin so deposited. For example, depositing 10 cents will produce two clock pulses while depositing a dollar in a bill reader will produce 20 clock pulses which are applied both to the basic price selection divisor circuit **12** and to the bonus increment counter circuit **13.** The coin input counter and bonus increment counter may include a diode matrix arrangement which can be easily changed by altering the connections thereto so that variations in foreign coinage can be readily compensated for.

The basic price selection divisor circuit **12** is a preselected divisor which includes a manually operated programming mechanism so that the basic price per selection can be easily set. As mentioned above, the circuit can be set to divide a count pulse train by 1, 2, 3, 4 or

5 by merely rotating the selected switch. It will be understood that the rotary switch can be replaced by a plurality of single pole single throw switches or even jumper wires if desired. If the divisor is set to divide by two, then each selection will require two pulses, corresponding to two nickel inputs, for that given selection. However, if three pulses are needed the selection will cost fifteen cents, and so on. Therefore, the basic price per selection can be altered in the field so that maximum return on investment can be obtained. The bonus increment counter circuit **13** accumulates the output pulses from the coin input encoder and provides an output pulse for every 1, 2, 4 or 5 input pulses depending on the preset divisor. For example, a divide by five will produce one pulse out for every five pulses in; see FIG. **5**, line **25**. The divide by 1, 2, 4 or 5 is the bonus increment counter. The credit accumulator circuit of this invention may be readily adapted to accumulate credits up to 1 dollar and 75 cents or more, thus providing distinct bonus levels (5 cents, 10 cents, 20 cents, 25 cents) at which a different number of bonus pulses can be inserted into the credit accumulator. Each one of the outputs corresponding to the different bonus level can be connected to any one (or none) of seven preset bonus input selection circuits in the bonus and cancel output counter **16**. This allows bonus credits to be given in most any preset manner and the particular bonus credit circuit actuated will be automatically reset upon the user thereof making a selection, this causing actuation of the selection cancel gates **17**.

The bonus and cancel input counter is a three stage counter used for inserting a predetermined number of bonus credits and for cancelling credits after a selection has been made. Bonus output pulses or credits cause a count "up" condition to prevail in the selection accumulator **14** while credit cancellation as the result of tune selection causes a count "down" condition to prevail in the selection accumulator **14**. Preferably, the selection accumulator **14** includes a simple up-down counter arrangement rather than the more complex adder circuit which requires additional hardware. The selection cancel gates within the circuit **17** are formed by a diode or gate matrix which is preset to obtain the desired number of selection cancel counts for such selections as a single selection, an LP (long play selection) or TT selection (top tunes) all of which are preprogrammed into the juke box.

The selection accumulator circuit **14** includes a five stage up-down counter which will provide a maximum of 31 counts corresponding to the 31 selections that can be stored at one time. The selection accumulator circuit may easily be expanded to store **63** or more selection credits by increasing the number of counter stages to six or more. The selections circuit **18** contains the preset circuitry necessary to provide credit indication for either a single or LP or TT selection to give an indication to the user what types of selections he has remaining.

The entire coin operated credit accumulator and bonus circuit arrangement of FIG. **1** is operated by a regulated power supply **19** which is connected in common to all of the blocks in the figure, and the circuit is controlled by means of an oscillator or clock system **20** which is also connected to all of the blocks in FIG. **1**.

Referring now to FIG. **2** the arrangement of the detailed block diagram consisting of FIGS. **2A**, **2B**, **2C**, **2D** and **2E** is shown. The FIGS. **2A–2D** are to be placed on their sides with the top of the drawing to the right of the viewer and FIG. **2E** is to be placed upright adjacent FIGS. **2C** and **2D** as shown.

Referring now to FIG. **2A** the circuit arrangement of this invention includes a plurality of momentary contact switch elements **30**, **31**, **32**, **33** and **34** corresponding to coin valuations of 5 cents, 10 cents, 25 cents, 50 cents and 1 dollar, respectively. Preferably, the switches are to be actuated to a grounded condition which represents a logic 0 output in the system. The switch **30** is connected to a source of voltage at terminal **36** through a pair of resistors **37** and **38** which have a common connection connected through a capacitor **39** to ground potential. The capacitor **39** has connected thereto a diode **40** which has its anode connected to a line **41**. Similarly, the switch **31** is connected to the B+ terminal **36** through a pair of resistors **42** and **43** which have their common juncture connected to a capacitor **44** to ground potential and to a second diode **46** which also has its anode connected to line **41**. The switch **32** is connected to a B+ terminal **47** through a pair of resistors **48** and **49** which have their common juncture connected to ground potential through a capacitor **50**. The capacitor **50** is also connected to a diode **51** which has its anode connected to the common line **41**. In like manner the switch **33** is connected to the B+ line **47** through a pair of resistors **52** and **53** which have their common juncture connected to ground potential through a capacitor **54**. The juncture of resistors **52** and **53** and capacitor **54** are connected to line **41** through a diode **56**. The switch **34**, which corresponds to a 1 dollar valuation from a bill reader, is connected to a B+ terminal **57** through a pair of resistors **58** and **59** which have their juncture connected to ground potential through a capacitor **60**. The juncture of resistors **58** and **59** and capacitor **60** are connected to the line **41** through a diode **61**. Therefore, when any of the switches **30–34** are closed and ground potential is applied to the cathode of the respective diodes **40**, **46**, **51**, **56** and **61**, and the diodes will be forward biased to provide current flow from a B+ terminal **62** through a pair of series connected resistors **63** and **64**.

Resistors **63** and **64** form part of a transistorized differential enabling circuit designated generally by reference numeral **66**. The enabling circuit **66** comprises a pair of transistors **67** and **68** connected in such a manner that transistor **68** shunts the emitter resistor **69** of the transistor **67**. Therefore, once transistor **67** is rendered operative at a first initial voltage value it requires a higher subsequent voltage value to render the transistor inoperative. Conduction of transistor **67** will apply base emitter current through a transistor **70** which becomes saturated to apply ground potential to the clear input of a JK flip-flop network **71**, shown in FIG. **2B**.

The logic 0 state developed by closure of switch **30** is applied to one of the inputs of an AND gate **72** and to one of the inputs of an AND gate **73** directly and through AND gate **72** to AND gates **74**, **75**, and **76** thus registering a one count through AND gate **72** corresponding to a nickel value. Closure of the ten cent switch **31** will produce a logic 0 state at the AND gate **74** and at one of the inputs of an AND gate **75**. The pulse from switch **31** is also applied to an input of the AND gate **73** and gate **76**. The 25 cent switch **32**, when closed, will apply a 0 state to the input of AND gate **72** and through gate **72** to AND gates **74**, **75**, and **76**. On

the other hand, closure of 50 cent switch **33** will apply a 0 state to the inputs of AND gates **74, 73, 75** responsive to the 50 cent switch **33.** Closure of the 1 dollar bill reader switch **34** will apply a 0 state to the AND gates **73** and **76.** The outputs of AND gates **72, 73, 74, 75** and **76** are connected to a counter circuit arrangement comprising a plurality of JK flip-flops **77, 78, 79, 80,** and **81,** respectively which have their $\bar{Q}$ outputs connected to the toggle input of the adjacent flip-flop and the Q outputs of the flip-flops **77, 78,** and **79** are connected to a NAND gate **82** which also receives an input from a NOR gate **83** via the flip-flops **80** and **81.** When all of the inputs to NAND gate **82** are high the outputs thereof will go low and apply a logic 0 pulse to the input of NAND gate **84,** in FIG. **2B.**

The Q output of the JK flip-flop **71** is also connected to an input of the NAND gate **84** and to the input of NAND gate **86,** which in turn, has its output connected back to the input of a second NAND gate **87** which is connected in like manner, i.e., with its output connected back to the input of NAND gate **86** and to an output terminal **88** and can be used to energize a coin indicating lamp when the system is in use.

Also connected to an input of the NAND gate **84** is a clock circuit **90** comprising a multivibrator oscillator circuit **91** having an output thereof connected to a pair of AND gates **92** and **93** through a flip-flop circuit **94.** The output of AND gate **93** is inverted through an inverter **96** thereby producing pulses which are opposite in polarity to those pulses produced at the output of AND gate **92.** This will produce two outputs from the four phase clock circuit which are out of phase by 180°. The output from the clock circuit **90** is also applied to the toggle input of the flip-flop circuit **71,** through a line **97,** to the input of a flip-flop circuit **98** and to a NAND gate **99,** shown in FIG. **2D.** A set reset flip-flop **100** of the bonus level output circuit has one output thereof connected through a line **101** to the input of NAND gate **84** and to the input of an AND gate **102,** which, in turn, has the output thereof connected to a gate circuit **103** for resetting a plurality of flip-flop circuits **104, 105, 106.**

The clock circuit **90** provides the control pulses for all of the system counting and sequencing operations. As mentioned previously, there is provided two clock signals arranged in a predetermined timed relation from one another, as, for example, 180° out of phase. The first clock pulse at the output of AND gate **92** is the main clock signal while the second clock pulse from the output of the inverter **96** is used to recycle the bonus level indicator circuits, the bonus pulse trigger circuits, and the basic price counter circuits. To provide the two basic clock signals the output of the multivibrator circuit **91** is applied to the toggle input of the flip-flop circuit **94** and simultaneously to an input of the AND gate **92.** This will provide two 10 KHz signals which are 180° out of phase with one another.

When the coin accumulating circuit is first turned on the overall control circuit or system is set to a cleared or initial condition. This can be done with a transistor circuit which has a first transistor which is turned on which, in turn, results in turning off a second transistor to provide the clear or reset signal. During this initialization period the flip-flop circuits **77, 79, 78, 81** and **80** of the coin input pulse counter are allowed to toggle until all of the Q outputs are at a logic 1. This will cause the output of gate **82** to go to a logic 0 which inhibits further clock pulses or toggling signals to pass through the gate circuit **84.**

Also during the initialization period, i.e., when the system is turned on, the basic price counter circuit **110** is reset directly by the output of the clear circuit which is connected to input terminal **111** of a NAND gate **112** which, in turn, has the output thereof connected to the input of a second AND gate **113.** This action will set the clear lines of flip-flop circuits **114, 115** and **116** so that there respective Q outputs are at a logic 0 and their $\bar{Q}$ outputs are at a logic 1.

Also during the initialization period the reset signal is also routed through the AND gate **103** to reset the flip-flop circuits **104, 105** and **106** of the bonus increment counter circuit. Therefore, the Q outputs are set to a logic 0 while the $\bar{Q}$ outputs are set to a logic 1. In addition, this initialization pulse is delivered to the bonus level output gates **120, 121, 122** and **123** at a terminal **124** so that the number of bonus pulses to be generated, at the outset of operation, is zero.

A bonus cancel counter circuit **126** is allowed to toggle during the initialization period until all the Q outputs of the individual flip-flop circuits **127, 128** and **129** are at a logic 1 condition. This action will inhibit further toggling of the flip-flops by setting the NAND gate **130** to a logic 0 which, in turn, inhibits further toggling by means of clock pulses through the NAND gate **99** and NAND gate **131** which has the output thereof connected to the input of the first flip-flop **127.**

Also during the initialization period the main up-down credit counter **132,** FIG. **2C,** is reset to have the output thereof at a logic 0 when the input to the direct clear terminal **133** is at a logic 1. Now that the entire circuit is set to an initial condition, it is ready to perform a credit accumulating and bonus pulse generating function.

Referring back to FIG. **2A,** the coin input pulse generator circuit encodes the credit input in order to provide a credit input signal to the other parts of the system in terms of the multiple of the basic unit of credit; in this instance each 5 cents. When a coin is inserted into the coin receiving mechanism, one of the switches **30, 31, 32, 33** or **34** is closed and connected to ground potential. At the outset of operation the $\bar{Q}$ output of flip-flops **77, 79, 78, 81** and **80** are set at a logic 0. By inserting a nickel to close switch **30** the $\bar{Q}$ output of these flip-flops are set to a logic 1 state. On the other hand, inserting 10 cents to close switch **31** will set flip-flops **79, 78, 81** and **80** to a logic 1 state while flip-flop circuit **77** remains in the logic 0 state. Inserting 25 cents to close switch **32** will cause flip-flop circuits **77** and **79** and flip-flop circuits **81** and **80** to have their $\bar{Q}$ outputs in the logic 1 state while flip-flop circuit **78** has its $\bar{Q}$ output in the logic 0 state. A 50 cent insertion into the coin mechanism will close switch **33** thereby producing a logic 0 at the $\bar{Q}$ output of flip-flop circuits **77** and **81** while a logic 1 state exists at the Q output of flip-flop circuits **79, 78** and **80.** By closing the dollar acceptance switch **34** the flip-flop circuits **77, 79** and **80** have their $\bar{Q}$ output set to a logic 0 state while flip-flop circuits **78** and **81** have their $\bar{Q}$ outputs set to a logic 1 state. This then is the different logic state configurations for the respective input signals from the coin receiving mechanism.

The five flip-flop circuits in the coin counting circuit are arranged in a "count up" configuration so that one input pulse is required to set the $\bar{Q}$ outputs of the flip-

flops from a state of (11111) to a state of (00000). This counter arrangement will reset to an all $\overline{Q} = 0$ output condition on the first clock pulse received after a count of 31 is reached.

In addition to setting the credit counter, the closing of any one of the coin switches will activate the double threshold circuit **66** which inhibits the clocking of the coin input pulse generator. This is accomplished by the fact that transistor **67** is normally high and when a coin switch is closed the output of transistor **70** goes low thereby forcing the Q output of the flip-flop circuit **71** to a low state thereby blocking the clock pulses at the NAND gate **84**. After the coin has passed through the coin receiving mechanism and the appropriate actuated switch is again opened the capacitor **136** is discharged, and after approximately 45 milliseconds, the output of transistor **70** again goes high so that clock pulses will again pass through the NAND gate **84**. The next clock pulse changes the Q output of flip-flop circuit **71** to a logical 1 state and allows the clock signals to pass through the NAND gate **84**. This action allows the input pulse counter to count up to an initial state and transmit this credit information into the basic price counter circuit **110**.

The basic price counter circuit **10** is a programmable divide-by -*n* ($n = 1, 2, 3, 4$ or 5) counter which is used to set the number of basic units of credit, i.e., the number of nickels required, for a single play selection when the coin accumulator circuit of this invention is used in conjunction with a juke box or the like. The desired number of credit pulses required to select a single play is selected by a plug-in program card which may include a rotary switch **138**. The credit information from the coin input pulse counter is transmitted to the basic price counter through a NOR gate **139** via a line **140** to the toggle input of the first flip-flop circuit **114**. The three flip-flop circuits **114, 115** and **116** make up the basic price counter circuit arrangement and in operation count to a condition one less than the desired number. At a count of $n - 1$ pulses a logic 1 state is present so that the next clock pulse input therein will be transmitted through an AND gate **142** to the next main credit counter circuit via a line **143** and to the basic price counter reset flip-flop circuit **144**.

The $\overline{Q}$ output of flip-flop circuit **144** is in a normally high state. When a clock pulse is transmitted through the AND gate **142** the $\overline{Q}$ output of flip-flop circuit **144** goes to a logic 0 which, in turn, passes through an AND gate **146** and through the AND gate **113** to a reset line **147** to reset the flip-flop circuits **114, 115** and **116**. The next out of phase clock pulse, the pulse developed from the inverter **96**, is applied to the counter circuit and will enable the counter circuit so that when the next regular input clock pulse is received it will begin to count.

A partial credit cancel circuit may be included as an optional circuit and connected to a terminal **148** at the input of the AND gate **146**. When a partial credit cancel feature is used the cancel pulses from the bonus cancel counter circuit **126** are transmitted through a logic circuit to reset the basic price counter to a 0 count condition whenever a selection is made. However, if a partial credit is to be retained the input terminal **148** receives a hold signal. In this configuration partial credit is cancelled only when a bonus credit is allowed. The Q output of the flip-flop circuit **100** goes to a logic 1 only when a bonus pulse is to be entered into the bonus and cancel input counter circuit. This logic 1 pulse then is transmitted through to cancel any remaining partial credits in the circuit. For example, if a quarter is inserted and the basic price per credit is 10 cents, two single selections will be allowed in the basic price counter. An additional selection(s) will be allowed by the bonus arrangement at the quarter level and will cancel the 5 cent partial credit in the basic price counter.

The bonus credit increment counter, comprising flip-flop circuits **104, 105** and **106**, will continue to accumulate input pulses from the coin input pulse counter and provide an output pulse therefrom for every five such input pulses when $n = 5$. The output pulses from the coin input pulse counter circuit enter the basic increment counter circuit through a line **150** from the NOR gate **139** to toggle the first input of flip-flop circuit **104**. The three stage binary counter counts to four making the Q output of the flip-flop circuit **106** a logic 1. A fifth clock pulse is then allowed to pass through the output AND gate **151** to a bonus level indicator circuit designated generally by reference numeral **152**. This pulse toggles the bonus trigger flip-flop circuit **100** and the bonus level indicator circuit **152** through a line **154** at the input of a first flip-flop circuit **156**. The bonus level indicator circuit **152** includes three flip-flop circuits, the flip-flop circuit **156** together with additional flip-flop circuits **157** and **158**. The $\overline{Q}$ output of the flip-flop circuit **100** is used to reset the basic bonus increment counter circuit through the output line **101**, the AND gates **102** and **103**, and to the reset input circuits of the flip-flops **104, 105** and **106**. This action will then reset the flip-flop circuit **100** to its normal state, that is with the output terminal $\overline{Q}$ in the logic 1 state, this being accomplished by the first out of phase clock pulse after the reset signal is applied thereto.

The bonus level indicator circuit **152** is a basic three stage binary counter system which counts the output pulses of the basic bonus increment counter through AND gate **151** in order to determine the bonus level, i.e., a 25 cent condition, a 50 cent condition, a 75 cent condition, or a 1 dollar condition. The output of the basic bonus increment counter is transmitted through the AND gate **151** to toggle the input of the first flip-flop circuit **156**. The normal state of the Q outputs of the flip-flops **156, 157** and **158** is a logic 0. Therefore, a first pulse input will produce a logic 1 pulse at the Q output of flip-flop **156** which, in turn, is passed through an associated buffer AND gate **160** through the NAND gate **120** to an input terminal of a program card shown generally by the broken lines at **161**. A second bonus level is indicated by having a logic 1 output at the Q terminal of flip-flop **157**, which, in turn, passes through the buffer AND gate **162** to the NAND gate **121**. A third pulse input to the bonus level indicator will toggle flip-flop circuit **158** and produce a logic 1 output therefrom and from the first flip-flop **156** to thereby produce an output signal through NAND gate **122** as the result of a signal passing through the buffer AND gate **163**. When the bonus trigger flip-flop circuit **100** toggles to a logic 1 output condition it will allow a pulse to pass through the appropriate output gates **120, 121, 122** or **123** to deliver the information to the program card **161**. Each bonus level can be programmed individually for up to and including seven bonus credits. The program card setting determines the routing of the bonus pulse to the appropriate AND gates **166, 167** or **168** of the bonus and cancel counter circuit **126**.

The bonus credit counter is recycled to a 0 output condition after a first selection on the juke box is made so that accumulation of coins again begins with a first bonus credit being given for the first 25 cents, a second bonus credit being given for the second 25 cents and so on. The reset signal for the bonus credit counter is obtained by the output of a pair of NOR gates **170** and **171** to a line **172** which passes through the input of an AND gate **173** and therefrom through a line **174,** FIG. 2C, to the reset line **176** of the bonus credit counter.

The main credit counter is a five stage up-down counter which stores all the accumulated selection credits, both coin credits and bonus credits, in the counter circuit **132,** FIG. 2C. The basic coin credits and bonus credits are applied thereto through a pair of NAND gates **180** and **181** and through a second pair of NAND gates **182** and **183.** There are two sets of inputs to the up-down counter **132,** one input **182** to count up, and the other input **183** to count down. The output signal from the NOR gates **170** and **171** determines which function the up-down counter **132** will perform, i.e., whether a count up or a count down condition is set therein. If the output of NOR gate **170** is a logic 1 the pulses applied to the up-down counter will count up in an accumulated mode. However, if the output signal from flip-flop **170** is a logic 0 then the up-down counter will cancel or count down.

A logic 0 output signal from a selection allowed decoder circuit **184,** blocks the output of the counter circuit **132** to a (00000) condition and prevents the counter from counting down. The selection allowed decoder circuit also provides a signal to the main credit counter to indicate that a count of 31 has been reached so that it will not recycle itself to 0 at the thirty-second count.

The selection allowed decoder circuit includes a plurality of NAND gates **186, 187, 188** and **189** which have their outputs connected to the card programmer **161** and therefrom to the appropriate indicating circuits. The NAND gate **186** has a switch **190** which may be selected to indicate a top tune selection while the AND gate **187** includes a switch **191** which is selected for an LP record while the AND gate **188** has connected thereto a switch **192** for normal single selections of 45 r.p.m. records. Closure of one of the switches **190, 191** or **192** will set the condition of the circuit so that the proper number of credits and bonus credits will be collected so that a top tune condition or an LP selection can be made.

The bonus cancel counter circuit **126** delivers data pulses signal information into the main counter circuit **132** in response to bonus trigger pulses or cancel pulses depending on whether the counter is to count up or count down. The output of the program card **161** is decoded by AND gates **166, 167,** and **168** and the bonus and cancel counter. These gates (**166, 167, 168**) receive a logic 0 pulse which presets a count in the three stage binary bonus and cancel counter. Whenever a bonus or cancel pulse is entered the output of the NAND gate **130** changes its state to a logic 1, and this signal is used to lock the coin input pulse counter to an off condition. The normal state of the Q outputs of the counters **127, 128** and **129** is (**111**), and when this condition is present the clock pulses are blocked by the off condition of NAND gate **99** which, in turn, is responsive to the logic 0 output of the NAND gate **130.**

The circuit including NAND gate **189** is a double-threshold circuit which controls the cancel function. When a selection is made the main credit counter is in the cancel mode and the correct number of cancel pulses are transmitted to the main credit counter by the bonus and cancel counter circuit **126.**

The allowed selection decoder circuit is designated generally by reference numeral **200** and monitors the state of the main credit counter **132** to provide a credit status information to the selection allowed relays of the juke box via a plurality of switches **201, 202** and **203** connected to transistors **204, 205,** and **206,** respectively. A plurality of OR gates **210, 211, 212** and **213** have their outputs connected to certain ones of the contact switches **201, 202** and **203** and the inputs thereof connected back to the output of the main credit counter **132.** With a 0 count in the main credit counter **132** the output condition of each of the gates **210, 211, 212** and **213** is as follows. A 0 count 0 output from each gate, a 1 count a single output from gate **213,** a 2 count an output from gates **212** and **213,** a 3 count outputs from gates **212** and **213,** a 4 to 7 count outputs from gates **211, 212** and **213,** and a count from between 8 and 31 will produce an output from each of the gates **210, 211, 212** and **213.** However, the output from the main credit counter **132** is also delivered to a plurality of AND gates **216, 217, 218** and **219** which acts as an intermediate decoding stage for the main credit counter outputs. These gates operate as follows. A 0 to 2 count will achieve 0 outputs from all of the gates. A 3 count will produce a 1 output from the gate **216** while a 4 count will produce 0 outputs from all of the gates. A 5 count, however, produces a 1 output from gate **217** while a 6 count produces a 1 output from gate **218,** and a count of 7 will produce a 1 output from all of the gates. A count of 8, 9 or 10 will again produce a 0 output from all of the gates. An 11 count will produce a 1 output from gate **216** while a 12 count will produce 0 outputs. A 13 count will produce a 1 output from gate **217** and a **14** count will produce a 1 output from the gate **218** while a 15 count will produce a 1 output from all of the gates. Since the only outputs of the main counter are used to recycle the AND gates it will produce an identical count for the number 16 as well as the number 0 and so forth.

The outputs of the AND gates **216, 217, 218** and **219** are connected to one of the inputs of NOR gates **226, 227, 228** and **229** which function as the final decoding stage of the main credit counter circuit **132.** The output of these gates will indicate the status of the main credit counter showing the attained level of credits present in the counter at any given time. Therefore, if the program card setting for LP selections is a three credit level, then as soon as at least three credits have been accumulated in the main credit counter **132** the output of gate **226** will be delivered to the LP enabling relay by energizing transistor **204.** In operation the output of the gates **226–229** are 0 when one or two credits are accumulated in the credit accumulator **132.** Upon receiving the third credit the output of gate **226** goes positive. Receiving four credits the output of gate **226** remains positive. When a fifth credit is received the output of gate **226** and the output of gate **227** are positive and when six credits are received the outputs of gates **226, 227** and **228** are positive. Upon receiving seven to 31 credits the output of all of the gates is at a logic 1 or a positive condition. The single selection enabling circuit

is turned on as soon as one credit or more is in the main credit counter. The long play or LP and the top tune (TT) selection enabling signals can be programmed on the program card **161** to enable the circuit at a level to form at least two to four credits or five to seven credits respectively, that is, the LP selection will require approximately three credits while a top tune selection will take six or seven credits in most cases. In each case the type of selection will not be allowed until the minimum number of credits for the program desired is set into the main credit accumulator circuit **132.**

Referring now to FIG. **3** there is seen a detailed schematic diagram of a voltage regulated power supply designated generally by reference numeral **300.** The power supply **300** includes a functional circuit regulator (Motorola 6030) **301** having one output thereof connected to the base electrode of a transistor **302** which, in turn, is connected in series between input and output terminals **303** and **304.** Short circuit protection is provided by means of a second transistor **306** which has the emitter thereof connected to a resistor **307** and the collector thereof connected to an output of the functional circuit regulator **301** and to a capacitor **308.** The output of transistor **302** is filtered by means of a plurality of capacitors **309, 310** and **311** whereupon the highly filtered and regulated voltage is applied to output terminals **313** and **314.** A pair of potentiometers **316** and **317** are provided to adjust the operational level of the voltage regulator circuit.

While a specific voltage regulator circuit is shown herein it will be understood that any voltage regulator circuit providing the necessary current and voltage tolerance requirements can be used.

Referring now to FIG. **4** there is seen an alternate input circuit arrangement which can be connected to each of the coin operated switches shown in FIG. **2A.** In this instance the five cent switch **30*a*** is shown, it being understood that all other switch arrangements are typical. Here a plurality of shift register stages **800, 801, 802** and **803** have one input thereof connected to the clock circuit and a second input, of the shift register **800,** connected to the switch **30a.** This circuit arrangement will prevent extraneous pulses due to switch contact bounce or static electricity from entering the credit accumulator which would produce unpaid for credit pulses. For example, FIG. **5** illustrates switch contact bounce at the beginning and end of each switch closure, the rapid making and breaking being represented by the spikes **806.** FIG. **6** shows a plurality of spikes **807** which are sometimes produced as the result of static electricity being introduced into the system. To prevent this type of switch contact bounce or static electricity from producing unwanted credit pulses the shift registers **800–803** are used to provide a certain time delay in the system so that only after sensing this time delay will an output pulse be developed. For example, FIG. **7** shows the initial part of a switch pulse designated generally by reference numeral **808.** The spikes **806,** due to switch contact bounce, have a duration of approximately one to 5 milliseconds and the time duration of the shift registers **800–803** is set to be approximately 20 milliseconds, 5 milliseconds each. This will produce an output through a NOR gate **809,** FIG. **4,** which may be inverted so as to produce a zero or ground signal at the output line **810.** The time delay between the closure of switch **30*a*** and the actual output pulse on line **810** is represented by the line **811** in FIG. **7.**

The operation of the circuit may be best understood by dividing the pulsing circuit into four distinct areas. First, there are the input matrixing gates **72, 73, 74, 75,** and **76** that are responsive to a single switch closure, of the switches **30, 31, 32, 33,** and **34,** to activate a multiplicity of the counter stages **77, 78, 79, 80,** and **81.** Secondly, there are the counter stages **77, 78, 79, 80,** and **81** that meter out the number of clock pulses called for by the closure of a specific switch. Thirdly, there is the clock pulse gating circuit which comprises the gates **82, 83** and **84.** The clock pulses come from the oscillator circuit **90** and are gated through the gate circuit **84** to have a number of pulses corresponding to the number of nickel values associated with the coin deposited, this being set forth clearly in applicants' specification. However, the manner in which this is achieved is set forth only generally. Therefore, the following details of operation are deemed helpful. Finally, there is the double-threshold circuit **66** which merely provides the time delay necessary to prevent erroneous switch operation.

The gate circuit **82** reads the state of the Q outputs of the five stage counter comprising flip-flops **77, 78, 79, 80,** and **81** and determines that all of the Q outputs are in a logic 1 state. This produces an inhibit signal to be applied to one of the inputs of gate **84** thereby not allowing any of the clock pulses to pass therethrough. The only way that the flip-flops of the counter can have their Q output changed from a logic 1 state to a logic 0 state is to have the input matrix gates activated by closure of the associated coin operated switches. When this occurs, the associated Q outputs will change to a logic 0 state. This action of one or more logic 0 states being sensed at the inputs of gate **82** will enable gate **84** thereby allowing clock pulses to pass therethrough. The clock pulses from gate **84** are delivered to one of the inputs of NOR gate **139** which, in turn, is connected back to the first toggle input of flip-flop **77.** The double threshold circuit **66,** however, inhabits the gates **84** while the coin switch is closed and holds the inhibit condition for approximately 50 to 60 milliseconds after the switch opens. This eliminates the possibility of contact bounce from producing extraneous signals. However, after this time interval the flip-flop circuit **71** will hold the inhibit condition on gate **84** until a proper phasing of the clock occurs, i.e., a logic 1 state changing to a logic 0 state. This condition allows the AND gate **84** to begin passing clock pulses which count the flip-flop circuits **77, 78, 79, 80,** and **81** back to their initial condition, namely all Q outputs being a logic 1. This then, automatically shuts off the passage of further clock pulses.

The following is a truth table of the counter flip-flop states and the input matrixing gates which are activated when specic coin switches are closed. The normal state of each coin switch and each input matrix gate output is a logic 1 and the active state of the counter flip-flops is a logic 0.

TABLE 1

	Input matrix gate output					Counter stage Q outputs				
Coin switch closed	72	74	73	76	75	77	79	78	81	80
SW. 30 5¢	0	0	0	0	0	0	0	0	0	0
SW. 31 10¢	0	0	0	0	0	1	0	0	0	0
SW. 32 25¢	1	0	0	0	0	0	0	1	0	0
SW. 33 50¢	0	0	1	0	0	1	0	1	1	0
SW. 34 1.00¢	1	1	0	0	1	1	1	0	0	1

What has been described is a circuit arrangement whereby the accumulation of coins is accomplished and provides accumulation of credit pulses by a simple counter circuit which enables a bonus pulse circuit for producing a bonus pulse on a predetermined count of the coin input counter. It will be understood that the bonus pulse can be produced on a count other than five, as for example three, seven or nine, as well as any even number selected. Accordingly, variations and modifications of this invention will be effected without departing from the spirit and scope of the novel concepts disclosed and claimed herein. Although the invention has been described with reference to coins, it will be appreciated that bills, credit units of non-legal tender such as metal or plastic chips or "wins" or paper, or punched or magnetically coded cards or the like ad infinitum could be used. All of the foregoing expedients are intended to be covered by the term "credit units" in the following claims.

The invention is claimed as follows:

1. A credit unit receiving and credit accumulating circuit, comprising: a credit unit input encoder system for receiving a plurality of credit units of different denominations for producing a series of output pulses in response to the value of such credit units, said output pulses corresponding in number to be proportional to the value of each different credit unit; a basic price selection decoder circuit for receiving said series of output pulses from said credit unit input encoder circuit to decode the pulses produced therein to units of the basic selection price; a credit accumulating circuit coupled to said basic price selection decoder circuit and including a circuit for registering credits and for cancelling such credits as they are used during a selection process; a bonus level control circuit responsive to the number of output pulses of said credit unit input encoder, said bonus level control circuit generating a bonus pulse or pulses to be delivered to said credit accumulating circuit as the accumulative number of output pulses from said credit unit input encoder reach successive predetermined numbers, and wherein said credit unit input encoder circuit is operative immediately to repeat its operation of producing output pulses corresponding to the value of credit units inserted therein.

2. The credit unit receiving and credit accumulator circuit according to claim **1** wherein said credit unit input encoder circuit includes a multi-stage counter having a logic encoding network input, and wherein a given credit unit input will result in at least one clock pulse output delivered to said basic price selection divisor circuit, and wherein additional pulse outputs from said credit unit input encoder circuit will correspond to a value which is a multiple of said given credit unit.

3. The credit unit receiving and credit accumulating circuit of claim **1** wherein said basic price selection decoder circuit is a preselected divisor to set the basic price of a selection, and wherein said divisor has a manually operated switch circuit for adjusting the number of pulses from said credit unit input encoder required to produce a single output from said basic price selection circuit.

4. The credit unit receiving and credit accumulating circuit according to claim **3** wherein said switch circuit includes a multi-position switch for adjusting the basic price of a selection to correspond to a given number of pulses from said credit unit input encoder circuit.

5. The credit unit receiving and credit accumulating circuit according to claim **1** wherein said credit accumulating circuit is a multi-stage up-down counter.

6. The credit unit receiving and credit accumulating circuit according to claim **1** wherein said bonus level control circuit is a counter and decoder which has a separate output for each of the plurality of levels corresponding to preprogrammed bonus levels, each of said outputs being arranged for connection to said credit accumulator circuit for inserting bonus credit pulses therein, and further including a counter circuit for inserting bonus selections and for cancelling credits after selections have been made.

7. The credit unit receiving and credit accumulating circuit according to claim **1** further including time delay means connected between credit unit switches and said credit unit input encoding circuit to sense the output pulses produced in response to the insertion of credit units for a predetermined time interval thereby eliminating extraneous noise signals being applied to said credit unit input encoder circuit which would otherwise produce false credit pulses.

8. The credit unit receiving and credit accumulating circuit according to claim **7** wherein said time delay means includes a plurality of storage element circuits interconnected between their output and input terminals, each circuit having a predetermined time controlled by a clock interval between an input pulse and the output pulse produced thereby, said circuits producing said time delay.

9. A credit unit receiving and credit accumulating circuit, comprising: a credit unit input encoder system for producing a series of output pulses in response to the value of credit units received, said output pulses corresponding in number to be proportional to the value of each different credit unit; a basic price selection decoder circuit for receiving said series of output pulses from said credit unit input encoder circuit to decode the pulses produced therein to units of the basic selection price; a credit accumulating circuit coupled to said basic price selection decoder circuit and including an up-down counter for registering credits and for cancelling such credits as they are used during a selection process; a bonus level control circuit responsive to said series of output pulses of said credit unit input encoder, said bonus control circuit generating a bonus pulse or pulses to be delivered to said credit accumulating circuit as the accumulated number of output pulses from said credit unit input encoder reaches successive predetermined numbers, and wherein said credit unit input encoder circuit is operative immediately to repeat its operation of producing output pulses corresponding to the value of credit units inserted therein; a bonus cancel and input counter circuit responsive to said bonus level counter circuit for inserting a bonus and for cancelling credits from said credit accumulator when purchase selections are made; and a selection cancel and input counter gate circuit connected to said bonus cancel circuit for providing a predetermined set condition of certain purchase selections so that the number of credits cancelled for a given purchase selection is automatically obtained.

10. The credit unit receiving and credit accumulator circuit according to claim **9**, wherein said credit unit input encoder circuit includes a multi-stage counter having a logic encoder circuit input, and wherein a nickel input will result in a clock pulse output signal

which is delivered to said basic price selection divisor circuit, and wherein each additional pulse output from said credit unit input counter will correspond to a value of 5 cents thus providing two pulses for a dime and five pulses for a quarter, 10 pulses for 50 cents and 20 pulses for a dollar

11. The credit unit receiving and credit accumulating circuit of claim **9** wherein said basic price selection circuit is a preselected divisor to set the basic price of a selection, and wherein said divisor has a programmable device for adjusting the number of pulses from said credit input encoder required to produce a basic output from said basic price selection circuit.

12. The credit unit receiving and credit accumulating circuit according to claim **11** wherein said switch means includes a multi-position switch for adjusting the basic price of a selection from between one to a plurality of pulses from said credit unit input encoder circuit.

13. The credit unit receiving and credit accumulating circuit according to claim **9** wherein said main credit accumulating circuit is a multi-stage up-down counter.

14. The credit unit receiving and credit accumulating circuit according to claim **9** wherein said bonus level control circuit is a counter and decoder which has a separate output for each of the plurality of levels corresponding to preprogrammed bonus levels, each of said outputs being arranged for connection to said credit accumulator for inserting bonus credits therein, and further including a multi-stage counter circuit for inserting bonus credits and for cancelling credits after selections have been made.

15. The credit unit receiving and credit accumulating circuit according to claim **9** further including time delay means connected between said credit unit switches and said credit unit input encoding circuit to sense the output signal produced in response to the insertion of credit units for a predetermined time interval thereby eliminating extraneous signals being applied to said credit unit input encoder circuit which would otherwise produce false credit pulses.

16. The credit unit receiving and credit accumulating circuit according to claim **15** wherein said time delay means includes a plurality of storage element circuits interconnected between their output and input terminals, each storage element circuit having a predetermined time controlled by a clock interval between an input pulse and the output pulse produced thereby, said storage element circuits producing said time delay.

17. The receiving and accumulating circuit according to claim **9** wherein the circuit for registering and cancelling credits comprises an up-down counter.

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UNITED STATES PATENT OFFICE

CERTIFICATE OF CORRECTION

Patent No. 3,815,720 Dated June 11, 1974

Inventor(s) William V. Machanian and Robert W. Wheelwright

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Col. 16, line 59, cancel "and input counter"

Col. 16, line 60, after "cancel" insert --and input counter--

Signed and sealed this 5th day of November 1974.

(SEAL)
Attest:

McCOY M. GIBSON JR.
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents

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