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(56) Documents Cited
EP 0506287 A1 EP 0456318 A2 JP 040152535 A
US 5920783 A US 5663586 A US 5654212 A
US 5274261 A

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(54) Abstract Title
Multi-layer structure for MOSFET Spacers

(57) A multi-layer spacer is formed adjacent a gate 301 of a FET structure. The multi-layer spacer includes a layer of low-k material 306 which reduces parasitic capacitance, and a layer of material which enables etch selectivity relative 307 to the substrate 101 and isolation oxides 301. The process helps avoid over-etching of active and isolation regions. The layers are preferably porous or carbon doped silicon dioxide 306 and silicon nitride 307. The transistor may be a lightly doped drain (LDD) structure.

FIG. 3

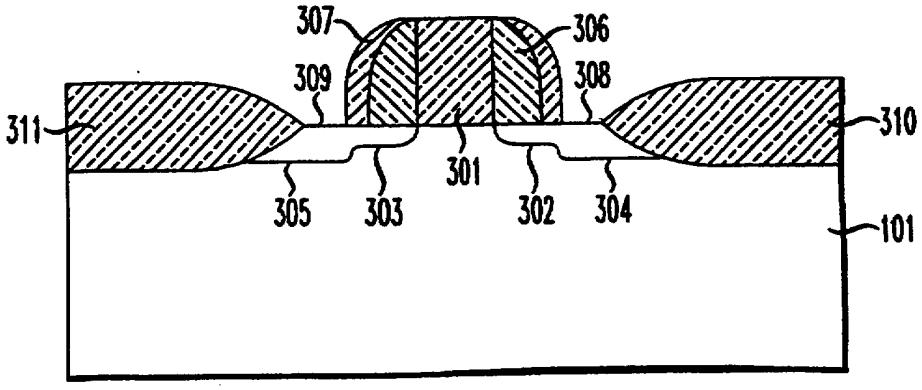

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FIG. 1

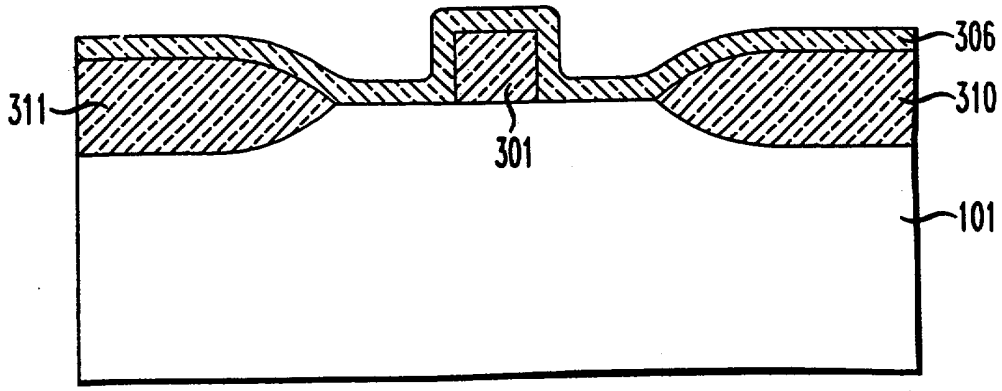


FIG. 2

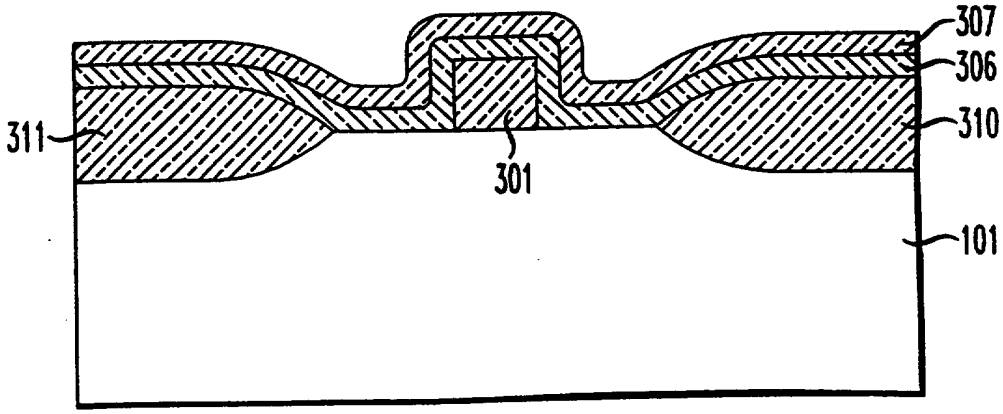
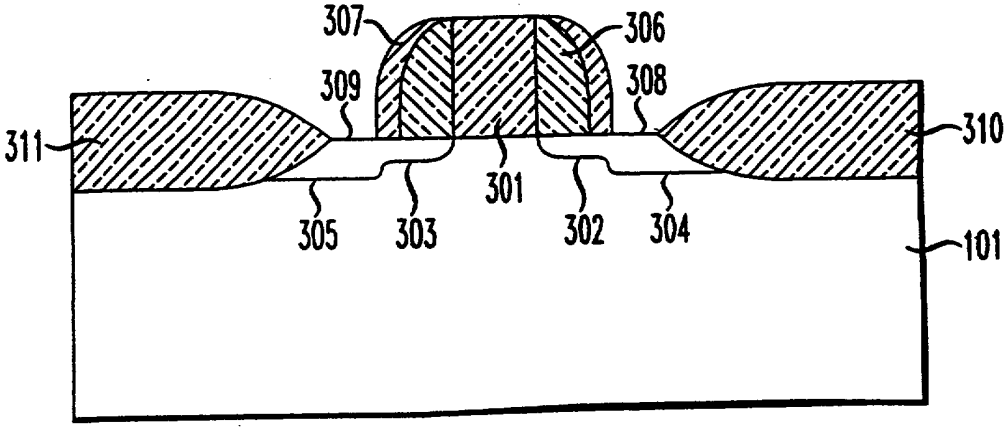


FIG. 3



Multi-Layer Structure For MOSFET Spacers

Field of the Invention

The present invention relates to a spacer for a metal-oxide-semiconductor field effect transistor (MOS FET).

Background of the Invention

Device scaling in integrated circuits often requires thinner gate oxides and more highly-doped channels. Thinner gate oxides and higher-doped channels result in an increase in the horizontal and vertical components of the electric field near the drain (referred to as the drain field). Carriers accelerated by the electric field can become "hot" and overcome the oxide barrier resulting in injection into the gate oxide. Hot carriers injected into the gate oxide may degrade device performance. Accordingly, it is desirable to reduce the incidence of hot carriers.

One technique used to reduce the incidence of hot carriers is to reduce the drain field. Lightly doped drain (LDD) structures are used to reduce the drain field and abate many of the problems associated with hot carriers. In an LDD structure, the source and drain are formed typically through two implantation steps. A first implant forms the lightly doped region. A spacer is then formed on either side of the gate and serves as a mask during formation of the more heavily doped regions of the source and drain.

While spacers are beneficial to the formation of LDD structures, there are certain drawbacks associated with them and their fabrication. To this end, in many instances a relatively thick field oxide region is used to electrically isolate active device areas. The field oxide is normally formed by the local oxidation of silicon (LOCOS). The LOCOS process consists essentially of depositing or thermally growing a thin pad

oxide of silicon dioxide (SiO_2) on the substrate surface. Thereafter a layer of silicon nitride (SiN) is deposited over the pad oxide. The SiN serves as a barrier to thermal oxidation. This silicon nitride layer is normally patterned leaving portions of the SiN over the silicon substrate where active devices are desired. The substrate is then annealed to form the field oxide in the exposed areas. During this process, a portion of the field oxide naturally forms under the perimeter of the nitride layer by lateral oxidation of the silicon substrate and is commonly referred in the industry as a "birds beak" because of its shape.

During the fabrication of the spacer, it is often necessary to account for variations in the spacer oxide layer thickness with an over-etch. Through the over-etch sequence, the source and drain regions at the silicon surface are subjected to over-etching to ensure a good ohmic contact to the source and drain. As a result of the over-etch sequence excessive etching of the field oxide may occur. This excess etching is known as birds beak "pullback" and may result in gate dielectric thinning and a reduction in isolation achieved by the field oxide. Thus, over-etching of the source and drain regions may result in leakage current at the source/drain junctions. The leakage at the source/drain junctions is typically localized in the junction directly beneath the spacer edge in the LDD structure. This leakage problem is generally attributed to silicon loss and etch damage in the substrate arising from the spacer over-etch.

In order to avoid the drawbacks associated with over-etch in conventional silicon dioxide spacer structures, alternative materials have been used as the spacer material in lieu of silicon dioxide. One such material is silicon nitride. Because different etch chemistries may be used, etch selectivity between the field oxide (silicon dioxide) and the silicon nitride can be achieved and problems associated with over-etch may be reduced. Unfortunately, the dielectric constant of silicon nitride is on the order of two times that of silicon dioxide. The higher dielectric constant of the silicon nitride increases parasitic capacitance between the gate oxide and the source/drain regions. This deleterious parasitic capacitance adversely impacts device response and speed. Therefore, while problems associated with over-etching may be reduced by the use of a silicon nitride spacer, device performance may be compromised.

Accordingly, what is needed is a lightly doped drain structure which overcomes the adverse effects of over-etch while simultaneously avoiding the adverse impact of parasitic capacitance associated with prior LDD structures.

Summary of the Invention

The present invention relates to a multi-layer spacer for a lightly doped drain field effect transistor structure (LDD-FET). The spacer includes a first layer adjacent a gate structure, and a second layer disposed over the first layer. Preferably, the first layer is a material having a relatively low dielectric constant, while the second layer is chosen to exhibit etch selectivity relative to the materials used for the active device and device isolation regions. This selectivity enables formation of the LDD spacer without substantial over-etch. Accordingly, the present invention reduces parasitic capacitance effects by virtue of the low-k dielectric while etch selectivity enables the formation of the spacer without the adverse impact of over-etch.

Brief Description of the Drawing

The invention is best understood from the following detailed description when read with the accompanying drawing figures. It is emphasized that the various features are not necessarily drawn to scale. In fact, the dimensions of the various features in the drawings may be arbitrarily increased or reduced for clarity of discussion.

Figure 1 shows the gate stack structure in an exemplary embodiment of the present invention with the layer of low-k dielectric material disposed thereover.

Figure 2 shows the gate stack structure of an exemplary embodiment of the present invention having a low-k layer and a subsequent layer disposed thereover.

Figure 3 is an exemplary embodiment of the present invention showing the resultant spacer structure with a first layer of low-k dielectric material and an outer layer of dielectric material.

Detailed Description of the Invention

Briefly, the present invention is drawn to a multi-layer spacer and its method of fabrication. Fig. 3 is a cross sectional view of an exemplary embodiment of the invention showing the gate 301 of a field effect transistor (FET) having a lightly doped drain region 302 and a lightly doped source region 303. The drain 304 and source 305 are more heavily doped. In the illustrative embodiment, the FET is NMOS with regions 302, 303 doped n^- and regions 304 and 305 doped n^+. The multi-layer spacer of the present invention has a first layer 306 and a second layer 307. In the exemplary embodiment, the first layer 306 is a low-k dielectric material. The material used to form second layer 307 is chosen to enable the fabrication of the spacer through etch selectivity in a manner which does not result in over-etching of active regions (308, 309) of the device nor of the field oxide isolation regions (310, 311). Accordingly, by virtue of the exemplary spacer structure shown in Fig. 3, parasitic capacitance between the gate 301 and the source 305 and drain 304 is reduced, while the problems of over-etch associated with single layer silicon dioxide spacers are overcome.

Turning to Fig. 1, local oxidation of silicon (LOCOS) is used to form the exemplary field oxide isolation regions 310, 311. Alternatively, trench isolation can be employed and formed by known techniques. The gate 301 is disposed over the substrate 101. Illustratively, the gate 301 is a bilayer of polysilicon with an oxide layer acting as the gate dielectric. The gate may also include a high dielectric constant (high-k) material. One example of a gate structure incorporating a high-k dielectric is disclosed in EP-A-0851473 the disclosure of which is specifically incorporated herein by reference.

The reduction in parasitic capacitance by virtue of the present invention affords particular benefits in MOS structures which use a high-k gate dielectric layer. When the high-k gate materials are used for the gate dielectric, the dimensional thickness of the gate dielectric is generally greater. This thicker high-k gate dielectric layer may result in an increase in the parasitic interaction between the gate and the source/drain. Accordingly, the low-k spacer layer of the present invention, which reduces the parasitic capacitance, is of particular benefit in high-k dielectric gate structures.

The first layer 306 is illustratively a low-k material having a dielectric constant approximately in the range of 2.1 to 2.6. In an exemplary embodiment shown in Fig. 1, the low-k dielectric 306 is silicon dioxide doped with carbon at a level of approximately 10% (carbon doped silicon dioxide is an example of porous silicon dioxide). However, other materials maybe used as the low-k layer 306. In the exemplary embodiment, the low-k layer 306 is fabricated by a standard spin-on technique, and has a thickness in the range of approximately 5-50 nm.

After the first layer 306 is deposited, the second layer 307 is deposited as shown in Figure 2. The material chosen for the second layer 307 is one which enables the selective etching to form the spacer layer, while avoiding the problems experienced in the prior art with over-etching. In an illustrative embodiment, the material chosen for the second layer 307 is silicon nitride, although other materials that would enable the desired etch selectivity may be used. The silicon nitride layer 307 may be deposited by standard technique, for example by plasma enhanced chemical vapor deposition (PECVD) or low temperature (<750°C) SiH_4 based low pressure chemical vapor deposition (LPCVD). In this embodiment, the layer of nitride 307 has a thickness on the order of approximately 20-80 nm. After the nitride layer 307 is deposited, an etching sequence is effected to form the spacer.

In an exemplary embodiment, the etching to selectively remove the layer 307 is done by reactive ion etching (RIE), which is anisotropic. In this first etch step, the first layer 306 and the second layer 307 act as mask for the field oxide regions (310, 311), as well for as the regions of the source and drain shown at 308, 309, respectively. The etch chemistry chosen for the first etch step should be one that will etch the layer 307 without appreciably etching the field oxide (310, 311) or regions 308, 309 of the source and drain. In the exemplary embodiment in which layer 307 is silicon nitride, C_2F_6 is used to carry out the nitride etch, and a CH_3F end point detection technique is used to determine the end of the etch. In this step, the nitride layer 307 will be etched but the underlying layers 306, 310 and 311 will not be etched appreciably due to the etch selectivity of the chosen chemistry. After the etching of the layer 307 is complete, the second etch step used to form the spacer is carried out. The chosen etch chemistry in this step will etch the first layer 306 much more rapidly than the field oxide (310, 311), which is normally a high temperature grown oxide. In the exemplary embodiment in which layer 306 is porous silicon dioxide, a RIE step is done with CH_4 used to carry out the selective etch.

By virtue of the present invention, certain advantages are realized. The chosen materials and etch chemistries result in etch selectivity which reduces over-etching of the isolation and active regions. In the illustrative embodiment, the multi-layer spacer is comprised generally of a relatively thick nitride layer disposed over a relatively thin low-k layer. Selective etching enables the removal of the nitride layer in selective areas. Thereafter, the low-k layer is removed by conventional techniques with the required over-etch to assure its proper removal from the active regions of the device for example. Over-etch tolerances are usually on the order of 10%-20% to assure removal of unwanted materials. In the invention of the present disclosure where the over-etch is carried out on a relatively thin layer of low-k material, a 10%-20% over-etch is acceptable. This is in contrast to conventional techniques in which a single layer having a thickness of greater than 100 nm is over-etched with a tolerance of 10%-20%. As outlined previously, such a degree of over-etch can have degrading effects on the device.

The invention having been described in detail above, it is clear that variations and modifications of the present inventions will be readily apparent to one having ordinary skill in the semiconductor art. To this end, the present invention discloses a structure and its method of manufacture for use in a MOSFET device which is preferably an LDD device using a spacer layer. The spacer layer has the benefits of reducing parasitic capacitance between the gate stack and the source/drain regions associated with certain dielectric materials by having a multi-layer spacer with at least one layer of low-k dielectric material incorporated into the spacer. At least the outer layer of the spacer is chosen for its etch selectivity, enabling the formation of the spacer, while avoiding the problems associated with over-etching as discussed above.

What is Claimed:

1. An integrated circuit, comprising:

a substrate;

a gate disposed over said substrate; and

a multi-layer spacer including a low-k layer.

2. An integrated circuit as recited in claim 1, wherein said low-k layer is porous silicon dioxide.

3. An integrated circuit as recited in claim 2, wherein said porous silicon dioxide is carbon doped.

4. An integrated circuit as recited in claim 1, wherein multi-layer spacer includes a layer of silicon nitride.

5. An integrated circuit as recited in claim 2, wherein said porous silicon dioxide has a thickness in the range of 5-50 nm.

6. An integrated circuit as recited in claim 4, wherein said silicon nitride has a thickness in the range of 20-80 nm.

7. An integrated circuit as recited in claim 1, wherein said low-k dielectric has a dielectric constant in the range of approximately 2.1 to 2.6.

8. An integrated circuit, comprising:

a gate disposed over a substrate; and

a spacer disposed adjacent said gate, said spacer having at least two layers and one of said layers is a low-k layer.

9. An integrated circuit as recited in claim 8, wherein said low-k material is porous silicon dioxide.

10. An integrated circuit as recited in claim 8, wherein said porous silicon dioxide has a thickness on the order of 5-50 nm.

11. An integrated circuit as recited in claim 8, wherein one of said at least two layers is silicon dioxide.

12. An integrated circuit as recited in claim 8, wherein said low-k layer has a thickness in the range of approximately 2.1 to 2.6.

13. An integrated circuit, comprising:

a substrate;

a gate disposed over said substrate; and

a multi-layer spacer including a layer which exhibits etch selectivity relative to said substrate.

14. An integrated circuit as recited in claim 13, wherein an isolation material is disposed near said gate and said layer exhibits etch selectivity relative to said isolation material.

15. An integrated circuit as recited in claim 13, wherein said multi-layer spacer further includes a low-k dielectric layer.

16. An integrated circuit as recited in claim 14, wherein said isolation material is a field oxide.

17. An integrated circuit as recited in claim 14, wherein said isolation material is a trench oxide.

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Application No: GB 0025340.1
Claims searched: 1-12

Examiner: Darren Handley
Date of search: 29 August 2001

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.S): H1K (CAL)

Int Cl (Ed.7): H01L 21/28, 29/423, 29/49

Other: Online: WPI, EPODOC, JAPIO

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	EP 0506287 A1	(AMERICAN) - see column 2, line 57- column 4, line 29	1, 2, 4, 5, 7-17
X	EP 0456318 A2	(N V PHILLIPS) - see figure 7 and column 3, line 35- column 4, line 26	1, 2, 4-17
X	US 5920783 A	(TSENG) - see column 3, lines 39-65.	1, 4, 8, 13-17
X	US 5663586 A	(LIN) - see column 3, lines 42-48 and column 3, line 63- column 4, line 7.	1, 8, 11, 13-17
X	US 5654212 A	(JANG) - see column 6, line 48- column 7, line 33	1, 4, 8, 13-17
X	US 5274261 A	(CHEN) - see column 4, lines 6-32.	1, 8, 11, 13-17
X	JP 4152535 A	(SANYO) - see figure 2a-d and PAJ abstract.	1, 2, 7, 8, 9, 11-17

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.