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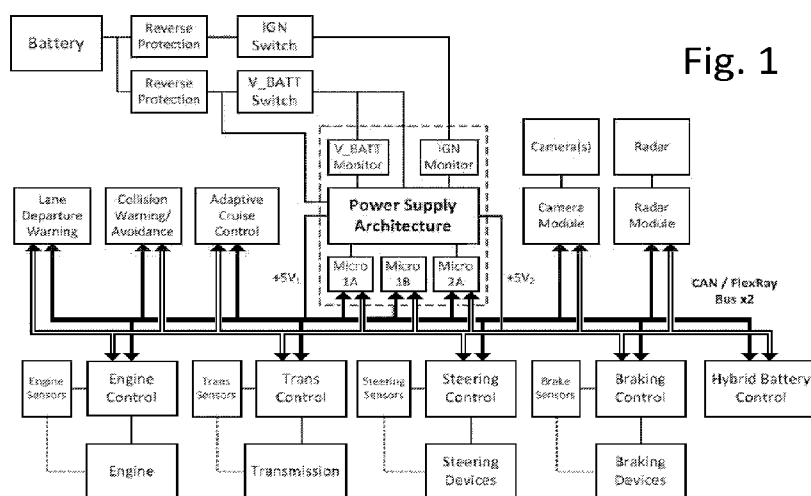


Fig. 1

- (57) **Abstract:** A power supply architecture provides for the efficient distribution and failsafe monitoring of power in a microcontroller system. The power supply architecture incorporates various components with high integrity and diverse monitoring schemes that allow the associated control processors to operate with high safety standards. The various embodiments provide an integrated method or apparatus for an electronic module safety architecture which includes diversity, time and space independence for power supplies for the various microprocessors and control communication buses.

OPTIMIZED POWER SUPPLY ARCHITECTURE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of United States Provisional Application No. 61/830,934; filed June 4, 2013; the disclosure of which is incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

[0002] This invention relates in general to a power supply architecture that may be used in a control system comprising one or more microprocessors and, in particular, to a power supply architecture that provides for safety monitoring of the various supply voltages associated with the power supply and/or peripheral components.

[0003] In automotive applications, the particular safety standards to which a component or system must adhere are determined by a risk classification scheme known as Automotive Safety Integrity Level (ASIL) and defined by the ISO 26262 Functional Safety for Road Vehicles standard. This classification helps define the safety requirements necessary to be in line with the ISO 26262 standard. The ASIL is established by performing a risk analysis of a potential hazard by looking at the Severity, Exposure and Controllability of the vehicle operating scenario. The safety goal for that hazard in turn carries the ASIL requirements. There are four ASILs identified by the standard: ASIL A, ASIL B, ASIL C, and ASIL D. ASIL D dictates the highest integrity requirements on the product and ASIL A the lowest.

[0004] ASIL D refers to the highest classification of initial hazard (injury risk) defined within ISO 26262 and to that standard's most stringent level of safety measures to apply for avoiding an unreasonable residual risk. ASIL D is noteworthy, not only because of the elevated risk it represents and the exceptional rigor required in development, but because automotive electrical, electronic, and software suppliers make claims that their products have been certified or otherwise accredited to ASIL D.

SUMMARY OF THE INVENTION

[0005] This invention relates to a power supply architecture which incorporates various components and high integrity and diverse monitoring schemes that potentially enable one or more associated control processors to operate under ASIL D standards.

[0006] According to one aspect of the invention, a circuit for providing redundant monitoring of an operating voltage V present at a predetermined point in an electrical system comprises a voltage divider, a first monitor, and a second monitor. The voltage divider is connected between the predetermined point and a ground. The voltage divider defines a first intermediate node at a potential V_1 , that is less than the operating voltage V . The voltage divider further defines a second intermediate node at a potential V_2 less than the potential V_1 . The first monitor is coupled to the first node and is operable to detect a voltage fault or discrepancy in the level of the operating voltage V . The second monitor is coupled to the second node and is operable to detect a voltage fault or discrepancy in the level of the operating voltage V . A protection circuit may be connected between the first intermediate node and the ground for limiting the voltages at the first and second node within a predetermined safe operating range of the first and second monitors. In addition, a third monitor may be coupled to one of the first and second nodes and operable to detect a voltage fault or discrepancy in the level of the operating voltage V . In certain embodiments, each of the monitors is coupled to the respective first or second nodes via a low pass filter.

[0007] According to another aspect of the invention, a power supply architecture comprises a first processor, a second processor, a first power supply, and a second power supply. The first power supply is configured to supply a first group of operating voltages to the first processor. At least a portion of the first group of operating voltages is also coupled to monitoring inputs of both the first and second processors. The second power supply is configured to supply a second group of operating voltages to the second processor. At least a portion of the second group of operating voltages is also coupled to

monitoring inputs of both the first and second processors. Each of the first and second processors operates to monitor and evaluate the statuses of the portion of the first group of operating voltages and also to determine whether any anomalies are present. Each of the first and second processors operates to monitor and evaluate the statuses of the portion of the second group of operating voltages and also to determine whether any anomalies are present. In one embodiment, the first processor discretely monitors and evaluates the statuses of the portion of the first group and the second processor discretely monitors and evaluates the statuses of the portion of the second group.

[0008] The power supply architecture, above, may also include a third processor and a third power supply. The third power supply is configured to supply a third group of operating voltages to the third processor,. At least a portion of the third group of operating voltages is also coupled to monitoring inputs of the third processor. The third processor operates to evaluate the statuses of the portion of the third group and to determine whether any anomalies are present. In another embodiment, the third processor generates multiple core voltages that are connected to the monitoring inputs of one of the first and second processors. One of the first and second processors may operate to evaluate the statuses of the multiple core voltages and to determine whether any anomalies are present. In yet another embodiment, an over/under voltage circuit may be coupled to receive the multiple core voltages from the third processor. The over/under circuit is operative to generate digital status signals which in turn are supplied to the monitoring inputs of one of the first and second processors. Additionally, one of the first and second processors is operative to evaluate the statuses of the portion of the digital status signals and to determine whether any anomalies are present. In another embodiment, the first and second processors may be located on a first circuit board, and the third processor may be located on a second, separate circuit board, and the digital status signal are transmitted therebetween.

[0009] According to still another aspect of the invention, a power supply architecture comprises a first processor, a first power supply, and a first control section. The first

processor is partitioned into two MPU applications to define a first control section and first monitoring section. The first power supply is configured to supply a first group of operating voltages to the first processor. At least a portion of the first group is coupled to monitoring inputs of the both the first control section and the first monitoring section. The first control section and the first monitoring section are operative to evaluate the statuses of the portion of the first group and to determine whether any anomalies are present. In one embodiment of this power supply architecture, a second processor may be partitioned into two MPU applications to define into a second control section and second monitoring section. A second power supply may be provided for supplying a second group of operating voltages to the second processor. At least a portion of the second group of operating voltages may also be connected to monitoring inputs of the second control section and the second monitoring section. The second control section and second monitoring section are operative to evaluate the statuses of the portion of the second group and to a determine whether any anomalies are present.

[0010] According to still yet another aspect of the invention, a power supply architecture comprises a processor, a power management controller (PMC), and first and second voltage regulators. The PMC is operable to supply a group of different operating voltages to the processor. The first voltage regulator connected to supply a voltage V1 to a first input of the PMC. The second voltage regulator is connected to supply a voltage V2 to a second input of the PMC and to a memory associated with the processor. The PMC is operable to generate a delayed enable signal to an enable input of the second voltage regulator such that the memory of the processor is activated with a delay relative to its core voltages.

[0011] According to yet another aspect of the invention, a power supply architecture comprises a processor; a power management controller (PMC), and a voltage regulator. The PMC is operable to supply a group of different operating voltages to the processor. The voltage regulator is connected to supply a voltage V1 signal to an input of the PMC. The processor is operative to monitor and evaluate the status of the voltage V1 signal to

determine whether an anomaly is present. In one embodiment, the regulator may be a first regulator and may include a second voltage regulator connected to supply a voltage V2 signal to a second input of the PMC. The processor is also operative to monitor and evaluate the status of the voltage V2 to determine whether an anomaly is present. In one embodiment, the V1 and V2 voltage signals may be discretely monitored by the processor. In another embodiment, the at least a portion of the group of operating voltages supplied to the processor may also be coupled to monitoring inputs of the processor. The processor may be operative to evaluate the at least a portion of the group of operating voltages to determine whether an anomaly is present. In yet another embodiment, the at least a portion of the group of operating voltages may be discretely monitored by the processor. In addition, a third voltage regulator for supplying an operating voltage V3 signal to a memory may be associated with the processor. Here, the processor may also monitor the status of the V3 voltage signal to determine whether an anomaly is present.

[0012] In yet another embodiment of the power supply architecture, above, the processor may be a first processor that generates an output reference source signal and the power supply architecture may include a second processor that is operative to monitor and evaluate the output reference source signal to determine whether an anomaly is present. Additionally, the output reference source signal of this embodiment may be discretely monitored by the second processor.

[0013] According to another aspect of the invention, a power supply architecture comprises a processor, a power management controller (PMC), and a voltage regulator. The PMC is operable to supply a group of different operating voltages to the processor. The voltage regulator is connected to supply an operating voltage to the PMC. The processor is operative to monitor and evaluate at least a portion of the group of operating voltages to determine whether an anomaly is present. In one embodiment, the at least a portion of the group of operating voltages may be discretely monitored by the processor. In another embodiment, the processor is a first processor that generates an output

reference source signal and a second processor is provided that is operative to monitor and evaluate the output reference source signal to determine whether an anomaly is present. Here, the output reference source signal may be discretely monitored by the second processor.

[0014] In yet another aspect of the invention, a power supply architecture for a vehicle comprises a processor, a first communication bus connected between the processor and a vehicle control system, and a first power supply for supplying a first operating voltage to the first communication bus. A second communication bus is connected between the processor and the vehicle control system. A second power supply, separate from the first power supply, is configured to supply a second operating voltage to the second communication bus.

[0015] Various aspects of this invention will become apparent to those skilled in the art from the following detailed description of the preferred embodiment, when read in light of the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] **Fig. 1** is a block diagram showing one example of an operating environment for a power supply architecture embodying the principles of the invention, wherein the invention is utilized as a power supply with multiple vehicle control system.

[0017] **Fig. 2** is a block diagram showing one example of the arrangement of components which comprise the power supply architecture of **Fig. 1**.

[0018] **Fig. 3** is a typical prior art circuit for providing redundant monitoring of an operating voltage in an electrical system.

[0019] **Fig. 4** is a simplified circuit for providing redundant monitoring of an operating voltage in an electrical system, and embodying the principles of the invention.

[0020] **Figs. 5a** and **5b** show circuits using the principles of **Fig. 4** for monitoring the switched battery and ignition voltages across three processors, 1A, 1B, and 2A, and representing one example of section A of **Fig. 2**.

[0021] **Fig. 6a** represents one example of section B of **Fig. 2**, wherein multiple supply voltages from two independent power supplies are cross-monitored through diverse analog and digital (discrete) methods.

[0022] **Fig. 6b** is similar to **Fig. 6a**, but showing additional details of the monitoring of a 1.2V core voltage, and wherein the 1.2V core voltage has opposite analog/digital routing than the rest of the outputs from the respective power supply.

[0023] **Fig. 7a** represents an alternate embodiment of **Fig. 6a** (Section B of **Fig. 2**), wherein the analog and digital routing is switched.

[0024] **Fig. 7b** represents an alternate embodiment of **Fig. 6b**, wherein the analog and digital routing is switched.

[0025] **Fig. 8a** and **8b** represent alternate embodiments of **Fig. 6a** (Section B of **Fig. 2**), wherein each microprocessor 1A and 2A is partitioned into two MPU applications, which enables each microprocessor to check itself (including its own 1.2V core voltage), without memory corruption.

[0026] **Fig. 9a** represents one example of section C of **Fig. 2**.

[0027] **Fig. 9b** represents an alternate embodiment of **Fig. 9a**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0028] This invention concerns various embodiments directed to the efficient distribution and failsafe monitoring of power in a microcontroller system. While the various embodiments are particularly suitable for use in vehicular applications (including both automotive and truck), it will be readily appreciated that the invention and its various embodiments can be used, either singly or collectively, in other control applications having similar operating requirements. In one application, the inventions are used in a Multiple ASIL Optimized Power Supply Architecture for an electronic control module used for supervisory input processing (radar, camera, etc.) and output commands (engine torque, transmission torque, steering angle or torque, brake commands or torque, suspension commands, etc.) for driver assistance systems. The various inventions

provide an integrated method or apparatus for an electronic module safety architecture which includes diversity, time and space independence for power supplies for the varied ASIL microprocessors and vehicle communication buses.

[0029] Referring now to the drawings, there is illustrated in **Fig. 1** a block diagram showing one example of an operating environment for a power supply architecture embodying the principles of the invention, wherein the invention is utilized as a power supply in a vehicle control system. Generally, referring to Fig. 1, the functional aspects of the Multiple ASIL Optimized Power Supply Architecture of the electronic module may be characterized as follows:

- a. includes two high integrity ASIL D compatible microprocessors (1A and 1B) for supervisory input processing and output commands for driver assistance systems.
- b. receives the input processing and output command information from two or more pairs of automotive communication buses (CAN, Flexray, etc.). These communication buses transfer high integrity information. Each external bus type has a complementary role if one of them is severed. As shown in Figs. 1 and 2, each communication bus receives power from a separate and independent power supply.
- c. includes one other high throughput processing microprocessor (microprocessor 2A) with external memory. The microprocessor 2A may have a quality management (non-ASIL) hardware requirement. Alternatively, the microprocessor 2A may have a higher level designation, such as ASIL B.
- d. microprocessors 1A and 2A may be used predominantly for control and microprocessor 1B may be used predominantly for checking microprocessor 1A and 2A.
- e. in one alternative, a minimal set of functions microprocessor 1B is used for control and for these functions microprocessor 1A is used for checking.

- f. providing independence between the 2 high integrity Automotive Safety Integrity Level (ASIL D) microprocessors (1A and 1B) and the high throughput processing quality management microprocessor (microprocessor 2A) with ASIL B monitoring for external microprocessor hardware.

[0030] The recently approved ISO 26262 safety standards have time and space independence to be achieved for power supplies and their monitoring for the microprocessors and varied vehicle communication buses - CAN, Flexray, etc.

[0031] **Fig. 2** is a block diagram showing one example of the arrangement of components which comprise the power supply architecture of Fig. 1, including Section A (switched battery and ignition voltage monitoring), Section B (independent power supplies and cross-monitoring between processors 1A and 1B) and Section C (power management controller and processor 2A).

[0032] **Fig. 3** shows a typical prior art circuit for monitoring the switched battery and ignition voltages across two processors, A and B, embodying the principles of the invention, and which represents Section A of Fig. 2. Switched battery voltage, which in one embodiment may be on the order of 26.5V in an automobile, can be divided down to an acceptable input level for a microprocessor. There may also be protection components in place to protect the processor in the case of over/under voltage transients. Typically, there exists a divider and a protection circuit for every processor that is monitoring the switched battery input.

[0033] **Fig. 4** represents an embodiment of a circuit for monitoring battery voltages across two or more microprocessors having improved economy and reliability. In case of using two monitoring processors, instead of having two separate voltage dividers, the processors share three dividing resistors. This configuration still divides the voltage to a safe level for the processors, but it also sets up a diverse configuration where the battery voltage translates to different operational voltage ranges for each processor. For example, processor A may read a full battery at 4.5+V, while processor B may read the full battery at 2.5V, invoking algorithmic diversity. Another benefit of this topology is

the ability to use one protection circuit, even while using two or more processors. Because the protection circuit is placed at the first intermediate node of the dividing resistors (near Processor A), it will protect any other processors from voltage transients whether they are at that node or below that node.

[0034] Fig. 5a is the switched battery monitoring topology used by the invention. Similar to Fig. 4, it uses one set of protection components. In addition to Fig. 4, there is a third processor, and two of the processors share an operational voltage range at the first intermediate node on the divider. The resistors leading to each processor isolate the processors from each other, and they can also be incorporated in low-pass filters to reduce noise.

[0035] Fig. 5b is an ignition voltage monitoring circuit, using the same topology as Fig. 5a. Certain embodiment of the invention described herein can make use of this cost effective circuit for both the battery and ignition voltages. To add further diversity to the system, the reference points of processor 1A and 1B may be switched between Fig. 5a and Fig. 5b. This allows each processor to have algorithmic diversity within itself, reading battery voltage on one operational range while reading ignition voltage on another. This results in improved failure mode detection.

[0036] Fig. 6a represents section B of Fig. 2, wherein multiple supply voltages from two independent power supplies are cross-monitored through diverse analog and discrete methods across two processors. For the sake of clarity, it should be noted that the physical power supply inputs to the processors, which provide operational voltages rather than monitored voltages, are not shown in Figs. 6a-9b. The illustrated lines represent the monitored reference voltages of these supply voltages, and no significant power is consumed through these illustrated reference lines. In Fig. 6a, a group of reference voltages for processor 1A are monitored through analog-to-digital (A/D) inputs on a second processor 1B. Simultaneously, the same voltages are sent to one or several overvoltage/undervoltage (OV/UV) monitor(s), which calculate discrete pass/fail outputs depending on the state of the power supplies. Processor 1A reads these outputs using

digital (I/O) pins. Processor 1B uses precisely the same method, monitoring its own supply through OV/UV monitor(s) and monitoring 1A's supply through its A/D inputs. This embodiment incorporates time and space diversity, where the independent power supplies are monitored by two processors, both using analog (A/D) and discrete (I/O) methods.

[0037] **Fig. 6b** is similar to Fig. 6a but shows additional details of the circuit. In Fig. 6b, a 1.2V core reference voltage is separated from the rest of the referenced voltage in order to show that it is monitored in an opposite fashion. The same time and space diversity exists for the 1.2V reference, but it is monitored as an analog signal by its own processor and by a digital(or discrete) signal for the other processor. In one embodiment, the processor monitors its own 1.2V core with a direct analog connection to respond quickly to a failure, thus minimizing or eliminating a delay that could come from the inter-processor bus. Another additional detail in Fig. 6b is the specified supply and pull-up voltages for the OV/UV monitors. This applies to all OV/UV blocks in Figures 6a,b; 7a,b; and 8a,b. The discrete monitors used by 1A uses voltages from power supply 2, and the discrete monitors used by 1B uses voltages from power supply 1. This allows the cross monitoring system to operate in a situation where one of the power supplies fails completely.

[0038] **Fig. 7a** is very similar to Fig. 6a, except that all assignments of analog and digital paths have been swapped between the supplies. Each processor now monitors its own reference voltages using analog means and the other processor's voltages through discrete means.

[0039] **Fig. 7b** is very similar to Fig. 7a, but includes an inverted method of monitoring the 1.2V core voltages. A similar embodiment was previously described in Fig. 6b. However, the embodiment of Fig. 6b may represent certain advantages over the embodiment of Fig. 7b.

[0040] **Fig. 8a** represents an alternate embodiment of the invention. Some processors have the ability to run memory partition units, where partitions of the memory are

separated, or otherwise segregated, in such a way that they cannot corrupt other partitions. This opens up the possibility of using one microprocessor to represent two microprocessors. Fig. 8a is a simplified memory partition unit application. Power supply voltages do not cross from one processor to the other. However, they are diversely monitored by two distinct partitions in each processor, which are represented by the shaded portions of the processor blocks (grey and white).

[0041] Fig. 8b represents an alternate embodiment of Fig. 8a, where the 1.2V core voltage is cross-monitored between processors, while the rest of the voltages are cross-monitored between partitions in their respected processor. In certain environments, Fig. 8a may be a preferred arrangement because the same level of diversity can be accomplished as Fig. 8b without transferring delayed monitor signals on an inter-processor bus.

[0042] Fig. 9a represents section C of Fig. 2 and includes the function and monitoring of microprocessor 2A. A power management controller (PMC) provides the necessary core and peripheral voltages for 2A. Two switching regulators provide power to the PMC. Regulator 1 turns on with a signal from V_BATT_SW, and the essential supplies are provided to 2A. Some peripherals, such as DDR memory may require that their power supplies be turned on after the processor's core power supplies. To accomplish this, a naturally delayed output from the PMC enables Regulator 2, which powers up a dedicated regulator for the high-current DDR memory. The power supply voltages for processor 2A are monitored only with a discrete method, and 2A does not include A/D converters. Because 2A is located on a separate printed circuit board (PCB) than 1A and 1B, discrete signals are preferred for their immunity to noise, which could affect analog signals. It is also preferred to limit the number of signals that must be passed from one PCB to the other. For this reason, voltages that are not generated in 2A are monitored by individual OV/UV monitors and read by 2A. Examples include core input voltages and memory DDR memory voltages. Processor 2A generates operational voltages for its

cores, as well as several peripheral voltages. These voltages are monitored by individual OV/UV processors and read by processor 1B, located on a separate PCB.

[0043] Fig. 9b is very similar to Fig. 9a, except that the OV/UV monitors no longer exist as individual modules for each supply voltage. Instead, they are grouped into collective monitors, which generate one or more discrete outputs based on the status of several input voltages. Collective as well as individual voltage monitors should be considered for the embodiment of section C. If packaging requirements allow for additional signals to be transferred between PCBs, processor 1B could discretely monitor all the supply voltages in section C, which is another embodiment to consider.

[0044] The principle and mode of operation of this invention have been explained and illustrated in its preferred embodiment. However, it must be understood that this invention may be practiced otherwise than as specifically explained and illustrated without departing from its spirit or scope.

What is claimed is:

1. A circuit for providing redundant monitoring of an operating voltage V present at a predetermined point in an electrical system, the circuit comprising:
 - a voltage divider connected between the predetermined point and a ground, the voltage divider defining a first intermediate node at a potential V_1 less than the operating voltage V and a second intermediate node at a potential V_2 less than the potential V_1 ;
 - a first monitor coupled to the first node and operable to detect a voltage fault or discrepancy in the level of the operating voltage V ; and
 - a second monitor coupled to the second node and operable to detect a voltage fault or discrepancy in the level of the operating voltage V .
2. The circuit according to claim 1 and further including a protection circuit connected between the first intermediate node and the ground for limiting the voltages at the first and second node within a predetermined safe operating range of the first and second monitors.
3. The circuit according to claims 1 and further including a third monitor coupled to one of the first and second nodes and operable to detect a voltage fault or discrepancy in the level of the operating voltage V .
4. The circuit according to claim 1 wherein each of the monitors is coupled to the respective first or second nodes via a low pass filter.

5. A power supply architecture comprising:
- a first processor;
 - a second processor;
 - a first power supply for supplying a first group of operating voltages to the first processor, at least a portion of the first group also coupled to monitoring inputs of both the first and second processors;
 - a second power supply for supplying a second group of operating voltages to the second processor, at least a portion of the second group also coupled to monitoring inputs of both the first and second processors;
 - each of the first and second processors operates to monitor and evaluate the statuses of the portion of the first group and to determine whether any anomalies are present; and
 - each of the first and second processors operates to monitor and evaluate the statuses of the portion of the second group and to a determine whether any anomalies are present.
6. The power supply architecture according to claim 5 wherein the first processor discretely monitors and evaluates the statuses of the portion of the first group and wherein the second processor discretely monitors and evaluates the statuses of the portion of the second group.
7. The power supply architecture according to claim 5 and further including:
- a third processor;
 - a third power supply for supplying a third group of operating voltages to the third processor, at least a portion of the third group also coupled to monitoring inputs of the third processor; and
 - the third processor operates to evaluate the statuses of the portion of the third group and to a determine whether any anomalies are present.

8 The power supply architecture according to claim 7 wherein the third processor generates multiple core voltages that are connected to the monitoring inputs of one of the first and second processors, and wherein the one of the first and second processors operates to evaluate the statuses of the multiple core voltages and to a determine whether any anomalies are present.

9. The power supply architecture according to claim 8 and further including an over/under voltage circuit coupled to receive the multiple core voltages from the third processor, and operative to generate digital status signals which in turn are supplied to the monitoring inputs of one of the first and second processors, and wherein the one of the first and second processors is operative to evaluate the statuses of the portion of the digital status signals and to a determine whether any anomalies are present.

10. The power supply architecture according to claim 9 wherein the first and second processors are located on a first circuit board, and the third processor is located on a second, separate circuit board, and the digital status signal are transmitted therebetween.

11. A power supply architecture comprising:
a first processor partitioned into two MPU applications to define a first control section and first monitoring section;
a first power supply for supplying a first group of operating voltages to the first processor, at least a portion of the first group coupled to monitoring inputs of the both the first control section and the first monitoring section; and
the first control section and the first monitoring section operative to evaluate the statuses of the portion of the first group and to determine whether any anomalies are present.

12. A power supply architecture according to claim 11 comprising:
a second processor partitioned into two MPU applications to define a second control section and second monitoring section;
a second power supply for supplying a second group of operating voltages to the second processor, at least a portion of the second group also connected to monitoring inputs of the second control section and the second monitoring section; and
the second control section and second monitoring section operative to evaluate the statuses of the portion of the second group and to determine whether any anomalies are present.

13. A power supply architecture comprising:
a processor;
a power management controller (PMC) operable to supply a group of different operating voltages to the processor;
a first voltage regulator connected to supply a voltage V1 to a first input of the PMC;
a second voltage regulator connected to supply a voltage V2 to a second input of the PMC and to a memory associated with the processor;
the PMC operable to generating a delayed enable signal to an enable input of the second voltage regulator such that the memory of the processor is activated with a delay relative to its core voltages.

14. A power supply architecture comprising:
a processor;
a power management controller (PMC) operable to supply a group of different operating voltages to the processor;
a voltage regulator connected to supply a voltage V1 signal to an input of the PMC; and
the processor is operative to monitor and evaluate the status of the voltage V1 signal to determine whether an anomaly is present.
15. The power supply architecture according to claim 14 wherein the regulator is a first regulator and including a second voltage regulator connected to supply a voltage V2 signal to a second input of the PMC, and wherein the processor is also operative to monitor and evaluate the status of the voltage V2 to determine whether an anomaly is present.
16. The power supply architecture according to claim 15 wherein the V1 and V2 voltage signals are discretely monitored by the processor.
17. The power supply architecture according to claim 14 wherein the at least a portion of the group of operating voltages supplied to the processor are also coupled to monitoring inputs of the processor, and wherein the processor is operative to evaluate the at least a portion of the group of operating voltages to determine whether an anomaly is present.
18. The power supply architecture according to claim 14 wherein the at least a portion of the group of operating voltages are discretely monitored by the processor.

19. The power supply architecture according to claim 15 and further including a third voltage regulator for supplying an operating voltage V3 signal to a memory associated with the processor, and wherein the processor monitors the status of the V3 voltage signal to determine whether an anomaly is present.

20. The power supply architecture according to claim 14 wherein the processor is a first processor that generates an output reference source signal and including a second processor, and wherein the second processor is operative to monitor and evaluate the output reference source signal to determine whether an anomaly is present.

21. The power supply architecture according to claim 19 wherein the output reference source signal is discretely monitored by the second processor.

22. A power supply architecture comprising:
a processor;
a power management controller (PMC) operable to supply a group of different operating voltages to the processor;
a voltage regulator connected to supply an operating voltage to the PMC; and
the processor is operative to monitor and evaluate at least a portion of the group of operating voltages to determine whether an anomaly is present.

23. The power supply architecture according to claim 22 wherein the at least a portion of the group of operating voltages is discretely monitored by the processor.

24. The power supply architecture according to claim 22 wherein the processor is a first processor that generates an output reference source signal and including a second processor, and wherein the second processor is operative to monitor and evaluate the output reference source signal to determine whether an anomaly is present.

25. The power supply architecture according to claim 24 wherein the output reference source signal is discretely monitored by the second processor.

26. A power supply architecture for a vehicle comprising:
a processor;
a first communication bus connected between the processor and a vehicle control system;
a first power supply for supplying a first operating voltage to the first communication bus;
a second communication bus connected between the processor and the vehicle control system; and
a second power supply separate from the first power supply for supplying a second operating voltage to the second communication bus.

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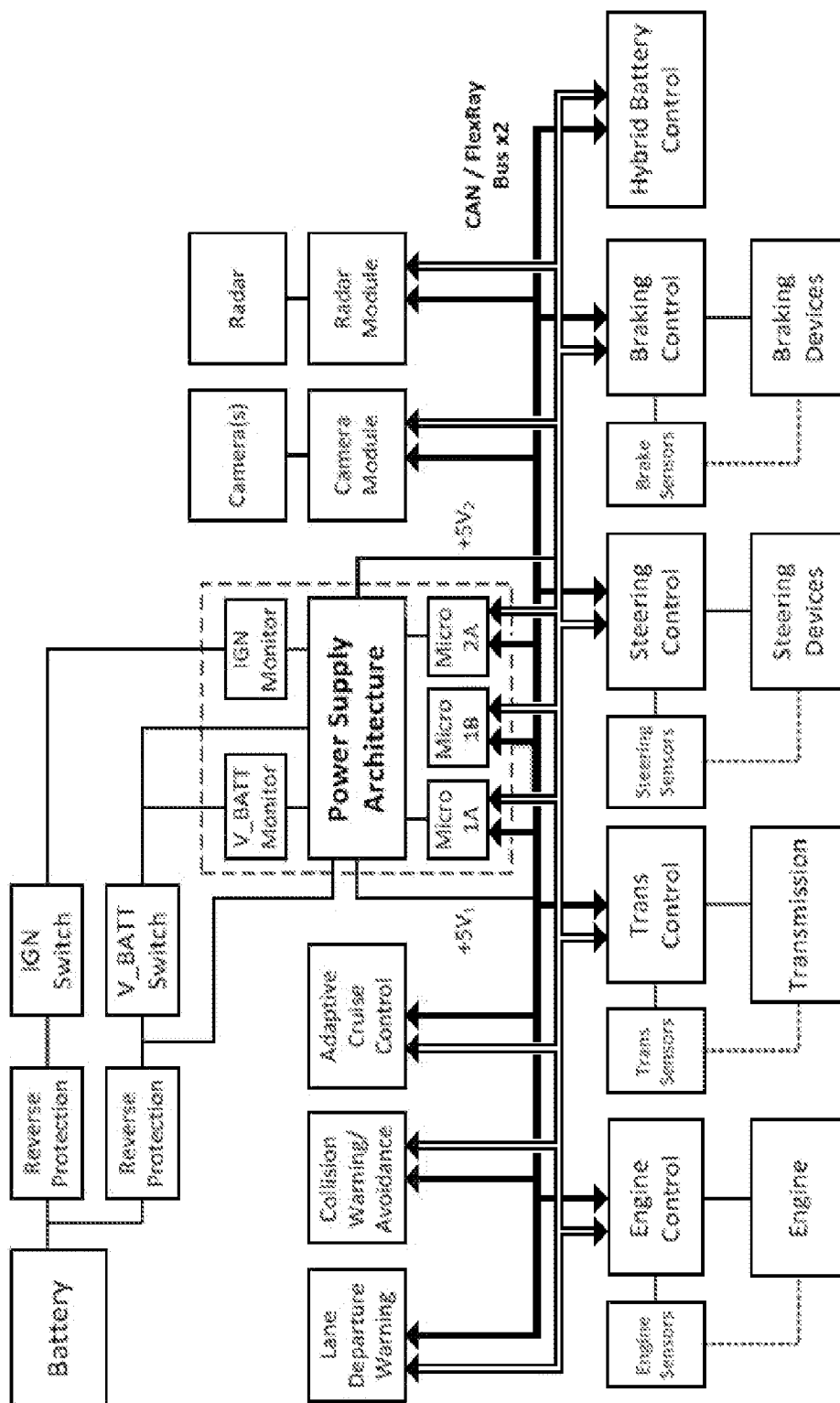


Fig. 1

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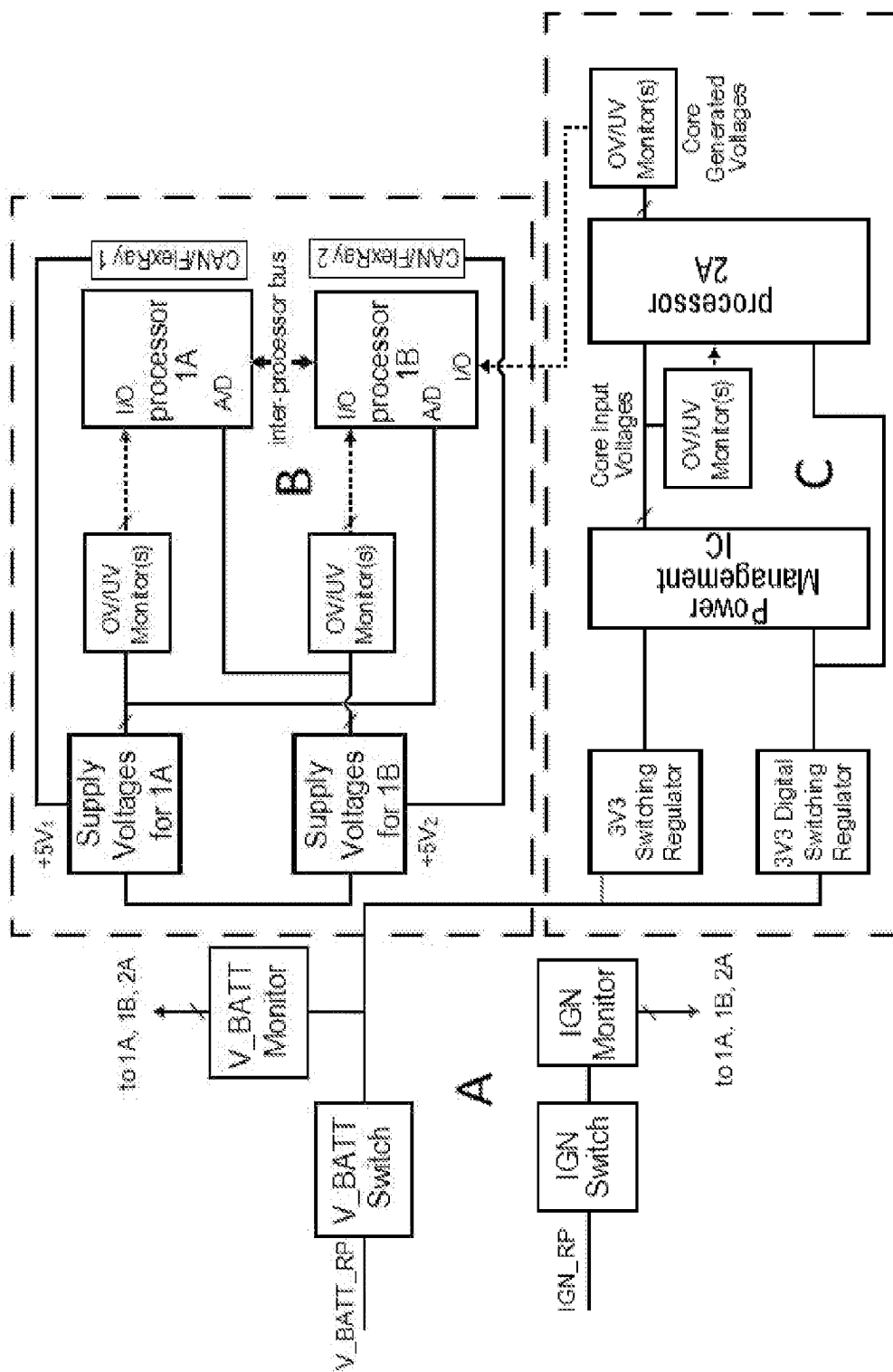


Fig. 2

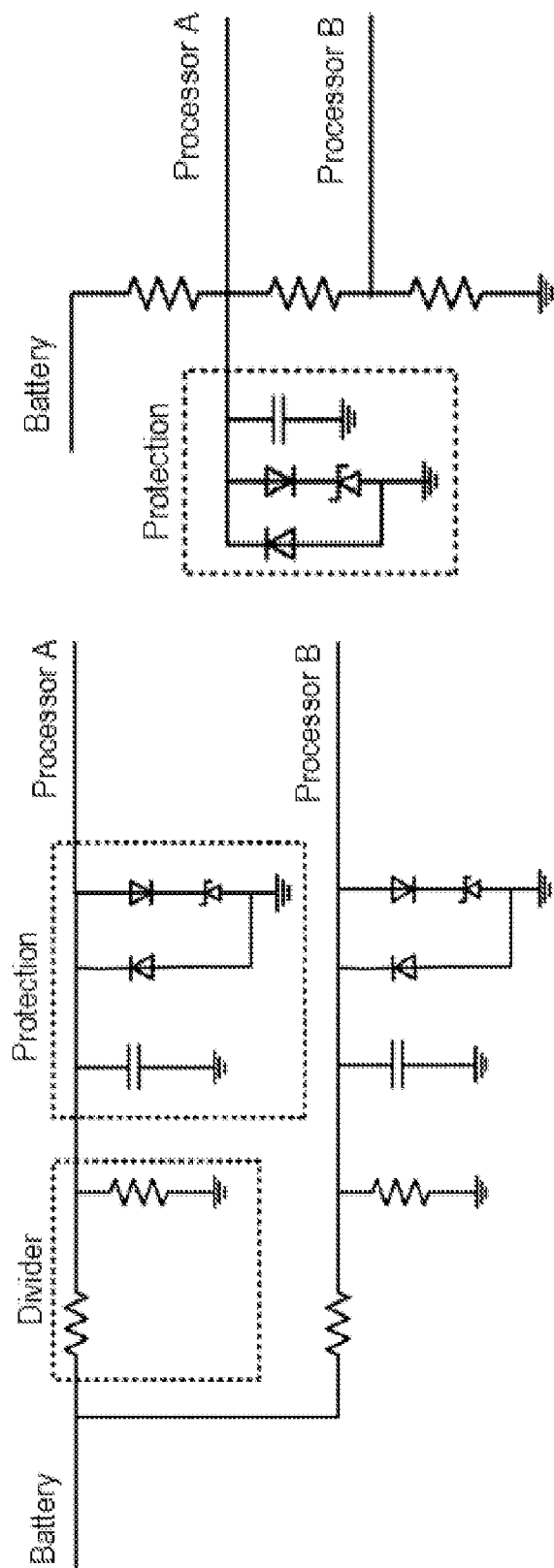


Fig. 4

Fig. 3

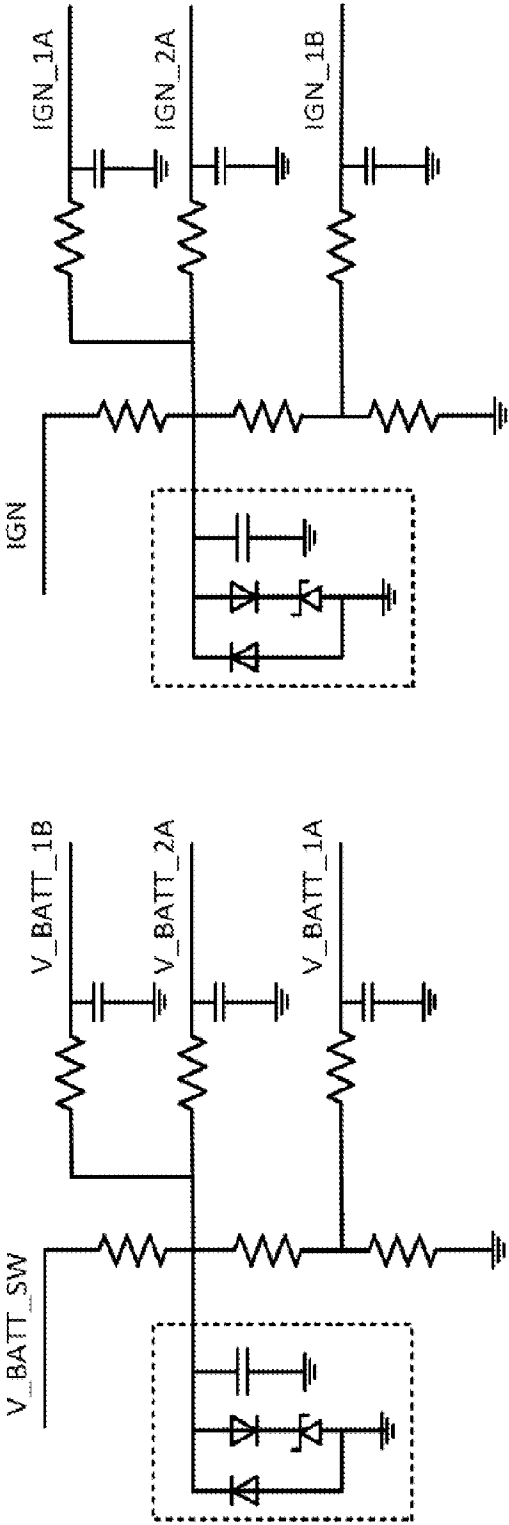


Fig. 5b

Fig. 5a

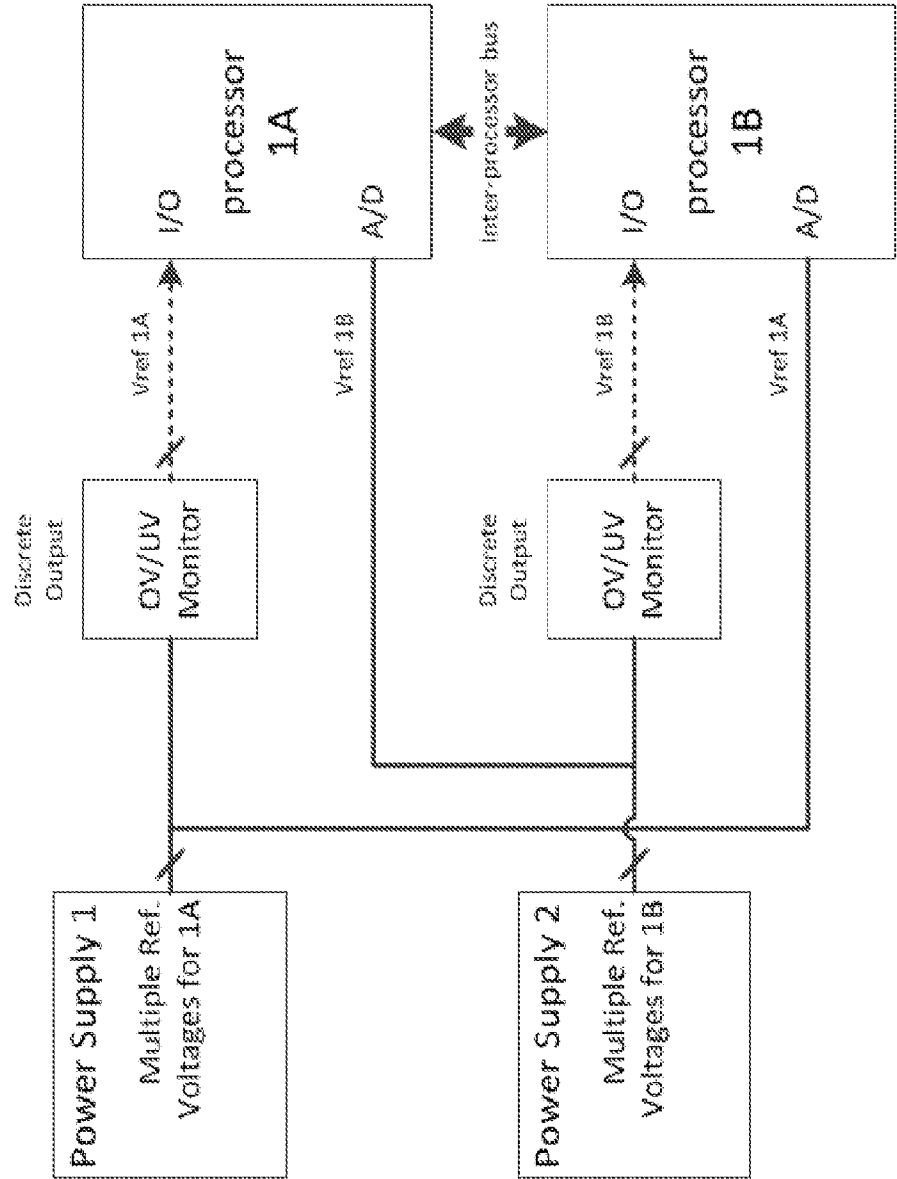


Fig. 6a

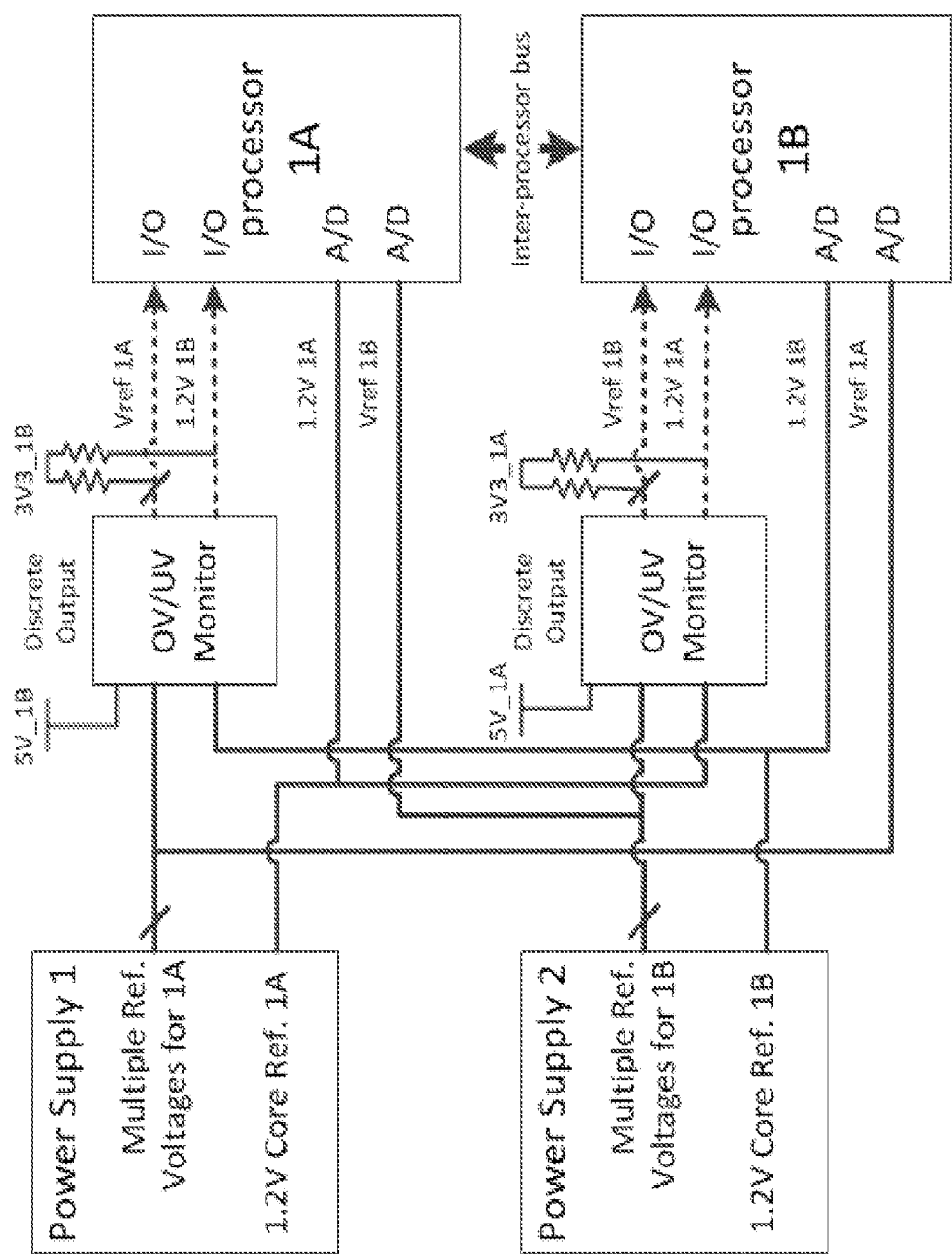


Fig. 6b

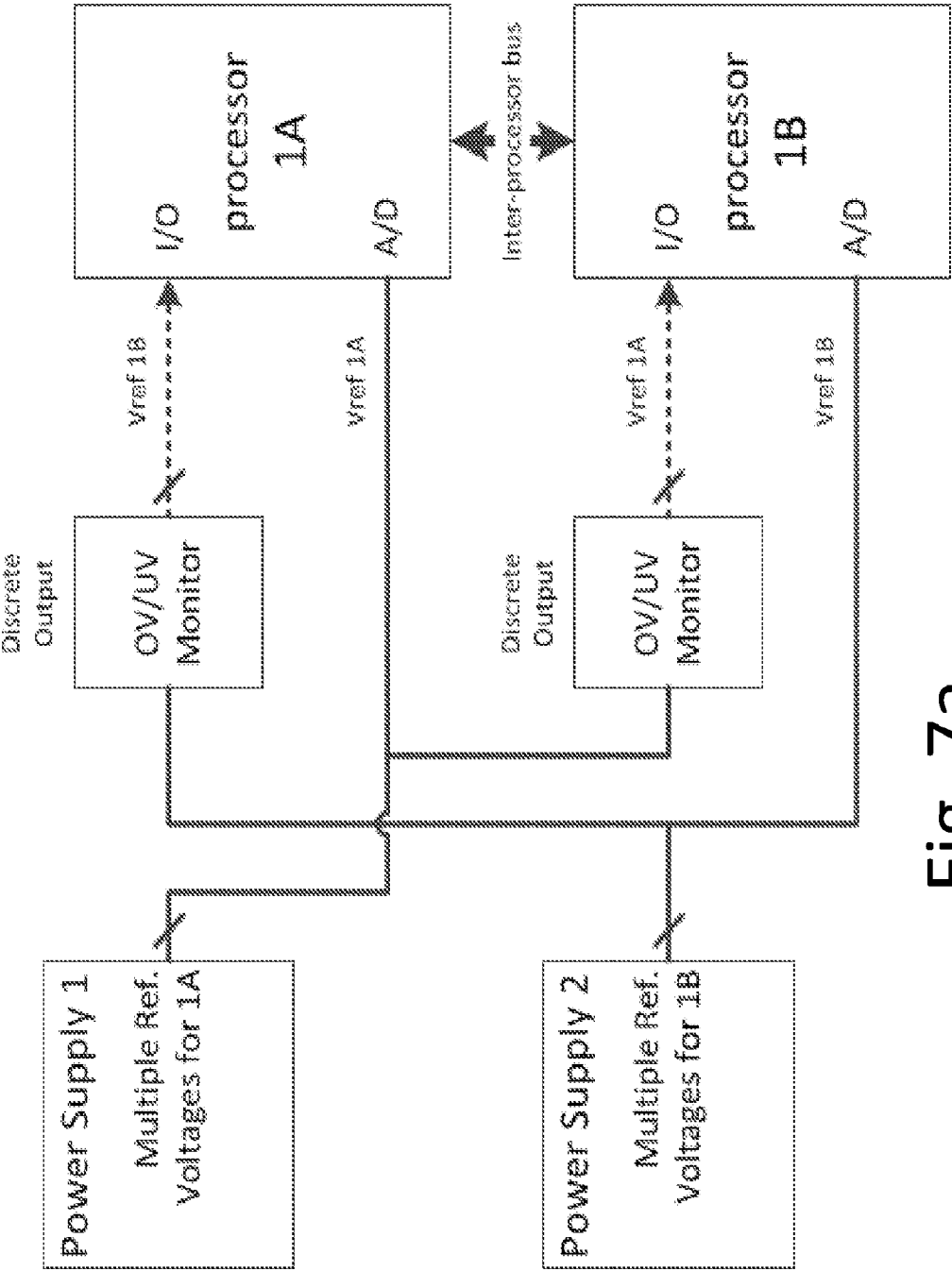


Fig. 7a

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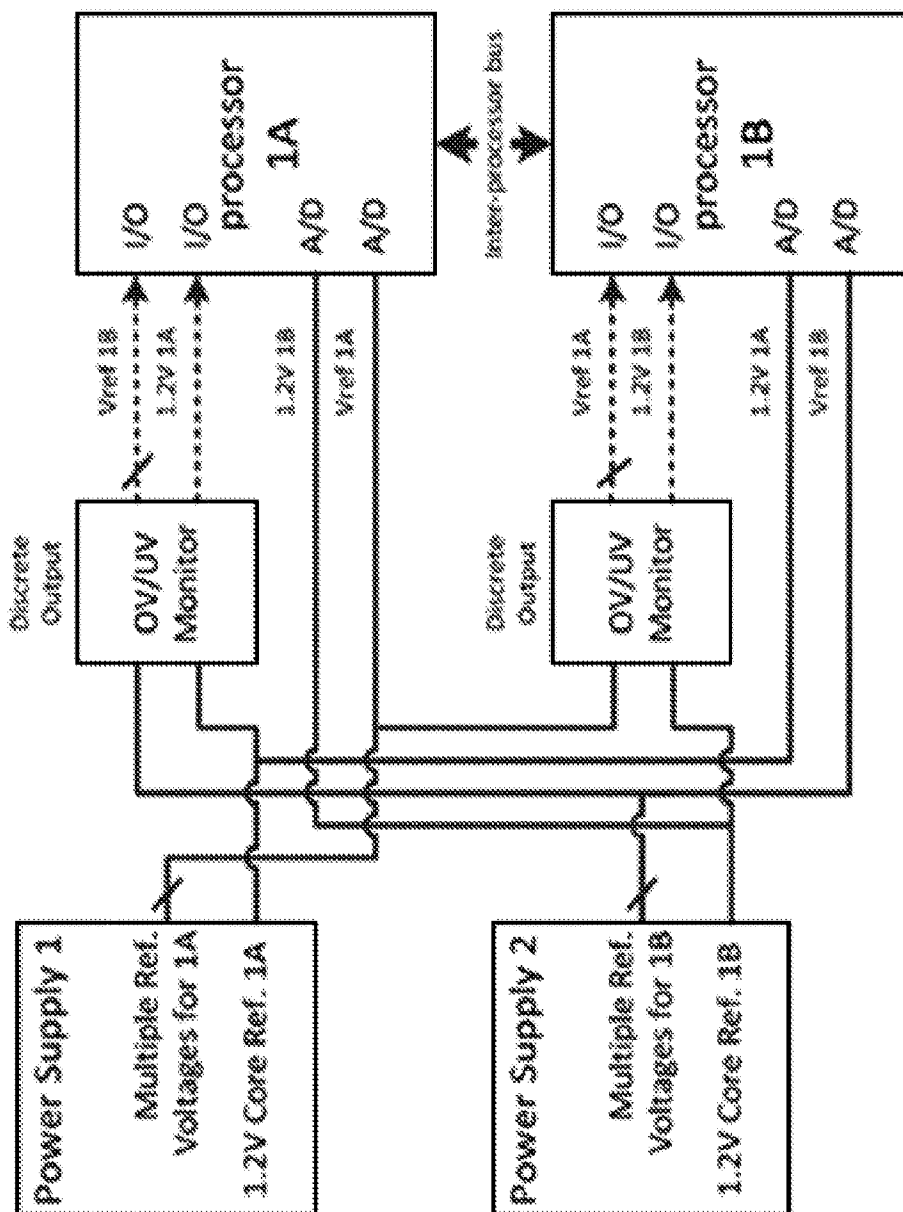


Fig. 7b

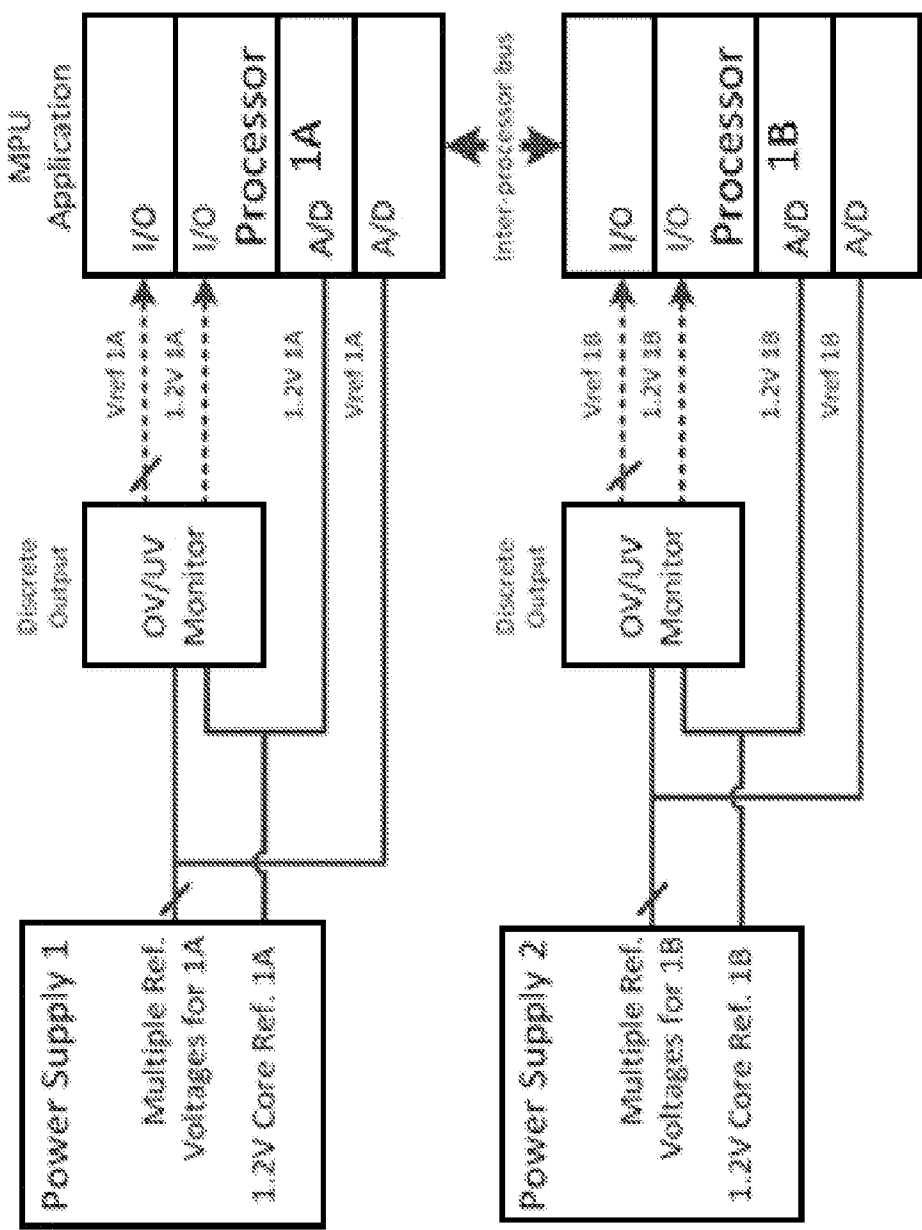


Fig. 8a

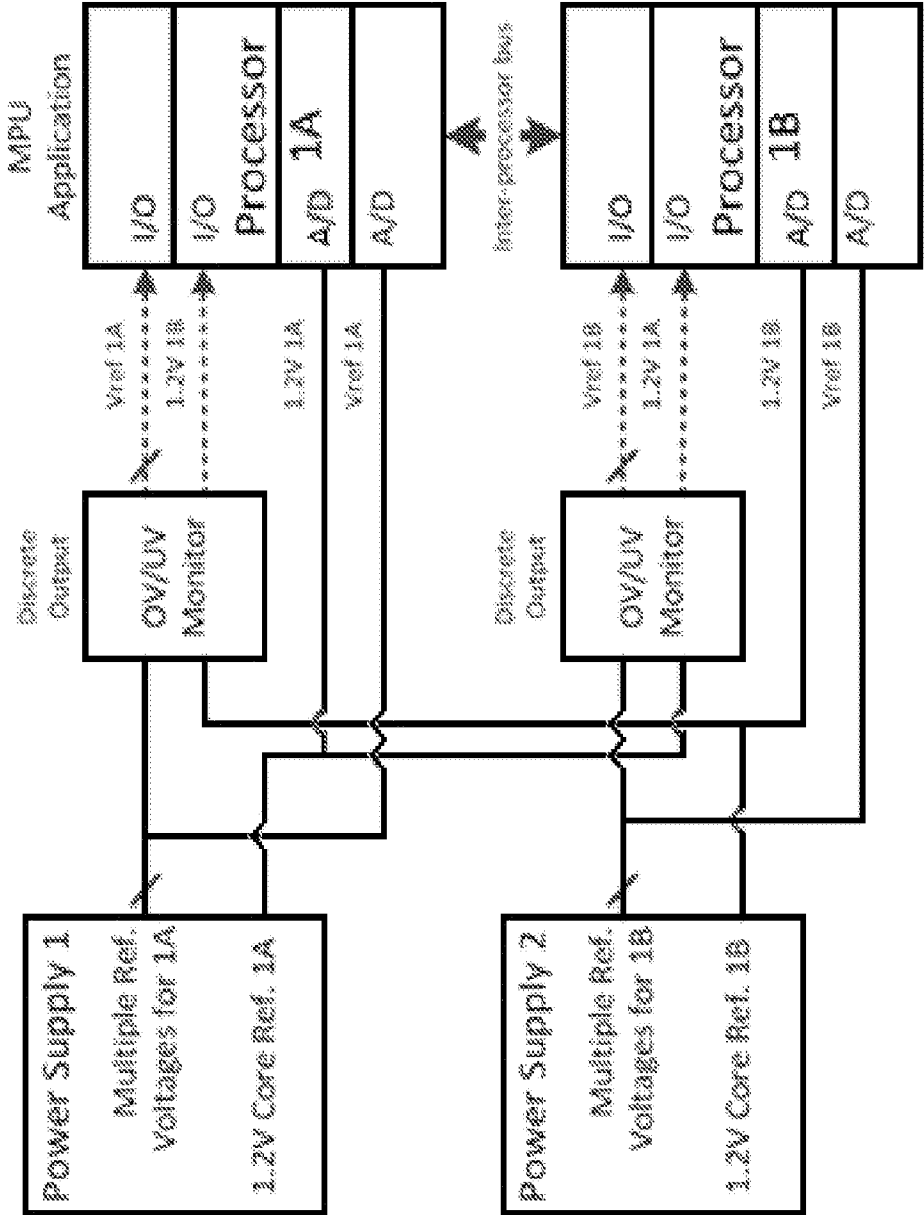


Fig. 8b

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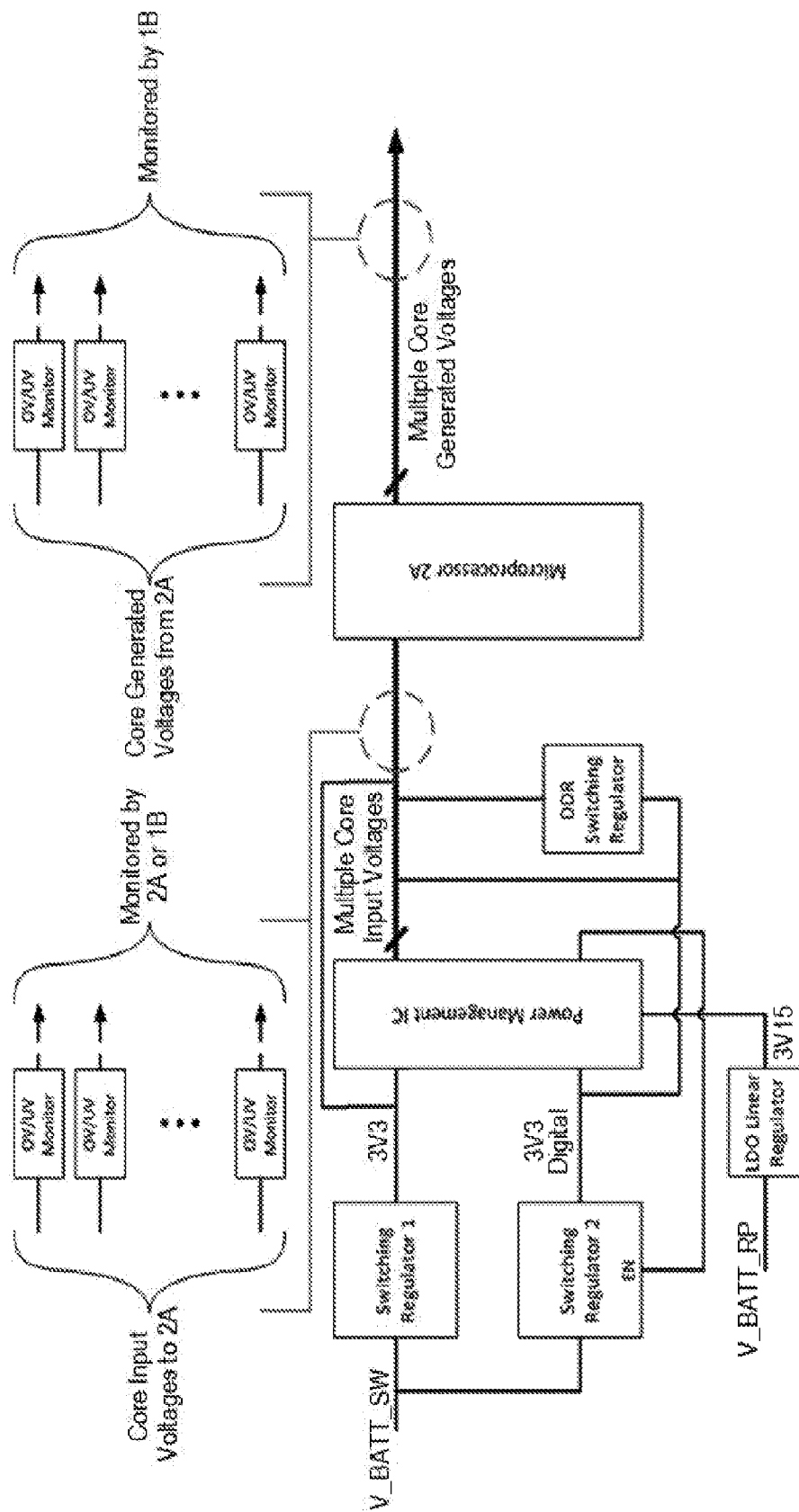
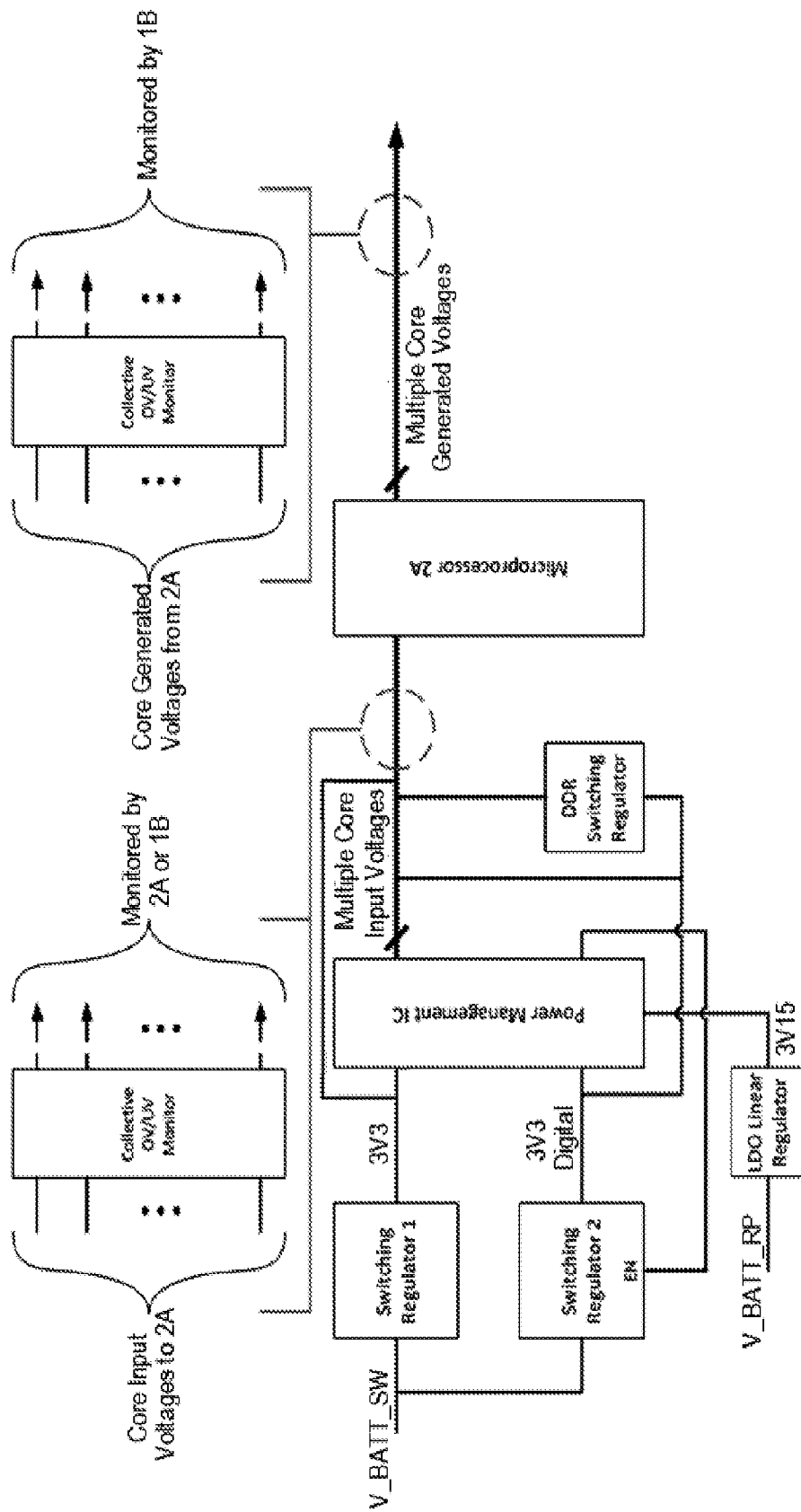


Fig. 9a



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/040967**A. CLASSIFICATION OF SUBJECT MATTER****G06F 1/26(2006.01)i, G06F 1/28(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F 1/26; G06F 1/28; H02J 1/00; G06F 19/00; H02H 5/04; H04M 1/00; G06F 13/38; G06F 9/46; H02H 7/12; G06F 13/36; H02H 007/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: circuit, redundant, monitor, voltage, divider; first, second, processor, power, supply, anomalies; and vehicle, communication, bus

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2010-0103567 A1 (KLAUS-PETER SAECK et al.) 29 April 2010 See paragraphs [0004], [0011], [0017]; and figure 1.	1-4
Y	US 2004-0042135 A1 (BERND STRUTT et al.) 04 March 2004 See paragraphs [0032], [0047]; and figures 1-2.	1-4
Y	US 2004-0145242 A1 (EDWARD T. RODRIGUEZ et al.) 29 July 2004 See paragraphs [0071], [0098]; and figure 3.	2,4
A		1,3
A	US 2011-0022871 A1 (DANIEL L. BOUVIER et al.) 27 January 2011 See paragraphs [0006], [0015], [0059], [0060], [0063]; and figure 1.	5-25
A	US 2006-0146467 A1 (HELEN RUAN et al.) 06 July 2006 See paragraphs [0014], [0024]; and figures 1-2.	5-25
A	US 2005-0250557 A1 (ERIC MARSCHALKOWSKI et al.) 10 November 2005 See paragraphs [0019]-[0022]; and figure 2.	5-25
A	US 2010-0332715 A1 (GEORGE DANIEL HADDEN et al.) 30 December 2010 See paragraphs [0003], [0006], [0036], [0056]; and figure 1.	26



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

22 October 2014 (22.10.2014)

Date of mailing of the international search report

23 October 2014 (23.10.2014)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/040967

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

Group I, claims 1-4, drawn to a circuit for providing redundant monitoring of an operating voltage in an electrical system.

Group II, claims 5-25, drawn to a power supply architecture.

Group III, claim 26, drawn to a power supply architecture for a vehicle.

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☒ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of any additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2014/040967

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2001-0001319 A1 (RICHARD D. BECKERT et al.) 17 May 2001 See paragraph [0032]; and figures 1-2.	26
A	US 6732285 B1 (RAINER SOMMER et al.) 04 May 2004 See column 2, lines 50-65; and figure 1.	26

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2014/040967

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2010-0103567 A1	29/04/2010	DE 102008053702 A1 EP 2182605 A1	06/05/2010 05/05/2010
US 2004-0042135 A1	04/03/2004	AT 491255 T AU 1231002 A AU 2002-12310 A1 DE 10049994 A1 DE 50115735 D1 EP 1327290 A1 EP 1327290 B1 US 07113375 B2 WO 2002-031941 A1	15/12/2010 22/04/2002 22/04/2002 11/04/2002 20/01/2011 16/07/2003 08/12/2010 26/09/2006 18/04/2002
US 2004-0145242 A1	29/07/2004	US 2003-0031034 A1	13/02/2003
US 2011-0022871 A1	27/01/2011	US 08639862 B2	28/01/2014
US 2006-0146467 A1	06/07/2006	US 06693412 B2 US 07049802 B2 US 07543164 B2 US 2003-0234636 A1 US 2004-0158749 A1	17/02/2004 23/05/2006 02/06/2009 25/12/2003 12/08/2004
US 2005-0250557 A1	10/11/2005	EP 1596270 A1 US 07684833 B2	16/11/2005 23/03/2010
US 2010-0332715 A1	30/12/2010	EP 2275890 A1 US 08442690 B2	19/01/2011 14/05/2013
US 2001-0001319 A1	17/05/2001	AU 1125997 A AU 1998-78528 B2 AU 691434 B2 CA 2211660 A1 CA 2211660 C DE 69629663 D1 DE 69629663 T2 DE 69637069 D1 DE 69637069 T2 EP 0804351 A2 EP 0804351 B1 EP 1376882 A2 EP 1376882 A3 EP 1376882 B1 JP 11500084 A US 05794164 A US 06009363 A US 06175789 B1 US 06202008 B1 WO 1997-019833 A2	19/06/1997 13/04/2000 14/05/1998 05/06/1997 11/04/2006 02/10/2003 01/07/2004 14/06/2007 10/01/2008 30/07/2003 27/08/2003 02/01/2004 29/12/2004 02/05/2007 06/01/1999 11/08/1998 28/12/1999 16/01/2001 13/03/2001 05/06/1997

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2014/040967

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6732285 B1	04/05/2004	WO 1997-019833 A3	24/07/1997
		DE 19947251 A1	31/05/2001
		DE 50014648 D1	25/10/2007
		EP 1089148 A2	04/04/2001
		EP 1089148 A3	23/08/2006
		EP 1089148 B1	12/09/2007
		ES 2289986 T3	16/02/2008
		JP 04855568 B2	18/01/2012
		JP 2001-109502 A	20/04/2001