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(71) Demandeur/Applicant:
HUAWEI TECHNOLOGIES CO., LTD., CN

(72) Inventeurs/Inventors:
CHEN, JUN, CN;
LI, BIN, CN;
SHEN, HUI, CN

(74) Agent: GOWLING WLG (CANADA) LLP

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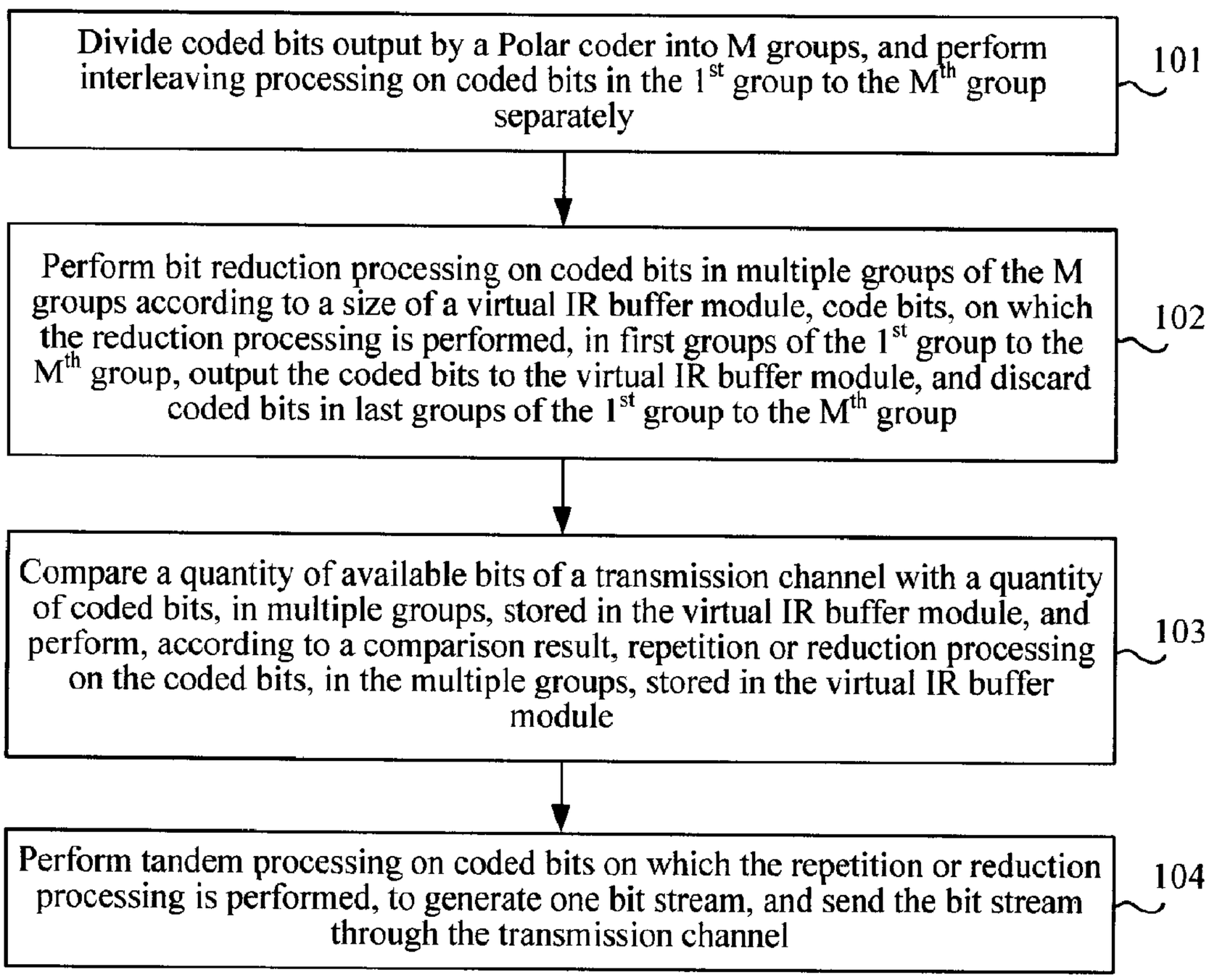

FIG. 1

(57) Abrégé/Abstract:
A coding rate matching processing method and device, the method comprising: dividing coded bits outputted by a Polar encoder into M groups and conducting interleave processing on the coded bits in group 1 to group M respectively, M being a positive

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(57) **Abrégé(suite)/Abstract(continued):**
integer; according to the size of a virtual IR buffer module, conducting bit reduction on the coded bits in the multiple groups in M groups, and outputting the reduced coded bits in each of the first groups of group 1 to group M to the virtual IR buffer module, and discarding the coded bits in last groups of group 1 to group M; comparing the number of available bits of the transmission channel with the number of coded bits in the multiple groups stored in the virtual IR buffer module; based on the comparison result, repeating or reducing the coded bits in the multiple groups stored in the virtual IR buffer module; connecting in series the repeated or reduced coded bits to generate a bit stream, and transmitting the bit stream over the transmission channel.

ABSTRACT

A rate matching processing method and apparatus for coding are disclosed. The method includes: dividing coded bits output by a Polar encoder into M groups, and performing interleaving processing on coded bits in the 1st group to the M th group separately, where M is a positive integer; performing bit reduction processing on coded bits in multiple groups of the M groups according to a size of a virtual IR buffer module, coding bits, on which the reduction processing is performed, in first groups of the 1st group to the Mth group, outputting the coded bits to the virtual IR buffer module, and discarding coded bits in last groups of the 1st group to the M th group; comparing a quantity of available bits of a transmission channel with a quantity of coded bits, in multiple groups, stored in the virtual IR buffer module, and performing, according to a comparison result, repetition or reduction processing on the coded bits, in the multiple groups, stored in the virtual IR buffer module; and performing tandem processing on coded bits on which the repetition or reduction processing is performed, to generate one bit stream, and sending the bit stream through the transmission channel.

RATE MATCHING PROCESSING METHOD AND APPARATUS FOR CODING

TECHNICAL FIELD

[0001] Embodiments of the present invention relate to communications technologies, and in particular, to a rate matching processing method and apparatus for coding.

BACKGROUND

[0002] At present, a basic principle of Polar code is to determine a row vector (or column vector) of a coding matrix according to a particular condition by using a Bhattacharyya (Bhattacharyya) parameter or a capacity (symmetric capacity), or to determine a row vector (or column vector) of a corresponding coding matrix by using a bit error rate. In this way, the Polar code can obtain better performance, for example: a better bit error rate or transmission rate, by using the row vector (or column vector) of the coding matrix selected in the foregoing manner.

[0003] In addition, the Polar code may further support a hybrid automatic repeat request (Hybrid Automatic Repeat Request; HARQ for short) function by using a two-step rate matching algorithm. Specifically, a specific implementation manner of rate matching processing of the Polar code is: dividing coded bits output by a Polar encoder into three groups, and performing an independent and uniform puncturing operation or repetition operation on each group, so that a length of a coded bit can be matched to a size of a virtual incremental redundancy buffer (Incremental Redundancy buffer; IR buffer for short) and a size of a transmission resource.

[0004] However, when the two-step rate matching algorithm is used, coded bits output by a Polar encoder need to be divided into three groups, which therefore conflicts with selection of a row vector (or column vector) of a coding matrix of Polar code. That is, in a case in which an arrangement order and an output order of priority bits are not considered, a row vector (or column vector) of a coding matrix cannot be selected in the foregoing manner, and consequently a loss in a performance gain occurs during decoding, causing severe decoding error transmission, and further causing a problem of poor performance of the Polar code.

SUMMARY

[0005] Embodiments of the present invention provide a rate matching processing method and apparatus for coding, so as to overcome a problem in the prior art that use of a two-step rate matching algorithm may conflict with selection of a row vector (or column vector) of a coding matrix of Polar code, which leads to a loss in a performance gain during decoding, causing severe decoding error transmission, and further causing poor performance of the Polar code.

[0006] A first aspect of the embodiments of the present invention provides a rate matching processing method for coding, including:

dividing coded bits output by a Polar encoder into M groups, and performing interleaving processing on coded bits in the 1st group to the M th group separately, where M is a positive integer;

performing bit reduction processing on coded bits in multiple groups of the M groups according to a size of a virtual IR buffer module, coding bits, on which the reduction processing is performed, in first groups of the 1st group to the Mth group, outputting the coded bits to the virtual IR buffer module, and discarding coded bits in last groups of the 1st group to the M th group;

comparing a quantity of available bits of a transmission channel with a quantity of coded bits, in multiple groups, stored in the virtual IR buffer module, and performing, according to a comparison result, repetition or reduction processing on the coded bits, in the multiple groups, stored in the virtual IR buffer module; and

performing tandem processing on coded bits on which the repetition or reduction processing is performed, to generate one bit stream, and sending the bit stream through the transmission channel.

[0007] In a first possible implementation manner of the first aspect, when the j th group includes $f_N(j)$ coded bits, $f_N(j)$ represents a substitution function, $j=(i-1)P+t$, where $i=1,2,\cdots,M$, $t=0,1,\cdots,P-1$, and $P=N/M$, N is a positive integer, and N represents a length of a coded bit output by the Polar encoder, the performing bit reduction processing on coded bits in multiple groups of the M groups according to a size of a virtual IR buffer module, coding bits, on which the reduction processing is performed, in first groups of the 1st group to the Mth group, outputting the coded bits to the virtual IR buffer module, and discarding coded bits in last groups of the 1st group to the M th group includes:

starting from the 1st group, sequentially outputting coded bits, on which the interleaving processing is performed, in each group to the virtual IR buffer module, until N_{IR1} coded bits on

which the interleaving processing is performed are output, where $N_{RM1}=\min(N,N_{IR})$, and N_{IR} represents the size of the virtual IR buffer module.

[0008] With reference to the first possible implementation manner of the first aspect, in a second possible implementation manner of the first aspect, the comparing a quantity of available bits of a transmission channel with a quantity of coded bits, in multiple groups, stored in the virtual IR buffer module, and performing, according to a comparison result, repetition or reduction processing on the coded bits, in the multiple groups, stored in the virtual IR buffer module includes:

when $N_{data}\le N_{RM1}$, starting from the S1th group, corresponding to a preconfigured first start position, in the virtual IR buffer module, sequentially outputting, from each group, the coded bits on which the interleaving processing is performed, until N_{data} coded bits on which the interleaving processing is performed are output; and

when $N_{data}>N_{RM1}$, starting from the S1th group, sequentially and cyclically starting to output, from each group, the coded bits.on which the interleaving processing is performed, until the N_{data} coded bits on which the interleaving processing is performed are output, where N_{data} represents the quantity of available bits of the transmission channel.

[0009] With reference to the possible implementation manner of the first aspect, in a third possible implementation manner of the first aspect, when the $^{j\ th}$ group includes $f_N(j)$ coded bits, $f_N(j)$ represents a substitution function, $j=(i-1)P+t$, where $i=1,2,\cdots,M$, $t=0,1,\cdots,P-1$, and $P=N/M$, N is a positive integer, and N represents a length of a coded bit output by the Polar encoder, the performing bit reduction processing on coded bits in multiple groups of the M groups according to a size of a virtual IR buffer module, coding bits, on which the reduction processing is performed, in first groups of the 1st group to the Mth group, outputting the coded bits to the virtual IR buffer module, and discarding coded bits in last groups of the 1st group to the $^{j\ th}$ group includes:

sequentially outputting coded bits, on which the interleaving processing is performed, in the 1st group to the Wth group to the virtual IR buffer module, and outputting the 1st to the $N_{RM1}-WP^{th}$ coded bits, on which the interleaving processing is performed, in the (W+1)th group to the virtual IR buffer module, where W meets $WP<N_{RM1}\le(W+1)P$, $N_{RM1}=\min(N,N_{IR})$, and N_{IR} represents the size of the virtual IR buffer module.

[0010] With reference to the third possible implementation manner of the first aspect, in a fourth possible implementation manner of the first aspect, the comparing a quantity of available bits

of a transmission channel with a quantity of coded bits, in multiple groups, stored in the virtual IR buffer module, and performing, according to a comparison result, repetition or reduction processing on the coded bits, in the multiple groups, stored in the virtual IR buffer module includes:

when $N_{data} \le N_{RM1}$, starting from the S2th group, corresponding to a preconfigured second start position, in the virtual IR buffer module, sequentially outputting coded bits, on which the interleaving processing is performed, in V groups, and outputting the 1st to the $N_{data} - VP^{th}$ coded bits, on which interleaving coding processing is performed, in a next group after the V groups, where V meets $VP < N_{data} \le (V+1)P$; and N_{data} represents the quantity of available bits of the transmission channel; and

when $N_{data} > N_{RM1}$, starting from the S2th group, sequentially and cyclically outputting coded bits, on which the interleaving processing is performed, in W+1 groups, where a quantity of cycles is W'; and then starting from the S2th group again, sequentially outputting the 1st to the $N_{data} - W'N_{RM1}{}^{th}$ coded bits, on which the interleaving processing is performed, in each group of $V'+1$ groups; where W' meets $W'P < N_{data} \le (W'+1)N_{RM1}$, V' meets $V'P < N_{data} - W'NN_{RM1} \le (V'+1)P$, and N_{data} represents the quantity of available bits of the transmission channel.

[0011] With reference to the possible implementation manner of the first aspect, in a fifth possible implementation manner of the first aspect, when the 1st group includes system bits, the 2nd group to the M^{th} group include parity bits, the j^{th} group includes $f_{N-K}(j)$ parity bits, $f_N(j)$ represents a substitution function, $j = (i-1)P + t$, where $i = 1, 2, \cdots, M-1$, $t = 0, 1, \cdots, P-1$, and $P = (N-K)/(M-1)$, N is a positive integer and represents a length of a coded bit output by the Polar encoder, and K represents the foremost K bits of the coded bits output by the Polar encoder, the performing bit reduction processing on coded bits, in multiple groups, of the M groups according to a size of a virtual IR buffer module, coding bits, on which the reduction processing is performed, in first groups of the 1st group to the Mth group, outputting the coded bits to the virtual IR buffer module, and discarding coded bits in last groups of the 1st group to the M^{th} group includes:

outputting system bits, on which the interleaving processing is performed, in the 1st group to the virtual IR buffer module; sequentially outputting parity bits, on which the interleaving processing is performed, in the 2nd group to the Wth group to the virtual IR buffer module; and then

outputting the 1st to the $N_{RM1}-K-WP$ th parity bits, on which the interleaving processing is performed, in the (W+1)th group to the virtual IR buffer; where W meets $WP<N_{RM1}-K\leq(W+1)P$, $N_{RM1}=\min(N,N_{IR})$, and N_{IR} represents the size of the virtual IR buffer.

[0012] With reference to the fifth possible implementation manner of the first aspect, in a sixth possible implementation manner of the first aspect, the comparing a quantity of available bits of a transmission channel with a quantity of coded bits, in multiple groups, stored in the virtual IR buffer module, and performing, according to a comparison result, repetition or reduction processing on the coded bits, in the multiple groups, stored in the virtual IR buffer module includes:

when $N_{data}\leq N_{RM1}$, outputting, from the virtual IR buffer module, the system bits, on which the interleaving processing is performed, in the 1st group; and starting from the S3th group, corresponding to a preconfigured third start position, in the virtual IR buffer module, sequentially outputting parity bits, on which the interleaving processing is performed, in V groups, and outputting the 1st to the $N_{data}-K-VP$ th coded bits, on which interleaving coding processing is performed, in a next group after the V groups, where V meets $VP<N_{data}-K\leq(V+1)P$, and N_{data} represents the quantity of available bits of the transmission channel; and

when $N_{data}>N_{RM1}$, cyclically outputting, from the virtual IR buffer module for W' times, the system bits, on which the interleaving processing is performed, in the 1st group, and starting from the S3th group in the virtual IR buffer module, sequentially and cyclically outputting parity bits, on which the interleaving processing is performed, in W+1 groups, where a quantity of cycles is W'; then outputting the system bits, on which the interleaving processing is performed, in the 1st group, and starting from the S3th group, sequentially outputting parity bits, on which the interleaving processing is performed, in V' groups; and finally, outputting the 1st to the $N_{data}-W'N_{RM1}-V'P$ th parity bits in a next group after the V' groups, where W' meets $W'P<N_{data}\leq(W'+1)N_{RM1}$; V' meets $V'P<N_{data}-W'NN_{RM1}\leq(V'+1)P$; and N_{data} represents the quantity of available bits of the transmission channel.

[0013] A second aspect of the embodiments of the present invention provides a rate matching processing apparatus for coding, including:

a dividing module, configured to divide coded bits output by a Polar encoder into M groups, where M is a positive integer;

an interleaving processing module, configured to perform interleaving processing on

coded bits in the 1st group to the M th group separately;

a first rate matching module, configured to perform bit reduction processing on coded bits in multiple groups of the M groups according to a size of a virtual IR buffer module, code bits, on which the reduction processing is performed, in first groups of the 1st group to the Mth group, output the coded bits to the virtual IR buffer module, and discard coded bits in last groups of the 1st group to the M th group;

the IR buffer module, configured to store coded bits, in multiple groups, output by the first rate matching module;

a second rate matching module, configured to compare a quantity of available bits of a transmission channel with a quantity of coded bits, in multiple groups, stored in the virtual IR buffer module, and perform, according to a comparison result, repetition or reduction processing on the coded bits, in the multiple groups, stored in the virtual IR buffer module; and

a coded bit collecting module, configured to perform tandem processing on coded bits on which the repetition or reduction processing is performed, to generate one bit stream, and send the bit stream through the transmission channel.

[0014] In a first possible implementation manner of the second aspect, when the j th group includes $f_N(j)$ coded bits, $f_N(j)$ represents a substitution function, $j=(i-1)P+t$, where $i=1,2,\cdots,M$, $t=0,1,\cdots,P-1$, and $P=N/M$, N is a positive integer, and N represents a length of a coded bit output by the Polar encoder, the first rate matching module is specifically configured to: starting from the 1st group, sequentially output coded bits, on which the interleaving processing is performed, in each group to the virtual IR buffer module, until N_{RM1} coded bits on which the interleaving processing is performed are output, where $N_{RM1}=\min(N,N_{IR})$, and N_{IR} represents the size of the virtual IR buffer module.

[0015] With reference to the first possible implementation manner of the second aspect, in a second possible implementation manner of the second aspect, the second rate matching module includes:

a bit reduction processing unit, configured to: when $N_{data}\le N_{RM1}$, starting from the S1th group, corresponding to a preconfigured first start position, in the virtual IR buffer module, sequentially output, from each group, the coded bits on which the interleaving processing is performed, until N_{data} coded bits on which the interleaving processing is performed are output; and

a bit repetition processing unit, configured to: when $N_{data}>N_{RM1}$, starting from the S1th group, sequentially and cyclically start to output, from each group, the coded bits on which the

interleaving processing is performed, until the N_{data} coded bits on which the interleaving processing is performed are output, where N_{data} represents the quantity of available bits of the transmission channel.

[0016] With reference to the possible implementation manner of the second aspect, in a third possible implementation manner of the second aspect, when the j th group includes $f_N(j)$ coded bits, $f_N(j)$ represents a substitution function, $j=(i-1)P+t$, where $i=1,2,\cdots,M$, $t=0,1,\cdots,P-1$, and $P=N/M$, N is a positive integer, and N represents a length of a coded bit output by the Polar encoder, the first rate matching module is specifically configured to: sequentially output coded bits, on which the interleaving processing is performed, in the 1st group to the Wth group to the virtual IR buffer module, and output the 1st to the $N_{RM1}-WP$ th coded bits, on which the interleaving processing is performed, in the (W+1)th group to the virtual IR buffer module, where W meets $WP<N_{RM1}\leq(W+1)P$, $N_{RM1}=\min(N,N_{IR})$, and N_{IR} represents the size of the virtual IR buffer module.

[0017] With reference to the third possible implementation manner of the second aspect, in a fourth possible implementation manner of the second aspect, the second rate matching module includes:

a bit reduction processing unit, configured to: when $N_{data}\leq N_{RM1}$, starting from the S2th group, corresponding to a preconfigured second start position, in the virtual IR buffer module, sequentially output coded bits, on which the interleaving processing is performed, in V groups, and output the 1st to the $N_{data}-VP$ th coded bits, on which interleaving coding processing is performed, in a next group after the V groups, where V meets $VP<N_{data}\leq(V+1)P$; and N_{data} represents the quantity of available bits of the transmission channel; and

a bit repetition processing unit, configured to: when $N_{data}>N_{RM1}$, starting from the S2th group, sequentially and cyclically output coded bits, on which the interleaving processing is performed, in W+1 groups, where a quantity of cycles is W'; and then starting from the S2th group again, sequentially output the 1st to the $N_{data}-W'N_{RM1}$ th coded bits, on which the interleaving processing is performed, in each group of the $V'+1$ groups; where W' meets $W'P<N_{data}\leq(W'+1)N_{RM1}$, V' meets $V'P<N_{data}-W'NN_{RM1}\leq(V'+1)P$, and N_{data} represents the quantity of available bits of the transmission channel.

[0018] With reference to the possible implementation manner of the second aspect, in a fifth

possible implementation manner of the second aspect, when the 1st group includes system bits, the 2nd group to the M th group include parity bits, the j th group includes $f_{N-K}(j)$ parity bits, $f_N(j)$ represents a substitution function, $j=(i-1)P+t$, where $i=1,2,\cdots,M-1$, $t=0,1,\cdots,P-1$, and $P=(N-K)/(M-1)$, N is a positive integer and represents a length of a coded bit output by the Polar encoder, and K represents the foremost K bits of the coded bits output by the Polar encoder, the first rate matching module is specifically configured to output system bits, on which the interleaving processing is performed, in the 1st group to the virtual IR buffer module, sequentially output parity bits, on which the interleaving processing is performed, in the 2nd group to the Wth group to the virtual IR buffer module, and then output the 1st to the $N_{RM1}-K-WP$ th parity bits, on which the interleaving processing is performed, in the (W+1)th group to the virtual IR buffer module, where W meets $WP<N_{RM1}-K\leq(W+1)P$; $N_{RM1}=\min(N,N_{IR})$, and N_{IR} represents the size of the virtual IR buffer module.

[0019] With reference to the fifth possible implementation manner of the second aspect, in a sixth possible implementation manner of the second aspect, the second rate matching module includes:

a bit reduction processing unit, configured to: when $N_{data}\leq N_{RM1}$, output, from the virtual IR buffer module, the system bits, on which the interleaving processing is performed, in the 1st group; and starting from the S3th group, corresponding to a preconfigured third start position, in the IR buffer, sequentially output parity bits, on which the interleaving processing is performed, in V groups, and output the 1st to the $N_{data}-K-VP$ th coded bits, on which interleaving coding processing is performed, in a next group after the V groups, where V meets $VP<N_{data}-K\leq(V+1)P$; and N_{data} represents the quantity of available bits of the transmission channel; and

a bit repetition processing unit, configured to: when $N_{data}>N_{RM1}$, cyclically output, from the virtual IR buffer module for W' times, the system bits, on which the interleaving processing is performed, in the 1st group, and starting from the S3th group in the virtual IR buffer module, sequentially and cyclically output parity bits, on which the interleaving processing is performed, in W+1 groups, where a quantity of cycles is W'; then output the system bits, on which the interleaving processing is performed, in the 1st group, and starting from the S3th group, sequentially output parity bits, on which the interleaving processing is performed, in V' groups;

and finally, output the 1st to the $N_{data}-W'N_{RM1}-V'P$ th parity bits in a next group after the V' groups, where W' meets $W'P<N_{data}\leq(W'+1)N_{RM1}$; V' meets $V'P<N_{data}-W'NN_{RM1}\leq(V'+1)P$; and N_{data} represents the quantity of available bits of the transmission channel.

[0020] According to the rate matching processing method and apparatus for coding in the embodiments of the present invention, coded bits output by a Polar encoder are divided into M groups, and interleaving processing is performed on coded bits in the 1st group to the Mth group separately; bit reduction processing is performed on coded bits in multiple groups of the M groups according to a size of a virtual IR buffer module, bits, on which the reduction processing is performed, in first groups of the 1st group to the Mth group are coded and output to the virtual IR buffer module, and coded bits in last groups of the 1st group to the M th group are discarded; a quantity of available bits of a transmission channel is compared with a quantity of coded bits, in multiple groups, stored in the virtual IR buffer module, and repetition or reduction processing is performed, according to a comparison result, on the coded bits, in the multiple groups, stored in the virtual IR buffer module; and tandem processing is performed on coded bits on which the repetition or reduction processing is performed, to generate one bit stream, and the bit stream is sent through the transmission channel. Because coded bits output by a Polar encoder are randomly divided into multiple groups, and bit reduction processing or bit reduction processing and bit repetition processing are performed on the multiple groups continuously, not only an efficient and flexible rate matching technology can be supported, but also HARQ retransmission can be supported, and transmission efficiency can be further improved.

BRIEF DESCRIPTION OF DRAWINGS

[0021] To describe the technical solutions in the embodiments of the present invention or in the prior art more clearly, the following briefly introduces the accompanying drawings required for describing the embodiments or the prior art. Apparently, the accompanying drawings in the following description show some embodiments of the present invention, and persons of ordinary skill in the art may still derive other drawings from these accompanying drawings without creative efforts.

[0022] FIG. 1 is a flowchart of an embodiment of a rate matching processing method for coding according to the present invention;

[0023] FIG. 2 is a flowchart of another embodiment of a rate matching processing method for coding according to the present invention;

[0024] FIG. 3 is a flowchart of still another embodiment of a rate matching processing method for coding according to the present invention;

[0025] FIG. 4 is a flowchart of yet another embodiment of a rate matching processing method for coding according to the present invention;

[0026] FIG. 5 is a schematic structural diagram of an embodiment of a rate matching processing apparatus for coding according to the present invention; and

[0027] FIG. 6 is a schematic structural diagram of another embodiment of a rate matching processing apparatus for coding according to the present invention.

DESCRIPTION OF EMBODIMENTS

[0028] To make the objectives, technical solutions, and advantages of the embodiments of the present invention clearer, the following clearly and completely describes the technical solutions in the embodiments of the present invention with reference to the accompanying drawings in the embodiments of the present invention. Apparently, the described embodiments are some but not all of the embodiments of the present invention. All other embodiments obtained by persons of ordinary skill in the art based on the embodiments of the present invention without creative efforts shall fall within the protection scope of the present invention.

[0029] FIG. 1 is a flowchart of an embodiment of a rate matching processing method for coding according to the present invention. As shown in FIG. 1, the method in this embodiment may include:

[0030] Step 101: Divide coded bits output by a Polar encoder into M groups, and perform interleaving processing on coded bits in the 1st group to the Mth group separately.

[0031] In this embodiment, coded bits output by the Polar encoder may be non-systematic Polar coded bits or non-systematic Polar coded bits.

[0032] Step 102: Perform bit reduction processing on coded bits in multiple groups of the M groups according to a size of a virtual IR buffer module, code bits, on which the reduction processing is performed, in first groups of the 1^{st} group to the M^{th} group, output the coded bits to the virtual IR buffer module, and discard coded bits in last groups of the 1^{st} group to the M^{th} group.

[0033] Step 103: Compare a quantity of available bits of a transmission channel with a quantity of coded bits, in multiple groups, stored in the virtual IR buffer module, and perform, according to a comparison result, repetition or reduction processing on the coded bits, in the multiple groups, stored in the virtual IR buffer module.

[0034] In this embodiment, a quantity of available bits of a transmission channel is a quantity of

available resources of a physical layer air interface.

[0035] In this embodiment, if the quantity of the coded bits, in the multiple groups, stored in the virtual IR buffer module is greater than or equal to the quantity of available bits of the transmission channel, bit reduction processing is performed, that is, first coded bits of a group corresponding to a selected start position are output preferentially, and rest coded bits are discarded. In addition, if the quantity of the coded bits, in the multiple groups, stored in the virtual IR buffer module is less than the quantity of available bits of the transmission channel, bit repetition processing is performed, and starting from the group corresponding to the selected start position, coded bits of groups are output cyclically and repeatedly, first coded bits of the groups are output preferentially, and last coded bits are discarded.

[0036] The selected start position may be pre-defined, or is a received hybrid automatic repeat request (Hybrid Automatic Repeat Request; HARQ for short) redundancy version (Redundancy Version; RV for short) indication sent by a wireless communications system.

[0037] Step 104: Perform tandem processing on coded bits on which the repetition or reduction processing is performed, to generate one bit stream, and send the bit stream through the transmission channel.

[0038] In this embodiment, coded bits output by a Polar encoder are divided into M groups, and interleaving processing is performed on coded bits in the 1st group to the Mth group separately; bit reduction processing is performed on coded bits in multiple groups of the M groups according to a size of a virtual IR buffer module, bits, on which the reduction processing is performed, in first groups of the 1st group to the Mth group are coded and output to the virtual IR buffer module, and coded bits in last groups of the 1st group to the M th group are discarded; a quantity of available bits of a transmission channel is compared with a quantity of coded bits, in multiple groups, stored in the virtual IR buffer module, and repetition or reduction processing is performed, according to a comparison result, on the coded bits, in the multiple groups, stored in the virtual IR buffer module; and tandem processing is performed on coded bits on which the repetition or reduction processing is performed, to generate one bit stream, and the bit stream is output through the transmission channel. Because coded bits output by a Polar encoder are randomly divided into multiple groups, and bit reduction processing or bit reduction processing and bit repetition processing are performed on the multiple groups continuously, not only an efficient and flexible rate matching technology can be supported, but also HARQ retransmission can be supported, and transmission efficiency can be further improved.

[0039] The technical solution in the method embodiment shown in FIG. 1 is described in detail below by using several specific embodiments.

[0040] FIG. 2 is a flowchart of another embodiment of a rate matching processing method for coding according to the present invention. On a basis of the foregoing embodiment shown in FIG. 1, as shown in FIG. 2, in this embodiment, an example in which coded bits output by a Polar encoder may be non-systematic Polar coded bits is used, that is, the j th group includes $f_N(j)$ coded bits, $f_N(j)$ represents a substitution function, and $j=(i-1)P+t$, where $i=1,2,\cdots,M$, $t=0,1,\cdots,P-1$, and $P = N / M$; N is a positive integer and represents a length of a coded bit output by the Polar encoder. The technical solution in this embodiment is described in detail, and a specific implementation manner of step 102 is:

[0041] Step 201: Starting from the 1st group, sequentially output coded bits, on which the interleaving processing is performed, in each group to the virtual IR buffer module, until N_{RM1} coded bits on which the interleaving processing is performed are output, where $N_{RM1}=\min(N,N_{IR})$, and N_{IR} represents the size of the virtual IR buffer module.

[0042] Optionally, a specific implementation manner of step 103 is:

[0043] Step 202: Compare N_{RM1} with the quantity of available bits of the transmission channel. If $N_{data} \le N_{RM1}$, perform step 203; if $N_{data} > N_{RM1}$, perform step 204.

[0044] Step 203: Starting from the S1th group, corresponding to a preconfigured first start position, in the virtual IR buffer module, sequentially output, from each group, the coded bits on which the interleaving processing is performed, until N_{data} coded bits on which the interleaving processing is performed are output.

[0045] Step 204: Starting from the S1th group, sequentially and cyclically start to output, from each group, the coded bits on which the interleaving processing is performed, until the N_{data} coded bits on which the interleaving processing is performed are output, where N_{data} represents the quantity of available bits of the transmission channel.

[0046] FIG. 3 is a flowchart of still another embodiment of a rate matching processing method for coding according to the present invention. On a basis of the foregoing embodiment shown in FIG. 1, as shown in FIG. 3, in this embodiment, an example in which coded bits output by a Polar encoder may be non-systematic Polar coded bits is used, that is, the j th group includes $f_N(j)$ coded bits, $f_N(j)$ represents a substitution function, and $j=(i-1)P+t$, where $i=1,2,\cdots,M$, $t=0,1,\cdots,P-1$, and $P = N / M$; N is a positive integer and represents a length of a coded bit output by the Polar encoder. The technical solution in this embodiment is described in detail, and

another specific implementation manner of step 102 is:

[0047] Step 301: Sequentially output coded bits, on which the interleaving processing is performed, in the 1st group to the Wth group to the virtual IR buffer module, and output the 1st to the $N_{RM1}-WP$ th coded bits, on which the interleaving processing is performed, in the (W+1)th group to the virtual IR buffer module.

[0048] W meets $WP<N_{RM1}\leq(W+1)P$, $N_{RM1}=\min(N,N_{IR})$, and N_{IR} represents the size of the virtual IR buffer module.

[0049] Optionally, another specific implementation manner of step 103 is:

[0050] Step 302: Compare N_{RM1} with the quantity of available bits of the transmission channel. If $N_{data}\leq N_{RM1}$, perform step 303; if $N_{data}>N_{RM1}$, perform step 304.

[0051] Step 303: Starting from the S2th group, corresponding to a preconfigured second start position, in the virtual IR buffer module, sequentially output coded bits, on which the interleaving processing is performed, in V groups, and output the 1st to the $N_{data}-VP$ th coded bits, on which interleaving coding processing is performed, in a next group after the V groups.

[0052] V meets $VP<N_{data}\leq(V+1)P$; and N_{data} represents the quantity of available bits of the transmission channel.

[0053] Step 304: Starting from the S2th group, sequentially and cyclically output coded bits on which the interleaving processing is performed, in W+1 groups, where a quantity of cycles is W'; and then starting from the S2th group again, sequentially output the 1st to the $N_{data}-W'N_{RM1}$ th coded bits, on which the interleaving processing is performed, in each group of $V'+1$ groups. W' meets $W'P<N_{data}\leq(W'+1)N_{RM1}$, V' meets $V'P<N_{data}-W'NN_{RM1}\leq(V'+1)P$, and N_{data} represents the quantity of available bits of the transmission channel.

[0054] FIG. 4 is a flowchart of yet another embodiment of a rate matching processing method for coding according to the present invention. On a basis of the foregoing embodiment shown in FIG. 1, as shown in FIG. 4, in this embodiment, an example in which coded bits output by a Polar encoder may be systematic Polar coded bits is used, that is, the 1st group includes system bits, the 2nd group to the Mth group include parity bits, the j th group includes $f_{N-K}(j)$ parity bits, $f_N(j)$ represents a substitution function, and $j=(i-1)P+t$, where $i=1,2,\cdots,M-1$, $t=0,1,\cdots,P-1$, and $P=(N-K)/(M-1)$; N is a positive integer and represents a length of a coded bit output

by the Polar encoder; K represents the foremost K bits of the coded bits output by the Polar encoder. The technical solution in this embodiment is described in detail, and still another specific implementation manner of step 102 is:

[0055] Step 401: Output system bits, on which the interleaving processing is performed, in the 1st group to the virtual IR buffer module; sequentially output parity bits, on which the interleaving processing is performed, in the 2nd group to the Wth group to the virtual IR buffer module; and then output the 1st to the $N_{RM1}-K-WP$ th parity bits, on which the interleaving processing is performed, in the (W+1)th group to the virtual IR buffer; where W meets $WP<N_{RM1}-K\leq(W+1)P$, $N_{RM1}=\min(N,N_{IR})$, and N_{IR} represents the size of the virtual IR buffer.

[0056] Optionally, still another specific implementation manner of step 103 is:

[0057] Step 402: Compare N_{RM1} with the quantity of available bits of the transmission channel. If $N_{data}\leq N_{RM1}$, perform step 403; if $N_{data}>N_{RM1}$, perform step 404.

[0058] Step 403: Output, from the virtual IR buffer module, the system bits, on which the interleaving processing is performed, in the 1st group; and starting from the S3th group, corresponding to a preconfigured third start position, in the virtual IR buffer module, sequentially output parity bits, on which the interleaving processing is performed, in V groups, and output the 1st to the $N_{data}-K-VP$ th coded bits, on which interleaving coding processing is performed, in a next group after the V groups, where V meets $VP<N_{data}-K\leq(V+1)P$, and N_{data} represents the quantity of available bits of the transmission channel.

[0059] Step 404: Cyclically output, from the virtual IR buffer module for W' times, the system bits, on which the interleaving processing is performed, in the 1st group; starting from the S3th group in the virtual IR buffer module, sequentially and cyclically output parity bits, on which the interleaving processing is performed, in W+1 groups, where a quantity of cycles is W'; then output the system bits, on which the interleaving processing is performed, in the 1st group, and starting from the S3th group, sequentially output parity bits, on which the interleaving processing is performed, in V' groups; and finally, output the 1st to the $N_{data}-W'N_{RM1}-V'P$ th parity bits in a next group after the V' groups; where W' meets $W'P<N_{data}\leq(W'+1)N_{RM1}$, V' meets $V'P<N_{data}-W'NN_{RM1}\leq(V'+1)P$, and N_{data} represents the quantity of available bits of the transmission channel.

[0060] FIG. 5 is a schematic structural diagram of an embodiment of a rate matching processing

apparatus for coding according to the present invention. As shown in FIG. 5, the apparatus of this embodiment may include: a dividing module 11, an interleaving processing module 12, a first rate matching module 13, an IR buffer module 14, a second rate matching module 15, and a coded bit collecting module 16, where the dividing module 11 is configured to divide coded bits output by a Polar encoder into M groups, where M is a positive integer; the interleaving processing module 12 is configured to perform interleaving processing on coded bits in the 1st group to the M th group separately; the first rate matching module 13 is configured to perform bit reduction processing on coded bits in multiple groups of the M groups according to a size of the virtual IR buffer module 14, code bits, on which the reduction processing is performed, in first groups of the 1st group to the Mth group, output the coded bits to the virtual IR buffer module 14, discard coded bits in last groups of the 1st group to the M th group, and discard the coded bits of the last groups; the IR buffer module 14 is configured to store coded bits, in multiple groups, output by the first rate matching module; the second rate matching module 15 is configured to compare a quantity of available bits of a transmission channel with a quantity of coded bits, in multiple groups, stored in the virtual IR buffer module, and perform, according to a comparison result, repetition or reduction processing on the coded bits, in the multiple groups, stored in the virtual IR buffer module 14; and the coded bit collecting module 16 is configured to perform tandem processing on coded bits on which the repetition or reduction processing is performed, to generate one bit stream, and send the bit stream through the transmission channel.

[0061] The apparatus in this embodiment may be configured to execute the technical solution in the method embodiment shown in FIG. 1. Implementation principles and technical effects of this embodiment and the method embodiment are similar, and details are not described herein again.

[0062] FIG. 6 is a schematic structural diagram of another embodiment of a rate matching processing apparatus for coding according to the present invention. As shown in FIG. 6, on a basis of the apparatus structure shown in FIG. 5, in the apparatus in this embodiment, when the j th group includes $f_N(j)$ coded bits, $f_N(j)$ represents a substitution function, $j=(i-1)P+t$, where $i=1,2,\cdots,M$, $t=0,1,\cdots,P-1$, and $P=N/M$, N is a positive integer, and N represents a length of a coded bit output by the Polar encoder, the first rate matching module 13 is specifically configured to: starting from the 1st group, sequentially output coded bits, on which the interleaving processing is performed, in each group to the virtual IR buffer module 14, until N_{RM1} coded bits on which the interleaving processing is performed are output, where $N_{RM1}=\min(N,N_{IR})$, and N_{IR} represents the size of the virtual IR buffer module 14.

[0063] Optionally, the second rate matching module 15 includes: a bit reduction processing unit 151 and a bit repetition processing unit 152, where the bit reduction processing unit 151 is configured to: when $N_{data} \le N_{RM1}$, starting from the S1th group, corresponding to a preconfigured first start position, in the virtual IR buffer module, sequentially output, from each group, the coded bits on which the interleaving processing is performed, until N_{data} coded bits on which the interleaving processing is performed are output; and the bit repetition processing unit 152 is configured to: when $N_{data} > N_{RM1}$, starting from the S1th group, sequentially and cyclically start to output, from each group, the coded bits on which the interleaving processing is performed, until the N_{data} coded bits on which the interleaving processing is performed are output, where N_{data} represents the quantity of available bits of the transmission channel.

[0064] The apparatus in this embodiment may be configured to execute the technical solution in the method embodiment shown in FIG. 2. Implementation principles and technical effects of this embodiment and the method embodiment are similar, and details are not described herein again.

[0065] Further, in still another embodiment of the present invention, on a basis of the foregoing embodiment shown in FIG. 5, when the j^{th} group includes $f_N(j)$ coded bits, $f_N(j)$ represents a substitution function, $j=(i-1)P+t$, where $i=1,2,\cdots,M$, $t=0,1,\cdots,P-1$, and $P = N / M$, N is a positive integer, and N represents a length of a coded bit output by the Polar encoder, the first rate matching module 13 is specifically configured to: sequentially output coded bits, on which the interleaving processing is performed, in the 1st group to the Wth group to the virtual IR buffer module 14, and output the 1st to the $N_{RM1}-WP^{th}$ coded bits, on which the interleaving processing is performed, in the (W+1)th group to the virtual IR buffer module 14, where W meets $WP < N_{RM1} \le (W+1)P$, $N_{RM1} = \min(N, N_{IR})$, and N_{IR} represents the size of the virtual IR buffer module 14.

[0066] Optionally, the second rate matching module 15 includes: a bit reduction processing unit and a bit repetition processing unit, where the bit reduction processing unit is configured to: when $N_{data} \le N_{RM1}$, starting from the S2th group, corresponding to a preconfigured second start position, in the virtual IR buffer module 14, sequentially output coded bits, on which the interleaving processing is performed, in V groups, and output the 1st to the $N_{data}-VP^{th}$ coded bits, on which interleaving coding processing is performed, in a next group after the V groups, where V meets $VP<N_{data}\le(V+1)P$; and N_{data} represents the quantity of available bits of the transmission

channel; and the bit repetition processing unit is configured to: when $N_{data} > N_{RM1}$, starting from the S2th group, sequentially and cyclically output coded bits, on which the interleaving processing is performed, in W+1 groups, where a quantity of cycles is W'; and then starting from the S2th group again, sequentially output the 1st to the $N_{data} - W'N_{RM1}$ th coded bits, on which the interleaving processing is performed, in each group of $V'+1$ groups; where W' meets $W'P < N_{data} \leq (W'+1)N_{RM1}$, V' meets $V'P < N_{data} - W'NN_{RM1} \leq (V'+1)P$, and N_{data} represents the quantity of available bits of the transmission channel.

[0067] The apparatus in this embodiment may be configured to execute the technical solution in the method embodiment shown in FIG. 3. Implementation principles and technical effects of this embodiment and the method embodiment are similar, and details are not described herein again.

[0068] Further, in yet another embodiment of the present invention, on a basis of the foregoing embodiment shown in FIG. 5, when the 1st group includes system bits, the 2nd group to the Mth group include parity bits, the j th group includes $f_{N-K}(j)$ parity bits, $f_N(j)$ represents a substitution function, $j=(i-1)P+t$, where $i=1,2,\cdots,M-1$, $t=0,1,\cdots,P-1$, and $P=(N-K)/(M-1)$, N is a positive integer and represents a length of a coded bit output by the Polar encoder, and K represents the foremost K bits of the coded bits output by the Polar encoder, the first rate matching module 13 is specifically configured to output system bits, on which the interleaving processing is performed, in the 1st group to the virtual IR buffer module 14, sequentially output parity bits, on which the interleaving processing is performed, in the 2nd group to the Wth group to the virtual IR buffer module 14, and then output the 1st to the $N_{RM1} - K - WP$ th parity bits, on which the interleaving processing is performed, in the (W+1)th group to the virtual IR buffer module 14, where W meets $WP < N_{RM1} - K \leq (W+1)P$, $N_{RM1} = \min(N, N_{IR})$, and N_{IR} represents the size of the virtual IR buffer module 14.

[0069] Optionally, the second rate matching module 15 includes: a bit reduction processing unit and a bit repetition processing unit, where the bit reduction processing unit is configured to: when $N_{data} \leq N_{RM1}$, output, from the virtual IR buffer module, the system bits, on which the interleaving processing is performed, in the 1st group, and starting from the S3th group, corresponding to a preconfigured third start position, in the IR buffer, sequentially output parity bits, on which the interleaving processing is performed, in V groups, and output the 1st to the $N_{data} - K - VP$ th coded bits, on which interleaving coding processing is performed, in a next group after the V groups,

where V meets $VP<N_{data}-K\leq(V+1)P$, and N_{data} represents the quantity of available bits of the transmission channel; and the bit repetition processing unit is configured to: when $N_{data}>N_{RM1}$, cyclically output, from the virtual IR buffer module for W' times, the system bits, on which the interleaving processing is performed, in the 1st group, and starting from the S3th group in the virtual IR buffer module, sequentially and cyclically output parity bits, on which the interleaving processing is performed, in W+1 groups, where a quantity of cycles is W'; then output the system bits, on which the interleaving processing is performed, in the 1st group, and starting from the S3th group, sequentially output parity bits, on which the interleaving processing is performed, in V' groups; and finally, output the 1st to the $N_{data}-W'N_{RM1}-V'P$ th parity bits in a next group after the V' groups, where W' meets $W'P<N_{data}\leq(W'+1)N_{RM1}$; V' meets $V'P<N_{data}-W'NN_{RM1}\leq(V'+1)P$; and N_{data} represents the quantity of available bits of the transmission channel.

[0070] The apparatus in this embodiment may be configured to execute the technical solution in the method embodiment shown in FIG. 4. Implementation principles and technical effects of this embodiment and the method embodiment are similar, and details are not described herein again.

[0071] Persons of ordinary skill in the art may understand that all or some of the steps of the method embodiments may be implemented by a program instructing relevant hardware. The program may be stored in a computer-readable storage medium. When the program runs, the steps of the method embodiments are performed. The foregoing storage medium includes: any medium that can store program code, such as a ROM, a RAM, a magnetic disk, or an optical disc.

[0072] Finally, it should be noted that the foregoing embodiments are merely intended for describing the technical solutions in the present invention, but not for limiting the present invention. Although the present invention is described in detail with reference to the foregoing embodiments, persons of ordinary skill in the art should understand that they may still make modifications to the technical solutions described in the foregoing embodiments or make equivalent replacements to some or all technical features thereof, without departing from the scope of the technical solutions in the embodiments of the present invention.

CLAIMS

What is claimed is:

1. A rate matching processing method for coding, comprising:

dividing coded bits output by a Polar encoder into M groups, and performing interleaving processing on coded bits in the 1st group to the M th group separately, wherein M is a positive integer;

performing bit reduction processing on coded bits in multiple groups of the M groups according to a size of a virtual IR buffer module, coding bits, on which the reduction processing is performed, in first groups of the 1st group to the Mth group, outputting the coded bits to the virtual IR buffer module, and discarding coded bits in last groups of the 1st group to the M th group;

comparing a quantity of available bits of a transmission channel with a quantity of coded bits, in multiple groups, stored in the virtual IR buffer module, and performing, according to a comparison result, repetition or reduction processing on the coded bits, in the multiple groups, stored in the virtual IR buffer module; and

performing tandem processing on coded bits on which the repetition or reduction processing is performed, to generate one bit stream, and sending the bit stream through the transmission channel.

2. The method according to claim 1, wherein when the j th group comprises $f_N(j)$ coded bits, $f_N(j)$ represents a substitution function, $j=(i-1)P+t$, wherein $i=1,2,\cdots,M$, $t=0,1,\cdots,P-1$, and $P = N / M$, N is a positive integer, and N represents a length of a coded bit output by the Polar encoder, the performing bit reduction processing on coded bits in multiple groups of the M groups according to a size of a virtual IR buffer module, coding bits, on which the reduction processing is performed, in first groups of the 1st group to the Mth group, outputting the coded bits to the virtual IR buffer module, and discarding coded bits in last groups of the 1st group to the M th group comprises:

starting from the 1st group, sequentially outputting coded bits, on which the interleaving processing is performed, in each group to the virtual IR buffer module, until N_{RM1} coded bits on which the interleaving processing is performed are output, wherein $N_{RM1}=\min(N,N_{IR})$, and N_{IR} represents the size of the virtual IR buffer module.

3. The method according to claim 2, wherein the comparing a quantity of available bits of a transmission channel with a quantity of coded bits, in multiple groups, stored in the virtual IR buffer module, and performing, according to a comparison result, repetition or reduction processing on the coded bits, in the multiple groups, stored in the virtual IR buffer module comprises:

when $N_{data} \le N_{RM1}$, starting from the S1th group, corresponding to a preconfigured first start position, in the virtual IR buffer module, sequentially outputting, from each group, the coded bits on which the interleaving processing is performed, until N_{data} coded bits on which the interleaving processing is performed are output; and

when $N_{data} > N_{RM1}$, starting from the S1th group, sequentially and cyclically starting to output, from each group, the coded bits on which the interleaving processing is performed, until the N_{data} coded bits on which the interleaving processing is performed are output, wherein N_{data} represents the quantity of available bits of the transmission channel.

4. The method according to claim 1, wherein when the $_j$ th group comprises $f_N(j)$ coded bits, $f_N(j)$ represents a substitution function, $j=(i-1)P+t$, wherein $i=1,2,\cdots,M$, $t=0,1,\cdots,P-1$, and $P = N / M$, N is a positive integer, and N represents a length of a coded bit output by the Polar encoder, the performing bit reduction processing on coded bits in multiple groups of the M groups according to a size of a virtual IR buffer module, coding bits, on which the reduction processing is performed, in first groups of the 1st group to the Mth group, outputting the coded bits to the virtual IR buffer module, and discarding coded bits in last groups of the 1st group to the M th group comprises:

sequentially outputting coded bits, on which the interleaving processing is performed, in the 1st group to the Wth group to the virtual IR buffer module, and outputting the 1st to the $N_{RM1}-WP$ th coded bits, on which the interleaving processing is performed, in the (W+1)th group to the virtual IR buffer module, wherein W meets $WP<N_{RM1}\le(W+1)P$, $N_{RM1}=\min(N,N_{IR})$, and N_{IR} represents the size of the virtual IR buffer module.

5. The method according to claim 4, wherein the comparing a quantity of available bits of a transmission channel with a quantity of coded bits, in multiple groups, stored in the virtual IR buffer module, and performing, according to a comparison result, repetition or reduction processing on the coded bits, in the multiple groups, stored in the virtual IR buffer module comprises:

when $N_{data} \le N_{RM1}$, starting from the S2th group, corresponding to a preconfigured second start position, in the virtual IR buffer module, sequentially outputting coded bits, on which the interleaving processing is performed, in V groups, and outputting the 1st to the $N_{data}-VP$ th coded bits, on which interleaving coding processing is performed, in a next group after the V groups, wherein V meets $VP<N_{data}\le(V+1)P$, and N_{data} represents the quantity of available bits of the transmission channel; and

when $N_{data} > N_{RM1}$, starting from the S2th group, sequentially and cyclically outputting coded bits, on which the interleaving processing is performed, in W+1 groups, wherein a quantity of cycles is W'; and then starting from the S2th group again, sequentially outputting the 1st to the $N_{data} - W'N_{RM1}$ th coded bits, on which the interleaving processing is performed, in each group of $V'+1$ groups; wherein W' meets $W'P < N_{data} \leq (W'+1)N_{RM1}$, V' meets $V'P < N_{data} - W'NN_{RM1} \leq (V'+1)P$, and N_{data} represents the quantity of available bits of the transmission channel.

6. The method according to claim 1, wherein when the 1st group comprises system bits, the 2nd group to the M th group comprise parity bits, the j th group comprises $f_{N-K}(j)$ parity bits, $f_N(j)$ represents a substitution function, $j=(i-1)P+t$, herein $i=1,2,\cdots,M-1$, $t=0,1,\cdots,P-1$, and $P=(N-K)/(M-1)$, N is a positive integer and represents a length of a coded bit output by the Polar encoder, and K represents the foremost K bits of the coded bits output by the Polar encoder, the performing bit reduction processing on coded bits, in multiple groups, of the M groups according to a size of a virtual IR buffer module, coding bits, on which the reduction processing is performed, in first groups of the 1st group to the Mth group, outputting the coded bits to the virtual IR buffer module, and discarding coded bits in last groups of the 1st group to the M th group comprises:

outputting system bits, on which the interleaving processing is performed, in the 1st group to the virtual IR buffer module; sequentially outputting parity bits, on which the interleaving processing is performed, in the 2nd group to the Wth group to the virtual IR buffer module; and then outputting the 1st to the $N_{RM1} - K - WP$ th parity bits, on which the interleaving processing is performed, in the (W+1)th group to the virtual IR buffer; wherein W meets $WP < N_{RM1} - K \leq (W+1)P$, $N_{RM1} = \min(N, N_{IR})$, and N_{IR} represents the size of the virtual IR buffer.

7. The method according to claim 6, wherein the comparing a quantity of available bits of a transmission channel with a quantity of coded bits, in multiple groups, stored in the virtual IR buffer module, and performing, according to a comparison result, repetition or reduction processing on the coded bits, in the multiple groups, stored in the virtual IR buffer module comprises:

when $N_{data} \leq N_{RM1}$, outputting, from the virtual IR buffer module, the system bits, on which the interleaving processing is performed, in the 1st group; and starting from the S3th group,

corresponding to a preconfigured third start position, in the virtual IR buffer module, sequentially outputting parity bits, on which the interleaving processing is performed, in V groups, and outputting the 1st to the $N_{data}-K-VP$ th coded bits, on which interleaving coding processing is performed, in a next group after the V groups, wherein V meets $VP<N_{data}-K\leq(V+1)P$, and N_{data} represents the quantity of available bits of the transmission channel; and

when $N_{data}>N_{RM1}$, cyclically outputting, from the virtual IR buffer module for W' times, the system bits, on which the interleaving processing is performed, in the 1st group, and starting from the S3th group in the virtual IR buffer module, sequentially and cyclically outputting parity bits, on which the interleaving processing is performed, in W+1 groups, wherein a quantity of cycles is W'; then outputting the system bits, on which the interleaving processing is performed, in the 1st group, and starting from the S3th group, sequentially outputting parity bits, on which the interleaving processing is performed, in V' groups; and finally, outputting the 1st to the $N_{data}-W'N_{RM1}-V'P$ th parity bits in a next group after the V' groups, wherein W' meets $W'P<N_{data}\leq(W'+1)N_{RM1}$; V' meets $V'P<N_{data}-W'NN_{RM1}\leq(V'+1)P$; and N_{data} represents the quantity of available bits of the transmission channel.

8. A rate matching processing apparatus for coding, comprising:

a dividing module, configured to divide coded bits output by a Polar encoder into M groups, wherein M is a positive integer;

an interleaving processing module, configured to perform interleaving processing on coded bits in the 1st group to the M th group separately;

a first rate matching module, configured to perform bit reduction processing on coded bits in multiple groups of the M groups according to a size of a virtual IR buffer module, code bits, on which the reduction processing is performed, in first groups of the 1st group to the Mth group, output the coded bits to the virtual IR buffer module, and discard coded bits in last groups of the 1st group to the M th group;

the IR buffer module, configured to store coded bits, in multiple groups, output by the first rate matching module;

a second rate matching module, configured to compare a quantity of available bits of a transmission channel with a quantity of coded bits, in multiple groups, stored in the virtual IR buffer module, and perform, according to a comparison result, repetition or reduction processing on the coded bits, in the multiple groups, stored in the virtual IR buffer module; and

a coded bit collecting module, configured to perform tandem processing on coded bits on

which the repetition or reduction processing is performed, to generate one bit stream, and send the bit stream through the transmission channel.

9. The apparatus according to claim 8, wherein when the j th group comprises $f_N(j)$ coded bits, $f_N(j)$ represents a substitution function, $j=(i-1)P+t$, wherein $i=1,2,\cdots,M$, $t=0,1,\cdots,P-1$, and $P = N / M$, N is a positive integer and N represents a length of a coded bit output by the Polar encoder, the first rate matching module is specifically configured to: starting from the 1st group, sequentially output coded bits, on which the interleaving processing is performed, in each group to the virtual IR buffer module, until N_{RM1} coded bits on which the interleaving processing is performed are output, wherein $N_{RM1}=\min(N,N_{IR})$, and N_{IR} represents the size of the virtual IR buffer module.

10. The apparatus according to claim 9, wherein the second rate matching module comprises:

a bit reduction processing unit, configured to: when $N_{data} \le N_{RM1}$, starting from the S1th group, corresponding to a preconfigured first start position, in the virtual IR buffer module, sequentially output, from each group, the coded bits on which the interleaving processing is performed, until N_{data} coded bits on which the interleaving processing is performed are output; and

a bit repetition processing unit, configured to: when $N_{data} > N_{RM1}$, starting from the S1th group, sequentially and cyclically start to output, from each group, the coded bits on which the interleaving processing is performed, until the N_{data} coded bits on which the interleaving processing is performed are output, wherein N_{data} represents the quantity of available bits of the transmission channel.

11. The apparatus according to claim 8, wherein when the j th group comprises $f_N(j)$ coded bits, $f_N(j)$ represents a substitution function, $j=(i-1)P+t$, wherein $i=1,2,\cdots,M$, $t=0,1,\cdots,P-1$, and $P = N / M$, N is a positive integer, and N represents a length of a coded bit output by the Polar encoder, the first rate matching module is specifically configured to: sequentially output coded bits, on which the interleaving processing is performed, in the 1st group to the Wth group to the virtual IR buffer module, and output the 1st to the $N_{RM1}-WP$th coded bits, on which the interleaving processing is performed, in the (W+1)th group to the virtual IR buffer module, wherein W meets $WP<N_{RM1}\le(W+1)P$, $N_{RM1}=\min(N,N_{IR})$, and N_{IR} represents the size of the virtual IR buffer module.

12. The apparatus according to claim 11, wherein the second rate matching module comprises:

a bit reduction processing unit, configured to: when $N_{data} \le N_{RM1}$, starting from the S2th group, corresponding to a preconfigured second start position, in the virtual IR buffer module, sequentially output coded bits, on which the interleaving processing is performed, in V groups, and output the 1st to the $N_{data} - VP$ th coded bits, on which interleaving coding processing is performed, in a next group after the V groups, wherein V meets $VP < N_{data} \le (V+1)P$; and N_{data} represents the quantity of available bits of the transmission channel; and

a bit repetition processing unit, configured to: when $N_{data} > N_{RM1}$, starting from the S2th group, sequentially and cyclically output coded bits, on which the interleaving processing is performed, in W+1 groups, wherein a quantity of cycles is W'; and then starting from the S2th group again, sequentially output the 1st to the $N_{data} - W'N_{RM1}$ th coded bits, on which the interleaving processing is performed, in each group of the $V'+1$ groups; wherein W' meets $W'P < N_{data} \le (W'+1)N_{RM1}$, V' meets $V'P < N_{data} - W'NN_{RM1} \le (V'+1)P$, and N_{data} represents the quantity of available bits of the transmission channel.

13. The apparatus according to claim 8, wherein when the 1st group comprises system bits, the 2nd group to the M th group comprise parity bits, the $_j$ th group comprises $f_{N-K}(j)$ parity bits, $f_N(j)$ represents a substitution function, $j=(i-1)P+t$, wherein $i=1,2,\cdots,M-1$, $t=0,1,\cdots,P-1$, and $P=(N-K)/(M-1)$, N is a positive integer and represents a length of a coded bit output by the Polar encoder, and K represents the foremost K bits of the coded bits output by the Polar encoder, the first rate matching module is specifically configured to output system bits, on which the interleaving processing is performed, in the 1st group to the virtual IR buffer module, sequentially output parity bits, on which the interleaving processing is performed, in the 2nd group to the Wth group to the virtual IR buffer module, and then output the 1st to the $N_{RM1} - K - WP$ th parity bits, on which the interleaving processing is performed, in the (W+1)th group to the virtual IR buffer module, wherein W meets $WP < N_{RM1} - K \le (W+1)P$, $N_{RM1} = \min(N, N_{IR})$, and N_{IR} represents the size of the virtual IR buffer module.

14. The apparatus according to claim 13, wherein the second rate matching module comprises:

a bit reduction processing unit, configured to: when $N_{data} \le N_{RM1}$, output, from the virtual IR

buffer module, the system bits, on which the interleaving processing is performed, in the 1st group; and starting from the S3th group, corresponding to a preconfigured third start position, in the IR buffer, sequentially output parity bits, on which the interleaving processing is performed, in V groups, and output the 1st to the $N_{data}-K-VP$ th coded bits, on which interleaving coding processing is performed, in a next group after the V groups, wherein V meets $VP<N_{data}-K\leq(V+1)P$, and N_{data} represents the quantity of available bits of the transmission channel; and

a bit repetition processing unit, configured to: when $N_{data}>N_{RM1}$, cyclically output, from the virtual IR buffer module for W' times, the system bits, on which the interleaving processing is performed, in the 1st group, and starting from the S3th group in the virtual IR buffer module, sequentially and cyclically output parity bits, on which the interleaving processing is performed, in W+1 groups, wherein a quantity of cycles is W'; then output the system bits, on which the interleaving processing is performed, in the 1st group, and starting from the S3th group, sequentially output parity bits, on which the interleaving processing is performed, in V' groups; and finally, output the 1st to the $N_{data}-W'N_{RM1}-V'P$ th parity bits in a next group after the V' groups, wherein W' meets $W'P<N_{data}\leq(W'+1)N_{RM1}$; V' meets $V'P<N_{data}-W'NN_{RM1}\leq(V'+1)P$; and N_{data} represents the quantity of available bits of the transmission channel.

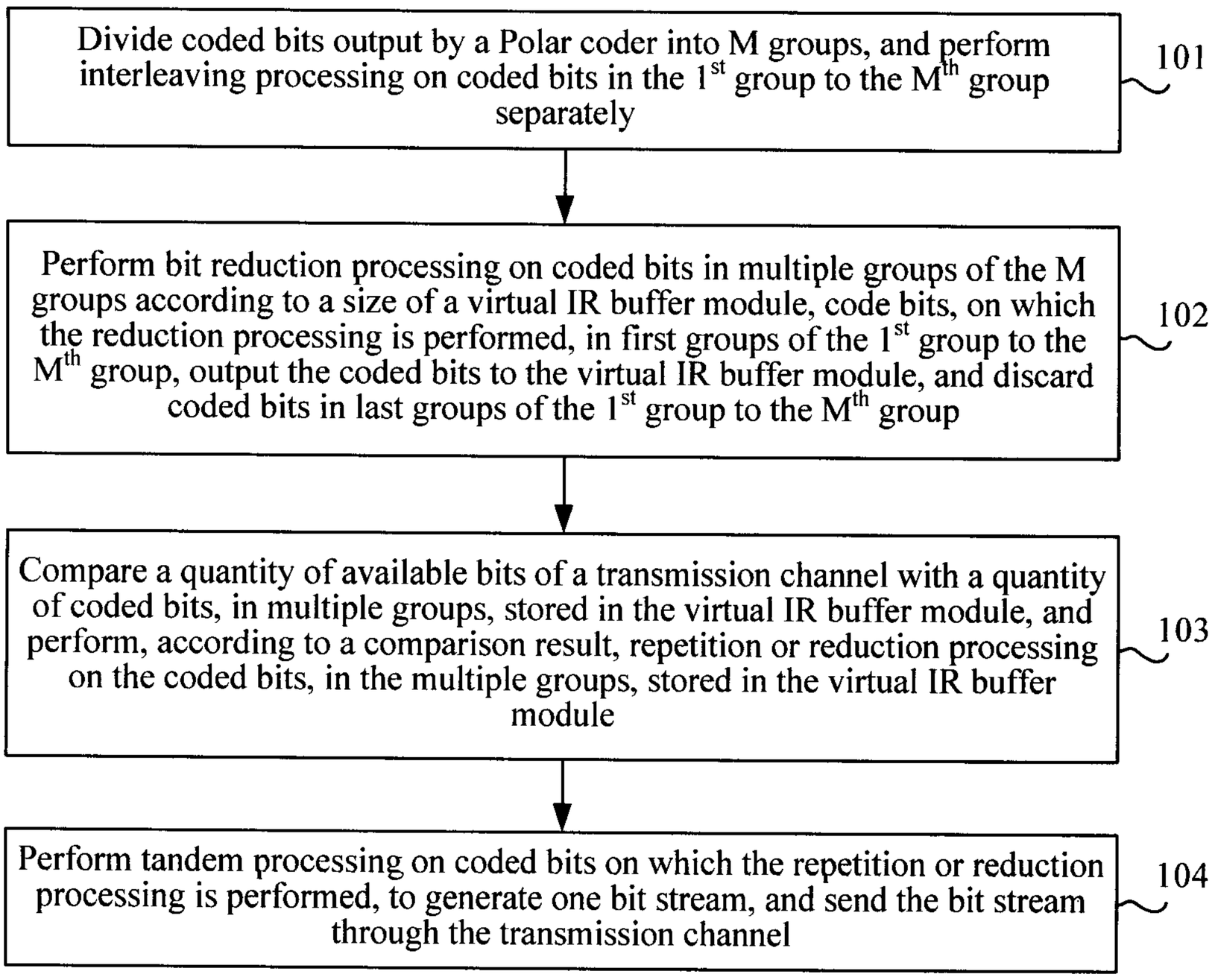
Divide coded bits output by a Polar coder into M groups, and perform interleaving processing on coded bits in the 1st group to the Mth group separately
101
Perform bit reduction processing on coded bits in multiple groups of the M groups according to a size of a virtual IR buffer module, code bits, on which the reduction processing is performed, in first groups of the 1st group to the Mth group, output the coded bits to the virtual IR buffer module, and discard coded bits in last groups of the 1st group to the Mth group
102
Compare a quantity of available bits of a transmission channel with a quantity of coded bits, in multiple groups, stored in the virtual IR buffer module, and perform, according to a comparison result, repetition or reduction processing on the coded bits, in the multiple groups, stored in the virtual IR buffer module
103
Perform tandem processing on coded bits on which the repetition or reduction processing is performed, to generate one bit stream, and send the bit stream through the transmission channel
104

FIG. 1

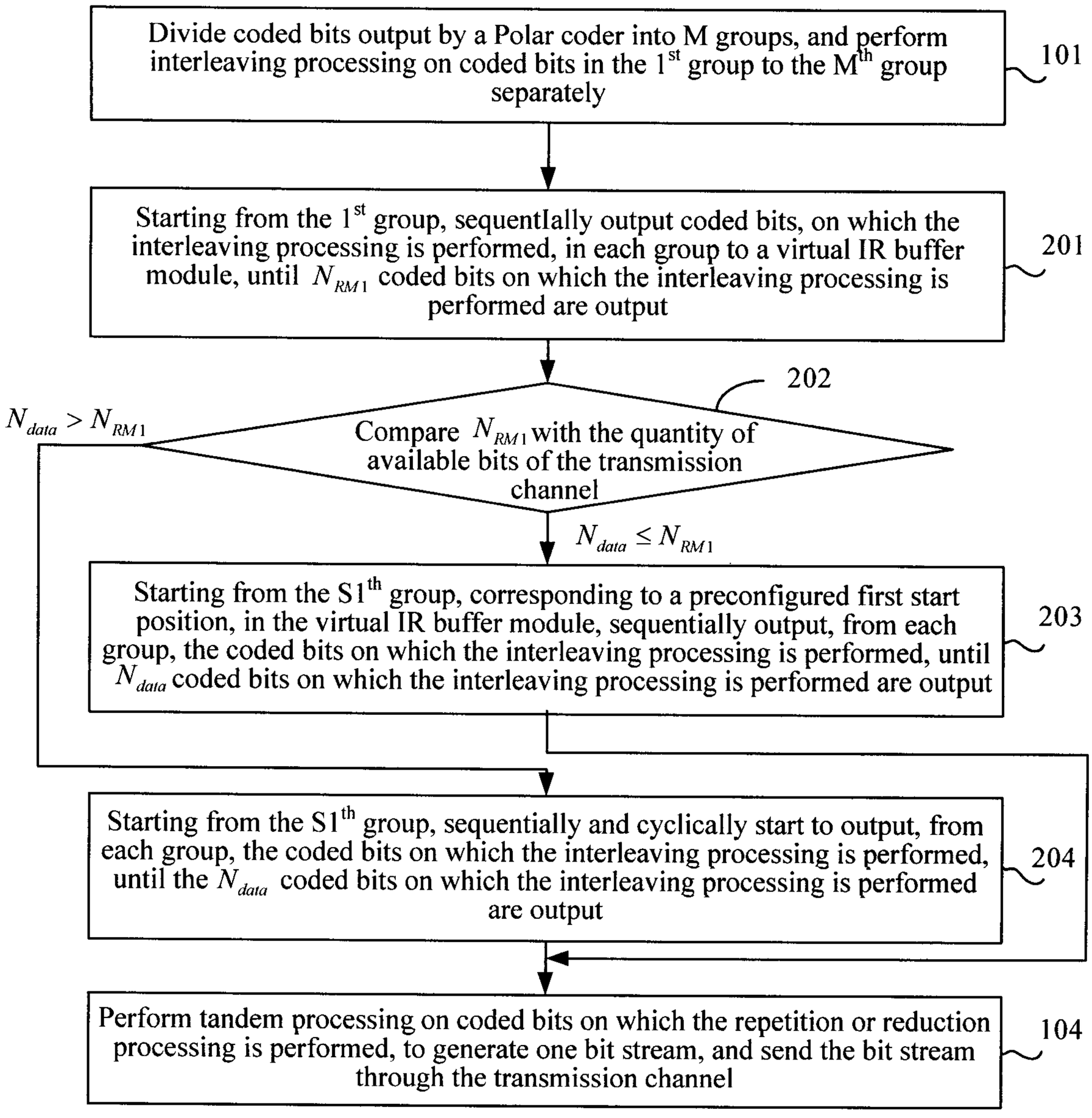
Divide coded bits output by a Polar coder into M groups, and perform interleaving processing on coded bits in the 1st group to the Mth group separately
101
Starting from the 1st group, sequentIally output coded bits, on which the interleaving processing is performed, in each group to a virtual IR buffer module, until N_{RM1} coded bits on which the interleaving processing is performed are output
201
202
$N_{data} > N_{RM1}$
Compare N_{RM1} with the quantity of available bits of the transmission channel
$N_{data} \leq N_{RM1}$
Starting from the S1th group, corresponding to a preconfigured first start position, in the virtual IR buffer module, sequentially output, from each group, the coded bits on which the interleaving processing is performed, until N_{data} coded bits on which the interleaving processing is performed are output
203
Starting from the S1th group, sequentially and cyclically start to output, from each group, the coded bits on which the interleaving processing is performed, until the N_{data} coded bits on which the interleaving processing is performed are output
204
Perform tandem processing on coded bits on which the repetition or reduction processing is performed, to generate one bit stream, and send the bit stream through the transmission channel
104

FIG. 2

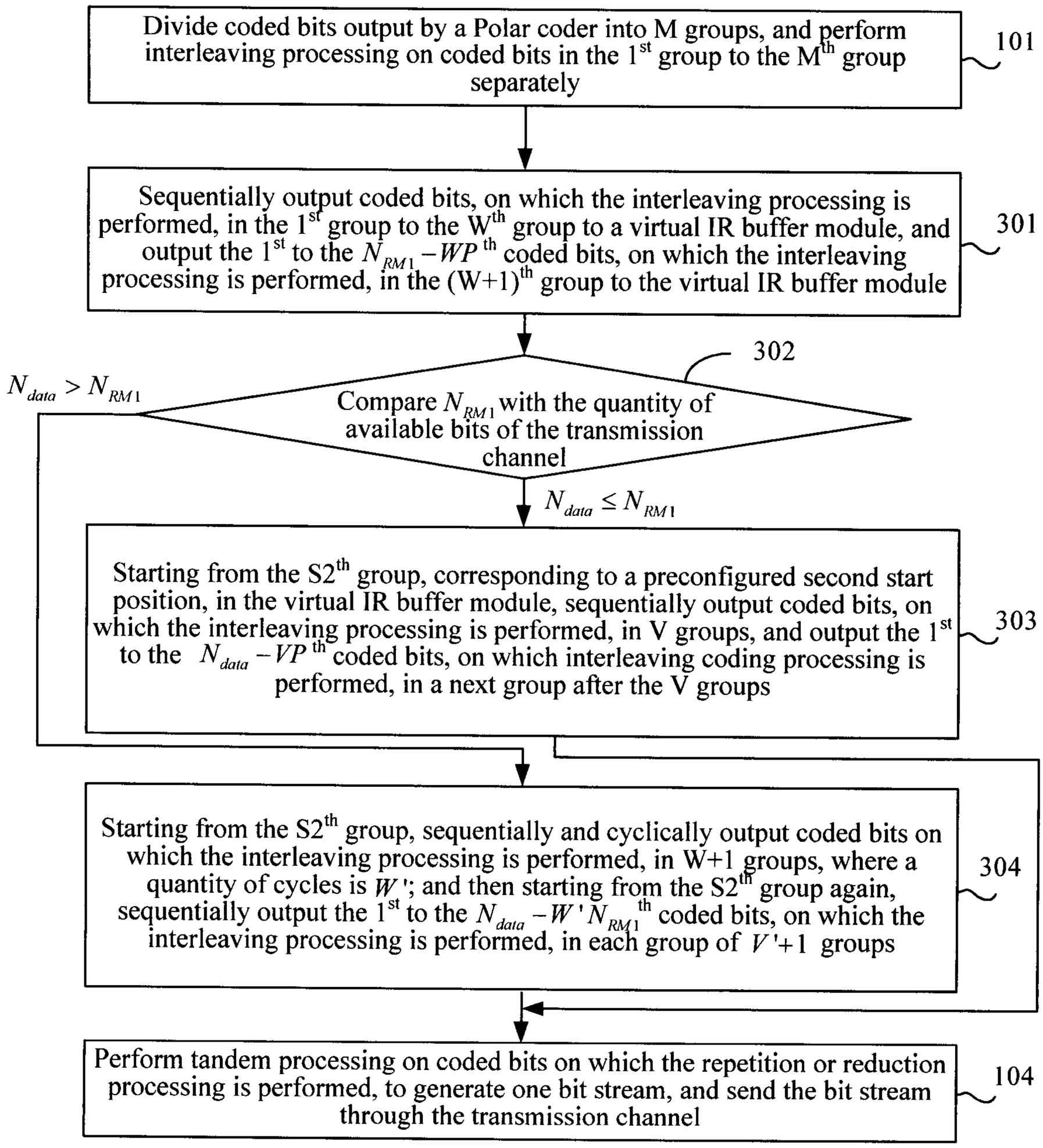
Divide coded bits output by a Polar coder into M groups, and perform interleaving processing on coded bits in the 1st group to the Mth group separately
101
Sequentially output coded bits, on which the interleaving processing is performed, in the 1st group to the Wth group to a virtual IR buffer module, and output the 1st to the $N_{RM1} - WP$ th coded bits, on which the interleaving processing is performed, in the (W+1)th group to the virtual IR buffer module
301
302
Compare N_{RM1} with the quantity of available bits of the transmission channel
$N_{data} > N_{RM1}$
$N_{data} \le N_{RM1}$
Starting from the S2th group, corresponding to a preconfigured second start position, in the virtual IR buffer module, sequentially output coded bits, on which the interleaving processing is performed, in V groups, and output the 1st to the $N_{data} - VP$ th coded bits, on which interleaving coding processing is performed, in a next group after the V groups
303
Starting from the S2th group, sequentially and cyclically output coded bits on which the interleaving processing is performed, in W+1 groups, where a quantity of cycles is W'; and then starting from the S2th group again, sequentially output the 1st to the $N_{data} - W' N_{RM1}$ th coded bits, on which the interleaving processing is performed, in each group of $V'+1$ groups
304
Perform tandem processing on coded bits on which the repetition or reduction processing is performed, to generate one bit stream, and send the bit stream through the transmission channel
104

FIG. 3

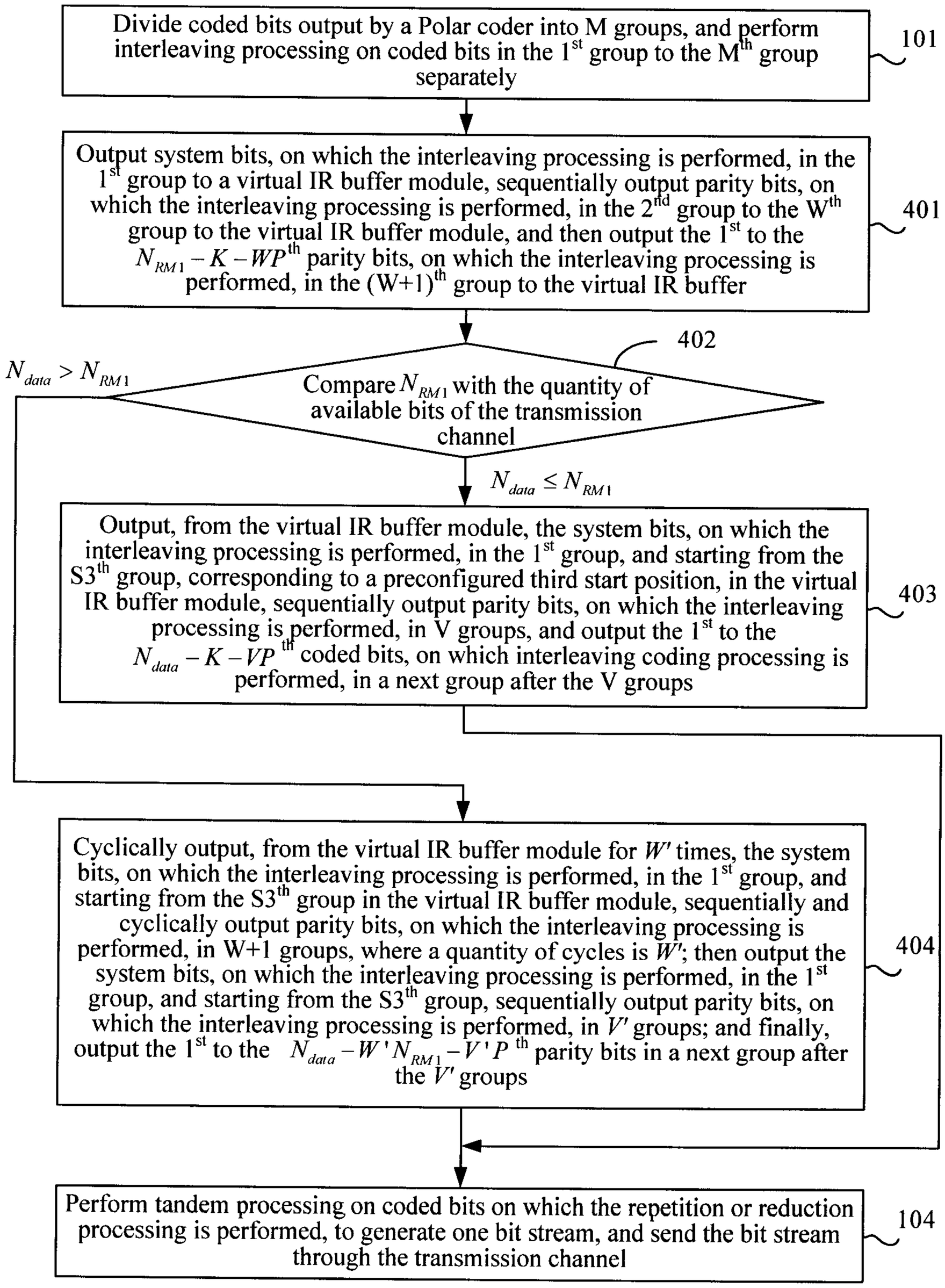
Divide coded bits output by a Polar coder into M groups, and perform interleaving processing on coded bits in the 1st group to the Mth group separately
101
Output system bits, on which the interleaving processing is performed, in the 1st group to a virtual IR buffer module, sequentially output parity bits, on which the interleaving processing is performed, in the 2nd group to the Wth group to the virtual IR buffer module, and then output the 1st to the $N_{RM1}-K-WP^{th}$ parity bits, on which the interleaving processing is performed, in the (W+1)th group to the virtual IR buffer
401
402
$N_{data} > N_{RM1}$
Compare N_{RM1} with the quantity of available bits of the transmission channel
$N_{data} \le N_{RM1}$
Output, from the virtual IR buffer module, the system bits, on which the interleaving processing is performed, in the 1st group, and starting from the S3th group, corresponding to a preconfigured third start position, in the virtual IR buffer module, sequentially output parity bits, on which the interleaving processing is performed, in V groups, and output the 1st to the $N_{data}-K-VP^{th}$ coded bits, on which interleaving coding processing is performed, in a next group after the V groups
403
Cyclically output, from the virtual IR buffer module for W' times, the system bits, on which the interleaving processing is performed, in the 1st group, and starting from the S3th group in the virtual IR buffer module, sequentially and cyclically output parity bits, on which the interleaving processing is performed, in W+1 groups, where a quantity of cycles is W'; then output the system bits, on which the interleaving processing is performed, in the 1st group, and starting from the S3th group, sequentially output parity bits, on which the interleaving processing is performed, in V' groups; and finally, output the 1st to the $N_{data}-W'N_{RM1}-V'P^{th}$ parity bits in a next group after the V' groups
404
Perform tandem processing on coded bits on which the repetition or reduction processing is performed, to generate one bit stream, and send the bit stream through the transmission channel
104

FIG. 4

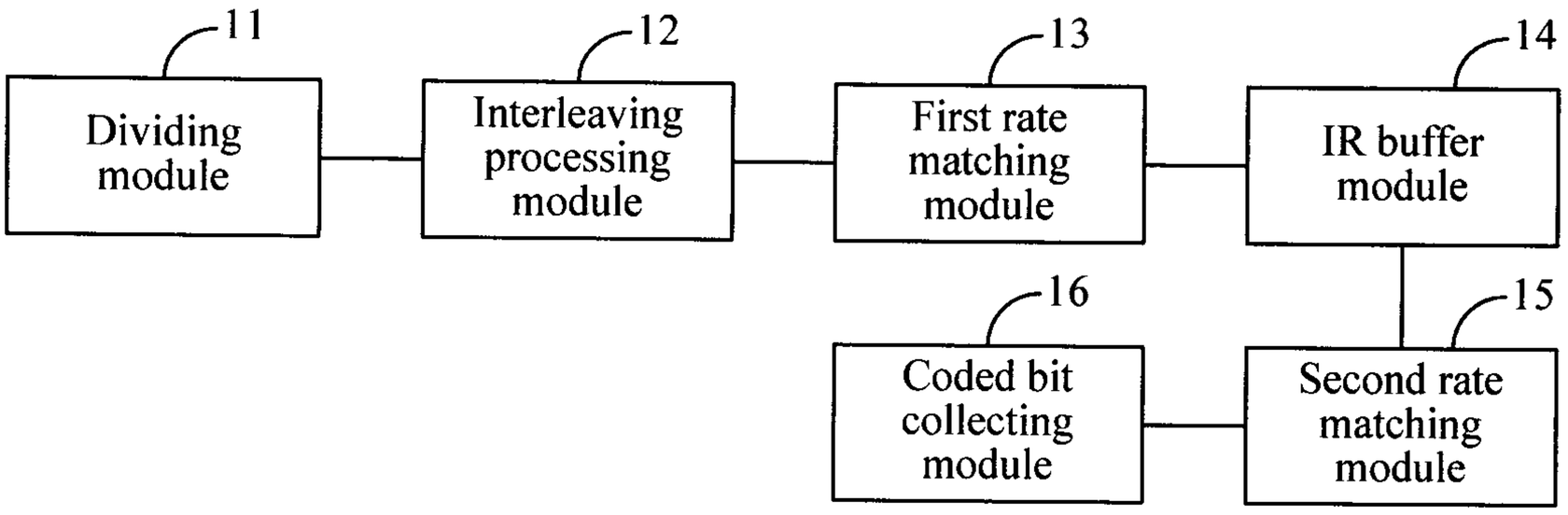
11
Dividing module
12
Interleaving processing module
13
First rate matching module
14
IR buffer module
16
Coded bit collecting module
15
Second rate matching module

FIG. 5

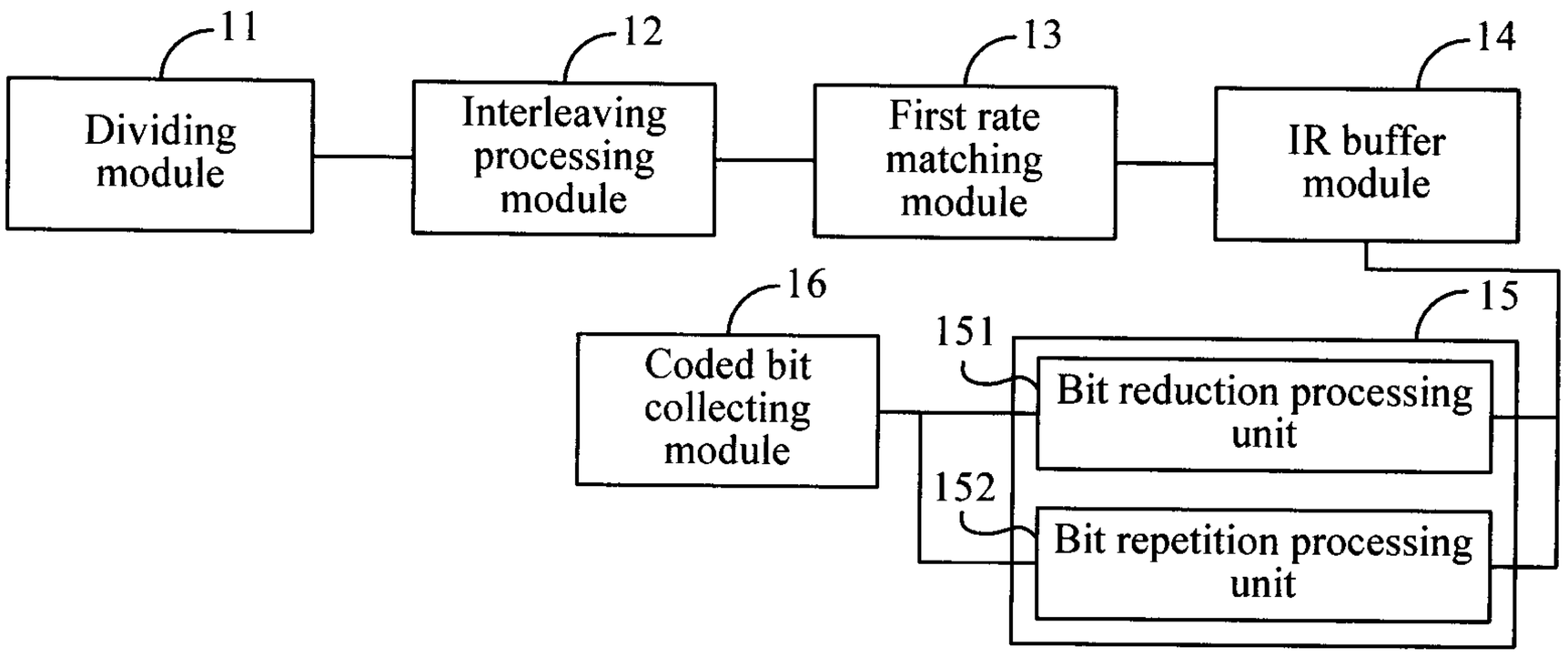
11
Dividing module
12
Interleaving processing module
13
First rate matching module
14
IR buffer module
16
Coded bit collecting module
15
151
Bit reduction processing unit
152
Bit repetition processing unit

FIG. 6

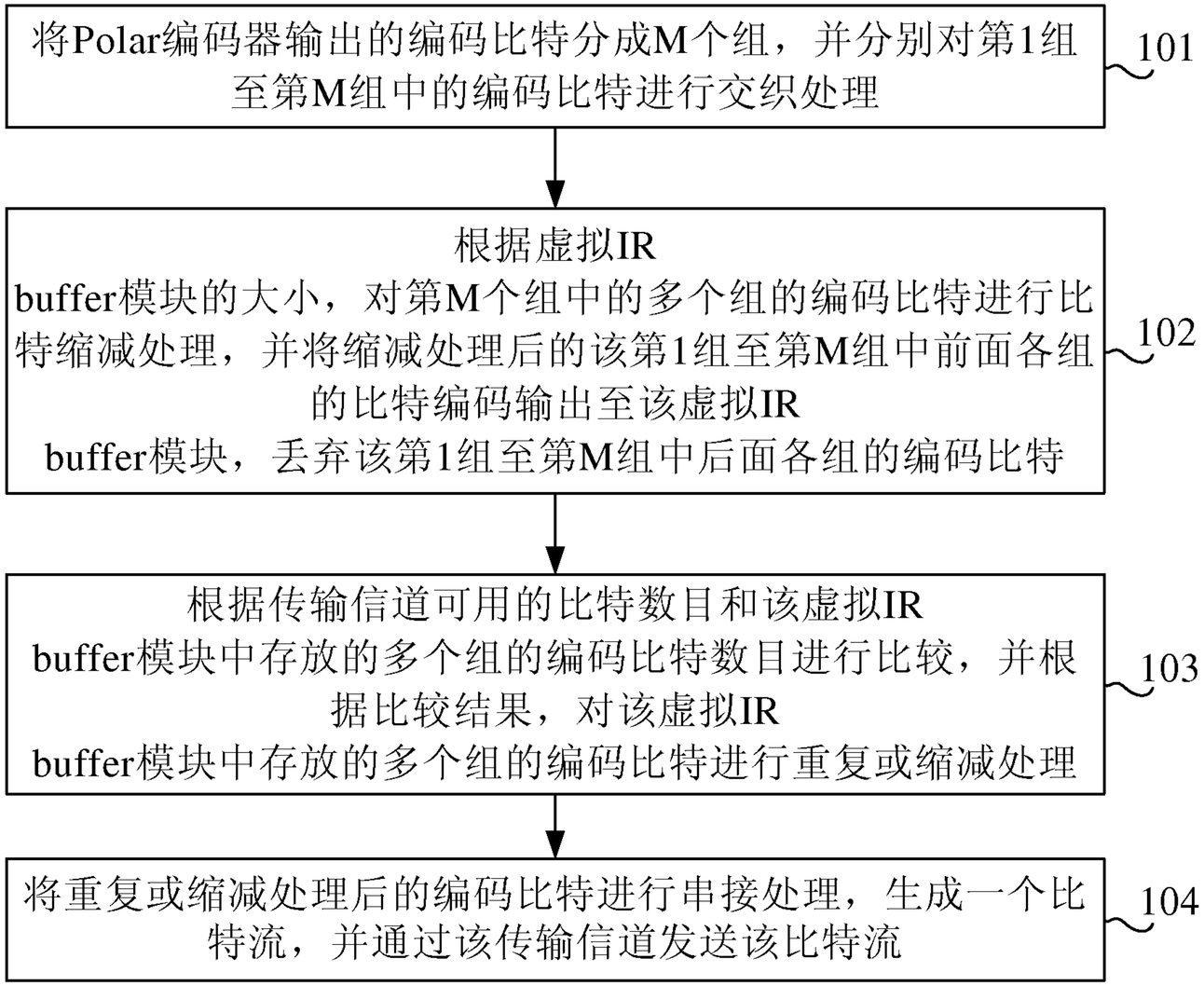

图 1 / FIG. 1

101 DIVIDING CODED BITS OUTPUTTED BY A POLAR ENCODER INTO M GROUPS AND CONDUCTING INTERLEAVE PROCESSING ON THE CODED BITS IN GROUP 1 TO GROUP M RESPECTIVELY

102 ACCORDING TO THE SIZE OF A VIRTUAL IR BUFFER MODULE, CONDUCTING BIT REDUCTION PROCESSING ON THE CODED BITS IN THE MULTIPLE GROUPS OF M GROUPS, AND OUTPUTTING REDUCED CODED BITS IN EACH OF THE FIRST GROUPS OF GROUP 1 TO GROUP M TO THE VIRTUAL IR BUFFER MODULE, AND DISCARDING THE CODED BITS OF THE LAST GROUPS OF GROUP 1 TO GROUP M

103 COMPARING THE NUMBER OF AVAILABLE BITS OF THE TRANSMISSION CHANNEL WITH THE NUMBER OF CODED BITS IN THE MULTIPLE GROUPS STORED IN THE VIRTUAL IR BUFFER MODULE; BASED ON THE COMPARISON RESULT, REPEATING OR REDUCING THE CODED BITS IN THE MULTIPLE GROUPS STORED IN THE VIRTUAL IR BUFFER MODULE

104 CONNECTING IN SERIES THE REPEATED OR REDUCED CODED BITS TO GENERATE A BIT STREAM, AND TRANSMITTING THE BIT STREAM OVER THE TRANSMISSION CHANNEL