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(54) **DOUBLE-SIDED CIRCUIT BOARD AND MULTI-CHIP PACKAGE INCLUDING SUCH A CIRCUIT BOARD AND METHOD FOR MANUFACTURE**

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(57) **ABSTRACT**

A multi-chip package includes a double-sided circuit board having first and second surfaces. Each surface has a package area and a peripheral area. Each package area has a chip mounting area on which a chip is attached, and a bonding area with which the chip is electrically connected. The peripheral area of the first surface has a runner area on which molding compound flows, and the peripheral area of the second surface has an external connection pattern with which the bonding areas are electrically connected. In particular, the circuit board has gate holes, which are co-located on each surface to result in a common hole.

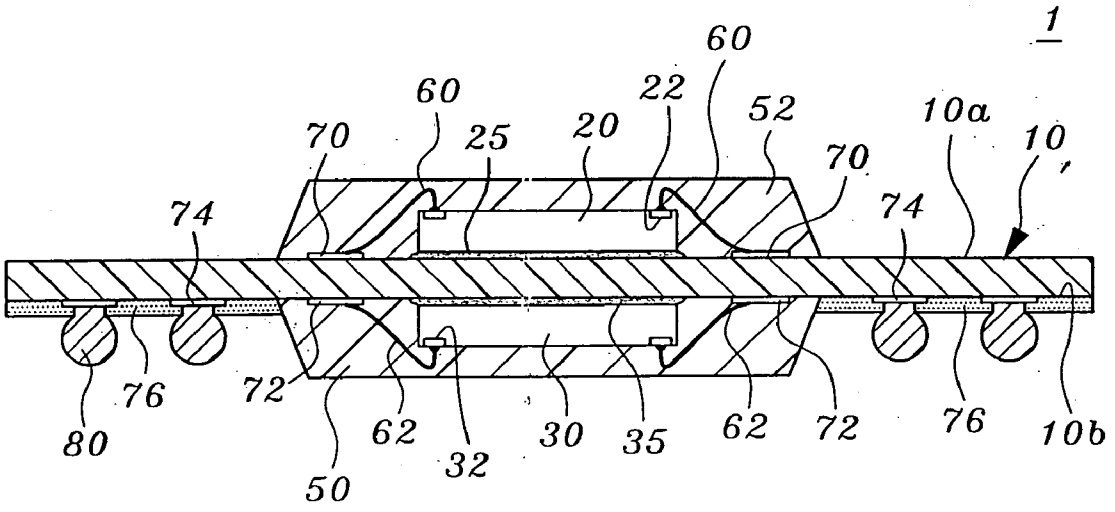


FIG. 1
(Prior Art)

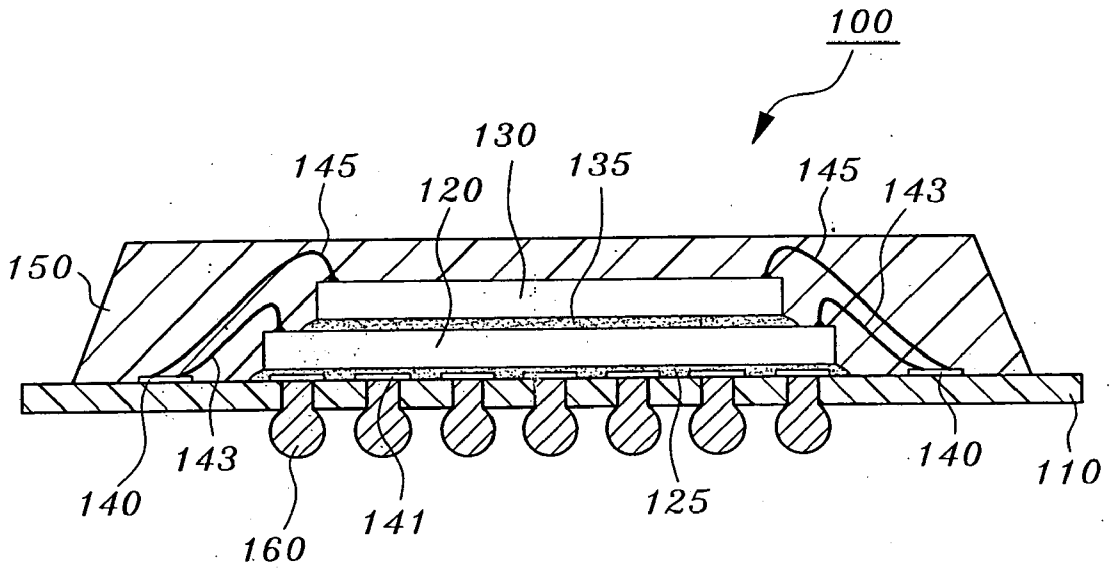


FIG. 2

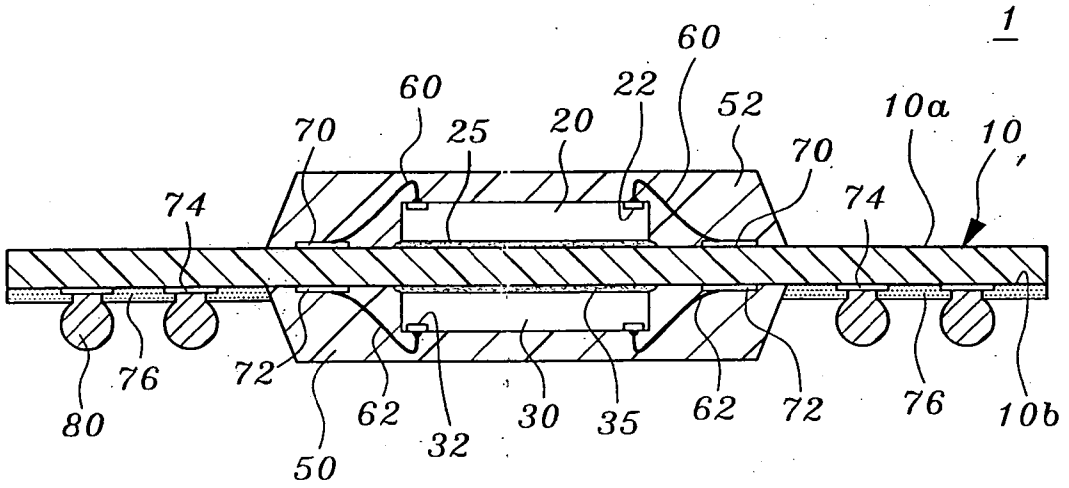

1
60
60
22
52
10a
10
70
25
20
70
74
74
76
72
62
30
35
62
72
76
80
32
50
10b

FIG. 3

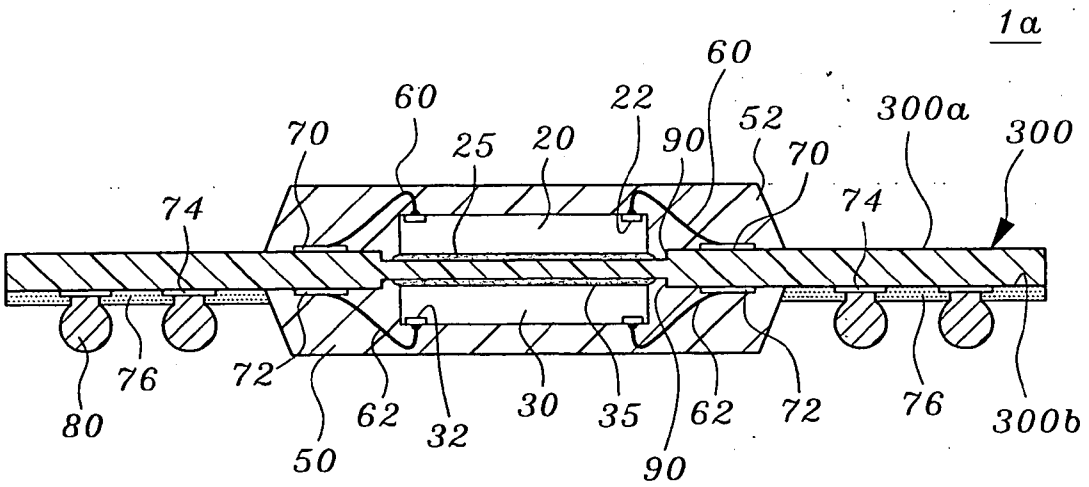

1a
60
60
22
300a
300
70
25
20
90
52
70
74
74
76
72
62
30
35
62
72
76
80
32
50
90
300b

FIG. 5

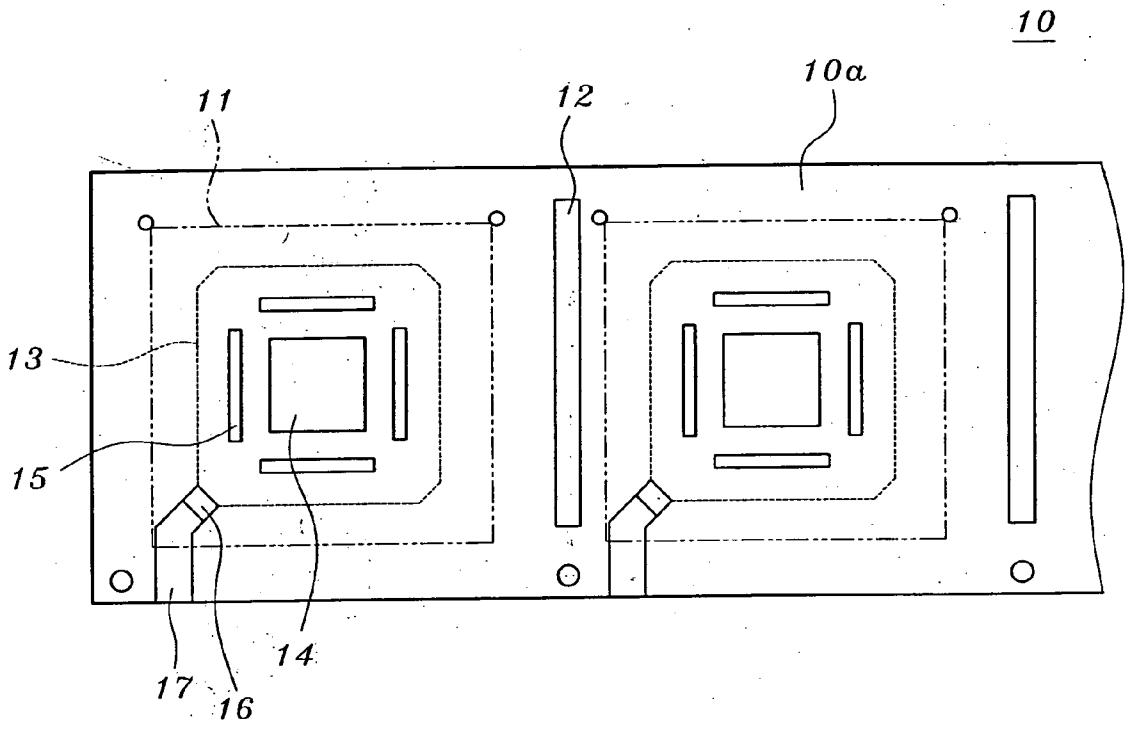

10
10a
11
12
13
15
14
17
16

FIG. 4

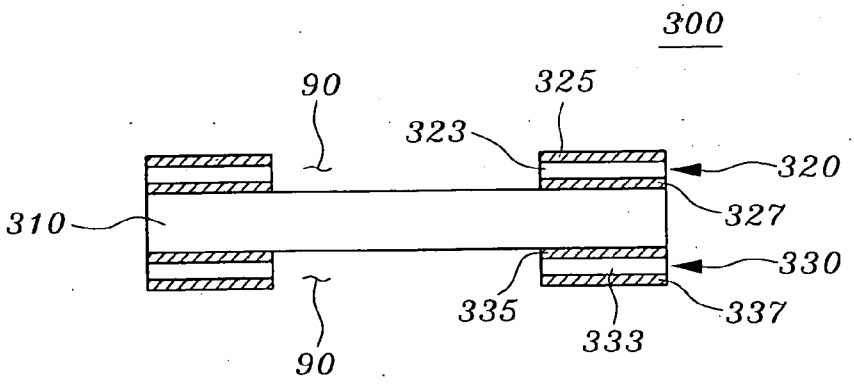

300
90
325
323
320
310
327
330
335
333
337
90

FIG. 6

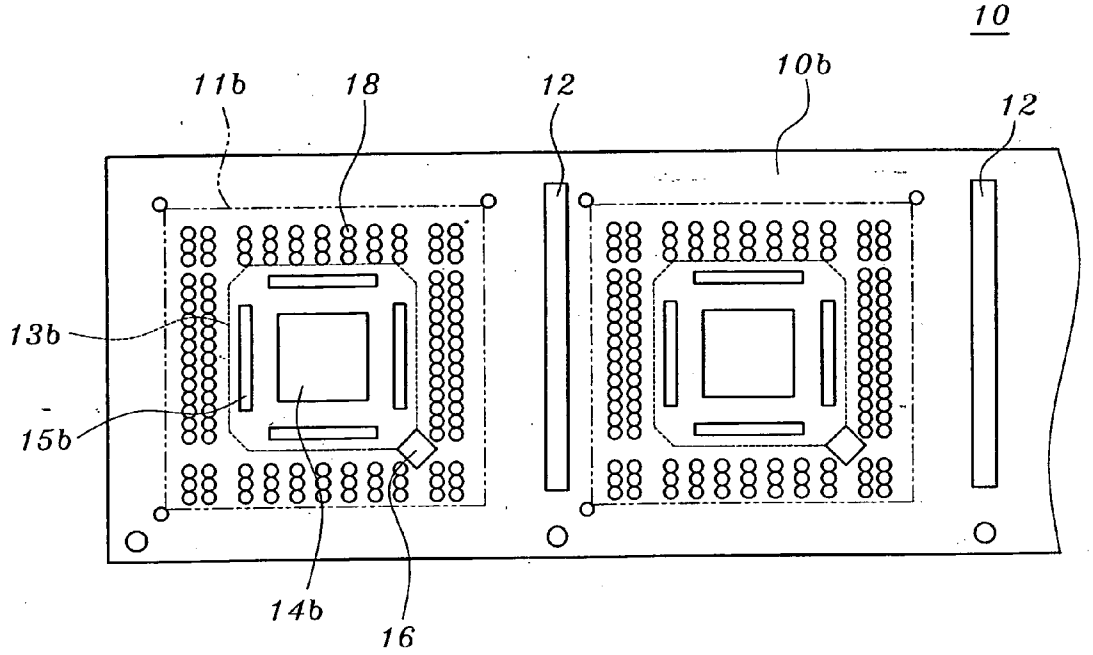

10
11b
18
12
10b
12
13b
15b
14b
16

FIG. 7α

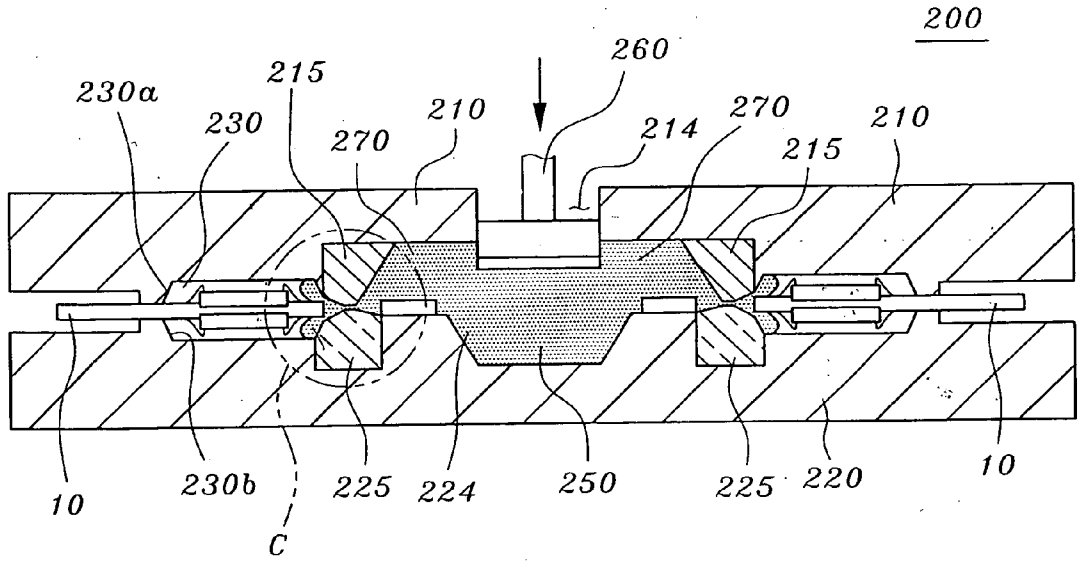

200
260
230α
215
230
210
270
214
270
215
210
10
230b
225
224
250
225
220
10
C

FIG. 7b

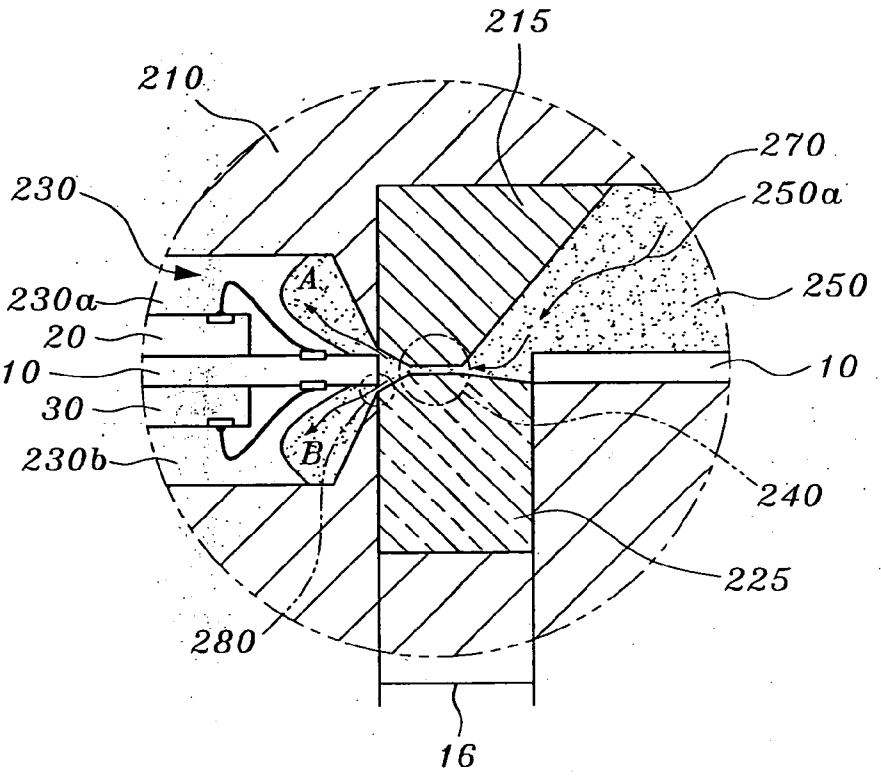

215
210
270
230
250a
230a
A
250
20
10
10
30
B
230b
240
225
280
16

FIG. 8a

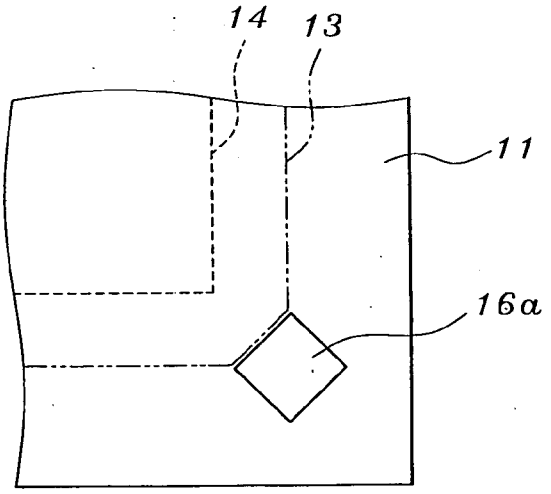

14
13
11
16a

FIG. 8b

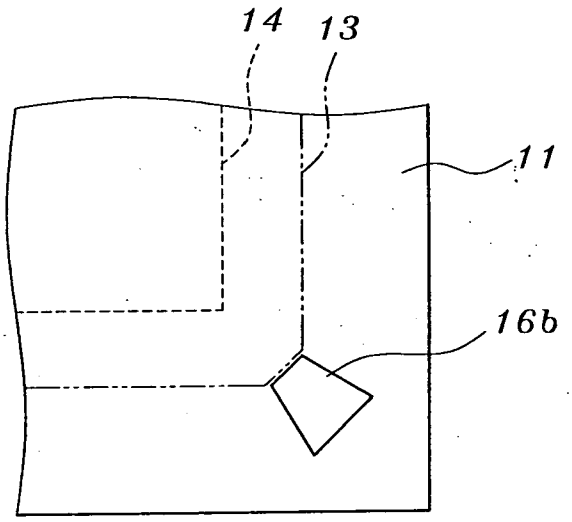


FIG. 8c

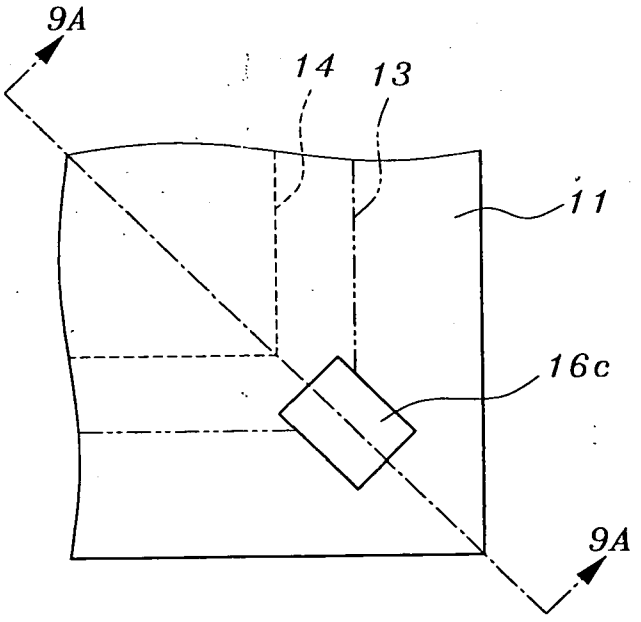


FIG. 9a

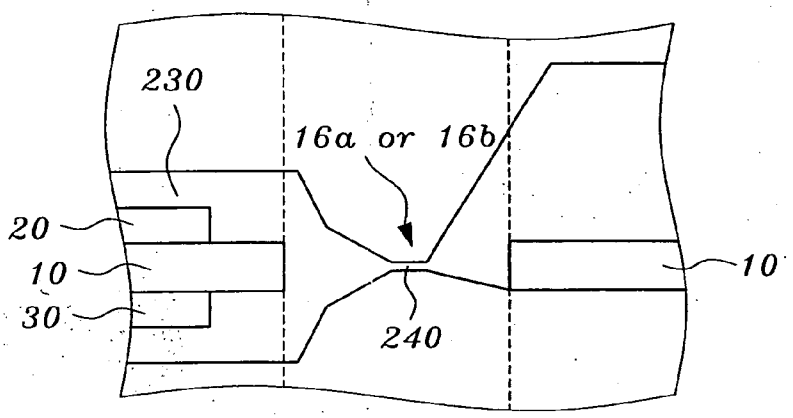
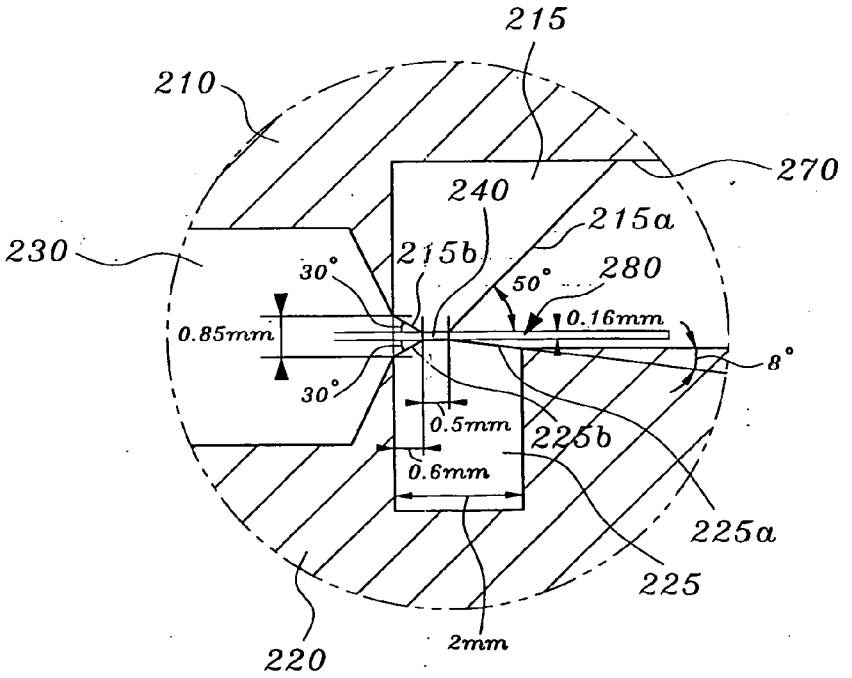

230
16a or 16b
20
10
30
240
10

FIG. 9b


215
210
270
240
215a
230
215b
30°
50°
280
0.16mm
0.85mm
8°
30°
0.5mm
225b
0.6mm
225a
225
220
2mm

DOUBLE-SIDED CIRCUIT BOARD AND MULTI-CHIP PACKAGE INCLUDING SUCH A CIRCUIT BOARD AND METHOD FOR MANUFACTURE

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a semiconductor chip packaging technique and more particularly to a double-sided circuit board and a multi-chip package including the circuit board.

[0003] 2. Description of the Related Art

[0004] Since recent trends in electronics development have been toward miniaturization and high performance, chips (integrated circuits) are more integrated. In addition, different types of chips need to be contained in a single package body, in order to achieve various semiconductor devices. In order to satisfy these pressing demands, a multi-chip packaging technique is applied.

[0005] FIG. **1** is a sectional view showing a conventional multi-chip package using a circuit board.

[0006] A conventional multi-chip package **100** is a fine-pitch ball grid array (FBGA). A first chip **120** is attached to a first surface of a circuit board **110**, and a second chip **130** is attached to the first chip **120** with an adhesive tape **135**. The first chip **120** and the second chip **130** are electrically connected to bonding pads **140** by bonding wires **143**, **145** which are formed on the circuit board **110**. The conventional FBGA multi-chip package **100** uses a chip stacking technique and a wire bonding technique.

[0007] The first and second chips **120**, **130** and the bonding wires **143**, **145** are protected by package body **150** of molding compound. A plurality of solder balls **160** is attached on the second surface of the circuit board **110**. The solder balls **160** are connected to solder ball pads **141**, which are formed on the first surface of the circuit board **110**, thereby electrically connecting the multi-chip package **100** with a mother-board or other electrical devices.

[0008] In the conventional multi-chip package **100**, adhesive tape **135**, which is used for attaching the second chip **130** to the first chip **120**, does not encroach upon the wire bonding area of the first chip **120**. Therefore, the second chip **130** must be smaller than the first chip **120**. Since the second chip **130** is distant from the bonding pads l**40** of the circuit board **110**, the bonding wire **145** must be formed in an almost straight-lined loop, so as to shorten the length of the bonding wires **145**. Accordingly, it requires an additional apparatus and technique for the wire bonding process.

SUMMARY OF THE INVENTION

[0009] The present invention provides a circuit board that embodies a multi-chip package without requiring necessarily a special wiring technique and apparatus.

[0010] Further, the present invention provides a multi-chip package that can easily be embodied regardless of the size of the chips and circuit board.

[0011] Additionally, the present invention provides a multi-chip package manufactured using wire bonding techniques and molding techniques which are used in conventional plastic packaging processes.

[0012] Also, the present invention provides a multi-chip package that has a thin width regardless of the stacked chips and the circuit board used in such multi-chip packages.

[0013] A multi-chip package according to the present invention provides chips mounted to two obverse sides of a circuit board. These chips may be mounted in recesses in the board. This mounting arrangement allows for chips of differing sizes to be mounted without the concerns raised by chip stacking methods. The chips may be mounted in package areas which have both a chip mounting area and a bonding area used to electrically connect a mounted chip to the circuit board. The circuit board may also have a peripheral area and may provide for a connection area which is used to connect the chip or chips to external devices or other electrical connections. The circuit board surfaces may have gate holes which are co-located on each surface to result in a through hole in the board.

[0014] The gate hole allows for the encapsulation of the chips in a molding compound to occur on both sides of the board in one molding process that uses a molding die over each of the two circuit board surfaces. The molding dice may enter the gate holes to some extent to form a gate neck which enhances the strength of the gate hole area after the molding process.

[0015] The circuit board according to the present invention supports the fabrication of the multi-chip package as described above.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] These and other objects, features and advantages of the present invention will be readily understood with reference to the following detailed description thereof provided in conjunction with the accompanying drawings, wherein like reference numerals designate like structural elements, and in which:

[0017] FIG. **1** is a sectional view showing a conventional multi-chip package using a circuit board;

[0018] FIG. **2** is a sectional view showing a multi-chip package using a double-sided circuit board according to one embodiment of the present invention;

[0019] FIG. **3** is a sectional view showing a multi-chip package using a double-sided circuit board according to another embodiment of the present invention;

[0020] FIG. **4** is a detailed sectional view showing the circuit board used in the multi-chip package of FIG. **3**;

[0021] FIG. **5** is a plan view showing the first surface of a double-sided circuit board according to one embodiment of the present invention;

[0022] FIG. **6** is a plan view showing the second surface of a double-sided circuit board according to one embodiment of the present invention;

[0023] FIG. **7***a* is a sectional view showing a molding die used in a molding process of the present invention;

[0024] FIG. **7***b* is a partially enlarged sectional view of a position C of the molding die of FIG. **7***a;*

[0025] FIGS. **8***a* to FIG. **8***c* are plan views showing examples of a gate hole formed on the circuit board of the present invention; and

[0026] FIGS. **9***a* and **9***b* are detailed sectional views of the molding die of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0027] Preferred embodiments of the present invention will be described below with reference to the accompanying drawings.

[0028] In some embodiments, as shown in FIG. **2** a multi-chip package is manufactured using a double-sided circuit board.

[0029] A multi-chip package **1** comprises a circuit board **10**, chips **20**, **30**, package bodies **50**, **52**, bonding wires **60**, **62** and solder balls **80**. The circuit board **10** has a first surface **10***a* and a lower surface **10***b*. Circuit board **10**, is a printed circuit board with dielectric layers and wiring patterns thereon in some embodiments. The dielectric layers may comprise FR-4 material and glass fiber and the wiring patterns are made of copper.

[0030] The first chip **20** is attached to the first surface **10***a* with an adhesive tape **25** and the second chip **30** is attached to the second surface **10***b* with an adhesive tape **35** or other methods. The same or different types of chips may be used. For example, the Flash memory and SRAM or logic IC and memory chip may both be in one multi-chip package. The adhesive tapes **25**, **35** may be silver filled epoxy compound adhesive. A substrate area to which the first and second chip **20**, **30** are attached, may be plated with nickel(Ni) and platinum(Pt) in order to increase the adhesion force. The electrode pads **22** of the first chip **20** are electrically connected with bonding pads **70** by wires **60**,**62**. Bonding pads**70** are formed on the first surface **10***a* of the circuit board **10**. The electrode pads **32** of the second chip **30** are also electrically connected with bonding pads **72**, which are formed on the second surface **30***b* of the circuit board **10**. The bonding pads **70**, **72** may be formed by photolithography using copper.

[0031] The first and second chip **20**, **30** and bonding wire **60**, **62** are sealed by package body **50**, **52** in order to protect them from external environmental stress. The package bodies **50**, **52** are made of epoxy molding compound (EMC) and are simultaneously formed by a transfer molding process (or an injection molding process) at the same time. This molding process is described below.

[0032] External connection pattern **74** is formed on the second surface **10***b* of the circuit board **10** and may serve as an electrical connection means for electrically connecting the multi-chip package **1** to an, external apparatus. The solder bump area **80** is formed on the external connection patterns **74**. The external connection patterns **74** are exposed from a solder mask **76** coated on the second surface **10***b* of the circuit board **10**. A solder ball is mounted on the exposed external connection patterns **74** and heated by reflow-soldering, thereby forming the solder bump area **80**.

[0033] Since the above-identified multi-chip package **1** of the first embodiment of the present invention comprises dies mounted on both surfaces of the circuit board **10**, multi-chip packages can be achieved regardless of the die size, Further, the multi-chip package **1** may be manufactured by using conventional wire bonding and injection molding techniques, thereby being able to achieve mass-production. Moreover since the chips are closer to the bonding pads, additional wire looping technique is not required.

[0034] FIG.**3** is a sectional view showing a multi-chip package using a double-sided circuit board according to another embodiment of the present invention.

[0035] The same elements are represented with the same reference numerals in both FIG. **2** and FIG. **3**.

[0036] As shown in FIG. **3**, the multi-chip package **1***a* has recess **90** on the first surface **300***a* and the second surface **300***b*. This recess **90** is located on both sides of the circuit board in some embodiments. The first and second chips **20**, **30** are mounted in recesses **90** by means of adhesive tape **25**, **35**.

[0037] With such an embodiment it is possible to decreases the total thickness of the package and to increase the reliability of bonding wires. The recess **90** is formed on the circuit board **300** of FIG. **4**.

[0038] FIG. **4** is a detailed section view showing a circuit board which is suited to be used in the manufacture of the multi-chip package of FIG. **3** according to one embodiment of the present invention.

[0039] Like a conventional circuit board, the circuit board **300** may comprise BT prepare **310** and a first and second BT CCL(Bisamaleimide-Triazine copper clad laminate) **320**, **330** attached to the upper and lower surface of the BT prepare. The first BT CCL **320** has copper foils **325**, **327**, which are attached to both sides of the BT compound **323**, and the second BT CCL **330** also has copper foils **335**, **337**, which are attached to both sides of the BT compound **333**. The first and second BT CCL **320**, **330** have the hole on the center. The hole, formed by a punching process, has the same size as the chip mounting area and becomes to the recess **90** on the circuit board **300**.

[0040] FIG. **5** is a plan view showing a first surface of a double-sided circuit board according to one embodiment of the present invention. FIG. **6** is a plan view showing a second surface of the double-sided mounting circuit board according to one embodiment of the present invention. The circuit boards in FIGS. **5** and **6** are an array type which is suitable for mass production of multi-chip packages.

[0041] The circuit board in the array type is separated into a plurality of unit circuit boards along to the slot **12**. An electrically conductive wiring pattern is formed on the circuit board **10** but the detailed configuration of the wiring pattern is omitted here. The wiring pattern varies according to the chip. The wiring patterns may be formed on the surfaces or the inside of the circuit board.

[0042] The package area **13** and the peripheral area **11** are formed on the first surface **10***a* of the circuit board **10**. The package area **13** comprises the chip mounting area **14** to which the chip is attached and the bonding area **15** connected to the chip by bonding wires. The bonding area **15** is a portion where the bonding pads **70** of FIGS. **2** and **3** are formed. On the other side, the gate hole **16** and the runner area **17** are formed on the peripheral area **11**. The gate hole **16** is formed on the boundary between the packaging area **13**

and the peripheral area **11**, and is a through-hole which passes through the first and second surface **10***a* and **10***b* of the circuit board **10**. The runner area **17** is formed on the gate hole **16**, the peripheral area **11** and the outer boundary of the circuit board **10**. This runner area **17** is a path for injecting the molten molding compound to form package body.

[**0043**] In some embodiments as shown in FIG. **6**, the package area **13***b* and the peripheral area **11***b* are formed on the second surface **10***b* of the circuit board **10**. The package area **13***b* comprises the chip mounting area **14***b* to which the chip is attached and the bonding area **15***b* connected to the chip by bonding wires. Outer connection patterns **18** are formed on the peripheral area **11***b* of the second surface **10***b* and serve to electrically connect the chips attached to the chip mounting area **14** and **14***b* of the first and second surface. For example, the outer connection pattern **18** may be a solder ball land or the external connection pattern **74** of FIGS. **2** and **3**.

[**0044**] The gate hole **16** passes through the circuit board **10**. Therefore, the molten molding compound coming from the runner area **17** of the first surface **10***a* is injected to the first and second surface **10***a*, **10***b* through the gate hole **16**.

[**0045**] FIG. **7***a* is a sectional view showing a molding die used in the molding process of the present invention and FIG. **7***b* is a partially enlarged sectional view of a position C of the molding die of FIG. **7***a*.

[**0046**] As shown in FIG. **7***a*, a molding die **200** comprises an upper molding die **210** and a lower molding die **220**. The circuit board comprising the upper and lower chips is interposed between the upper molding die **210** and lower molding die **220**. The upper molding die **210** encompasses concave area **230***a*. The lower molding die **220** encompasses concave area **230***b*. After closing the upper molding die **210** and the lower molding die **220**, the first and second chips **20**, **30** are kept in the cavity **230**. The cavity **230** is a space for forming the package body (**50**, **52** of FIG. **2**) and is surrounded by the concave areas **230***a*, **230***b*.

[**0047**] In some embodiments of the present invention a solid state pellet is positioned on a port **224** of the lower molding die **220**. Upper molding die **210** has a through hole **214** through which transfer ram **260** may pass. The runner **270** is formed between the port **224** and the cavity **230**.

[**0048**] In some embodiments of the present invention, the circuit board **10** is placed on the molding die **200** so that the second chip **30** is located in the concave area **230***b* of the lower molding die **220**. Pellet **250** is put on the post **224** and the upper molding die **210** is combined with the lower molding die **220**. The pellet **250** is compressed by descending the transfer ram **260**. At this time, the molten molding compound **250***a* is injected into the cavity **230** along the runner **270** by heating the molding die **200** and the pellet **250**.

[**0049**] The circuit board **10** has gate hole **16** which passes through the circuit board **10**. Therefore, the molten molding compound **250***a* is simultaneously injected into the concave areas **230***a*, **230***b* of the upper molding die **210** and the lower molding die **220** along the gate hole **16** (refer to the arrows "A" and "B" in FIG. **7***b*). The multi-chip package body formed on both the first and second surface of the circuit board **10** is made by one injection of molding compound. Preferably, the concave area **230***a* of the upper molding die **210** is symmetrical with the concave area **230***b* of the lower molding die **220**.

[**0050**] As shown in FIG. **7***b*, a gate neck **240** formed by the upper gate piece **215** of the upper molding die **210** and the lower gate piece **225** of the lower molding die **220** is located on the gate hole **16**. The gate neck **240** is a narrow pathway along which the molten molding compound **250***a* passes. Thereby, the molding compound of the runner area **270** can be easily removed after finishing the molding and adhesion force between the molding compound and the circuit board near the gate neck **240** does not decreased.

[**0051**] After completely filling the cavity **230** with the molten molding compound **250***a*, the molding compound **250***a* is cooled and hardened, the upper and lower molding die **210**, **220** are separated from each other. By cutting the circuit board **10** along the slot **12**, single multi-chip packages can be obtained.

[**0052**] Although FIG. **7***a* describes the molding die with two cavities, the molding die may comprise a plurality of cavities connected to radial runners. The number, arrangement and length of the runner **270** are determined by pressure and viscosity of the molten molding compound **250***a* and size of desired package body.

[**0053**] FIGS. **8***a* to FIG. **8***c* are plan views showing examples of a gate hole formed on the circuit board of the present invention. It is to be understood that other embodiments of the gate hole may be used.

[**0054**] The gate hole **16** can be embodied in various figures on the circuit board **10**, **300**. For example, the gate hole can be formed, in a plan view, into a square-shaped gate hole **16***a* as shown in FIG. **8***a* or a trapezoid-shaped gate hole **16***b* as shown in FIG. **8***b*. Alternatively, the gate hole in the peripheral area **11** can be extended to the package area **13** as designated by reference number **16***c* of FIG. **8***c*.

[**0055**] In order to facilitate the removal of the molded package body at the gate **280** without the adhesion force between the molded package body and the circuit board, the trapezoid shaped gate hole **16***b* may be used. Because the gate hole **16***b* has a gate with a narrow width and a small dimension, a gate neck may not be required.

[**0056**] In the case of the square shaped gate hole **16***a*, **16***c*, the molten molding compound **250***a* can easily flow because the width of the gate **280** is broad and the dimension of the gate **280** is large. As shown in FIG. **9***a*, the gate neck **240** is formed within the gate hole **16***a*, **16***c*. Therefore, the molding body of the runner area can be easily removed and the adhesion force between the molding body and the circuit board does not decrease in the gate area. Particularly, the extended gate hole **16***c* of the square type increases the flowing ability of the molten molding compound **250***a* passed through gate neck **240** into cavity **230**.

[**0057**] FIG. **9***b* is an enlarged sectional view of FIG. **9***a*. In this particular embodiment the gate has a length of the gate is 2 mm.

[**0058**] The upper gate piece **215** comprises a first incline **215***a* and a second incline **215***b*. The first incline **215***a* is connected to the runner **270** and the second incline **215***b* is connected to the cavity **230**. The first incline **215***a* and the second incline **215***b* form the upper surface of the gate. The

lower gate piece **225** comprises a third incline **225***a* and a forth incline **225***b*. The third incline **225***a* is connected to the runner **270** and the forth incline **225***b* is connected to the cavity **230**. The second incline **225***a* and the forth incline **225***b* form the second surface of the gate. The length of the gate neck **240** is 0.5 mm and the height of the gate neck **240** is 0.16 mm. The distance from the gate neck **240** to the cavity **230** is 0.6 mm. The dimension of the cavity **230** is 0.85 mm and the horizontal angle for the second and forth inclines **215***b*, **225***b* is 30 degrees. The horizontal angle for the first incline **215***a* is 50 degrees and the horizontal angle for the third incline **225***a* is 8 degrees.

[**0059**] In some embodiments of the present invention, a multi-chip package having a package body on both surfaces of the circuit board is manufactured by a wire bonding technique and an injection molding technique using conventional plastic package fabrication processes.

[**0060**] Since the package body is formed on both sides of the circuit board by one molding step, the productivity of manufacture of the multi-chip package can be increased.

[**0061**] Further, the multi-chip package of the present invention having the double dies may be thinner than conventional packages.

[**0062**] According to the present invention, mass production of the multi-chip package can be performed without any additional wire looping technique.

[**0063**] According to the present invention, the multi-chip package may use various chips.

[**0064**] Embodiments listed above illustrate, but do not limit, the invention. Although the present invention has been described in detail herein above with respect to the preferred embodiments thereof many variations and/or modifications thereof will be apparent to those of ordinary skill in the art. Therefore, all such variations and modifications are seen to fall within the true spirit and scope of the present invention as defined by the appended claims.

What is claimed is:

1-22. (canceled)

23. A method of manufacturing a multi-chip package, comprising:

providing a circuit board between an upper molding die and a lower molding die, the circuit board including a first surface having a first chip mounted and electrically connected thereto, a second surface having a second chip mounted and electrically connected thereto, and a gate hole formed from the first surface to the second surface, wherein the second surface faces the lower molding die;

closing the molding dies to form a cavity in which the chips are kept; and

injecting molding compound into the cavity, wherein the molding compound flows through the gate hole to encase portions of the first surface and the second surface.

24. The method of claim 23, further comprising:

compressing a molding pellet into a through hole in the upper molding die.

25. The method of claim 23, wherein the upper molding die and the lower molding die combine to form a gate neck located in the gate hole.

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