United States Patent [19]

Takahashi et al.

[11] **Patent Number: 5,003,358**

[45] **Date of Patent: Mar. 26, 1991**

[54] **SEMICONDUCTOR LIGHT EMITTING DEVICE DISPOSED IN AN INSULATING SUBSTRATE**

[75] Inventors: **Shogo Takahashi; Etsuji Omura,** both of Itami, Japan

[73] Assignee: **Mitsubishi Denki Kabushiki Kaisha,** Japan

[21] Appl. No.: **227,124**

[22] Filed: **Aug. 2, 1988**

[30] **Foreign Application Priority Data**

Aug. 5, 1987 [JP] Japan 62-196821

[51] **Int. Cl.**^{5} **H01L 27/15;** H01S 3/18

[52] **U.S. Cl.** **357/17;** 357/30; 357/16; 357/55

[58] **Field of Search** 357/17, 16, 30, 55; 437/129; 350/96.12; 372/48, 47

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,575,852	3/1986	Fujimoto et al.	357/17
4,608,695	8/1986	Oda et al.	357/17
4,644,552	2/1987	Ohshima et al.	357/17
4,675,710	6/1987	Ishikawa et al.	372/48
4,692,206	9/1987	Kaneiwa et al.	357/17
4,723,251	2/1988	Sakakibara et al.	357/17
4,725,112	2/1988	Bridges et al.	350/96.12
4,740,976	4/1988	Kajimura et al.	357/17
4,766,093	8/1988	Hovel et al.	437/129
4,779,281	10/1988	Naka et al.	357/17
4,779,283	10/1988	Ohnaka et al.	357/17
4,788,159	11/1988	Smith	437/129
4,799,227	1/1989	Kaneiwa et al.	357/17
4,801,993	1/1989	Ankri et al.	357/17
4,815,083	3/1989	Sugou et al.	357/17

FOREIGN PATENT DOCUMENTS

0030775	3/1981	Japan	357/17
0071987	6/1981	Japan	372/47
0135994	10/1981	Japan	357/17
0030385	2/1982	Japan	357/17
0162483	10/1982	Japan	357/17
0012389	1/1983	Japan	372/47
0204587	11/1983	Japan	372/48
0108382	6/1984	Japan	357/17
59-202676	11/1984	Japan .	
61-244082	10/1986	Japan .	
62-52985	3/1987	Japan .	
62-72185	4/1987	Japan .	

OTHER PUBLICATIONS

"1.55 μm InGaAsP P-Substrate Buried Crescent Laser Diode", Kakimoto et al, First Optoelectronics Conference (OEC '86) Technical Digest, Jul. 1986, Tokyo.

Primary Examiner—Andrew J. James
Assistant Examiner—Viet Q. Nguyen
Attorney, Agent, or Firm—Leydig, Voit & Mayer

[57] **ABSTRACT**

A semiconductor light emitting device includes a vertical aperture produced at a main surface of a semi-insulating or insulating substrate, a transverse aperture provided in the substrate communicating with the vertical aperture, a conducting semiconductor layer buried in the vertical aperture and the transverse aperture, a groove produced by etching the substrate from the surface thereof until reaching the conducting semiconductor layer at a portion of the transverse aperture, and a light emitting element produced in the groove, and the light emitting region of the element being buried in the groove and connected with the buried conducting semiconductor layer. Accordingly, no pn junction exists at the periphery of the light emitting region, and a semiconductor light emitting element of quite low parasitic capacitance is obtained at high yield. A planar structure in which two electrodes are produced at the same plane is obtained, resulting in ease of integration and enhancement of the integration density.

8 Claims, 6 Drawing Sheets

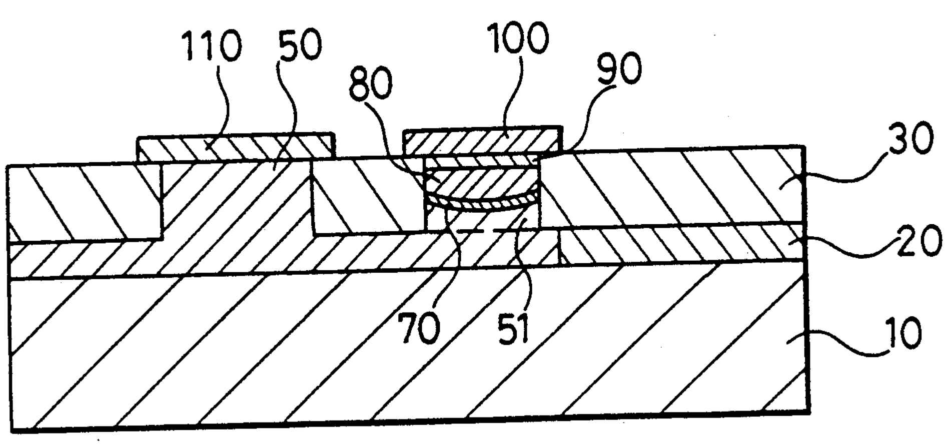


FIG. 1(a).

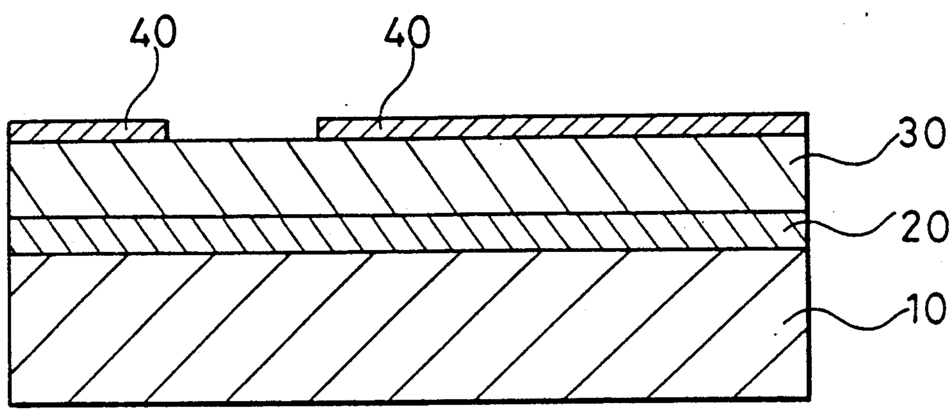


FIG. 1(b).

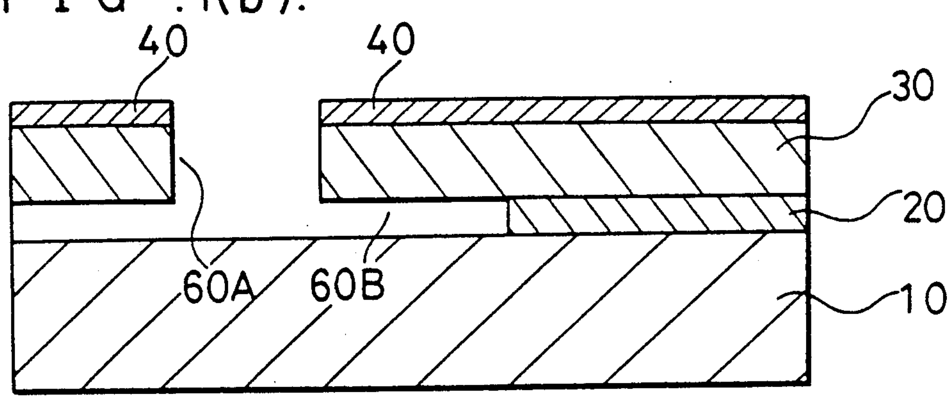


FIG. 1(c).

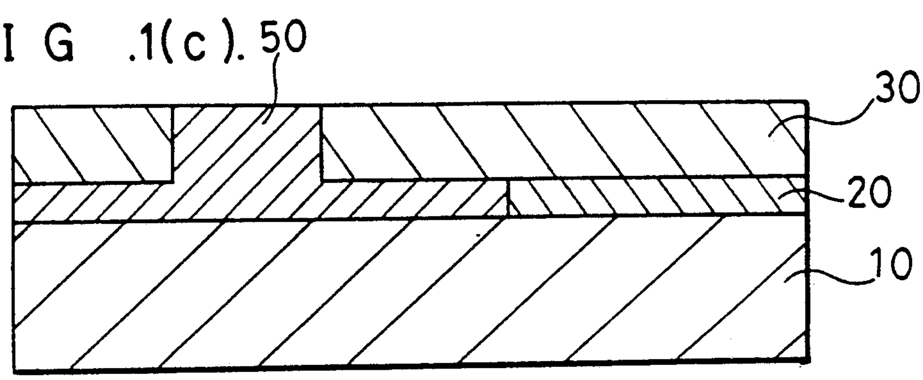


FIG.1(d).

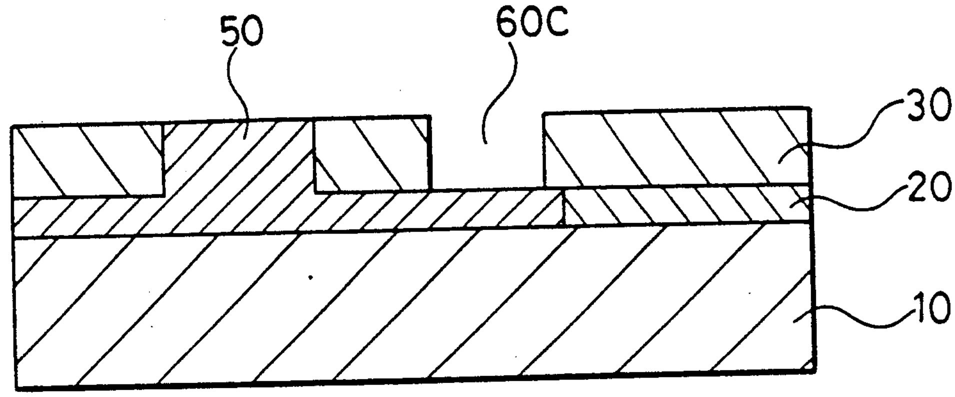


FIG.1(e).

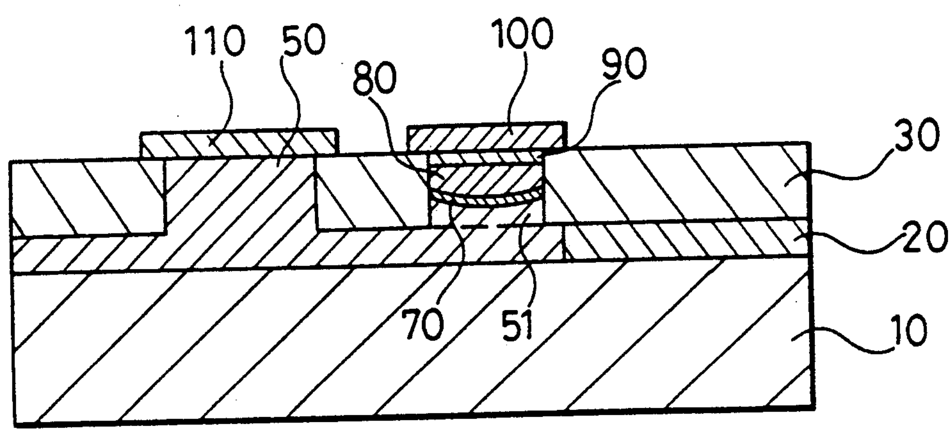


FIG. 2.

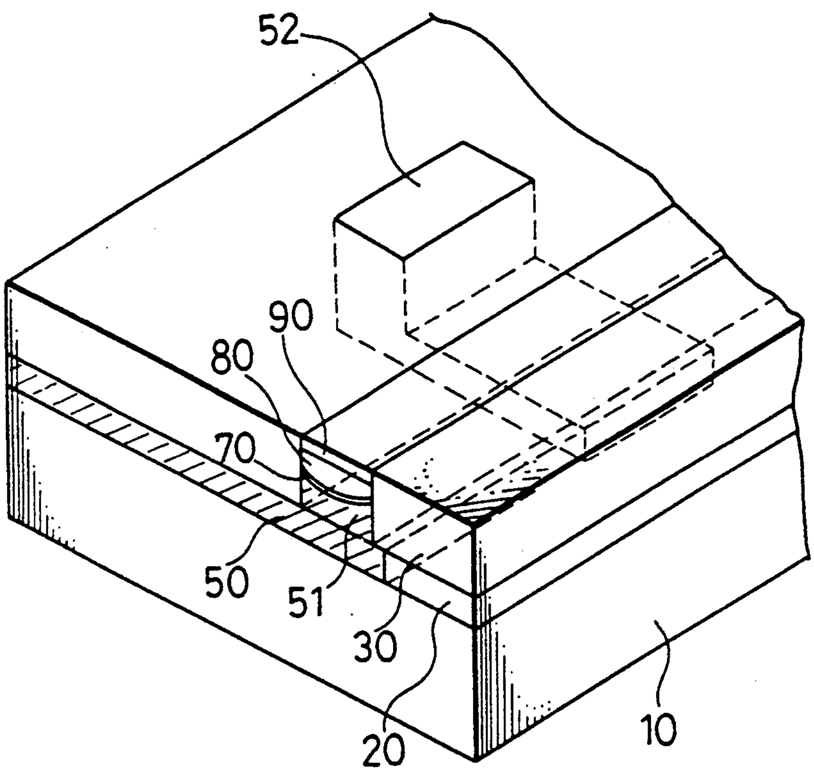


FIG. 3(a).

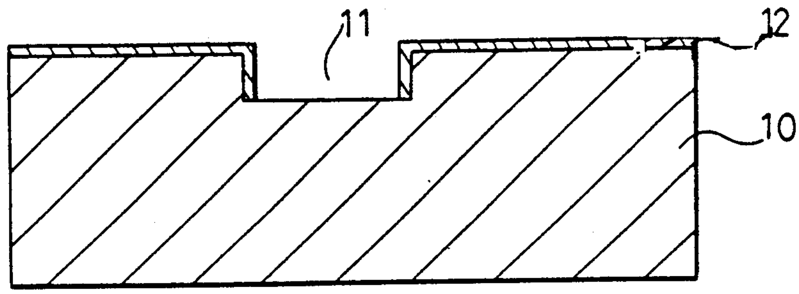


FIG. 3(b).

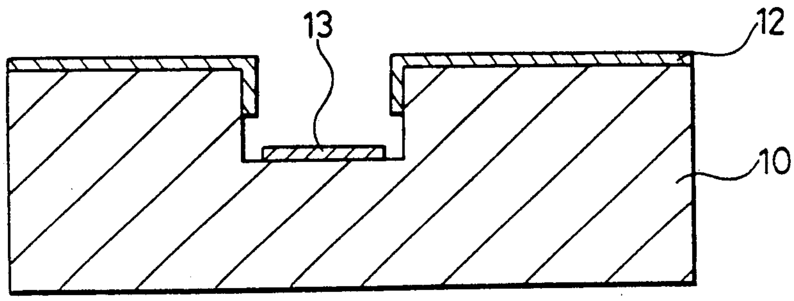


FIG. 3(c).

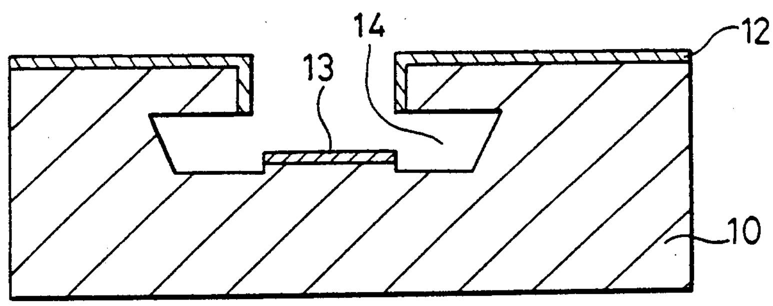


FIG. 3(d).

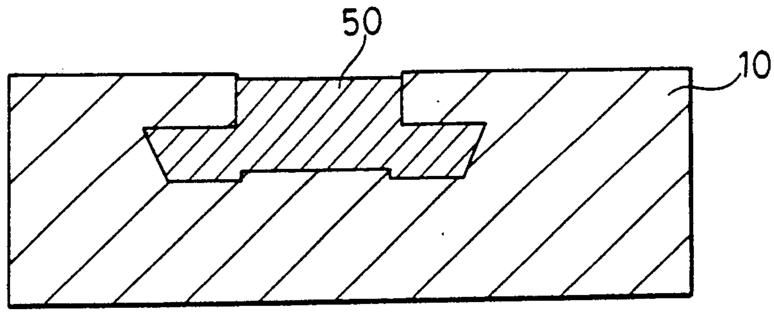
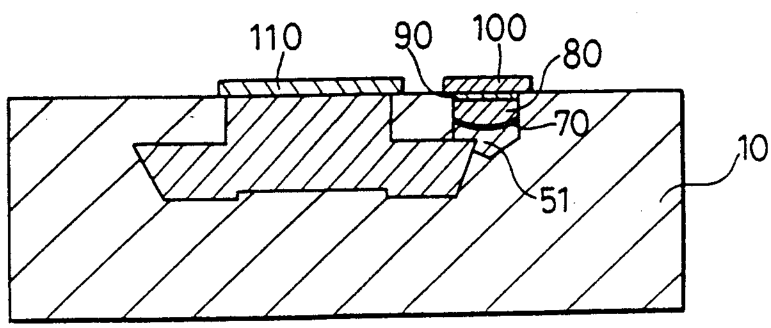
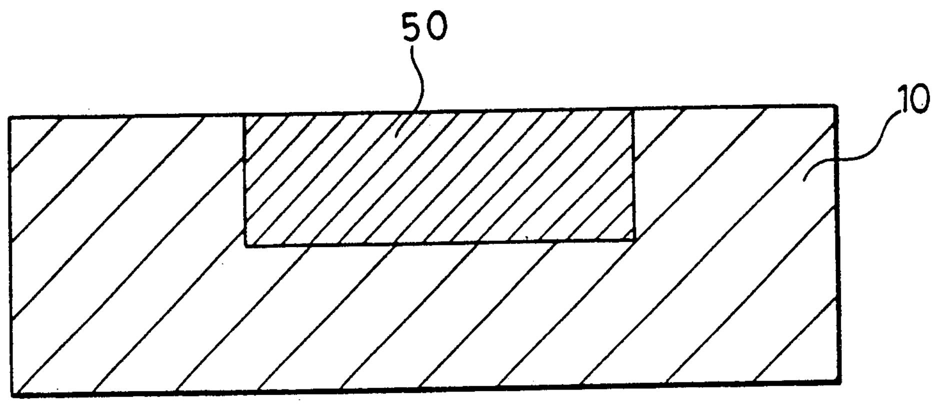


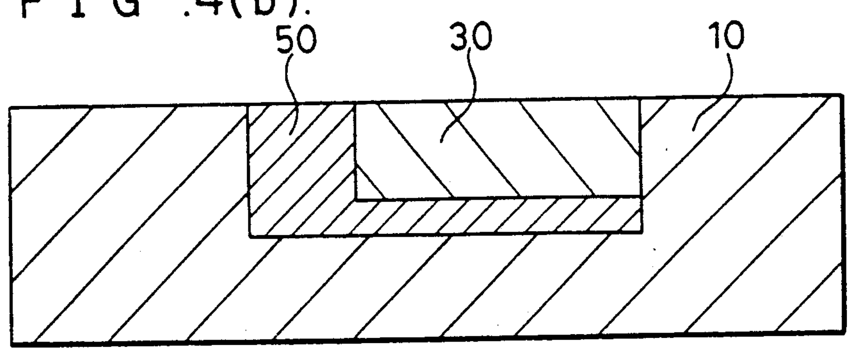
FIG. 3(e).



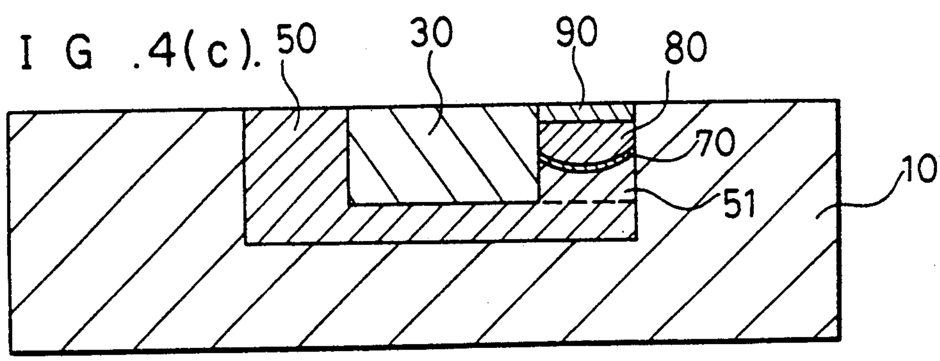
F I G .4(a).



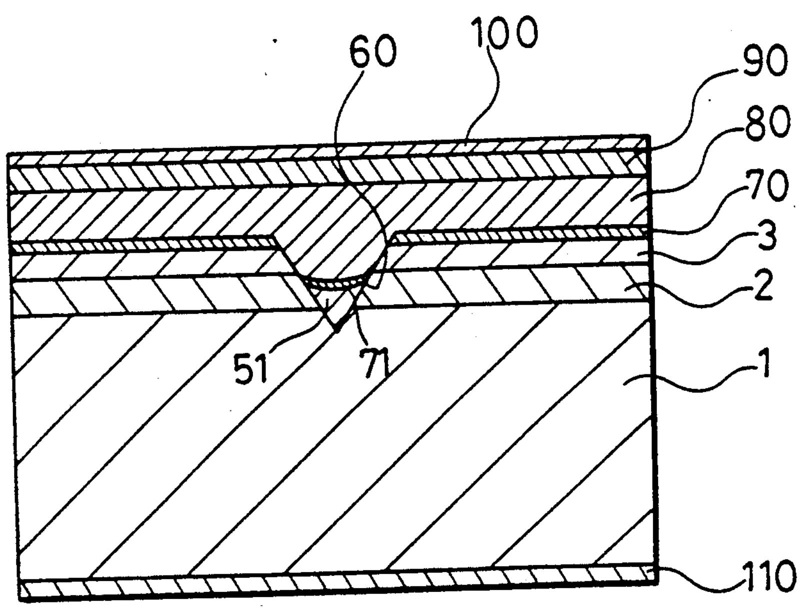
F I G .4(b).



F I G .4(c).



F I G .5. (PRIOR ART)



SEMICONDUCTOR LIGHT EMITTING DEVICE DISPOSED IN AN INSULATING SUBSTRATE

FIELD OF THE INVENTION

The present invention relates to a semiconductor light emitting device having an enhanced in operation speed and integration density.

BACKGROUND OF THE INVENTION

FIG. **5** shows a prior art buried type semiconductor laser as a semiconductor light emitting device.

As illustrated in FIG. **5**, a prior art buried type semiconductor laser starts with an n-type InP substrate **1**. A p-type InP blocking layer **2**, an n-type InP blocking layer **3**, and an InGaAsP active layer **70** are successively grown on the n-type InP substrate **1** by such as liquid phase epitaxy. A V-shaped groove **60** is produced through three layers **70**, **3**, and **2** so as to reach into the substrate **1** such as by etching. An n-type InP cladding layer **51** is buried in the V-shaped groove **60** and an InGaAsP active layer **71** is produced on the n-type InP cladding layer **51**. A p-type InP cladding layer **80** is grown on the InGaAsP active layer **71** in the groove **60** and on the InGaAsP active layer **70** outside the groove **60** and the surface thereof is made flat. A p-type InGaAsP contact layer **90** is produced on the p-type InP cladding layer **80**. A p side electrode **100** is provided on the p-type InGaAsP contact layer **90** and an n side electrode **110** is provided on the n-type InP substrate **1**.

The device operates as follows.

When a voltage is applied between the p side electrode **100** and the n side electrode **110** a current flows only through the V-shaped groove **60** which is between the p-type InP blocking layer **2** the n-type InP blocking layer **3**, and the current stimulates emission of laser light at the InGaAsP active layer **71** buried in the V-shaped groove **60**.

In this prior art buried type layer of such a construction, the position control of the InGaAsP active layer **71** in the V-shaped groove **60** is difficult because of the shape of the groove. Further, due to pn junctions existing at the periphery of the V-shaped groove the parasitic capacitance is a large valve resulting in leakage current and limitation of response speed. In addition, since the p side electrode **100** and the n side electrode **110** are produced at opposing surfaces of the n-type InP substrate **1**, the device with other electronic elements.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a semiconductor light emitting device with reduced critically in controlling the position of the active layer and preventing leakage current.

Another object of the present invention is to provide a semiconductor light emitting device having reduced parasitic capacitance and improved high speed response.

Still another object of the present invention is to provide such a device with a planar structure enhance integration density.

Yet another object of the present invention is to provide a method for producing such a device.

Other objects and advantages of the present invention will become apparent from the detailed description given hereinafter; it should be understood, however, that the detailed description and specific embodiment are given by way of illustration only, since various

changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from this detailed description.

According to the present invention, there is provided a semiconductor light emitting device comprising a vertical aperture produced at the main surface of a semi-insulating or insulating substrate, a transverse aperture communicated with the vertical aperture, a conducting semiconductor layer buried in the vertical aperture and the transverse aperture, a groove produced by etching the semi-insulating or insulating substrate from the surface thereof to one end portion of the transverse aperture, a light emitting element produced in the groove, including a light emitting region buried in the groove. Thus, the light emitting region is buried in the substrate, thereby making the current confinement complete. Further, since there is no pn junction at the periphery of the light emitting element, parasitic capacitances are gone. Furthermore, since one of two electrodes is taken to the surface of the substrate through the semiconductor layer buried in the transverse aperture, a planar structure is obtained.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1**(*a*) to **1**(*e*) are cross-sectional views illustrating a production process of a semiconductor light emitting device according to an embodiment of the present invention;

FIG. **2** is a perspective view showing a semiconductor light emitting device according to an embodiment of the present invention;

FIGS **3**(*a*) to **3**(*e*) are cross-sectional views illustrating a production process of a semiconductor light emitting device according to another embodiment of the present invention;

FIGS. **4**(*a*) to **4**(*c*) are cross-sectional views illustrating a production process of a semiconductor light emitting device according to still another embodiment of the present invention; and

FIG. **5** is a cross sectional view showing a prior art semiconductor light emitting device.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

An embodiment of the present invention will be described in detail with reference to the drawings.

FIGS. **1**(*a*) to **1**(*e*) show a production process of a semiconductor light emitting device according to an embodiment of the present invention. In FIG. **1**, reference numeral **10** designates a substrate such as a semi-insulating InP substrate. An InGaAsP layer **20** is disposed on the InP substrate **10**. A semi-insulating InP layer **30** is disposed on the InGaAsP layer **20**. Photoresist **40** is deposited on the InP layer **30**. An n-type InP layer **50** is buried in the vertical aperture **60A** and the transverse aperture **60B** therewith. An n-type InP cladding layer **51**, an InGaAsP active layer **70**, and a p-type InP cladding layer **80** are buried in a groove **60C** produced by etching layer **30** until reaching the InGaAsP layer **20** in the transverse aperture **60B**. A p-type InGaAsP contact layer **90** is deposited on the p-type InP cladding layer **80** in the groove **60C**. A p side electrode **100** is disposed on the contact layer **90** and an n side electrode **110** is disposed on the n-type InP layer **50**. The n-type or p-type InP layers **50**, **51**, **80** have impurity concentrations of about $1\times10^{18}/cm^3$ and the p-type

InGaAsP contact layer **90** has an impurity concentration of about $1\times10^{19}/cm^3$.

The production process will be described.

First of all, as shown in FIG. **1**(*a*), an InGaAsP layer **20** and a semi-insulating InP layer **30** are grown successively on a semi-insulating InP substrate **10** by vapor phase epitaxy. Thereafter, photoresist **40** is deposited and patterned by photolithography.

Next, as shown in FIG. **1**(*b*), the semi-insulating InP layer **30** is etched by an etchant such as hydrochloric acid to expose the InGaAsP layer **20** thereby to produce a vertical aperture **60A**. Thereafter the InGaAsP layer **20** is selectively etched by an etchant such as mixture solution of sulfuric acid, hydrogen peroxide, and water, thereby producing a transverse aperture **60B**.

Next as shown in FIG. **1**(*c*), a region **50** on n-type InP is deposited in vertical aperture **60A** and transverse aperture **60B**.

Next, as shown in FIG. **1**(*d*), a region of the semi-insulating InP growth layer **30** positioned above end of the n-type InP layer **50** is etched until the n-type InP layer **50** is reached to produce a groove **60C**.

Thereafter, as shown in FIG. **1**(*e*), an n-type InP cladding layer **51**, an InGaAsP active layer **70**, a p-type InP cladding layer **80**, and a p-type InGaAsP contact layer **90** are successively grown on the n-type InP layer **50** in the groove **60C**, and a buried type laser is produced buried in the semi-insulating InP growth layer **30**. Thereafter, a p side electrode **100** and an n side electrode **110** are formed on the n-type InP layer **50** and the p-type InGaAsP contact layer **90**, respectively, at the same plane.

The operation of the semiconductor light emitting device produced as such will be described.

In FIG. **1**(*e*), a current flowing from the p side electrode **100** and the n type electrode **110** is converted into a light output by the InGaAsP active layer **70** buried in the semi-insulating InP growth layer **30**. Then, since the semi-insulating InP growth layer **30** is disposed at the periphery of and surrounding the InGaAsP active layer **70** current does not leak at the periphery of the active layer **70**. Furthermore, since the n-type InP cladding layer **51** is connected with the conducting n-type InP layer **50** buried in the transverse aperture **60B**, it is possible to take the n side electrode **110** up to the surface of a wafer, thereby obtaining a planar structure.

While the n-type InP layer **50** in the vertical aperture is produced in a stripe configuration in FIG. **1**, the n-type InP layer may be produced only at a part of the region lying outside the light emitting region. FIG. **2** shows an embodiment of the present invention having an n-type InP layer **52** of such a construction. Also in this embodiment, the same effects as in the first embodiment are obtained.

FIGS. **3**(*a*) to **3**(*e*) show a production process according to another embodiment of the present invention.

In this second process embodiment, a vertical aperture **11** is produced by etching a semi-insulating InP substrate **10**, a SiO_2 mask **12** is produced by sputtering and photolithography (FIG. **3**(*a*)).

Next, as shown in FIG. **3**(*b*), the vertical aperture **11** is further etched into substrate **10**, and a SiO_2 mask **13** is produced at a bottom portion of the aperture **11** by evaporation, further etching is employed produce a transverse aperture **14** as shown in FIG. **3**(*c*).

Next, as shown in FIG. **3**(*d*), an n-type InP layer **50** is grown buried in the vertical aperture **11** and the transverse aperture **14**, and thereafter, a groove is produced by etching and a buried type laser is produced in the groove as shown in FIG. **3**(*e*) by the same process as that employed in the process of FIG. **1**.

This process embodiment has an advantage in that only two crystalline growth steps are required, contrary to the three crystalline growth steps required in the first process embodiment.

FIGS. **4**(*a*) to **4**(*c*) show a production process according to still another process embodiment of the present invention.

First of all, an n-type InP layer **50** is buried at a desired depth in the semi-insulating InP substrate **10**, and thereafter, a semi-insulating InP layer **30** is grown buried in a portion of the n-type InP layer **50** in a depth shallower than the n-type InP layer **50**. A partially completed device in which the n-type InP layer **50** is produced in a vertical aperture and a transverse aperture similar to the embodiments of FIGS. **1** and **3** is thus produced. Thereafter, a buried type laser is produced buried in a groove produced at an end portion of the semi-insulating InP growth layer **30** at the side opposite to the n-type InP layer **50**, according to the present invention.

While in the above-illustrated embodiment InP series compound semiconductors is employed, other compound semiconductor such as GaAs may be used.

As is evident from the foregoing description, according to the present invention, a vertical aperture is produced at a main surface of a semi-insulating or insulating substrate, a transverse aperture is produced communicating with this vertical aperture, a conducting semiconductor layer is buried in the vertical aperture and the transverse aperture, a groove reaching the semiconductor layer from the surface of the substrate is produced above an end portion of the transverse aperture, and a light emitting element is produced . . . ; buried in the groove in such a manner that the light emitting region thereof is buried in the groove and is connected to the buried semiconductor layer. Since the light emitting region is buried in the substrate, no pn junction exists at the periphery of the light emitting region, thereby eliminating leakage current, and a semiconductor light emitting device of quite low parasitic capacitance is obtained at high yield. Furthermore, the p and n side electrodes can be provided on a main surface of the substrate so that a planar structure is obtained. This property results in simplicity in integration with other electronic elements and enhancement in the integration density.

What is claimed is:

1. A semiconductor light emitting device comprising:

a semi-insulating or insulating first compound semiconductor substrate having a surface;

a semi-insulating or insulating second compound semiconductor layer disposed on part of said surface of said substrate, said second compound semiconductor having a different composition from said first compound semiconductor;

a conducting compound semiconductor layer disposed on the part of the surface of said substrate not occupied by said second compound semiconductor layer;

a semi-insulating or insulating third compound semiconductor layer of substantially the same composition as said first compound semiconductor disposed on said second compound semiconductor layer and said conducting compound semiconductor layer;

a first aperture in said third compound semiconductor layer extending to said conducting compound semiconductor layer and filled with said conducting compound semiconductor layer;

a second aperture in said third compound semiconductor layer spaced from said first aperture and extending to said conducting compound semiconductor layer; and

a semiconductor light emitting element disposed in said second aperture and electrically connected to said conducting compound semiconductor layer including first and second semiconductor cladding layers and a semiconductor active layer disposed between said first and second cladding layers, said first cladding layer being disposed on said conducting compound semiconductor layer.

2. A semiconductor light emitting device as defined in claim 1, wherein said semi-insulating or insulating first compound semiconductor substrate comprises InP.

3. A semiconductor light emitting deice as defined in claim 1, wherein said semi-insulating or insulating first compound semiconductor substrate comprises GaAs.

4. A semiconductor light emitting device as defined in claim 2 wherein said first and second semiconductor cladding layers comprise n-type InP and p-type InP, respectively.

5. A semiconductor light emitting device as defined in claim 2 wherein said semiconductor active layer comprises InGaAsP.

6. A semiconductor light emitting device as defined in claim 1 comprising a semiconductor contact layer disposed on said second cladding layer in said second aperture.

7. A semiconductor light emitting device as defined in claim 6 wherein said third compound semiconductor layer has a surface opposite said conducting semiconductor layer comprising first and second electrodes disposed on the surface of said third compound semiconductor layer and electrically connected to said conducting semiconductor layer and to said semiconductor contact layer, respectively.

8. A semiconductor light emitting device as defined in claim 1 wherein said first compound semiconductor and third compound semiconductor layer are InP and said second compound semiconductor layer is InGaAsP.

* * * * *