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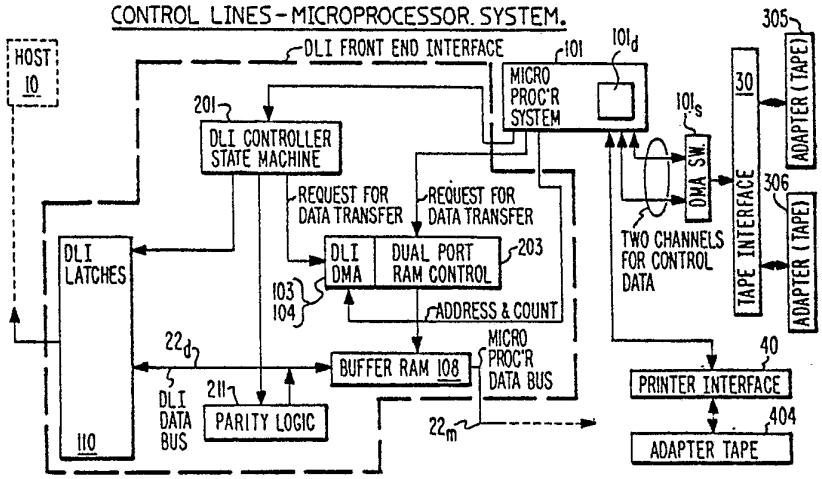

(57) Abstract

A peripheral controller (data link processor) controls data transfers between a host computer and a plurality of tape peripheral units and a single printer peripheral unit. A master microprocessor commands three subordinate controllers to permit concurrent data transfers through a buffer memory in both the Read and the Write directions. A dual channel control from the master microprocessor actuates a DMA switch so that data transfers to/from the tape units can be controlled by switching on alternate control lines which regulate the data transfer operations.

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TITLE

PRINTER-TAPE DATA LINK PROCESSOR

FIELD OF THE INVENTION

This disclosure relates to peripheral controllers which are used to transfer data and control signals from a main host processor system to remote peripherals and to provide the functions of an input-output controller for data transfer operations.

BACKGROUND OF THE INVENTION

It is one of the basic functions of a computer system to communicate with remote peripheral devices in order that data transfers and control signals may be interchanged in order to accomplish the purposes designed into the computer system or network.

In order to facilitate this data interchange, there have been developed peripheral controllers, also called I/O controllers or Data Link Processors (DLP's), which relieve the main host computer of many of its operating cycles for the purposes of seeing to it that

data exchanges between various remote peripheral devices and the main host computer system can be accomplished with minimal interruption to the main host computer system.

A series of specialized I/O controllers have been developed by the Burroughs Corporation for handling the specialized requirements of Burroughs computer systems and peripherals. These specialized peripheral controllers have been designated as "data link processors", or DLP's.

These specialized Burroughs data link processors have been specifically designed to handle the applicable protocols and the various data transfer requirements usable by Burroughs computer and Burroughs peripheral devices. Such types of data link processors have been described in such prior patents as:

U.S. Patent 4,313,162 entitled "I/O Subsystem Using Data Link Processors"; U.S. Patent 4,371,948 entitled "Train-Printer-Data Link Processor"; U.S. Patent 4,390,964 entitled "Input/Output Subsystem Using Card Reader Peripheral Controller".

These background patents are included herein by reference to furnish the background and functional operation of data link processors which are used to link a host computer and peripheral terminals.

These patents describe the unique features and operations of the Burroughs type of data link processors and provide specific details of operation of the data link processors in conjunction with Burroughs computer systems and networks. These prior patent applications describe the various types of possible operations and data transfer

control signals which are used in data link processors. Accordingly, these patent applications will provide an in depth background and explanation of the various hardware and intercooperating features which are used in data link processors.

The present invention is a data link processor which is compatible with Burroughs computer networks and systems but which has been specifically developed to handle two types of remote peripheral devices by means of one single data link processor. This data link processor is called the buffered printer-tape data link processor (PT-DLP) and is disclosed herein.

SUMMARY OF THE INVENTION

The present disclosure presents a combination of intercooperating hardware elements which interface the main host computer system on the one hand and provide for data transfers and communication to and from two different types of remote peripheral units. These peripheral units constitute a buffered-printer terminal unit and also a streamer tape peripheral unit which may be daisy chained to provide communication transfers between the host and four tape units.

Thus, the present system architecture permits the sharing of one host system interface between two peripheral interfaces by means of one particular unit designated as the printer-tape data link processor.

The present system also permits the interleaving of data in a data link interface (DLI) data storage unit (buffer memory) such that data coming into the buffer memory can be interleaved with data coming out of the

buffer memory simultaneously so that a buffer memory device can operate to permit the flow of data from a peripheral unit to the main host system and also simultaneously permit the flow of data from the main host system to the particularly selected remote terminal unit.

The data link processor system described herein also provides for the automatic switching of direct memory access control data (DMA) channels for control of data transfers to and from the peripheral tape units.

The system is organized such that one master microprocessor system can cooperate with three slave controllers to concurrently handle data transfers to and from the main host system concurrently with data transfers to and from the two types of remote peripheral units.

As heretofore mentioned, the DLI data storage unit (buffered memory) provides for the simultaneous function of interleaved data flow to and from the host system and to and from each of the two types of peripheral units. This is accomplished by a look-ahead function in hardware of the host and the peripheral interface units.

A direct memory access (DMA) switch unit is provided with two control data channels to the tape control unit which are used to manage data transfers between the master microprocessor and the tape peripheral units. When "control data" is being transferred from along one channel to a tape control unit and subsequently the actual "data" transfer cycle is concluded, then the tape control unit is automatically switched to connect to the other "control data" channel without the need for intervention by the master microprocessor system. This

is done to maintain more rapid data flow in both directions without having to burden the master microprocessor.

Thus, the architecture of the presently disclosed printer-tape data link processor provides for a very efficient and time saving method by which one particular I/O controller can regulate the data transfer flows between two types of peripheral terminal units (in particular a printer unit and up to four tape units) all the while permitting simultaneous data transfer operations from a buffer memory in both directions to and from the main host computer and to and from the peripheral units.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram showing how the printer-tape data link processor operates with a main host system in order to provide an interface to remote peripheral units;

FIG. 2 is a block diagram showing the main elements of the printer-tape data link processor with special reference to the data flow lines.

FIG. 3 shows a more detailed block diagram of the printer-tape data link processor indicating how the control lines of the microprocessor system links the data link interface front end to the peripheral terminal units;

FIG. 4 is an overall block diagram of the printer-tape data link processor;

FIG. 5 is a functional flow diagram which shows the basic operation of the printer interface state machine;

FIG. 6 is a functional flow diagram which shows the basic operation of the tape interface state machine;

FIG. 7 is a timing diagram of the Read cycle, Write cycle and DLI Access cycle of the microprocessor system and shows the DLI state machine controller access period interleaved with the microprocessor system access period for inserting or withdrawing data from the buffer memory of the data link processor.

FIG. 8 is a schematic diagram illustrating the automatic channel switching for control data utilization.

DESCRIPTION OF THE PREFERRED EMBODIMENT

As with other types of Burroughs data link processors, such as those described under the headline "Background of the Invention", the present data link processor is compatible with most computer systems which use the message level interface (MLI) for parallel transfer of data control signals and data between the main host system and the data link processor as was described in the earlier patent cases on data link processors. Thus, in FIG. 1, the distribution card 20 interfaces the host via the MLI, and interfaces the data link processor via the DLI.

The printer-tape data link processor (PTDLP), when seen from the viewpoint of the host computer system, will be seen by that system as a separate printer DLP and a separate streamer-tape DLP. Each of these two functional data link processors (which are here combined in one unit) have an address line (LCP address) and also a request line (LCP request) line just as if they were two separate data link processors. Thus, the functions and description of the present printer-tape data link processor will be presented descriptively in two sections which will be descriptive of the buffered printer section and another section which is descriptive of the streamer tape section.

All the hardware of the printer-tape data link processor is mounted on one logic board which interfaces to a data link interface backplane. There are front plane cables which connect to the peripheral adapter cards (PAC's) which are shown in FIGS. 1 and 4 as elements 305,

306 and 404. Thus, as seen, there is one PAC 404 used in the printer interface and there are two PACs (305, 306) which are used in the streamer tape interface unit.

The streamer tape interface unit will be seen on FIG. 2 as element 30 and it will allow direct connection to four magnetic tape streamer units such as developed by the Burroughs Corporation for magnetic tape peripheral units. This interface 30 does not require (and also does not permit) a tape control unit (TCU) in the path to the tape drive. The formatter and the control for the tape drive are contained within the tape drive.

As seen in FIG. 1 the tape drives can be daisy chained one to another such that up to four magnetic tape streamer units can be daisy chained using a single controller card and the two peripheral adapter cards 305 and 306 of FIG. 1. An interface cable is extended through a connector on each tape drive and the last tape drive in the chain uses a terminator connector.

The tape drive can operate at 25 or up to 100 inches per second under software control, with a rewind speed of 200 inches per second. Thus, this gives a data transfer rate of 40 or 160 kilobytes per second on the peripheral interface. Approximately 40 megabytes of data will fit on a 2400 foot 10½ inch tape reel when using 5,000 bytes for each record.

The tape format used is the ANSI standard X 3.39-1973 (PE) which is 1,600 bytes per inch, phase encoded (PE) with the standard inter-record gaps. This allows the same tapes to be written-on and read, on both the magnetic streamer unit tape drives and also the 75/125 inch per second phase encoded tape drive units.

The printer-tape data link processor is organized to provide a unique and selectable data link processor address for the tape interface.

The other interface is the printer interface 40 of the data link processor. The printer interface connects to a Burroughs high speed standard interface (HSSI) which is seen as element 40 in FIG. 2. This interface can be modified by the Burroughs printer interface protocol used in Burroughs systems. Only one printer unit, line printer 44, may be connected to the printer-tape data link processor through the single peripheral adapter card 404 of FIG. 1.

The data rate allowable to the printer interface is 31.25 kilobytes per second. The data rate from the printer interface can be 153.8 kilobytes per second on the Burroughs B 924 printers. On the Burroughs B 9246 printers, the data rate from the printer interface is 100 kilobytes per second.

As was previously mentioned in regard to the "tape" interface, the data link processor (DLP) also provides a uniquely selectable DLP address for the "printer" interface.

With reference to FIGS. 1, 2, 3 and 4, the following description will indicate the various functions of the hardware shown in these drawings and with special reference to FIG. 4.

The printer-tape data link processor consists of a microprocessor system 101 which controls three other state machines. The microprocessor system 101 also includes a DMA controller 101_d and microprocessor 101_m. The

controllers discussed herein are sometimes referred to as "state machines".

The three other state machine controllers involved are:

(a) The DLI interface 201 (FIG. 4);

(b) The printer interface state machine 401 (FIG. 4);

(c) The tape interface state machine 301 (FIG. 4).

A dual-port DLI buffer memory 108 (FIGS. 2, 4) of 8K bytes and the microprocessor local RAM memory (101_m, FIG. 2) of 4K bytes are used to buffer the data to and from the peripheral units.

Microprocessor System

The microprocessor system 101 shown in FIGS. 3 and 4 includes an interrupt controller (in 101), a DMA controller 101_d of FIG. 3, device selection logic (113, FIG. 4), a RAM (108 of FIGS. 3, 4) and an erasable PROM (EPROM) and a RAM which operates within block 101 of FIG. 4. All program storage is situated in the EPROM.

The microprocessor 101_m is an 8 megahertz 16-bit microprocessor of the type designated by Intel Corp. as the 8086. This processor unit is described in the handbook entitled "iAPX 86, 88 Users Manual", pages 1-2 through 2-72, copyright 1981, published by Intel Corp. of 3065 Bowers Avenue, Santa Clara, Ca. 95051.

The microprocessor system 101 provides for 64K bytes of addressing space in which there is provided a memory map which covers the following functions:

(a) 32 kilobytes of EPROM for interrupts and functional codes;

(b) 8 kilobytes for the dual-port RAM (108);

(c) 4 kilobytes for the memory-mapped I/O;

(d) 4 kilobytes for local RAM memory (101_{my});

(e) 16 kilobytes of EPROM for reset and MTR (Maintenance Test Routines) code.

This local EPROM memory is split into two banks which are separately enabled by a signal called the "Bus High Enable" and by the A0 address line.

Address decoding is done in two stages. The first stage is done by a programmed logic array designated FPLA. Devices which require a longer setup time for selection will use outputs from the first stage directly. These include the memory (in 101), the interrupt controller (in 101) and the DMA controller (101_d).

The control latches (110, FIGS. 3 and 4) and the status buffers such as 105 and 106 of FIG. 4 (which are accessed by the microprocessor 101) will use the outputs from the second stage which consists of three decoders (113, FIG. 4) which are enabled by the first stage.

The interrupt controller (in 101) is used in the edge-triggered mode in order to detect the DLI message designated DLIMESS (DLI Message) and also the signal DMAEND (direct-memory-access-end-of-transmission), in addition to the 500 microsecond timing signal. The interrupt controller (in 101) provides vector addresses for the microprocessor 101_m.

The clear/self test interrupt (70, FIG. 4) is tied to the non-maskable interrupt line of the microprocessor 101 (Intel 8086). The board self test/reset and the manual self test/reset are tied to the reset line of the

microprocessor 8086. The non-maskable interrupt and the reset interrupts will generate vectors internally within the 8086 and remove the interrupt controller (in 101) from the self test operations loop.

The DMA controller (101_d) is used to transfer data to and from the peripheral interfaces 30 and 40 (FIG. 3) and also the microprocessor local memory 101_{my} (FIG. 2). The DMA controller will also transfer data to and from the tape interface 30 and the dual port buffer memory 108 of FIGS. 3, 4.

One of the DMA channels will be dedicated to the printer interface. Then, two of the channels will be dedicated to the tape interface. The DMA controller 101_d, in the microprocessor system 101, has two "control data" channels to a DMA switch 101_s in FIG. 3 which are used to alternately switch "control data" to the tape interface 30.

A multiplexor (in 101_s, FIG. 3) is implemented in a programmed array logic unit which directs the request, the acknowledge, and the end-of-process signals to the appropriate channels. An "end of process" signal from the DMA controller (101_d), while servicing the tape interface, will cause a switch to the alternate tape "control" channel after the current acknowledge occurs.

A signal (OVRUN) produced from the DMASWITCH signal (of 101_s) in the programmed array logic will be used to indicate that the switch over has occurred before the microprocessor has had time to initialize the channel. Thus, the signal "UP.DSRST" is used to "reset" the internal OVRUN state when initializing the DMA channel, when this occurs.

Microprocessor System Clocks:

The clock for the microprocessor 101 is derived from the 8 megahertz DLI backplane clock (50, of FIG. 4) using a delay line and gating. The "ready" input to the microprocessor 101 (8086) is synchronized to a clock by a D flip-flop. The clock for the DMA controller 101_d uses the 8 megahertz backplane clock divided by two in order to yield a 4 megahertz clock for the DMA controller 101_d, FIG. 4.

DLI Interface:

The DLI interface (DLI Front End, FIG. 3) consists of the clear and the self test initiation logic 70, FIG. 4; the DLI send/receive registers (110); the burst counter 104, FIG. 4; the burst-end logic (103); the longitudinal parity word generator 111, FIG. 4; the vertical parity generator and routing (109); the request and emergency request logic (107) and the DLI/controller communication logic (in 201).

A 2K X 24 bit DLI state machine (201, FIG. 4), with parity, accepts condition signals from the microprocessor 101 and controls the data elements. The DLI state machine 201 (FIGS. 3, 4) also accepts status signals from and also provides control of portions of these elements. The specific types of control are as follows:

Functions of DLI State Machine Controller

(a) The clear and self test initialization logic (70 of FIG. 4) can detect when various types of clears and self tests are required. The signal LOCPAL detects the local address for either the printer or the tape data link processor and validates it with the signal ADRVLD (address valid) and the signal LOCAD (local address).

The comparison of the local address DIP switch to the "LOCAD" signals is synchronized by system 101 for the PS (printer select) and the TS (tape select) signals;

(b) Generation of the clear and the self test signals, the resets, and the interrupts is performed by the signal "ADSTCL" (address, self test, clear PAL) or the programmed array logic. It also generates the signal "CONNECT" using the DLPADP (printer DLP address) and the signal DLPADT which is the tape DLP address signal;

(c) The DLI send/receive registers are implemented by directional register latches (110 of FIG. 4). The output enable signal onto the DLI is generated by the "CONNECT" signal and by the IOSEND signal.

The latch enable from the DLI is controlled by the AF (asynchronous flag) signal. The clocking and enabling from the DLI front end is controlled by the DLI state machine 201, FIG. 4.

(d) The burst counter 104, FIG. 4, is implemented on a 20 X 8 PAL which is programmed as an 8 bit counter. It can be read and loaded by the master microprocessor 101_m, with the count enable generated by the DLI state machine 201;

(e) The burst end logic in 101 uses the signal TERM (terminate), the signal CO (carry out of the burst counter), and the signal STIOL (strobe I/O level) in order to provide a condition input to the DLI state machine 201, FIG. 4, to halt the burst mode;

(f) The longitudinal parity generator 111 of FIG. 4 is implemented in two program-array-logic units which are programmed to perform the longitudinal parity word accumulation. A data pipelining latch composed of two latches 111 is used to meet the timing requirements on the internal DLI data bus (200_b, FIG. 4). The microprocessor 101_m controls the clearing and examines the longitudinal parity word "zero" status (LPWZERO) which indicates whether or not the transmitted word is without error.

The DLI state machine 201 controls the accumulation and reading of the LPW

generator 111. The pipelining latch-enable (connecting 201 to unit 111) is also controlled by the DLI state machine 201;

(g) Vertical parity generation and routing is performed by two 9-bit parity generators (109, FIG. 4) in conjunction with quad 2 x 1 tri-state multiplexors. A bidirectional register/latch 111, FIG. 4, is used to send and receive the parity bit on the data link interface. Vertical parity is generated and written into the parity RAM (part of 108) when writing into the dual port RAM (108 of FIGS. 3, 4) from the microprocessor system 101.

Vertical parity is checked when writing into the dual port RAM (108) from the DLI interface (FIG. 3) and the actual DLI parity is written into the parity RAM (of 108). Vertical parity is read from the parity RAM when reading onto the DLI data link interface. The timing of the memory-write cycle is met by using a tri-state buffer instead of using the tri-state capability of a bidirectional register latch. A flip-flop is used to store the parity checking result and is used to produce the signal VPERR (vertical parity error) status signal to the microprocessor 101_m;

(h) Request and Emergency Request logic is implemented in a programmed array logic unit designated REQPAL (in 107). The microprocessor 101_m controls the setting of the printer request, the tape request and the emergency tape request signals. The signal REQPAL monitors the emergency request input to remove the printer request. It will also reset the tape request if the tape emergency request is not set. The DLI state machine controller 201 controls the clearing of the REQPAL requests when they are granted to meet the DLI timing requirements;

(i) The DLI/microprocessor communication logic, within 201, is contained in a programmed array logic unit called the DLI/UP PAL. Two settable and clearable flags are provided. the flags are:

(i) UPMESS - microprocessor message to the DLI;

(ii) DLIMESS - DLI state machine message to the microprocessor 101.

The DLI state machine parity error flip-flop is also implemented in the DLI/UP PAL. The microprocessor 101_m issues DLI operations (DOPS) to the DLI state machine 201 and sets a flag (UPMESS), which is fed into the state machine condition logic. The DLI state machine then carries out the operation.

The DLI state machine controller 201, then, can carry out the following operations:

Send strobe
Read data (one word)
Write data (one word)
Read burst
Write burst
Wait for connect
Wait for disconnect
Wait for AF signal (AF signal means handshake signal with host - so the controller 201 can wait for AF in order to tell the microprocessor 101_m when the host is ready)
Send LPW
Read host pointer
Move LPW to the RAM
Load the Send Register
Move Receive Register to the RAM
Load LPW from the RAM
No operation

Upon completing the given operation, the DLI state machine controller 201 will set the signal DLIMESS, which will provide an "interrupt" to the microprocessor 101_m. After the initial DLIMESS interrupt signal, the line DLIMESS will act as a "status input" to the microprocessor 101_m instead of the interrupt occurring constantly while connected to the host system 10.

The DLI state machine controller 201 is implemented using three 2K X 8 registers in the PROM for the control store and pipelined register. The condition logic in 201 is implemented in a program logic array, FPLA, and the condition latch is provided in two latch units.

The inputs to the condition logic of DLI state machine 201 (FIG. 4) are also available to the microprocessor 101_m as status inputs. A 3-bit microcode field is provided for condition selection. Another 3-bit field is provided for the unique next address selection of the DLI state machine 201 within any operation.

Four bits of the control store address in 201 are provided by the DOP (DLI operations). This gives the addressing environment for an operation. Three bits of the address are provided by the unique next address field. Four bits of the address are provided by the condition code inputs.

Parity checking of the control store (in 201) is done during the DLP operation by three 9-bit parity generators. The parity error indication is held in the programmable array logic designated DLI/UP PAL (201, FIG. 4).

Printer Interface

The printer interface consists of data send and data receive latches (403 of FIG. 4), parity generation and checking circuitry (not shown), a printer state machine controller 401 for interface control, and peripheral buffers (in 404) and loop back buffers (in 404).

The printer send/receive latches 403 are implemented by latching and enabling signals which are controlled by the printer interface state machine controller 401 (FIG. 4). Requests for data are made by the microprocessor system 101 (microprocessor 101_m or the DMA controller 101_d therein), together with the PUDAPSEL (printer-microprocessor data selection line).

The printer parity generation and checking is done by a 9-bit parity generator. Selection of the source of the inputs and the destination of the outputs is done by the printer state machine controller 401. The printer parity error is held in the printer program array logic in 401 (PRTPAL) and is used as a status indication to the microprocessor 101_m.

The printer interface state machine controller 401 is implemented by the array logic of the PRTPAL. It performs functional transitions which are shown as a flow chart in FIG. 5.

Tape Interface

The tape interface (30 of FIG. 2) consists of send/receive latches, read and write parity generation, command registers, status buffers, and a tape state machine controller 301 (FIG. 4) to control the interface, peripheral buffers, and loop back buffers.

The send/receive latches 302 are implemented by four bidirectional latch/registers which provide one 16-bit word of data latch. The tape state machine controller 301 controls the loading and the enabling of the two 8-bit halves of the data latch to multiplex or demultiplex the data.

The read and write parity generation for tape transfers is performed by two 9-bit parity generators. Parity is generated on the "write" data path and checked on the "read" data path. When writing data to the tape, the read-after-write head returns the data which was written and the drive validates it with a strobe signal IRSTR (inverted read strobe).

The parity error indication is caught and held in the tape programmed array logic 304 (TAPPAL). The drive also produces a hard error signal (IHER) and also a corrected error signal (ICER) to indicate that the drive has detected parity errors from the tape. These signals are also caught and held by the tape programmed array logic, TAPPAL.

Command registers are implemented with two registers in the tape interface 30. Command signals, address signals and strobe signals (IGO) are written in parallel onto these registers.

Status buffers return information on the currently addressed tape drive unit to the microprocessor 101_m. The following signals: IHER (hard error); ICER (corrected error); the IFMA (file mark detected); the IEOT (end of tape); and the TPARERR (tape parity error) are pulses from the tape drive which are caught and held for access by the microprocessor 101 by means of the TAPPAL. The TAPPAL 304 provides an error strobe signal as a tape data trap. It detects an error and holds the error signal until the end of the data transfer cycle at which time it informs 101_m. The other status signals are provided directly from the addressed tape drive.

The tape interface state machine controller 301 is implemented in the programmed array logic 304 (TAPPAL) which is programmed to catch pulses and to sequence through several states. It controls the multiplexing and the demultiplexing of the two 8-bit halves of the data latches and the request/acknowledge handshake signal with the DMA controller, 101_d, FIG. 4.

The tape interface state machine controller 301 will be seen to perform the functions which are flow charted in FIG. 6.

The tape peripheral buffers are on the two peripheral adapter cards 305 and 306 shown in FIG. 3 and in the interfaces 30 and 40 of FIG. 2. There are loop back buffers on the peripheral adapter cards to allow testing of the data and the control paths to the peripheral adapter cards, PAC 305, 306.

The signal M.TAPDAT is used to control the loop back paths in 305 and 306. When the maintenance program is enabled, the buffers to and from the peripherals are disabled and the path (in 302) between the read and the write paths is enabled. This allows the testing of the control and data paths between the main logic cards of the printer-tape DLP and the PAC's 305, 306, 404.

Dual Port Memory

The DLI buffer memory 108 (of FIGS. 2, 4) is a two port memory allowing access from the DLI state machine 201, and the master microprocessor system 101 which includes the microprocessor 101_m and the DMA controller, 101_d.

The address path for the DLI state machine 201 is from a counter implemented in two program array logic units. This counter is initialized by the microprocessor 101_m. The address path for the microprocessor system is through two buffers (address buffer 102, FIG. 4).

The "DLI data path" and the "microprocessor system data path" are separated by data latches. These data paths are shown in FIG. 2 as 22_d and 22_m.

The control of the dual port memory (108 of FIGS. 2, 3, 4) is done by the dual port program array logic (shown as element 203 in FIGS. 3 and 4). It is programmed to do a "look ahead" of the request requirements of the DLI state machine controller 201 and the microprocessor system 101. It provides the data and address path "enabling", the RAM chip select, the RAM write enable and the microprocessor system "ready" signal. It also uses the signal AF (asynchronous flag) and the BURST signals to do a clock by clock (FIG. 7) interleaving of the DLI 201 and the microprocessor 101_m memory requests during the burst mode.

Self-Test Operations

The printer-tape data link processor (PT-DLP) has been designed to support the "self-test" function with three methods of initiation and two methods of reporting functionality of the data link processor.

The data link processor will begin its self-test function upon receipt of any of three clear signals:

(a) forepIane clear which is generated by a pushbutton switch that is local to the main logic card;

(b) a power-up clear;

(c) two types of self-test initiation signals from the test bus on the DLI backplane. These two types consist of either being addressed and cleared while in the local mode, or by being generally addressed by the PT-DLP local general address and the complete self-test initiation signal being "true". The SWITCH lines are used to select between testing either (i) the printer portion; (ii) the tape portion; or (iii) a complete test of the printer-tape data link processor. The foreplane clear and the power-up clear both initiate a complete self-test of the printer-tape data link processor.

After initiation of the self-test of the data link processor portion being tested, this will disable its peripheral and DLI interfaces until such time as the data link processor passes its own self-test. A status of "zero" together with the signal LCPCON/O will be presented to the backplane whenever the addressed data link processor is executing or has failed to execute its self-test, or, in the case of a detectable on-line failure, such as a PROM parity error or a microcode sequencing error.

On the foreplane, four red light-emitting diodes (LED's) will also indicate the status of the test. When any of these LED's are "on", the data link processor is either in the process of self-testing, or has failed the self-test, or has detected an on-line failure.

The "top" LED displays the status of the self-test in relationship to the main logic card; the next one shows the status of the self-test with respect to the printer interface and its peripheral adapter card (PAC 404); the next LED light shows the status of the self-test with respect to the tape interface and the tape peripheral adapter card board #1 (305); and the fourth light shows the status of the self-test with respect to the tape interface and peripheral adapter card board #2 (306).

If a LED light is left on after the specified time for execution of the self-test, it indicates which card failed first. If the top LED light is "on" past the specified time for the test, it indicates that the peripheral adapter card (PAC) was not tested but that the main logic card has failed its self-test.

The scope of the self-test is a test of the main logic board hardware which affects the addressed device and the confirmation of the data paths to and from the peripheral adapter cards.

Drivers and receivers of the peripheral units (34, 44, FIG. 1) and the DLI interface (FIG. 3) are untestable by the self-test function and they require a stand-alone or a peripheral test driver test.

The length of the self-test for the printer section of the data link processor can be set not to exceed a predetermined number of seconds. Likewise, the length of the self-test for the tape section of the data link processor can be set so that it shall not exceed another set value of a predetermined number of seconds.

Likewise, the length of the self-test for the complete data link processor (including both printer section and tape section) shall not exceed another predetermined set number of seconds.

Referring to FIG. 3, there is seen the dual port RAM control 203 which is controlled by the microprocessor system 101; and the data link interface controller 201 in conjunction with the DLI-DMA (direct memory access unit 103, 104, also in FIG. 4).

The dual port RAM control 203 is used to control the RAM buffer 108 of FIG. 3.

It may be noted that while FIG. 3 mainly shows "control" lines, FIG. 3 also shows data buses where data can be transferred from the host 10 through the DLI latches 110 over through the DLI data bus 22_d, and into the RAM buffer 108. Here the data may be processed via bus 22_m through the microprocessor system 101 and transferred either to the tape interface 30 or the printer interface 40, for later transfer to the peripheral.

Likewise, the data from either the printer peripheral unit 44 or the tape peripheral unit 34 may be transferred through the interfaces 40 and/or 30 on to the microprocessor system 101 and hence through the buffer RAM 108 and over through the DLI data bus 22_d to the host 10.

The buffer RAM 108 may be considered a "dual port" RAM for the purpose of storing temporarily the data which is either travelling from a peripheral unit to the host system ("Read") or for data which is travelling from the host system to a selected peripheral unit ("Write"). Thus, data flow through the RAM buffer 108 is concurrent and simultaneous in either direction. This is accomplished through an "interleaving" process cycle.

Referring to FIG. 7, there is shown a series of timing diagrams which show the clocking signals used for data transfer in the "Read" direction and for data transfers in the "Write" direction. The "Read" direction means that data is being transferred from a peripheral terminal unit to the buffer memory 108 for later transfer over to the main host system. The "Write" direction means that data is being transferred from the main host system to the buffer memory 108 for later transfer to a selected peripheral terminal unit.

In FIG. 7 it will be seen that by the end of the clock 1 time, the dual-port RAM 108 will have the necessary access information to permit an interleaving of data to occur at the clock 2 time or the clock 3 time.

In the Read cycle of FIG. 7, the first line shows the clocking signal. The second line designated ALE is the signal which indicates the microprocessor address latch enable.

The third line designated M/IO is the signal which indicates whether microprocessor 101_m is selecting memory space or I/O space.

The fourth line designated AD015 indicates the relationship between the valid address signal and the actual valid data signal which is separated by 1 clock. It shows the use of the bus for address information and the time period available for data transfer.

The fifth line shows the signal $\overline{RD}$. This signal indicates when the read data can be transferred into or out of the RAM 108.

The sixth line which is labeled with DT/$\overline{R}$ indicates the Data Transmit/Receive condition which indicates the direction of data flow.

In the second portion of FIG. 7 there is seen the "Write" cycle. As before, the clock signal, the ALE signal, the M/IO signal, the address signal and the DT/$\overline{R}$ signal are the same except for line 5 where we have a $\overline{WR}$ or Write signal instead of a Read signal.

In the Write cycle it will be seen that immediately after the address is provided, the data for the Write direction can be transferred out to the peripheral adapter units.

It will also be noticed that, in the Read cycle, there is a 20 nanosecond set-up time for the read-data and a 10 nanosecond hold time for the read-data.

In the Write cycle there is a 60 nanosecond delay after the address data in order for the write data to be transferred. The write data has a 10 nanosecond delay which permits clearance of data from the buffer register in the RAM 108.

The third (lowest) portion of FIG. 7 shows the DLI access clock with a sequence of clock cycles numbered 1, 2, 3, 4, 5, etc. Here, during the first clock cycle, the DLI state machine 201 has access to the buffer memory 108 (for either transferring data out or transferring data in).

The next clock cycle (cycle 2) then provides the second time period for the microprocessor 101_m to gain access to buffer 108 (for either transferring data in or transferring data out). Then access periods alternate between availability for the DLI controller 201 and the master microprocessor 101_m.

Thus, it is possible to have "Read" data moving from a peripheral unit to the main host system concurrently and at the same time that "Write" data is moving from the main host system to a peripheral unit through the same RAM buffer 108 even though various registers of this RAM buffer are used.

With reference to FIG. 8, there is shown schematically how multiplexor 101_m is used to switch between channel 1 and channel 2 for control data operations. A toggle 101_t controls the channel switching in the multiplexor 101_m.

At the end of the transfer of a data block, the End-of-Block signal from DMA controller 101_d causes toggle 101_t to change state. This switches the tape DMA control signals (from 101 and 30 of FIG. 3) from channel 1 to channel 2, and vice versa using multiplexor 101_m.

The overrun detection circuitry 101_r will detect an "error" condition wherein the "other channel being switched to" has not yet been initialized by microprocessor 101. In this event, the non-initialized condition would cause invalid data to be transferred to the peripheral tape unit.

There has thus been described a peripheral controller where a master microprocessor commands and coordinates the operation of a DLI (data link interface) slave controller, a tape interface slave controller, and a printer interface slave controller which permits a buffer memory in the DLI interface front end to intake and to output data-being-transferred concurrently in either direction (host to peripheral or peripheral to host) in an interleaving cycle

process. Further the master microprocessor controls a DMA switch unit which permits alternate control data channels to manage data transfers to/from the tape peripheral units by causing a control channel switchover each time after a block of data is transferred to/from a tape unit.

While other possible embodiments may also be used to effectuate the features described herein, the invention should be understood to encompass the system described in the following claims:

What is claimed is:

1. A peripheral controller, designated as a data link processor, for managing data transfers between a host computer and a plurality of tape peripheral units and a printer peripheral unit, said peripheral controller comprising:

(a) data link interface (DLI) means providing a data path between said host computer and a master microprocessor means and for controlling data transfers between said host and master microprocessor means, said DLI interface means including:

(a1) a DLI slave controller for controlling data transfers between said host computer and said DLI means, said DLI slave controller operating under command of a master microprocessor means;

(b) said master microprocessor means for controlling data transfers between said data link interface means and a tape interface means and a printer interface means, said master microprocessor means including:

(b1) a DMA controller for executing data transfer operations in response to a data-transfer request from said printer interface means and said tape interface means;

(c) said printer interface means connected to a peripheral printer unit and including:

(c1) printer-slave interface controller means operating under command of said master microprocessor means, said printer-slave interface controller means controlling data transfers between said printer peripheral unit and said printer interface means;

(c2) means to generate a request signal to said master microprocessor means and said DMA controller for initiation of a data transfer operation;

(d) said tape interface means connected to a plurality of peripheral tape units and including:

(d1) tape-slave interface controller means operating under command of said master microprocessor means, said tape-slave interface controller means controlling data transfers between a selected tape peripheral unit and said tape interface means;

(d2) means to generate a request signal to said master microprocessor means and said DMA controller for initiation of a data transfer operation.

2. The peripheral controller of claim 1, wherein said data link interface means includes:

(a) buffer memory means for temporarily storing data being transferred between said host computer and said printer and tape peripheral units;

(b) data link interface (DLI) slave-controller means, operating under command of said master microprocessor means for synchronizing data transfer requests from said host computer with data transfer requests from said master microprocessor means to apply control signals to a dual port memory control means to select whether access control to said buffer memory means will be directed by said DLI slave controller means or said master microprocessor means;

(c) said dual port memory control means for controlling access to said buffer memory means.

3. The peripheral controller of claim 2, wherein said data link interface means includes:

(a) DLI-direct memory access (DMA) means, commanded by said data link interface slave-controller means, for enabling data access to said buffer memory means by said DLI-DMA means, and for providing address information to said buffer memory means and maintaining a count of words of data transferred into or out of said buffer memory means;

(b) and wherein said dual port control means receives control signals from said master microprocessor means and from said data link interface-direct memory access means (DLI-DMA), said dual port control means operating to alternate access-control of said buffer memory means between said master microprocessor means and said DLI-DMA means.

4. The peripheral controller of claim 3, which includes:

(a) first and second control line channels between said master microprocessor means and a DMA switch means;

(b) said DMA switch means receiving control data via said first and second control line channels and including:

(b1) means to sense when a data transfer operation has terminated;

(b2) means to switch control data automatically from a utilized one of said control line channels to said other control line channel;

(c) and wherein said DMA controller in said master microprocessor means generates a signal to said DMA switch means to indicate that a data transfer operation has just terminated.

5. The peripheral controller of claim 3, which includes:

(a) DMA switch means for automatically switching control data from a first control channel to a second control channel from said master microprocessor means;

(b) first and second control data channels from said master microprocessor means to said DMA switch means, and wherein said DMA switch means switches control data transmission from said first channel to said second channel and vice versa after each data block transfer cycle.

6. A peripheral controller, designated as a data link processor, for controlling data transfer operations between a host computer and a plurality of tape peripheral units, comprising:

(a) master processor means for controlling a plurality of slave controller means, said means including:

(a1) first and second output control data channels for transmitting control data to a tape interface means;

(b) a data link interface (DLI) means for connecting said host computer to said peripheral controller, and including:

(b1) a data link interface (DLI) slave controller means for controlling data transfer operations between said computer and a buffer memory means;

(b2) said buffer memory means being alternately accessed by said master processor means and said data link interface (DLI) slave-controller means, said buffer memory means being connected to said host computer via a DLI data bus and connected to a tape interface means via a master processor data bus;

(b3) said DLI data bus connecting said host computer via said DLI interface means to said buffer memory means;

(b4) said master processor data bus connecting said buffer memory means to said tape interface means;

(c) said tape interface means including:

(c1) tape-interface slave controller means for controlling data transfers between said buffer memory means and said plurality of tape peripheral units, said tape-interface slave controller means including:

(c1a) means for automatically switching the control of data transfer operations between said first and second output control data channels;

(c1b) peripheral bus connection means to said plurality of tape peripheral units;

(c1c) means to generate an end-of-transmission signal when a particular data transfer operation is terminated.

7. The peripheral controller of claim 6, wherein said means for automatically switching includes:

(a) DMA switch means for automatically switching the utilization of one said control data channel to said other control data channel, said DMA switch means connected to both said first and second control data channels from said master microprocessor means.

8. The peripheral controller of claim 7, wherein said DMA switch means includes:

(a) means to sense said end of transmission signal upon termination of control data transfers in said first and second channels;

(b) means to switch control data transfer operations to the other channel from that just utilized;

(i) and wherein said master microprocessor means includes:

(c) a DMA subcontroller for generating control data for transmission to said DMA switch means via said first or second control data channels.

9. The peripheral controller of claim 8, which includes:

(a) a printer interface means connected to said buffer memory means via said master microprocessor means, said printer interface means including:

(a1) bus connection means to a peripheral printer unit;

(a2) a printer send-receive latch for temporary storage of data being transferred between said printer peripheral unit and said buffer memory means;

(b) printer-slave controller means under command of said master processor means and including:

(b1) means for controlling data transfers between said printer send-receive latch and said printer interface means, and said buffer memory means;

(b2) means to control the allocation of data transfer requests from said DMA subcontroller and from said printer peripheral unit.

10. The peripheral controller of claim 9, which includes:

(a) access control means for controlling access to said buffer memory means for placing in or removing data therefrom, said access control means being controlled in alternate cycles by said DLI slave-controller means and said master processor means.

11. The peripheral controller of claim 10, wherein said access control means includes:

(a) dual port control means for receiving control and address data from said master processor means, said port control means including:

(a1) means to regulate the buffer memory means access time period permitted to said DLI slave controller means and to said master processor means;

(b) DLI-direct memory access means for receiving control and address data from said DLI slave-controller means.

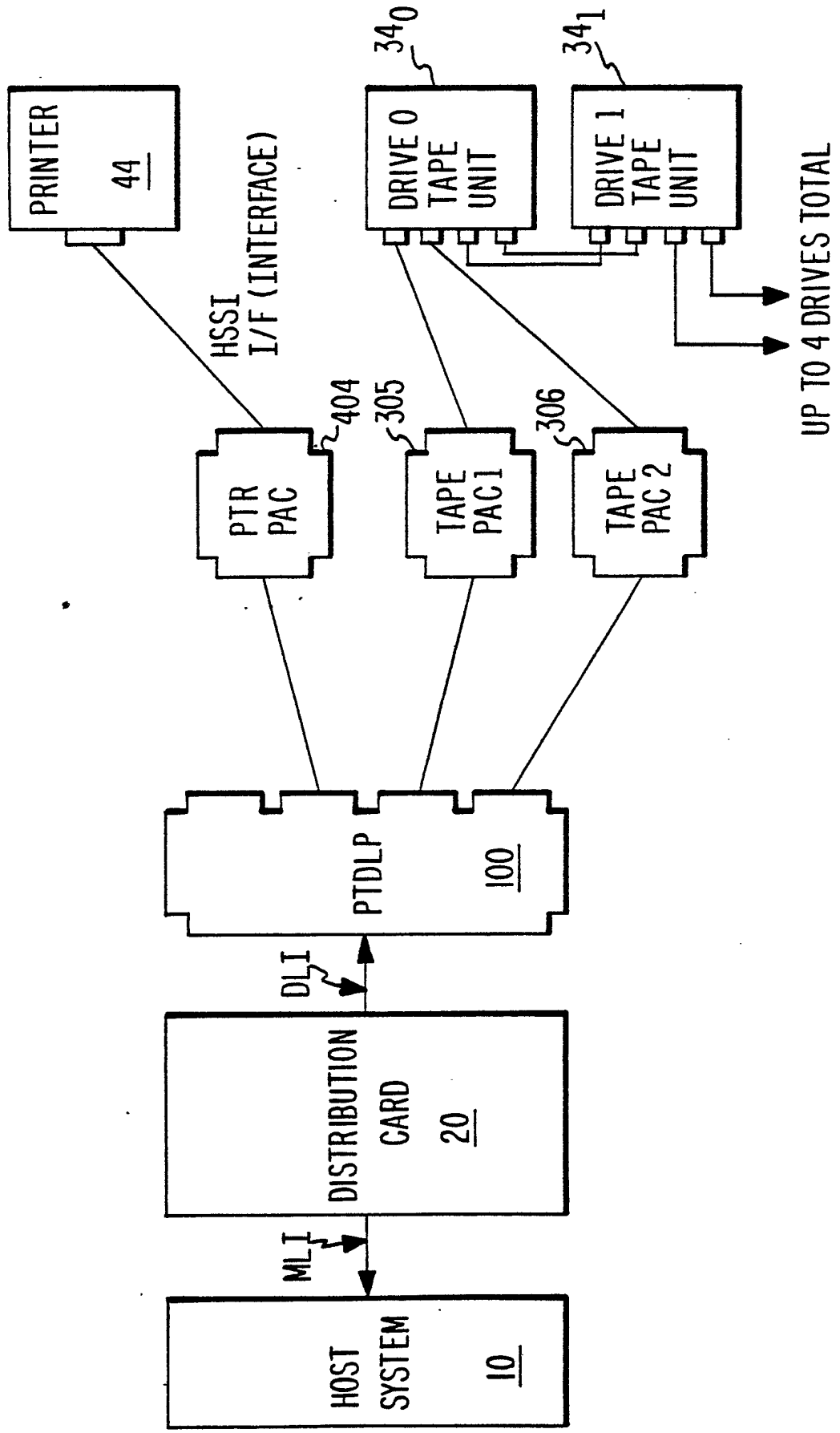
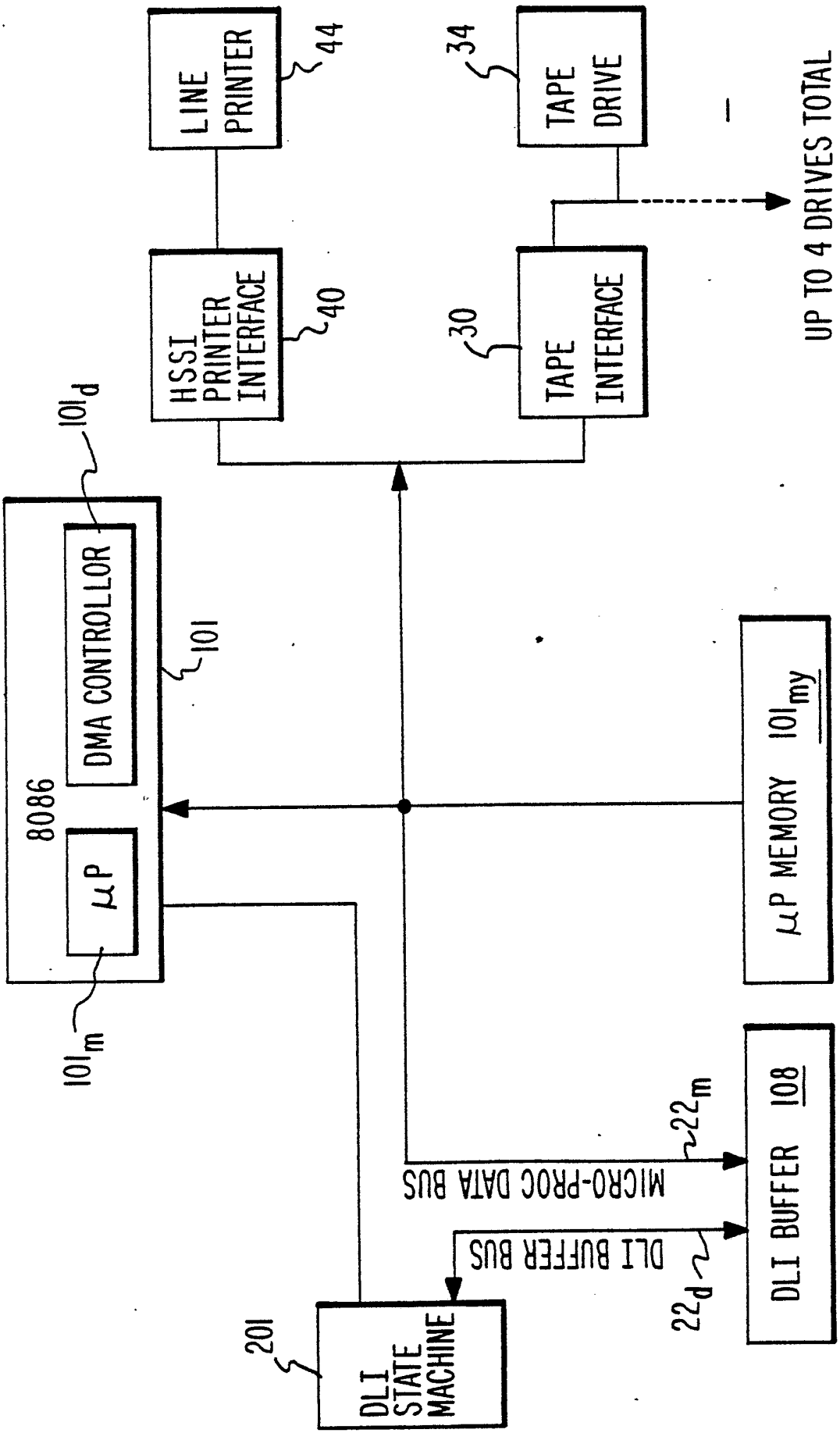

HOST SYSTEM 10
MLI
DISTRIBUTION CARD 20
DLI
PTDLP 100
PTR PAC
404
TAPE PAC1
305
TAPE PAC 2
306
HSSI I/F (INTERFACE)
PRINTER 44
DRIVE 0 TAPE UNIT
340
DRIVE 1 TAPE UNIT
341
UP TO 4 DRIVES TOTAL

FIG.1.

FIG.2. PRINTER / TAPE DLP (DATA FLOW).



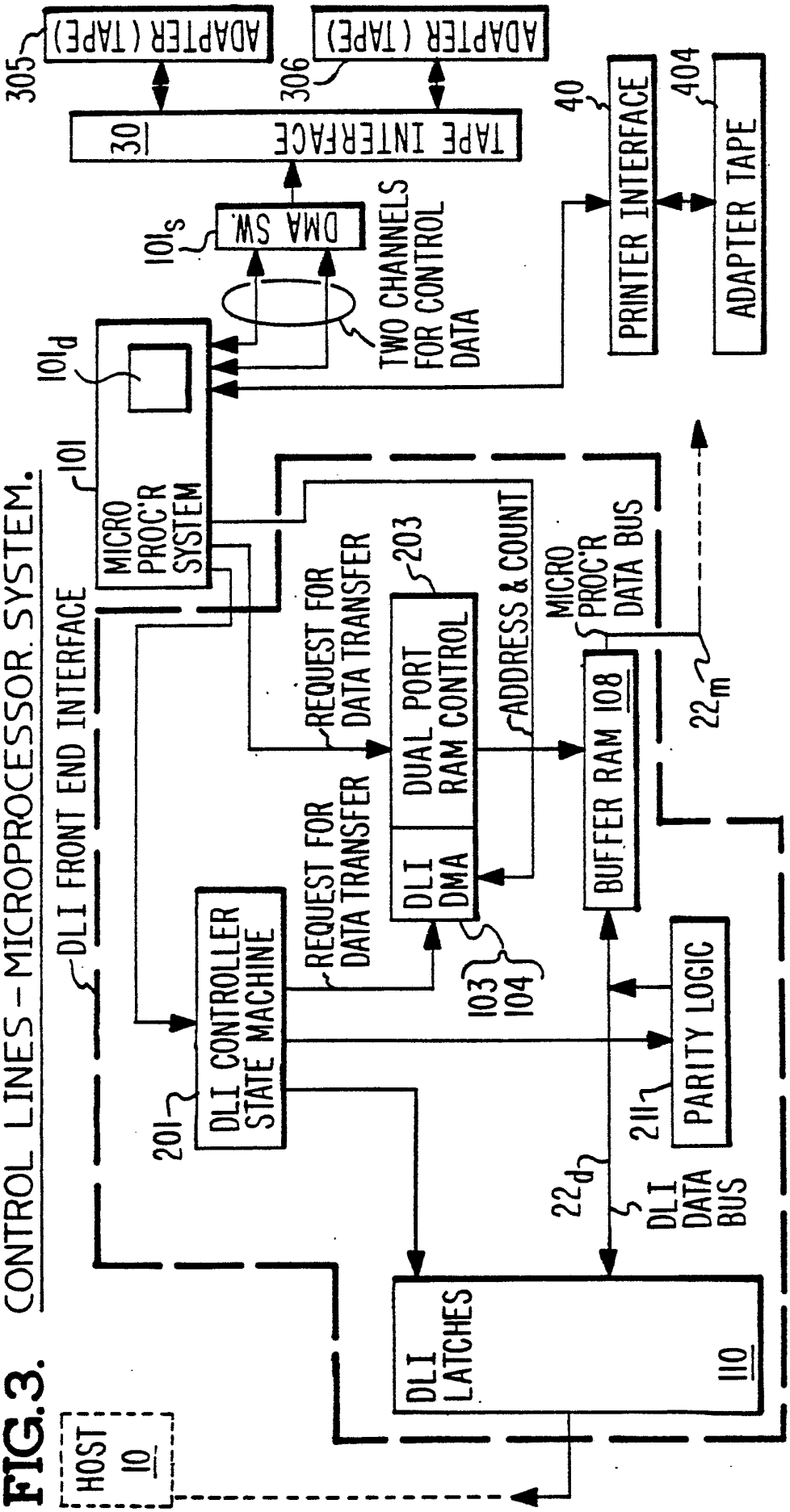

CONTROL LINES - MICROPROCESSOR SYSTEM.
HOST 10
DLI FRONT END INTERFACE
MICRO PROC'R SYSTEM 101
101d
DMA SW. 101s
TWO CHANNELS FOR CONTROL DATA
TAPE INTERFACE 30
ADAPTER (TAPE) 305
ADAPTER (TAPE) 306
PRINTER INTERFACE 40
ADAPTER TAPE 404
REQUEST FOR DATA TRANSFER
DUAL PORT RAM CONTROL 203
ADDRESS & COUNT
MICRO PROC'R DATA BUS
22m
BUFFER RAM 108
DLI DMA
103
104
REQUEST FOR DATA TRANSFER
DLI CONTROLLER STATE MACHINE
201
PARITY LOGIC
211
22d
DLI DATA BUS
DLI LATCHES
110

FIG.3.

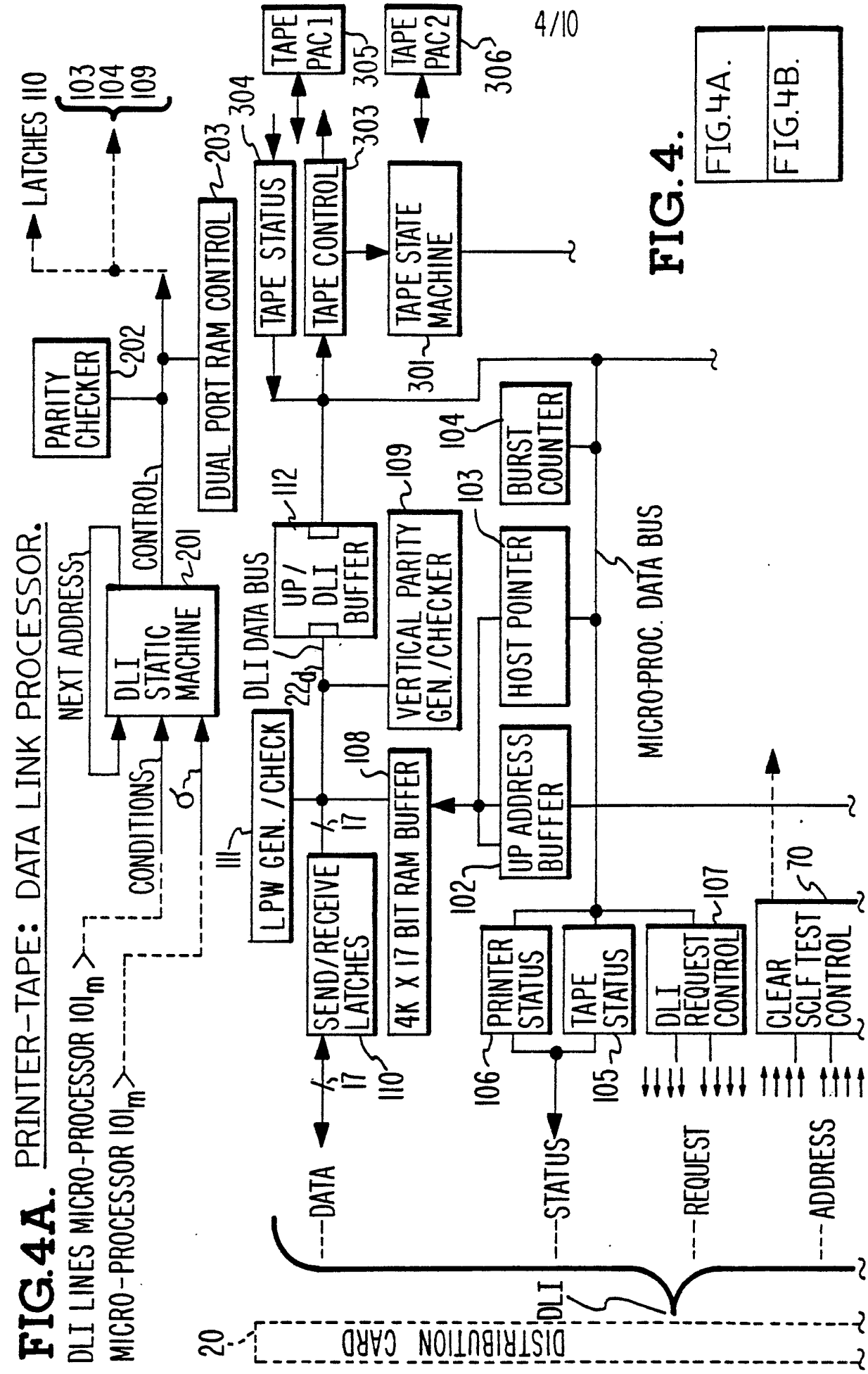


FIG.4A. PRINTER-TAPE: DATA LINK PROCESSOR.
DLI LINES MICRO-PROCESSOR 101m
MICRO-PROCESSOR 101m
CONDITIONS
NEXT ADDRESS
CONTROL
DLI STATIC MACHINE
201
PARITY CHECKER
202
LATCHES 110
103
104
109
DUAL PORT RAM CONTROL
203
TAPE STATUS
304
TAPE CONTROL
303
TAPE PAC 1
305
TAPE PAC 2
306
TAPE STATE MACHINE
301
DLI DATA BUS
UP/DLI BUFFER
112
VERTICAL PARITY GEN./CHECKER
109
BURST COUNTER
104
HOST POINTER
103
MICRO-PROC. DATA BUS
LPW GEN./CHECK
111
SEND/RECEIVE LATCHES
17
110
4K X 17 BIT RAM BUFFER
108
UP ADDRESS BUFFER
102
PRINTER STATUS
106
TAPE STATUS
105
DLI REQUEST CONTROL
107
CLEAR SCLF TEST CONTROL
70
DATA
STATUS
REQUEST
ADDRESS
DLI
DISTRIBUTION CARD
20
4/10
FIG. 4.
FIG.4A.
FIG.4B.

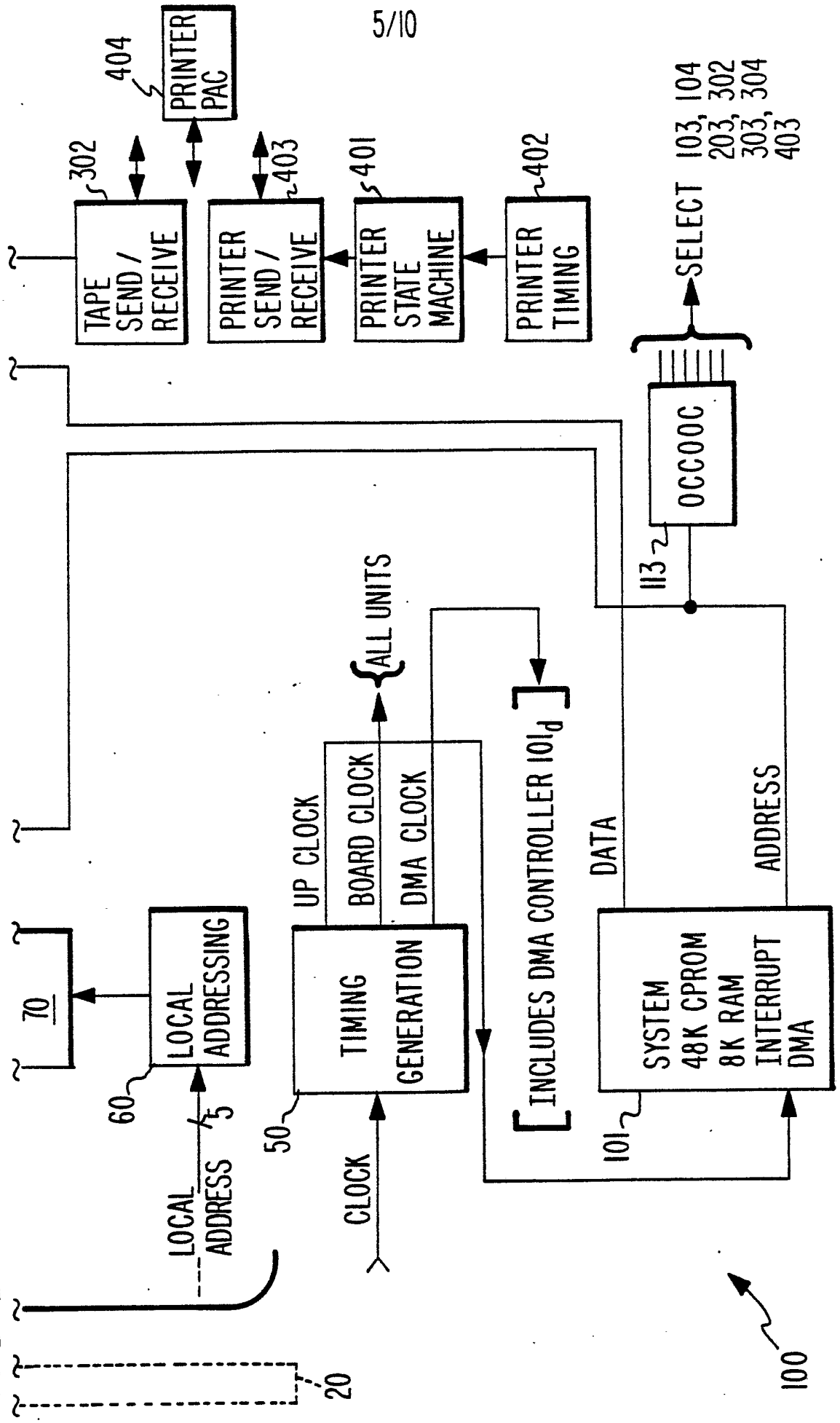
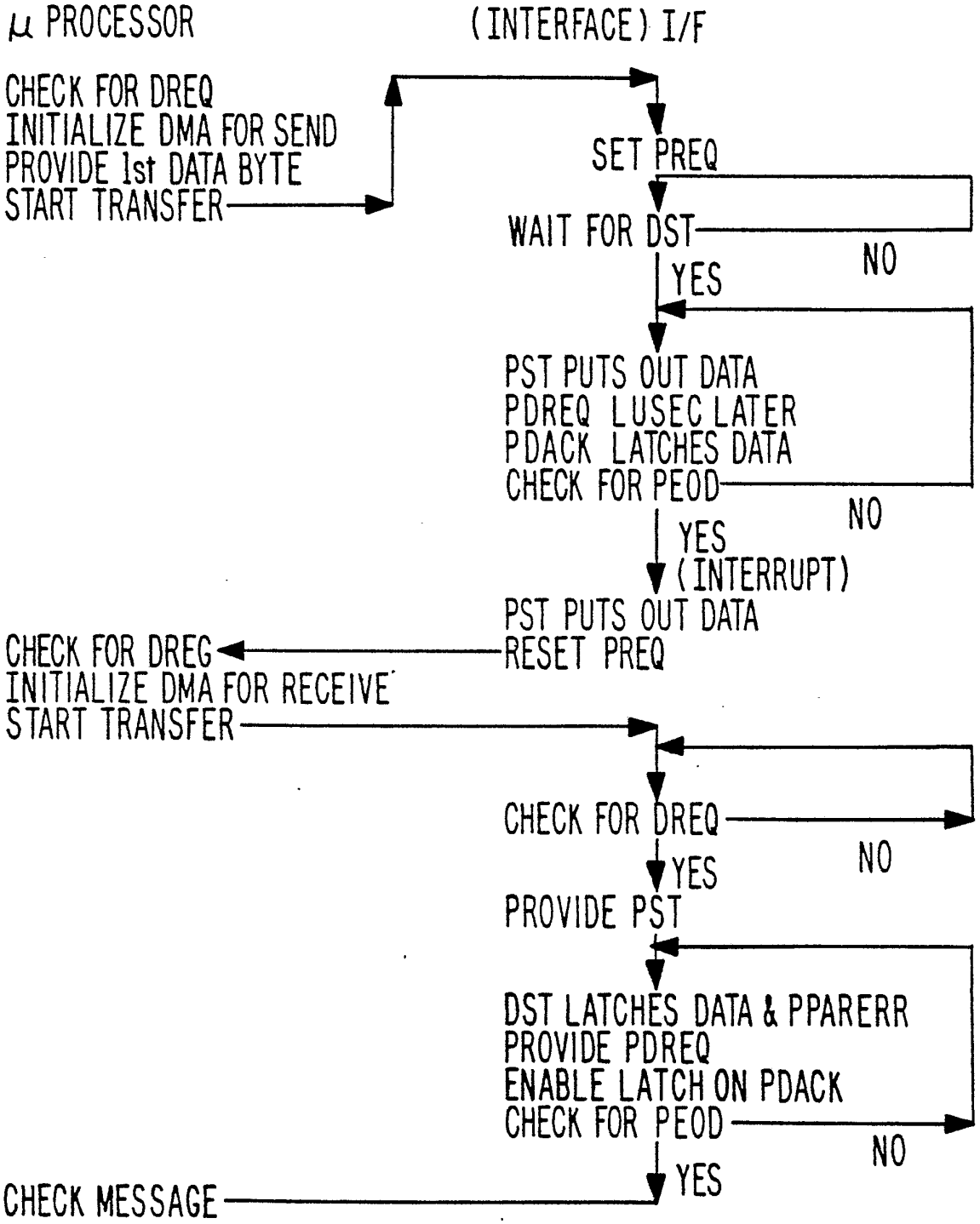

404
PRINTER PAC
302
403
401
402
TAPE SEND / RECEIVE
PRINTER SEND / RECEIVE
PRINTER STATE MACHINE
PRINTER TIMING
SELECT 103, 104 203, 302 303, 304 403
OCCOOC
113
ALL UNITS
UP CLOCK
BOARD CLOCK
DMA CLOCK
INCLUDES DMA CONTROLLER 101d
DATA
ADDRESS
70
LOCAL ADDRESSING
60
5
TIMING GENERATION
50
CLOCK
SYSTEM 48K CPROM 8K RAM INTERRUPT DMA
101
LOCAL ADDRESS
20
100

FIG.4B.

FIG.5.

PRINTER INTERFACE STATE MACHINE-FLOW CHART.



DREQ = DATA REQUEST
PREQ = PRINTER REQUEST
DST = DATA STROBE
PST = PRINTER STROBE
PDREQ = PRINTER-DATA REQ.

PEOD = PRINTER-END OF DATA
PDACK = PRINTER-DATA ACKn.

PPARERR = PRINTER-PARITY ERROR

FIG. 6. 7/10

TAPE INTERFACE STATE MACHINE-FLOW CHART.

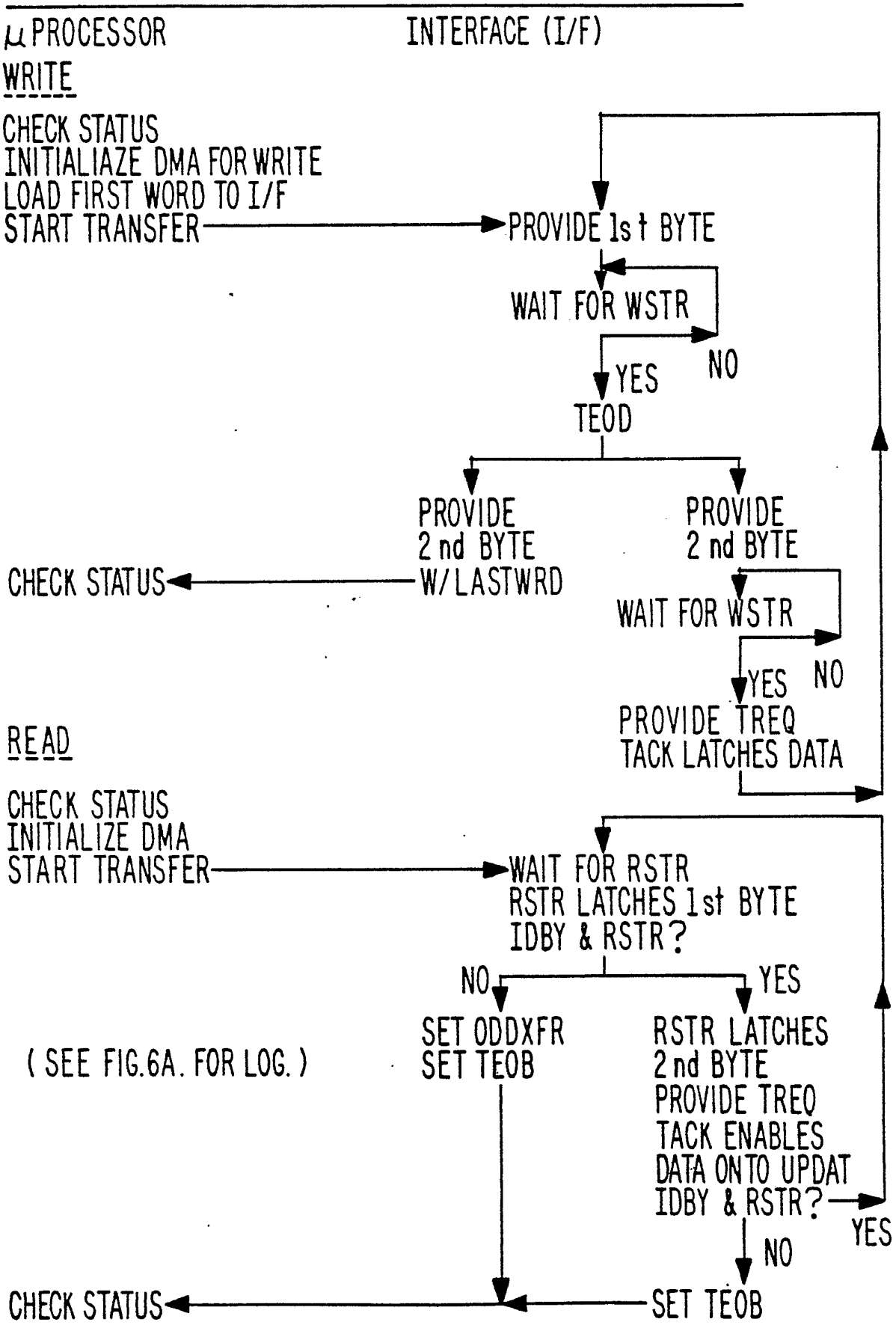


FIG.6A.

WSTR = WRITE STROBE
TEOD = TAPE-END OF DATA
WLASTWD = WRITE-LAST WORD
TEOB = TAPE-END OF BLOCK
TREQ = TAPE REQUEST
RSTR = READ STROBE
UPDAT = MICRO PROCESSOR DATA
IDBY = DATA-BUSY
ODD X FR = ODD BYTE-TRANSFER

FIG.7A.

CLK = CLOCK
ALE = ADDRESS LATCH ENABLE
M/IO = MEMORY or I/O SELECT
AD∅15 = ADDRESS LINES 0-15
$\overline{RD}$ = READ
DT/$\overline{R}$ = DATA { TRANSMIT / RECEIVE }

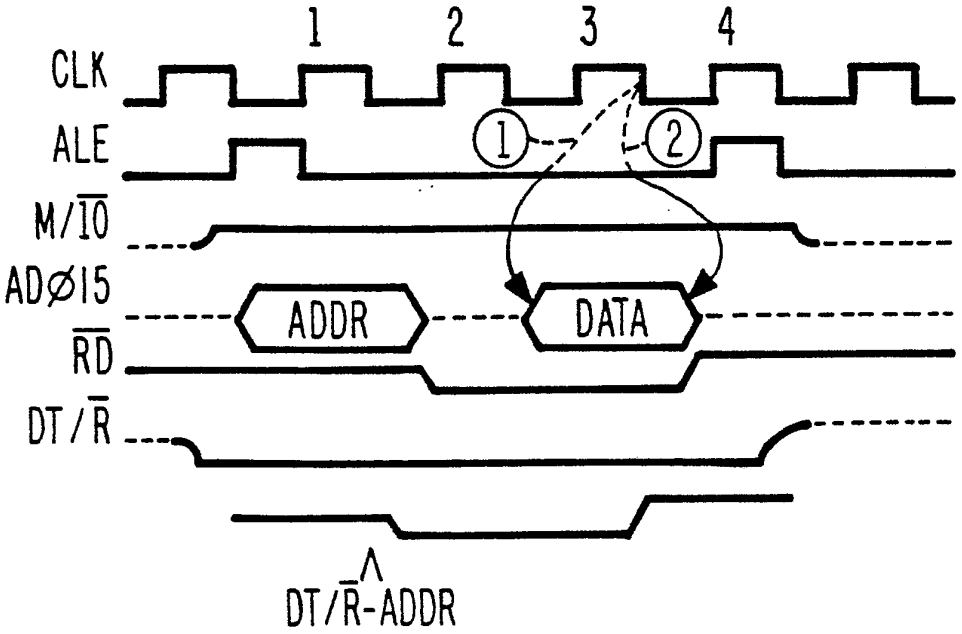
NOTE:

DUAL PORT RAM WILL HAVE NECESSARY ACCESS INFORMATION BY END OF CLOCK ONE (1), ALLOWING INTERLEAVED ACCESS IN EITHER CLOCK TWO (2) OR CLOCK THREE (3).

① 20 NS SETUP
② 10 NS HOLD
③ 60 NS DELAY
④ 10 NS DELAY

FIG.7. MICRO-PROCESSOR / DLI BUFFER TIMING.

READ: (MICRO-PROCESSOR SYSTEM.) (SEE FIG.7A.)



WRITE: (MICRO-PROCESSOR SYSTEM USING MICRO-PROC. DMA CONTROLLER.)

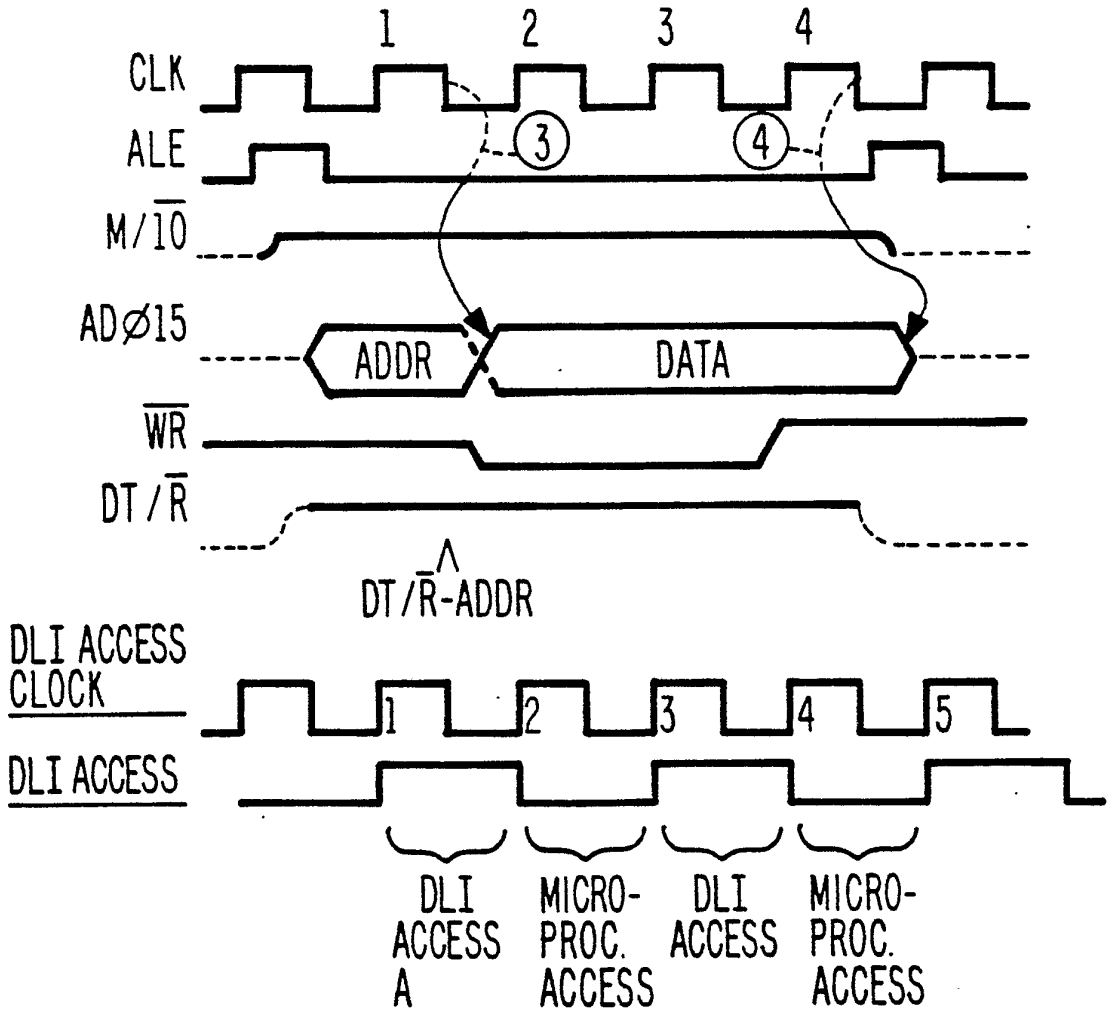
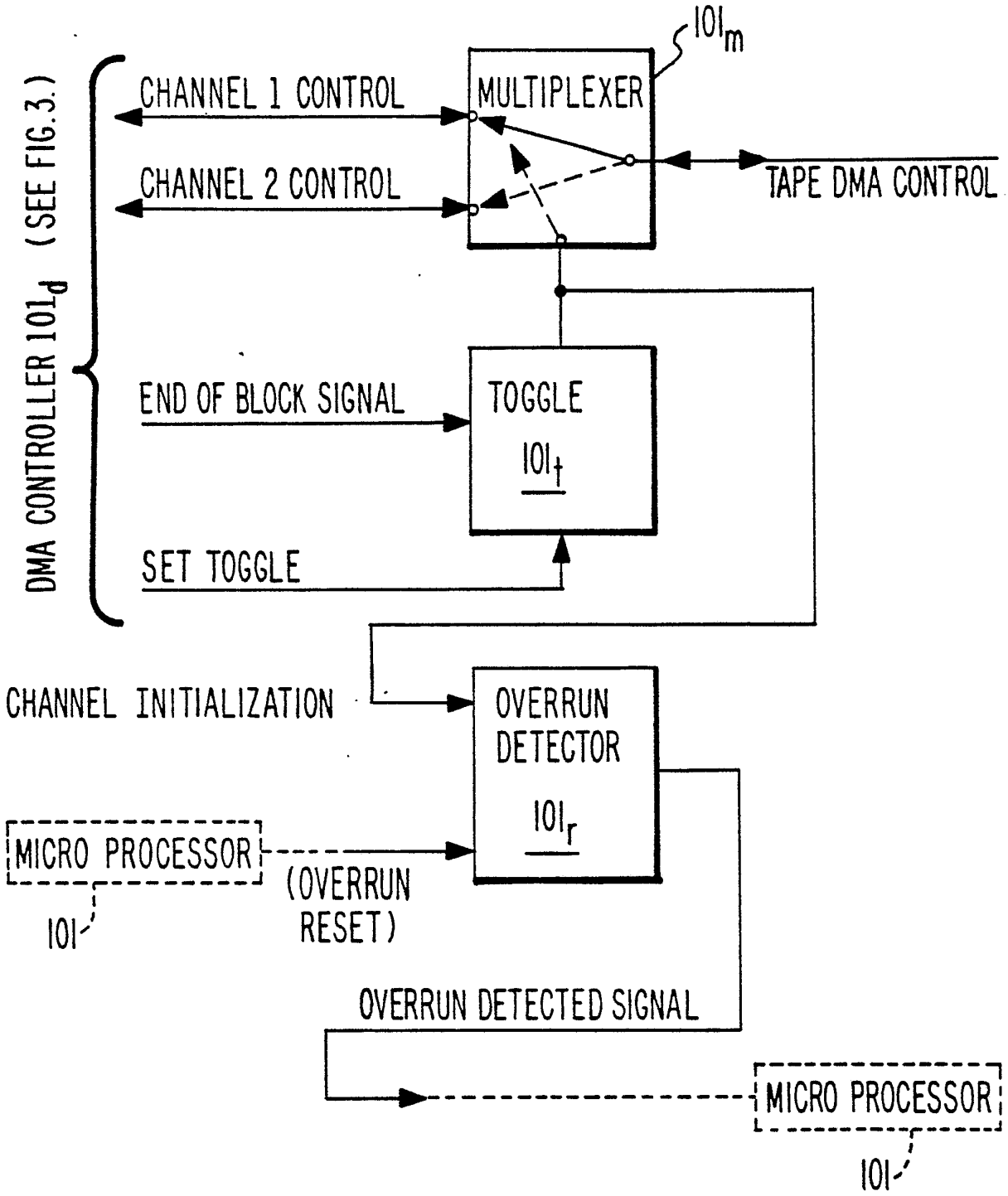


FIG.8. 10/10


101m
MULTIPLEXER
CHANNEL 1 CONTROL
CHANNEL 2 CONTROL
TAPE DMA CONTROL
DMA CONTROLLER 101d (SEE FIG.3.)
END OF BLOCK SIGNAL
TOGGLE
101t
SET TOGGLE
CHANNEL INITIALIZATION
OVERRUN DETECTOR
101r
MICRO PROCESSOR
101
(OVERRUN RESET)
OVERRUN DETECTED SIGNAL
MICRO PROCESSOR
101

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 86/00009

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[4]: G 06 F 13/12

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC[4]	G 06 F 13/12 G 06 F 13/42 G 06 D 13/38

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
A	US, A, 3573852 (WATSON) 6 April 1971, see column 1, lines 65-75; column 4, lines 9-33; column 17, lines 38-75; column 18, lines 1-42,72-75; column 19, lines 1-21; figures 2,10,11 --	1,2,6,10
A	Computer, volume 12, no. 6, June 1979, Long Beach, (US) El-Ayat:"Special feature the Intel 8089: An integrated I/o processor", pages 67-78, see page 68, column 1, lines 3-20; figure 1; page 70, column 1, lines 13-27; column 2, lines 1-22; figure 4; page 71, figure 6; page 75, column 1, lines 32-51; page 76, column 1, lines 1-6; column 2, lines 1-8; figure 8 --	1,4-7
A	EP, A2, 0121364 (SHETH) 10 October 1984, see page 1, lines 3-8; page 4, lines 11-28; page 5, lines 1-15; page 7, lines 30-32; page 9, lines 2-8; page 10, lines 9-14; page 11, lines 5-11; page 13, lines 8-20; page 14, lines 23-30; page 17, lines 14-19; page 19, lines 27-32	1,2,3,6 ./.

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
16th April 1986	22 MAI 1986
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	VAN MOL

Form PCT/ISA/210 (second sheet) (January 1985)

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category *	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No
	page 20, lines 1-2; page 21, lines 1-3; figures 1,2,4	
	--	
A	EP, A3, 0080890 (HARRIS) 8 June 1983, see page 7, lines 19-29; page 10, lines 29-32; page 11, lines 7-35; page 14, lines 5-10; page 53, lines 5-28; figures 1A,2, 7,8,9	1,2,4,6
	--	
A	US, A, 4162520 (COOK) 24 July 1979, see column 17, lines 53-68; column 18, lines 1-7,55-68; column 19, lines 1-63; figures 1A-1E (cited in the application)	1,2,6
	--	
A	IBM Technical Disclosure Bulletin, volume 26, no. 12, May 1984, New York, (US) Satoh:"Terminal communications adapter", pages 6504-6505, see figure 1 on page 6504; page 6505, lines 1-6,12-16	2,3,6,10, 11
	--	
A	IBM Technical Disclosure Bulletin, volume 22, no. 1, June 1979, New York, (US) Hays:"Standard printer or I/o adapter control method and apparatus", pages 269-271, see figure on page 269; page 270, lines 9-19	2,3,6,9,10, 11

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/US 86/00009 (SA 11896)

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 06/05/86

The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
US-A- 3573852	06/04/71	NL-A-	6913243	03/03/70
		DE-A-	1942005	05/03/70
		FR-A-	2017099	15/05/70
		GB-A-	1278103	14/06/72
		BE-A-	738171	02/02/70
EP-A- 0121364	10/10/84	JP-A-	59184927	20/10/84
EP-A- 0080890	08/06/83	WO-A-	8302021	09/06/83
		US-A-	4443850	17/04/84
US-A- 4162520	24/07/79	BE-A-	859169	16/01/78
		FR-A,B	2371730	16/06/78
		JP-A-	53043443	19/04/78
		GB-A-	1574470	10/09/80
		CA-A-	1112324	10/11/81
		CH-A-	632350	30/09/82