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(54) **Title:** ELIMINATION OF BASAL PLANE DISLOCATIONS IN POST GROWTH SILICON CARBIDE EPITAXIAL LAYERS BY HIGH TEMPERATURE ANNEALING WHILE PRESERVING SURFACE MORPHOLOGY

(57) **Abstract:** A method to remove basal plane dislocations in post growth silicon carbide epitaxial layers by capping post growth silicon carbide epilayers with a graphite cap and annealing the capped silicon carbon epilayers at a temperature of 1750 °C or greater with a nitrogen overpressure of 60-110 psi, wherein basal plane dislocations in the epilayers are removed while surface morphology is preserved. Also disclosed is the related silicon carbide substrate material made by this method.



ELIMINATION OF BASAL PLANE DISLOCATIONS IN POST GROWTH SILICON CARBIDE EPITAXIAL LAYERS BY HIGH TEMPERATURE ANNEALING WHILE PRESERVING SURFACE MORPHOLOGY

TECHNICAL FIELD

5 The present invention relates to removing basal plane dislocations in silicon carbide (SiC) epitaxially grown layers.

BACKGROUND ART

Basal plane dislocations (BPD) in SiC epilayers cause formation of stacking faults (SF) during device operation, which leads to forward voltage degradation in minority carrier devices.

10 Typical growth of SiC epilayers using conventional chemical vapor deposition techniques still results in BPD density of 100 cm^{-2} or more. These adversely affect the device yield and reliability. There are no known reports that successfully attempt to mitigate the BPDs in the SiC epilayers after the epi-growth. High temperature annealing in SiC epilayers has been performed by various methods for incorporation of implanted species and to reduce the lattice damage

15 caused by the implantation process. These previous anneals were typically performed up to 1700 °C, using a graphite cap to reduce surface degradation.

DISCLOSURE OF INVENTION

The aforementioned problems are overcome in the present invention which provides a method to remove basal plane dislocations in post growth silicon carbide epitaxial layers by

20 capping post growth silicon carbide epilayers with a graphite cap and annealing the capped silicon carbon epilayers at a temperature of 1750 °C or greater with a nitrogen overpressure of 60-110 psi, wherein basal plane dislocations in the epilayers are removed while surface morphology is preserved. Also disclosed is the related silicon carbide substrate material made by this method.

25 The purpose of this invention is to provide a means to remove basal plane dislocations already present in silicon carbide (SiC) epitaxially grown layers, while preserving the surface morphology. This method uses a high temperature annealing process under high ambient pressure and utilizes a surface protective coating on epitaxially grown SiC layers to remove the basal plane dislocations present in it. There are no reported methods for the removal of BPDs

30 after the growth of SiC epilayers, while preserving the surface morphology.

The subject of the invention is single crystal silicon carbide (SiC) substrate material and epilayers grown by any typical methods. The invention provides means to remove defects, while preserving the sample surface in SiC semiconductors. More specifically the invented method

uses a high temperature annealing process is used under high ambient pressure and utilizing a surface protective coating to eliminate basal plane dislocations (BPD) in SiC samples. This invention can be used to remove BPDs from SiC epitaxial layers after their growth, while preserving the surface morphology, which is important to realize high power density and high voltage SiC devices.

This invention can be used to anneal p-type implants in SiC to form higher conductivity p-type semiconductor regions, while preserving the surface.

This invention can be used to perform high temperature treatments to SiC to improve carrier lifetime in both p-type and n-type SiC layers.

Some advantages of the prevent invention include: BPDs are eliminated in SiC material while maintaining good surface morphology; compared to current methods, higher temperature annealing (in excess of 1750 °C) of SiC material can be used with no silicon sublimation from the surface, which prevents surface degradation; and higher temperature annealing (in excess of 1750 °C) can be used to improve the activation/incorporation of implanted species in the SiC lattice.

These and other features and advantages of the invention, as well as the invention itself, will become better understood by reference to the following detailed description, appended claims, and accompanying drawings.

BRIEF DESCRIPTION OF DRAWINGS

FIG. 1 is shows (a) an ultraviolet photoluminescence (UVPL) image of a pre-annealed sample and (b) a UVPL image showing the same exact region of the post-annealed sample that was treated at 1782 °C for 5 minutes under 100 psi nitrogen over pressure.

BEST MODE FOR CARRYING OUT THE INVENTION

The purpose of the present invention is to remove the existing BPDs in the SiC epilayers while preserving the surface morphology. This requires high temperature annealing in excess of 1750 °C and has been accomplished by annealing the SiC samples under high nitrogen overpressure of 60-110 psi. The samples are capped with a specially formulated graphite cap to further prevent the sublimation of Si from the surface and thus preserve the surface morphology.

For experimentation, commercially available, 4 degree offcut, 15 μm, n-type 6E15 4H-SiC epilayers were used. The as-grown samples were imaged using ultraviolet photoluminescence (UVPL) imaging, which shows the BPDs in the epitaxial layers prior to annealing. Carriers were excited with the 334 nm line from an Ar-ion laser, and images were

collected in the emission range of 600-1000 nm. The high resolution images of the entire sample was stitched together and analyzed

The samples were then graphite capped using the following process. The samples were cleaned with a pirana solution consisting of $\text{H}_2\text{SO}_4\text{:H}_2\text{O}_2\text{:H}_2\text{O}$ in the ratio 1:1:5, followed by a solvent clean SC1 process. Then AZ 4620 photoresist was applied using a revolution speed of 5000 rpm for 1 minute. The samples were then heated to a temperature of 1100 °C in nitrogen ambient for 30 minutes to form a graphite cap. This was followed by the high temperature high pressure annealing process.

The high pressure annealing was carried out in a custom designed chamber, where the sample was inductively heated using radio frequency (RF) power to temperatures 1750 - 1840 °C for around 5 minutes. The chamber was maintained at a nitrogen over pressure of 60-110 psi. The post-annealed samples were then imaged to observe the removal of BPDs in the epilayers.

The imaging of the BPDs post-annealing was again performed using the UVPL system as described above. The images were then compared to their pre-annealed state. FIG. 1(a) shows the UVPL image of the pre-annealed sample. The white (bright) lines observed are the BPDs that are present in the epilayers after growth. This image is compared with the image shown in FIG. 1(b), which shows the same exact region of the post-annealed sample that was performed at 1782 °C for 5 minutes under 110 psi nitrogen over pressure. It can be clearly seen that the BPDs (white lines) in the post annealed samples completely disappear. In addition the surface morphology of the sample is preserved as no scratches or surface imperfections are evident in the UVPL image. This was also further verified using optical microscopy.

The above descriptions are those of the preferred embodiments of the invention. Various modifications and variations are possible in light of the above teachings without departing from the spirit and broader aspects of the invention. It is therefore to be understood that the claimed invention may be practiced otherwise than as specifically described. Any references to claim elements in the singular, for example, using the articles “a,” “an,” “the,” or “said,” is not to be construed as limiting the element to the singular.

CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method to remove basal plane dislocations in post growth silicon carbide epitaxial layers, comprising:
 - capping post growth silicon carbide epilayers with a graphite cap; and
 - annealing the capped silicon carbon epilayers at a temperature of 1750 °C or greater with a nitrogen overpressure of 60-110 psi, wherein basal plane dislocations in the epilayers are removed while surface morphology is preserved.
2. The method of claim 1, wherein the annealing is for five minutes.
3. The method of claim 1, wherein the annealing is done by inductive heating using radio frequency power.
4. The method of claim 1, wherein the silicon carbon epilayers are capped by a method comprising:
 - cleaning the epilayers with a solution comprising H_2SO_4 , H_2O_2 , and H_2O followed by a solvent clean SC1 process;
 - applying a photoresist; and
 - heating to a temperature of 1100 °C in nitrogen ambient.
5. The method of claim 4, wherein the ratio of H_2SO_4 : H_2O_2 : H_2O is 1:1:5.
6. The method of claim 4, wherein the heating is for 30 minutes.
7. A silicon carbide substrate material made by the method comprising:
 - capping post growth silicon carbide epilayers with a graphite cap; and
 - annealing the capped silicon carbon epilayers at a temperature of 1750 °C or greater with a nitrogen overpressure of 60-110 psi, wherein basal plane dislocations in the epilayers are removed while surface morphology of the substrate material is preserved.
8. The silicon carbide substrate material of claim 7, wherein the annealing is for five minutes.

9. The silicon carbide substrate material of claim 7, wherein the annealing is done by inductive heating using radio frequency power.

10. The silicon carbide substrate material of claim 7, wherein the silicon carbon epilayers are capped by a method comprising:

cleaning the epilayers with a solution comprising H_2SO_4 , H_2O_2 , and H_2O followed by a solvent clean SC1 process;

applying a photoresist; and

heating to a temperature of 1100 °C in nitrogen ambient.

11. The silicon carbide substrate material of claim 10, wherein the ratio of $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ is 1:1:5.

12. The silicon carbide substrate material of claim 10, wherein the heating is for 30 minutes.

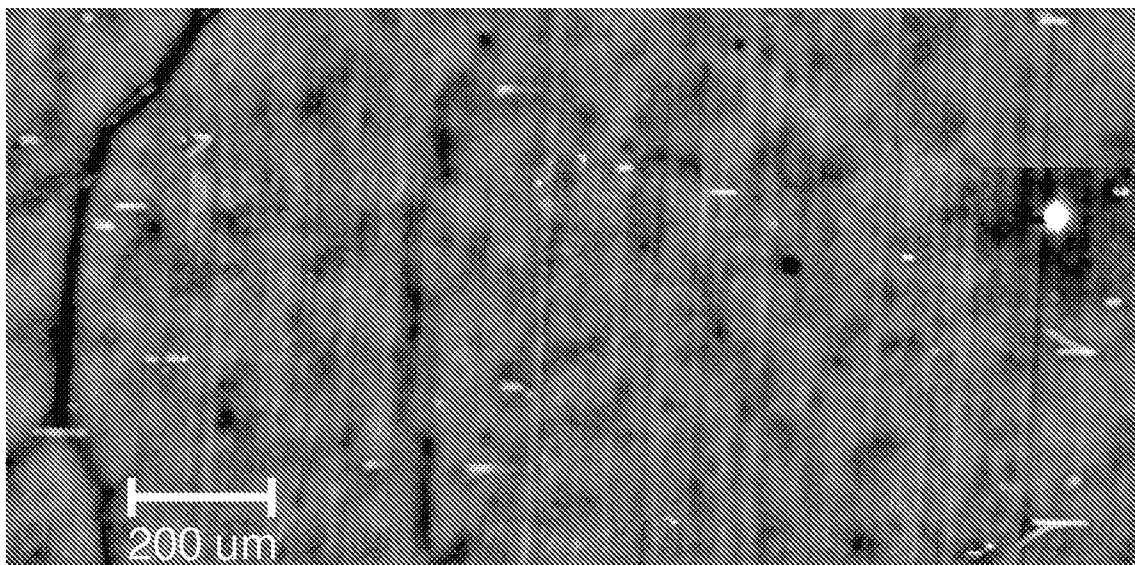


FIG. 1(a)

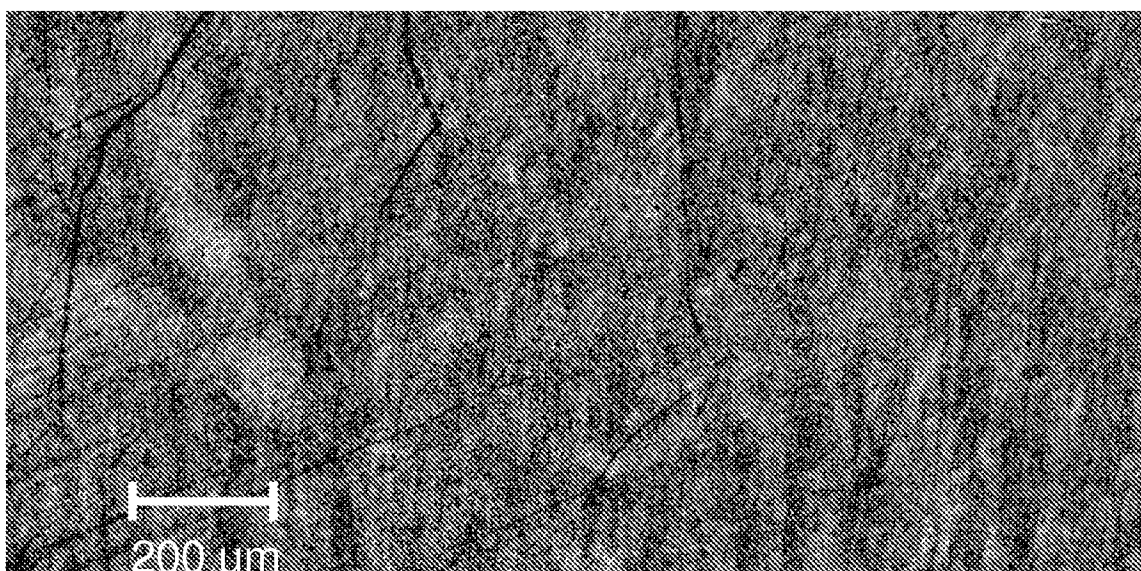


FIG. 1(b)

A. CLASSIFICATION OF SUBJECT MATTER**C30B 29/36(2006.01)i, C30B 15/00(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

C30B 29/36; C30B 15/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: basal plane dislocations, post growth, silicon carbide, epitaxial, graphite cap

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	MAHADIK, N. A. et al., "Basal Plane Dislocation Mitigation using High Temperature Annealing in 4H-SiC Epitaxy", ECS Transactions, 58 (4) pp. 325-329 See abstract; page 326.	1-3,7-9
Y		4-6,10-12
X	SANCHEZ, S et al., "Spontaneous direct bonding of thick silicon nitride", J. Micromech. Microeng. 7, 1997, pages 111-113 see page 111, right column.	1-3,7-9
Y		4-6,10-12
A	TSUCHIDA, H. et al., "Growth and characterization of thick 4H-SiC epilayers for very high voltage bipolar devices", ECS Transactions, 58 (3) pages 109-118 (2012) See abstract.	1-12
A	TADJER, MARKO J. et al., "Nanocrystalline diamond films as UV-semitransparent Schottky contacts to 4H-SiC", Applied Physics Letters 91, 163508, 2007 See abstract.	1-12



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

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INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2014/057722

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JONES, K. A. et al., "A Comparison of Graphite and AlN Caps Used for Annealing Ion-Implanted SiC", Journal of ELECTRONIC MATERIALS, Vol. 31, No. 6, 2002, pages 568-575 See abstract.	1-12

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2014/057722Patent document
cited in search reportPublication
datePatent family
member(s)Publication
date

None