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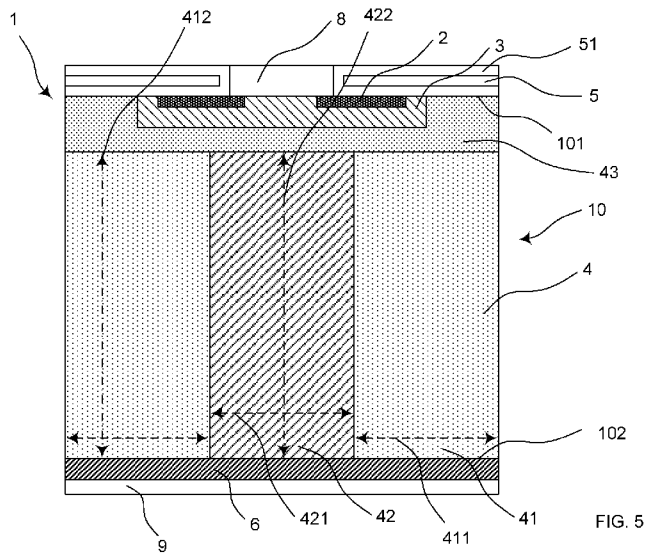

FIG. 5

(57) Abstract: A power semiconductor device (1) is provided with a semiconductor wafer (10) and a first electrical contact (8) being formed on a first main side (101) of the wafer and a second electrical contact (9) being formed on a second main side (102) of the wafer opposite the first main side (101). The wafer (10) comprises a structure with a plurality of layers of different conductivity types. It comprises at least one source region (2) of the first conductivity type contacting the first electrical contact (8), at least one base region (2) of a second conductivity type contacting the first electrical contact (8), a base layer (4) and a gate electrode, which is electrically insulated by an insulation layer (51) from the source region (2) and the base region (3). The base layer (4) comprises at least one first pillar (41) of the first conductivity type and at least one second pillar (42) of the second conductivity type, the first and second pillars (41, 42) being arranged alternately in the same plane. At least one second pillar (42) is not in contact with the base region (3).

WO 2010/142342 A1

Power semiconductor device

Description

Technical Field

The invention relates to the field of power electronics and more particularly to a power semiconductor device according to the preamble of claim 1.

Background Art

Often the driving force in ultra-high voltage insulated gate bipolar transistor (IGBTs) (above 3.3 kV) is not an improvement in the on-state versus switching trade-off as is the case in lower voltage IGBTs, but a wider safe operating area (SOA) and a long-term reliability when exposed to continuous high voltages. A dominant failure mode in high voltage IGBTs is the cosmic ray induced breakdown: when operated continuously at the rail voltage, which voltage is about half of the rated breakdown voltage, some devices start to loose their blocking capability far below the rated maximum blocking voltage. The failure in time (FIT) rate is highly dependent on the peak electric field in the drift region and increases with the applied blocking voltage as shown in the documents “Cosmic Ray induced failures in high power semiconductor devices”, Solid State Electron 1995 38(12): 2041-2046, by Zeller HR. Therefore, engineering the base layer to minimize the peak field under DC rail voltage is essential.

In the publications “The super junction bipolar transistor: a new silicon power device concept for ultra low loss switching applications at medium to high voltages”, Solid State Electronics, vol. 48, pp. 705-714, 2004, F.

Bauer; and "A Simulation Study on Novel Field Stop IGBTs Using Superjunction", IEEE Transactions On Electron Devices, Vol. 53, No. 4, April 2006, Kwang-Hoon Oh et al. it was shown that, for a 1.2 kV device layout, the Superjunction Insulated Gate Bipolar Transistor (SJ-IGBT) can open new paths to surpass the limitations of current state-of-the-art silicon IGBTs with respect to the on-state and the turn-off performance.

FIG. 1 shows a prior art superjunction IGBT 11 as described in "The super junction bipolar transistor: a new silicon power device concept for ultra low loss switching applications at medium to high voltages", Solid State Electronics, vol. 48, pp. 705-714, 2004, F. Bauer. It comprises a semiconductor wafer 10 and a cathode electrode 8', which is formed on a cathode side 101' of the wafer, and an anode electrode 9', which is formed on an anode side 102' of the wafer opposite the cathode side 101'. The semiconductor wafer 10 comprises a structure with a plurality of layers of different conductivity types:

- n doped source regions 2 contacting the cathode electrode 8',
- a p doped base region 3 contacting the cathode electrode 8',
- a base layer 4, which comprises n doped first pillars 41 and p doped second pillars 42, the first and second pillars 41, 42 being arranged alternately in the same plane,
- a planar gate electrode 5, which is electrically insulated by an insulation layer 51 from the source region 2 and the base region 3, and a buffer layer 62, which is arranged on the anode side 9' of the wafer.

The p doped second pillars 42 contact the p doped base region 3.

Unlike the field stop IGBT structure (which is shown in Fig. 3), also called soft punch-through IGBT, where the doping of the base layer has little influence on the static and dynamic characteristics of the device, it was shown in the document by Bauer F, "The super junction bipolar transistor: a new silicon power device concept for ultra low loss switching applications at

medium to high voltages", Solid State Electronics, vol. 48, pp. 705-714, 2004, that the SJ-IGBT overall efficiency is drastically influenced by the doping densities in the n and p pillars, in the n-buffer and the anode layer.

FIG. 2 shows a prior art semi superjunction IGBT 12 as it is for example described in "A Simulation Study on Novel Field Stop IGBTs Using Superjunction", IEEE Transactions On Electron Devices, Vol. 53, No. 4, April 2006, Kwang-Hoon Oh et al., which differs from the superjunction IGBT 11 in that between the buffer layer 62 and the first and second pillars 41, 42 a first n doped layer 44 is arranged, which is a continuous layer ranging over the whole plane of the wafer 10. By such a design, the costly manufacturing of the pillars can be reduced to a smaller height than for the case of a full superjunction IGBT.

Another concept for achieving low losses are Trench FS-IGBTs, with which an on state plasma distribution can be realized, which allows to achieve a better trade off between on-state and turn-off losses. This further makes it possible to introduce a transparent anode, which again is advantageous for the on-state and switching. The trench gate brings with it a more natural 1D current distribution, eliminates the parasitic JFET effect, enhances the PIN diode effect, i.e. the electron injection into the top side of the base layer, minimizes the MOS channel resistance and increases the immunity against latch-up. Fig. 3 shows the structure of such a Trench Field Stop IGBT 13. The Trench FS IGBT comprises a gate electrode 5, which is arranged in the same plane as the base region 3 and adjacent to the source region 2, separated from each other by an insulation layer 51, which also separates the gate electrode 5 from the base layer 10 and the first electrical contact 8. However, the trench gate IGBT has limits caused by the high electric field around the trench corners which can degrade its reliability and SOA performance. Further on, it is more difficult to achieve low short circuit currents in this particular IGBT geometry.

Disclosure of Invention

It is an object of the invention to provide a power semiconductor device

and its manufacturing method with an optimized structure concerning switching versus on-state losses, and cosmic ray induced breakdown immunity.

This object is achieved by a power semiconductor device according to claim 1.

The inventive power semiconductor device 1 comprises a semiconductor wafer 10 and a first electrical contact 8, which is formed on a first main side 101 of the wafer, and a second electrical contact 9, which is formed on a second main side 102 of the wafer opposite the first main side 101. The semiconductor wafer 10 comprises a structure with a plurality of layers of different conductivity types:

- at least one source region 2 of the first conductivity type contacting the first electrical contact 8,
- at least one base region 3 of a second conductivity type contacting the first electrical contact 8,
- a base layer 4, which comprises at least one first pillar 41 of the first conductivity type and at least one second pillar 42 of the second conductivity type, the first and second pillars 41, 42 being arranged alternately in the same plane,
- a gate electrode 5, 5', which is electrically insulated by an insulation layer 51 from the source region 2 and the base region 3.

Each source region 2 is arranged on the first main side 101 of the wafer and separated from the base layer 4 by a base region 3. At least one second pillar 42 is not in contact with the base region 3.

When comparing an inventive semiconductor device in form of an IGBT to a standard Trench FS IGBT the cosmic radiation induced breakdown rate is significantly improved in the inventive IGBT as the electric field at the first main side of the base layer is effectively flattened (Fig. 19). This means that the peak of the electric field in the structure is reduced (at the given rail voltage – i.e. half of the rated voltage).

FIG. 18 shows the improvement in reducing overvoltages during switching in the inventive semiconductor devices (an inventive device with a planar gate electrode has been used) compared to a prior art superjunction IGBT. Superjunction IGBTs with p doped second pillars in contact to the base region exhibit quasi-unipolar device characteristics in proximity of the cathode. During the switching high overvoltages are produced because no plasma is available between the base region and the second pillar. This results for these prior art devices in higher overvoltages during the switching as can be seen in Fig. 18, whereas the inventive device shows a much smoother behaviour of the voltage.

The inventive IGBT offers significant improvement in the on-state and switching trade-off compared to both prior art Field Stop (FS) Trench IGBT and the SJ IGBT or semi SJ IGBT. Especially for small on-state voltages, the inventive devices have much lower turn-off switching losses than the prior art devices as is shown in Fig. 17. Furthermore, the inventive devices can be operated at smaller absolute on-state voltages than the prior art SJ-IGBTs (90 µm pillar height) or semi SJ-IGBTs (10 and 50 µm pillar height).

Such an inventive semiconductor device maintains a high static and dynamic avalanche breakdown while at the same time improving dramatically (by one to two orders of magnitude) the FIT rate under cosmic ray exposure.

Furthermore the device offers considerably better robustness against cosmic rays when compared to a conventional FS IGBT. This can be proved via analytical modeling that the FIT (Failure in Time) levels can be improved by one to two orders of magnitude (see FIG. 20). All devices for the modeling have a wafer height of 400 µm and the inventive device has a pillar doping concentration of $2 * 10^{15}$ cm^{-3}.

In order to improve the on state voltage drop, p doped second pillars 42 are separated from the base region 3 by an n doped part of the base layer 4 (e.g. by a disconnection layer 43 or by an n doped first pillar 41) so that there is no direct connection between the p doped second pillar 42 and the

p doped base region 3 and the second pillar 42 is thereby separated from the base region 3. The inventive semiconductor device may comprise only one active cell with one or more separated second pillars 42. The device may also comprise a plurality of cells with one, a plurality or all of the second pillars 42 being separated from, i.e. not being in contact to, the p base region 3 of the corresponding cell. The at least one second pillar 42 is separated from the p doped base region 3 by a part of the base layer 4 of the first conductivity type.

The reason for this structure being advantageous compared to a structure like in FIG. 1 or FIG 2, in which a connection between the second pillar 42 and the base region 3 exists, is that an integral PNP bipolar transistor structure is activated via the gate thereby providing excess base charge close to the cathode 8. It can be advantageous to have such an activated integral PNP bipolar transistor structure only in one cell or in some of the active cells of a device.

In the device according to FIG 2, the holes have a direct path through the second pillar 42 to the base region 3. In the forward conduction mode, this path is controlled in the inventive IGBT by the gate setting the base current of the afore-mentioned PNP transistor. In this mode, the second pillar 42 acts as an emitter for the second carrier type, the disconnection layer and part of the first pillar 41 form the base of the PNP transistor and the base region 3 achieves the role of the collector layer. During turn-off and in the blocking state, the PNP base current has vanished – the first carrier type is extracted from the base layer 4 (41, 42) via the anode layer 9. Accordingly, anode layer 9 can no longer inject carriers of the second type and the second pillar 42 will cease to act as emitter.

Furthermore the switching losses of the Semi-SJIGBT are found to be substantially lower than the standard Trench FS IGBT. Comparing the technology curves of a Trench Field Stop IGBT to an inventive Semi-SJ-IGBT with a first and second pillar height of 10 µm, 50 µm and 90 µm, the switching-off losses as a function of the on-state voltage are lower for the

inventive devices as shown in FIG. 16. Furthermore, the figure shows the differences of the switching-off losses for second pillars being limited to an area below the trench gate electrode (designated in Fig. 16 as "contrench IGBT") and for second pillars, being arranged below the base region, but separated from it by a disconnection layer (designated in the figure as "trench IGBT").

Brief Description of Drawings

The subject matter of the invention will be explained in more detail in the following text with reference to the attached drawings, in which:

FIG 1 shows a prior art superjunction IGBT;

FIG 2 shows a prior art semi superjunction IGBT;

FIG 3 shows a prior art fieldstop IGBT;

FIG 4 shows a first embodiment of an inventive IGBT with a planar gate electrode;

FIGs 5 to 8 show further embodiments of inventive IGBTs with a planar gate electrode;

FIG 9 and 10 show other embodiments of inventive IGBTs with a trench gate electrode;

FIGs 11 and 12 show other embodiments of inventive IGBTs with a planar gate electrode;

FIG 13 and 14 show other embodiment of inventive JFEBTs (junction field effect bipolar transistor) with a planar gate electrode;

FIG 15 shows a comparison of the switching losses versus on-state voltage for inventive IGBTs with pillar heights of 10, 50 and 90 µm with planar gate electrodes or trench gate electrodes and a prior art trench FS IGBT;

FIG 16 shows a comparison of the switching losses versus on-state voltage for inventive IGBTs with pillar heights of 10, 50 and 90 µm with trench gate electrodes and second pillars being arranged

directly below the trench gate electrode and such devices, in which no second pillar is arranged below the trench gate electrode;

FIG 17 shows a comparison of the switching losses versus on-state voltage for inventive IGBTs with pillar heights of 10, 50 and 90 µm with planar gate electrodes and prior art SJ IGBTs;

FIG 18 shows a comparison of the voltages during switching-off versus time for inventive IGBTs with pillar heights of 50 µm with planar gate electrodes and prior art SJ IGBTs;

FIG 19 shows the electric field for a prior art FS IGBT and for inventive devices with pillar heights of 50 and 150 µm, the device comprising a first layer;

FIG 20 shows a plot of the room temperature cosmic ray induced failure rate as a function of the V_{anode} for the Trench FieldStop IGBT and inventive Semi-SJ IGBT with second pillar doping concentration of $2*10^{15}$ cm^{-3} and a wafer height equal to 400 µm;

FIG 21 shows a plot of the switching-off losses at room temperature as a function of the on-state voltage for a prior art Trench Field Stop IGBT and an inventive Semi SJ-IGBT with p-doped second pillar doping concentration of $1*10^{15}$ cm^{-3} and $2*10^{15}$ cm^{-3}, a wafer height equal to 400 µm, a pillar height equal to 50 µm and a cell width of 5 µm; and

FIG 22 shows a plot of the room temperature switching-off losses as a function of the on-state voltage for a prior art trench FS IGBT and an inventive Semi-SJ-IGBT with second pillar doping concentration of $2*10^{15}$ cm^{-3} for a wafer height equal to 400 µm and a second pillar height equal to 50, 150 and 200 µm, cell width = 5 µm.

The reference symbols used in the figures and their meaning are summarized in the list of reference symbols. Generally, alike or alike-functioning parts are given the same reference symbols. The described embodiments are meant as examples and shall not confine the invention.

Modes for Carrying out the Invention

FIG. 4 shows an inventive insulated gate bipolar transistor with a semiconductor wafer 10 and a first electrical contact 8 formed on a first main side 101 of the wafer and a second electrical contact 9 formed on a second main side 102 of the wafer opposite the first main side 101. For the IGBT, the first main side 101 is the cathode side, on which a cathode electrode as the first electrical contact 8 is arranged, and the second main side 102 is the anode side of the device, on which an anode electrode as the second electrical contact 9 is arranged. The inventive IGBT comprises n doped source regions 2 contacting the cathode electrode, and a p doped base region 3 also contacting the cathode electrode. It further comprises a base layer 4, with first n doped pillars 41 and p doped second pillars 42, the first and second pillars 41, 42 being arranged alternately in the same plane.

A gate electrode 5, 5', which is electrically insulated by an insulation layer 51 from the source region 2 and the base region 3, is arranged on the cathode side. On the anode side of the wafer, the inventive IGBT comprises a p doped anode layer 6, on which the anode electrode is arranged.

The source regions 2 are arranged on the cathode side of the wafer and separated from the base layer 4 by the base region 3. The second pillars 42 are separated from the base region 3, i.e. the second p doped pillars 42 are not in contact with the base region 3.

In an exemplary embodiment, the doping of anode layer is higher than the doping of second pillar 42, preferably about one order of magnitude higher than the doping of second pillar 42.

In another exemplary embodiment, the base layer 4 further comprises an n doped disconnection layer 43, which is arranged between the base region 3 and the first and second pillars 41, 42 as shown in FIG. 5. The disconnection layer 43 can be a continuous region over the whole wafer plane. Alternatively, the disconnection layer 43 can be a laterally limited region.

The positions of the first and second pillars 41, 42 can also be switched

as shown in FIG. 14 or shifted to a side, i.e. the first and second pillars 41, 42 do not necessarily have to be positioned symmetrical to the other layers of the device, e.g. to the cathode electrode or the gate electrode. One, a plurality of or all of the second pillars 42 are separated from the base region 3.

The disconnection layer 43 typically has a doping concentration of at maximum $1 * 10^{17}$ cm^{-3}. In another exemplary embodiment, the doping concentration of the disconnection layer is equal to or less than the doping concentration of the first pillars 41. In another exemplary embodiment, the height of the disconnection layer is at maximum 20 µm and in yet another embodiment the height of the disconnection layer is at maximum 3 µm. Typically, the height of the disconnection layer is at minimum 0.1 µm. For the disconnection layer 43, one or a combination or all of the above disclosed features can be present.

In another exemplary embodiment, the width 411 multiplied by the doping concentration of the first pillar is either equal to or differs by at maximum +/- 5 % from the width 421 multiplied by the doping concentration of the second pillar (in all figures the width is indicated by a dashed line; this line is not meant to show the real pillar width, e.g. the second pillars 42 in Fig. 4 continue beyond the sides of the device section shown in the figure). The Figs. 21 and 22 show the influence of doping concentration and pillar height on the on-state voltage and switching losses compared to a standard prior art Trench FS IGBT. The properties of the device improve with higher doping concentration and with base layers 4, which comprise "moderate" pillar heights 412, 422 together with n doped first layers 44, i.e. semi superjunction devices, which are explained in the paragraph below.

The base layer 4 may also comprise an n doped first layer 44, which is arranged as a continuous layer over the whole plane of the wafer on the first and second pillars 41, 42 on the side towards the anode electrode (FIG. 6). Such a first layer 44 may have a doping concentration, which is lower than the doping concentration of the first pillar. By the introduction of

the first layer 44 a semi superjunction semiconductor device is provided. Such a design with first and second pillars 41, 42 over a smaller depth than the total depth of the base layer 4 can be more easily fabricated. This makes the device superior for power semiconductor devices, for high voltages, e.g. for 3.3 kV or even greater voltage ranges (e.g. 6.5 kV). Furthermore, the dynamic avalanche breakdown is avoided as the doping of the second main side 102 of the base layer 4 is kept low.

The height of the first pillar 412, of the second pillar 422 or of any of the first and second pillar 412, 422 may be as low as 1 % of the total wafer height or in another embodiment at least 10 % of the total wafer height.

The IGBT may further comprise an n doped buffer layer 62, which is arranged between the anode layer 65 and base layer 4. Such an inventive device is shown in FIG. 8. In the case that the device comprises a first layer 44 and a buffer layer 62, the buffer layer has a higher doping concentration than the first layer 44, typically the doping concentration is two or three orders of magnitude higher than of the first layer.

The gate electrode may be formed as a planar gate electrode 5 as shown in FIG. 4. In that case, the electrically insulating insulation layer 51 is arranged on top of the cathode side of the wafer. Typically, the gate electrode 5 is completely embedded in the insulation layer 51 and thus, the gate electrode 5 is electrically separated from the source regions 2, the base region 3, the base layer 4 and the cathode electrode. The gate electrode 5 is typically made of a heavily doped polysilicon or a metal like aluminum.

Alternatively, the gate electrode may be formed as a trench gate electrode 5' as shown in the FIGs. 10 and 11.

The trench gate electrode 5' is arranged in the same plane as the source regions 2 and the base region 3 and adjacent to the latter. They are separated from each other by the insulation layer 51, which also separates the gate electrode 5' from the base layer 4. The trench gate electrode 5' is

typically completely embedded in the insulation layer 51, thus insulating the trench gate electrode 5' from the cathode electrode.

FIG. 15 shows the switching-off losses as a function of the on-state voltage for a prior art trench FS IGBT and for inventive devices with planar gate electrode 5 or trench gate electrode 5' respectively. The prior art FS IGBT has the highest switching-off losses for a given on-state voltage. For a given switching loss the on-state voltage for the inventive IGBT can be reduced by at least 0.7 V even for the case of a pillar height of merely 10 µm. For greater pillar heights, both losses and on-state voltage are lower for all conditions shown in FIG. 15. Furthermore, smaller on-state voltages cannot be achieved for the trench FS IGBT, because of insufficient excess base charge in the base layer 4 towards the cathode 101. For the same doping concentration and the same height of the pillars, the inventive devices with trench gate electrodes 5' have lower switching-off losses than devices with planar gate electrodes 5.

In a further exemplary embodiment, the second pillar 42 is limited to a region below the insulation layer 51 of the trench gate electrode 5' as shown in FIG. 10.

The base layer 4 may also comprise p doped fourth layers 45 and n doped fifth layers 46, each of which having a width, which is smaller than the width of the first and second pillars (Fig. 11). The doping concentration of the fifth layer is in an exemplary embodiment higher than the doping concentration of the first pillar. The doping concentration of the fourth layer is also preferably higher than the doping concentration of the second pillar. Furthermore, the doping concentration of the fourth and fifth layers are higher than the doping concentration of the second and first pillar, respectively. Such fourth and fifth layers may also be used in any prior art superjunction or semi superjunction power semiconductor device, i.e. in any device with planar or trench gate electrode, like IGBTs or reverse conducting IGBTs. The fourth and fifth layers 45, 46 can be arranged on the side of the base layer 4 towards the first electrical contact 8, between the

first and second pillars 41, 42 and the disconnection layer 43. Alternatively, the fourth and fifth layers 45, 46 can be arranged in any appropriate plane within the base layer 4, e.g. on the pillars 41, 42 or even on the first layer 44 on the side towards the second main electrode 9, or within the plane of the pillars 41, 42, of the first layer 44 or the disconnection layer 43.

The fourth and fifth layers 45, 46 can furthermore be arranged over the whole plane of the device or only over a part of the plane, e.g. without the termination region of the device.

In the Fig. 12 and 13, the inventive semiconductor device is shown in form of a Junction field effect bipolar transistor (JFEBT). The base region 3 comprises a first base region 31, which is arranged below the cathode electrode and which is in electrical contact with the source region 2 and the cathode electrode, a second base region 32 with a second base region width, which second base region 32 is arranged below the source regions 2 and in contact to the first base region 31 and which has a greater second base region width than the first base region width. The device further comprises at least one p doped first gate region 33, which is in electrical contact to the planar gate electrode 5 and which is separated from the first and second base region 31, 32 by a part of the base layer 4 of the first conductivity type, i.e. by a first pillar 41 and/or the disconnection layer 43.

The second base region 32 may be partly arranged below the first gate region 33, but separated from it by an n doped part of the base layer 4 as shown in FIG. 13 (i.e. disconnection layer 43 or n doped first pillar 41). Alternatively, no part of the second base region 32 is arranged below the first gate region 33 as shown in FIG. 12 (vertical JFEBT).

The inventive semiconductor device may also be a reverse conducting IGBT, which comprises the same layers as disclosed above for the IGBT and which further comprises an n doped third layer 45, which is arranged in the same plane as the p doped anode layer 6 (i.e. on the second main side 102 of the wafer) and alternately to it (FIG. 7). Typically, the total area of the third layers 45 is less than 25 %, less than 10 % of the total wafer area

or even less than 5 %

The second pillar may be limited to a region below the second base region, separated from it by the disconnection layer.

In another embodiment, the conductivity types of the layers are switched, i.e. all layers of the first conductivity type are p type (e.g. the source region) and all layers of the second conductivity type are n type (e.g. the base region).

Reference List

1	semiconductor device
10	wafer
101, 101'	first main side
102, 102'	second main side
11	SJ-IGBT
12	semi SJ-IGBT
13	Trench FS IGBT
2	source region
3	base region
31	first base region
32	second base region
33	first gate region
4	base layer
41	first pillar
411	width of first pillar
412	height of first pillar
42	second pillar

421	width of second pillar
422	height of second pillar
43	disconnection layer
44	first layer
45	third layer
45	fourth layer
46	fifth layer
47	sixth layer
5, 5'	gate electrode
51	insulation layer
6	anode layer
62	buffer layer
8, 8'	first electrical contact
9, 9'	second electrical contact

C L A I M S

1. Power semiconductor device (1) with a semiconductor wafer (10) and a first electrical contact (8) being formed on a first main side (101) of the wafer and a second electrical contact (9) being formed on a second main side (102) of the wafer opposite the first main side (101),

said semiconductor wafer (10) comprising a structure with a plurality of layers of different conductivity types,
said structure comprising

- at least one source region (2) of the first conductivity type, which is arranged on the first main side (101) of the wafer and which contacts the first electrical contact (8),
- at least one base region (3) of a second conductivity type contacting the first electrical contact (8),
- a base layer (4), which comprises at least one first pillar (41) of the first conductivity type and at least one second pillar (42) of the second conductivity type, the first and second pillars (41, 42) being arranged alternately in the same plane,
- a gate electrode, which is electrically insulated by an insulation layer (51) from the source region (2) and the base region (3),
- wherein each source region (2) is separated from the base layer (4) by a base region (3), characterized in, that

at least one second pillar (42) is not in contact with the base region (3).

2. Power semiconductor device (1) according to claim 1, wherein the base layer (4) further comprises a disconnection layer (43) of the first conductivity type, which is arranged between the base region (3) and the at least one of the first and second pillars (41, 42).

3. Power semiconductor device (1) according to claim 2, wherein the disconnection layer (43) fulfils at least one of the following rules:

- the doping concentration of the disconnection layer (43) is at maximum $1 * 10^{17}$ cm^{-3} ,

- the doping concentration of the disconnection layer (43) is equal to or less than the doping concentration of the at least one first pillar (41),
- the height of the disconnection layer (43) is at maximum 20 µm,
- the height of the disconnection layer (43) is at maximum 3 µm, or
- the height of the disconnection layer (43) is at minimum 0.1 µm.

4. Power semiconductor device (1) according to any of the preceding claims, wherein the width (411) multiplied by the doping concentration of the first pillar (41) is equal to or which differs by at maximum +/- 5 % from the width (421) multiplied by the doping concentration of the second pillar (42).

5. Power semiconductor device (1) according to any of the preceding claims, wherein the base layer (4) further comprises a first layer (44) of the first conductivity type, which is arranged as a continuous layer over the whole plane of the wafer on the first and second pillars (41, 42) on the side towards the second electrical contact (9).

6. Power semiconductor device (1) according to claim 5, wherein the doping concentration of the first layer (44) is lower than the doping concentration of the first pillar (41).

7. Power semiconductor device (1) according to any of the claims 2 to 6, wherein the height of the first pillar (412), of the second pillar (422) or of any of the first and second pillars (412, 422) is at least 1 % of the total wafer height.

8. Power semiconductor device (1) according to any of the preceding claims, wherein the semiconductor device is an insulated gate bipolar transistor, which comprises an anode layer (6) of the second conductivity type, which is arranged on the second main side (102) of the wafer.

9. Power semiconductor device (1) according to any of the preceding

claims, wherein the semiconductor device is a reverse-conducting insulated gate bipolar transistor, which comprises an anode layer (6) of the second conductivity type, which is arranged on the second main side (102) of the wafer, and wherein in the same plane as the anode layer (6) and alternately to it, at least one third layer (45) of the first conductivity type is arranged.

10. Power semiconductor device (1) according to claim 8 or 9, wherein a buffer layer (62) of the first conductivity type is arranged between the anode layer (6) and the base layer (4).

11. Power semiconductor device (1) according to any of the preceding claims, wherein the gate electrode is a trench gate electrode (5'), which is arranged in the same plane as the base region (3) and adjacent to the base region (3) and the source region (2), which trench gate electrode (5') is separated from the source region (2), the base region (3) and the base layer (4) by the electrically insulation layer (51).

12. Power semiconductor device (1) according to claim 11, wherein the second pillar (42) is limited to a region below the insulation layer (51).

13. Power semiconductor device (1) according to any of the preceding claims, wherein the base layer (4) comprises at least one fourth layer (45) of the second conductivity type and at least one fifth layer (46) of the first conductivity type, each of which having a width, which is smaller than the width of the at least one first and second pillar.

14. Power semiconductor device (1) according to claim 13, wherein at least one of the following rules is fulfilled:

- the doping concentration of the at least one fifth layer is higher than the doping concentration of the first pillar or
- the doping concentration of the at least one fourth layer is higher than the doping concentration of the second pillar.

15. Power semiconductor device (1) according to any of the claims 1 to 10, wherein the semiconductor device is a junction field effect bipolar

transistor, wherein the base region (3) comprises a first base region (31), which is arranged below the first electrical contact (8) and which is in electrical contact with the source region (2) and the first electrical contact (8),

at least one second base region (32) with a second base region width, which second base region (32) is arranged below at least one source region (2) and below and in contact to the first base region (31) and which has a greater second base region width than the first base region width,

and which device comprises at least one first gate region (33) of the second conductivity type, which is electrically contacted by the gate electrode (5), which is formed as a planar gate electrode (5), and which first gate region (33) is separated from the first and second base region (31, 32) by a part of the base layer (4) of the first conductivity type.

16. Power semiconductor device (1) according to claim 15, wherein the second base region (32) is partly arranged below at least one first gate region (33) or wherein no part of the second base region (32) is arranged below the third base region (33).

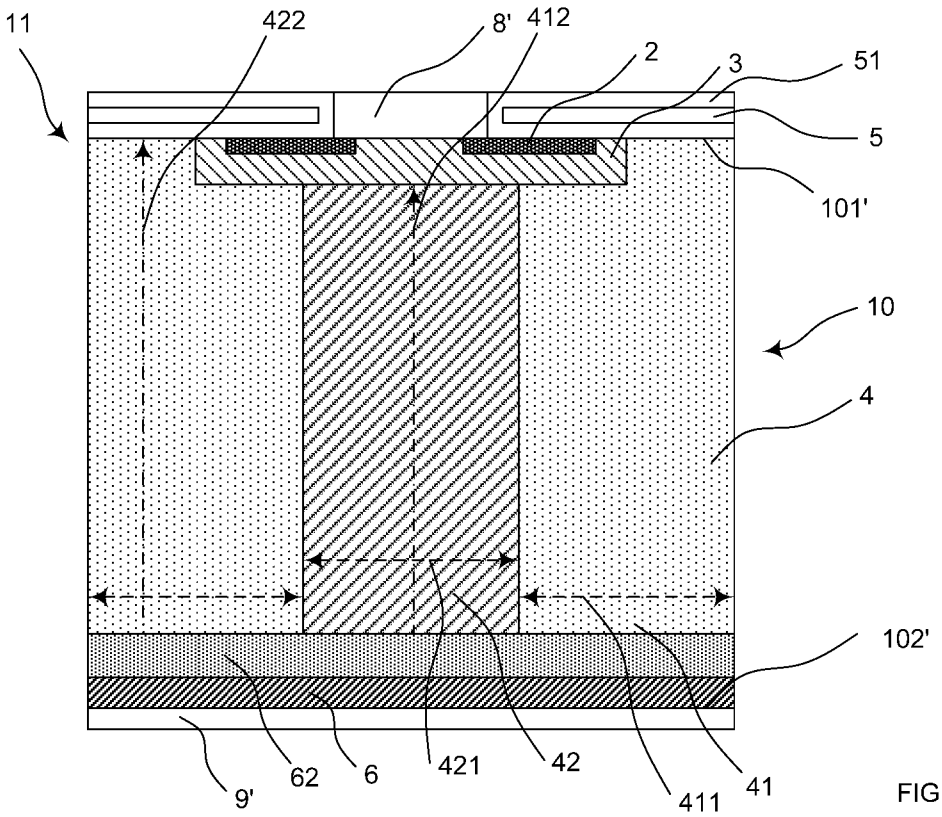

FIG. 1 Prior Art

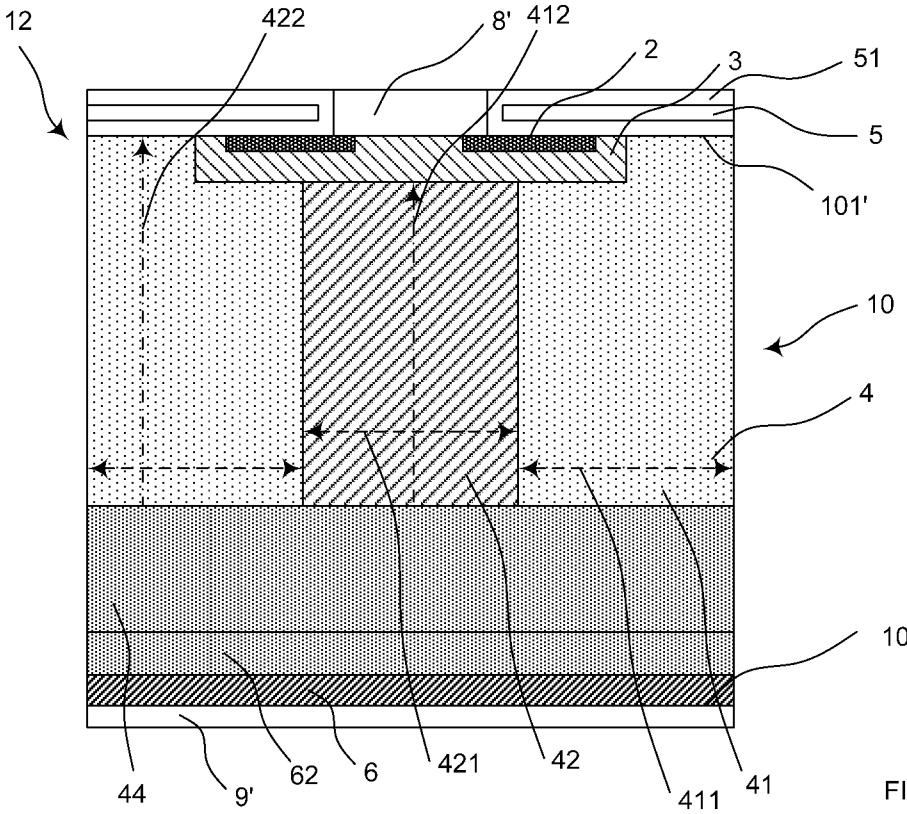

FIG. 2 Prior Art

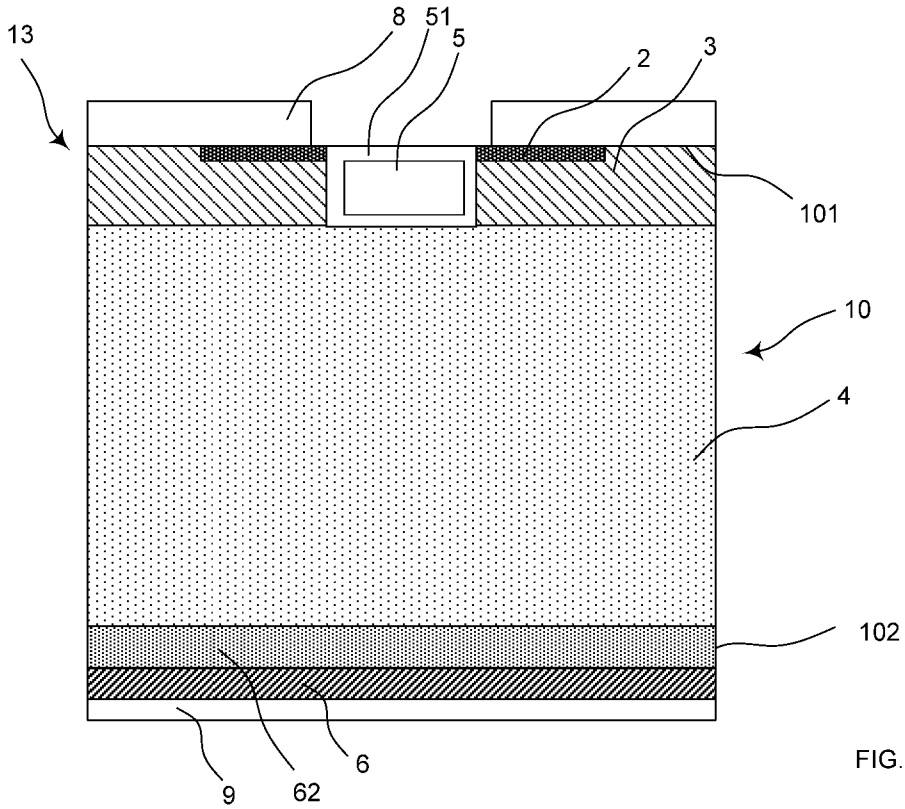

FIG. 3 Prior Art

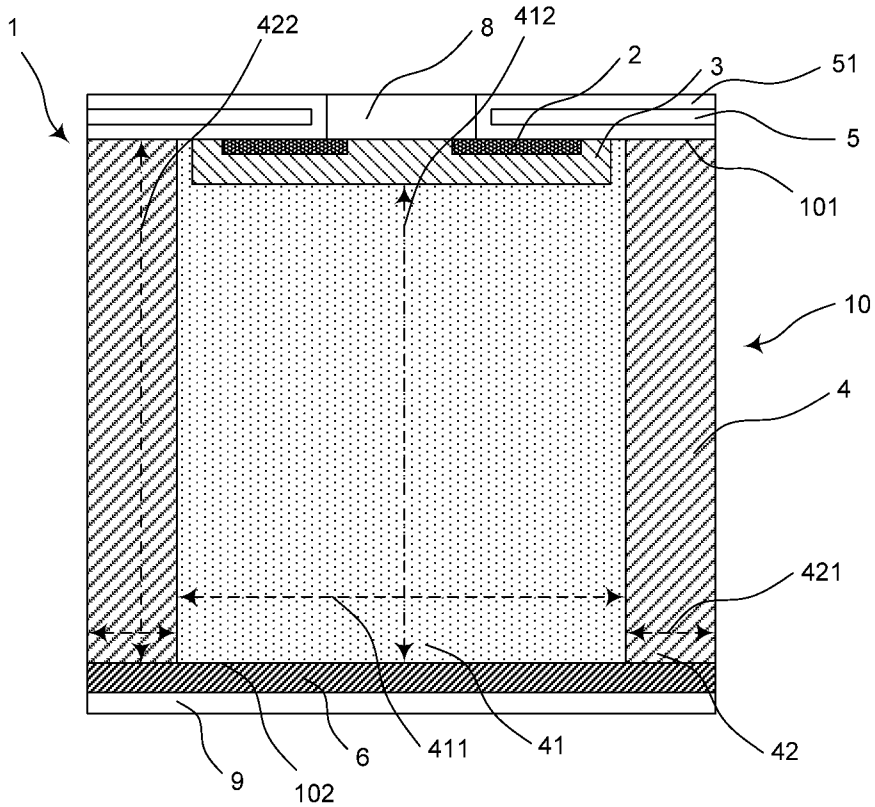

FIG. 4

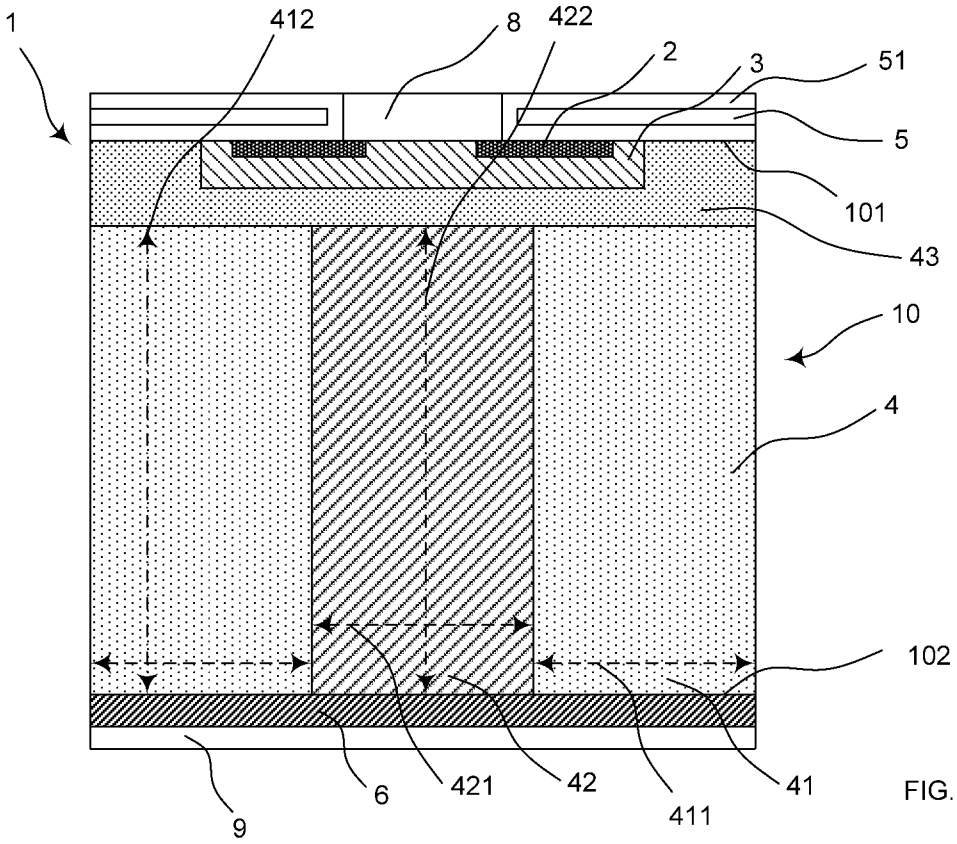
1
412
8
422
2
3
51
5
101
43
10
4
102
6
421
42
411
41
9

FIG. 5

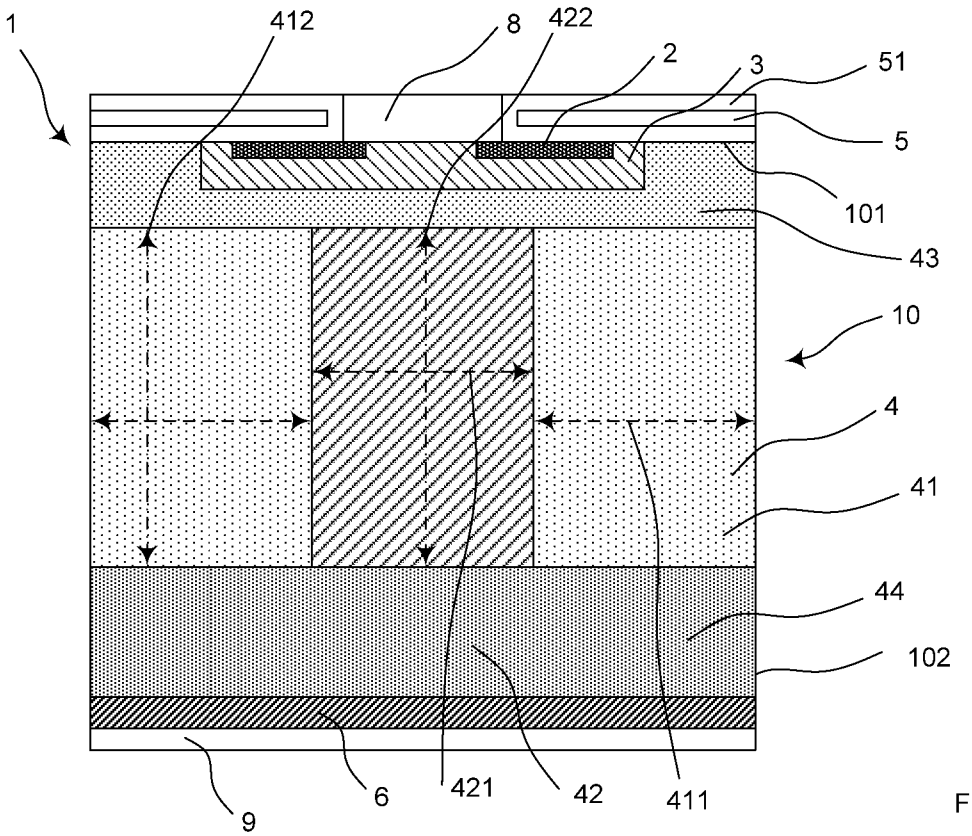
1
412
8
422
2
3
51
5
101
43
10
4
41
44
102
6
421
42
411
9

FIG. 6

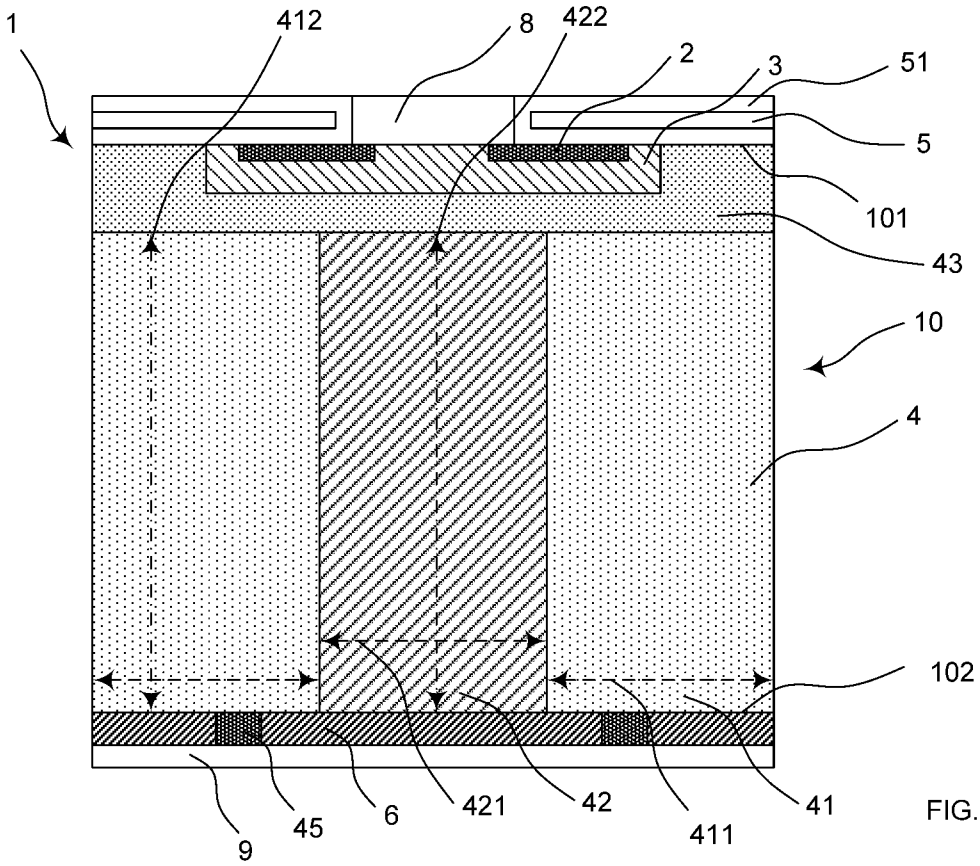
1
412
8
422
2
3
51
5
101
43
10
4
102
41
411
42
421
6
45
9

FIG. 7

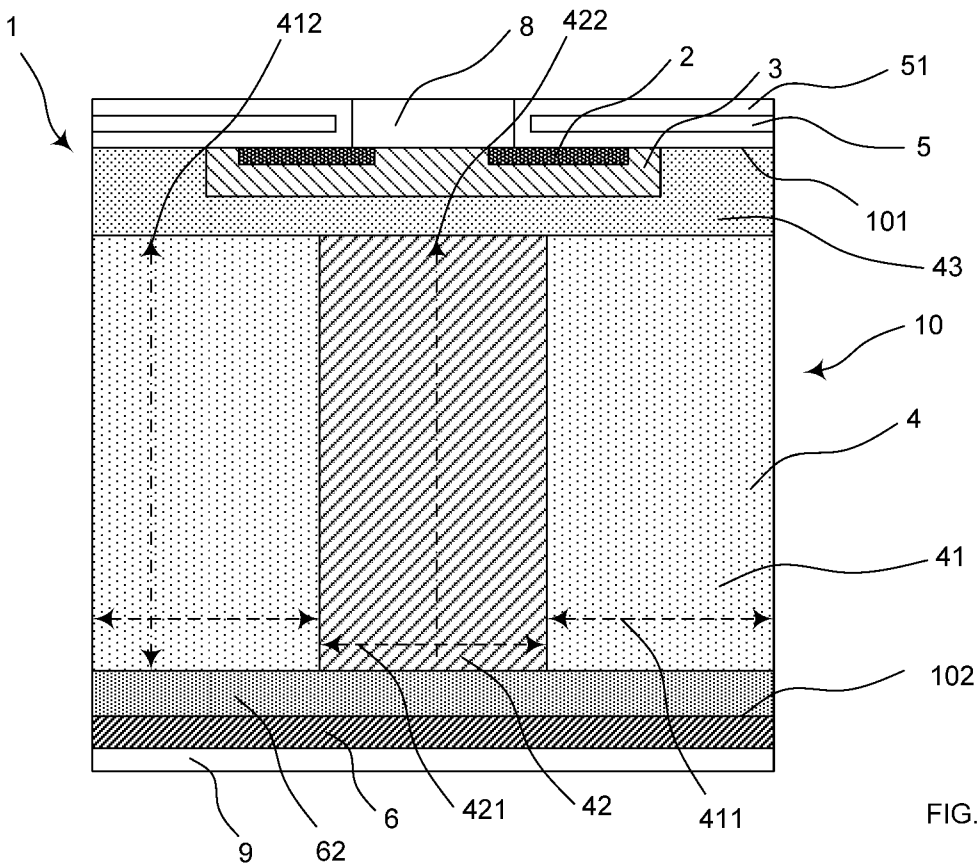
1
412
8
422
2
3
51
5
101
43
10
4
41
102
411
42
421
6
62
9

FIG. 8

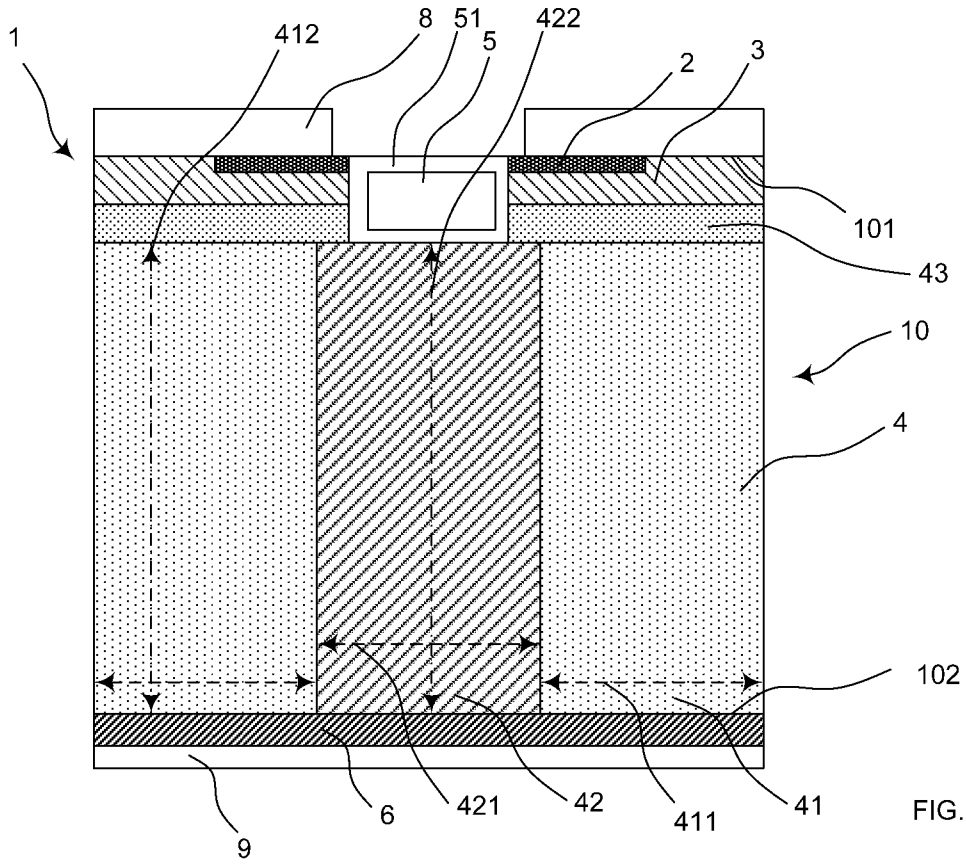
1
412
8
51
5
422
2
3
101
43
10
4
102
6
421
42
411
41
9

FIG. 9

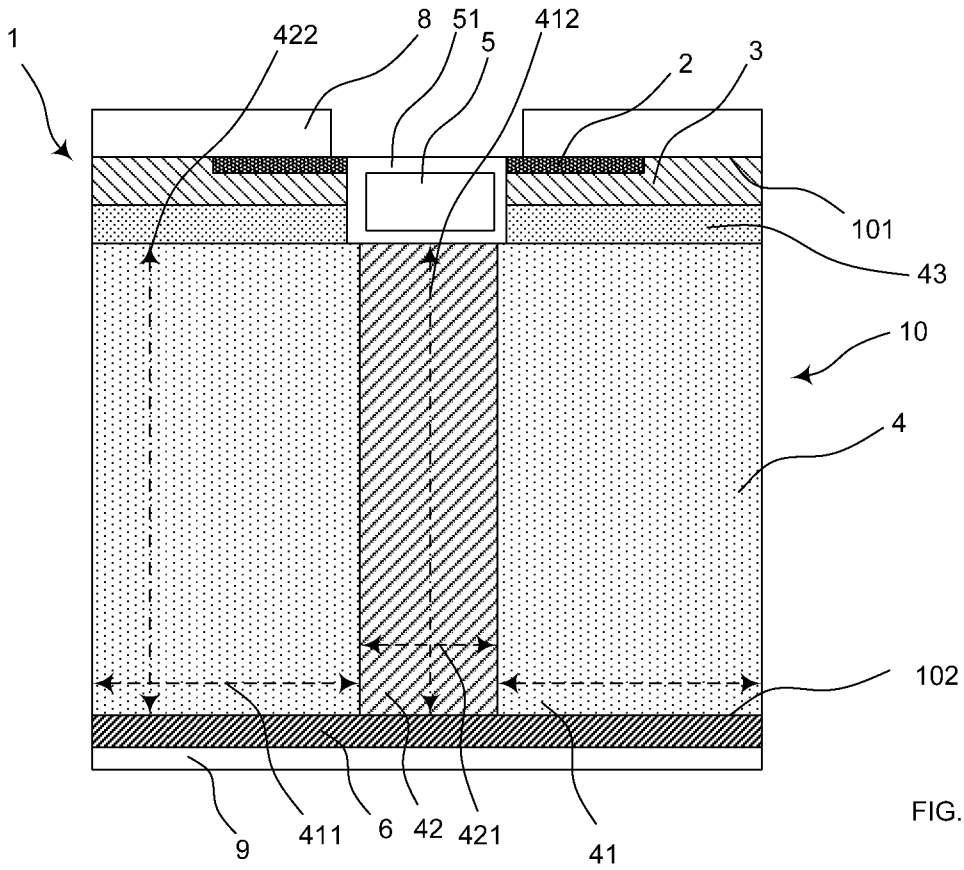
1
422
8
51
5
412
2
3
101
43
10
4
102
9
411
6
42
421
41

FIG. 10

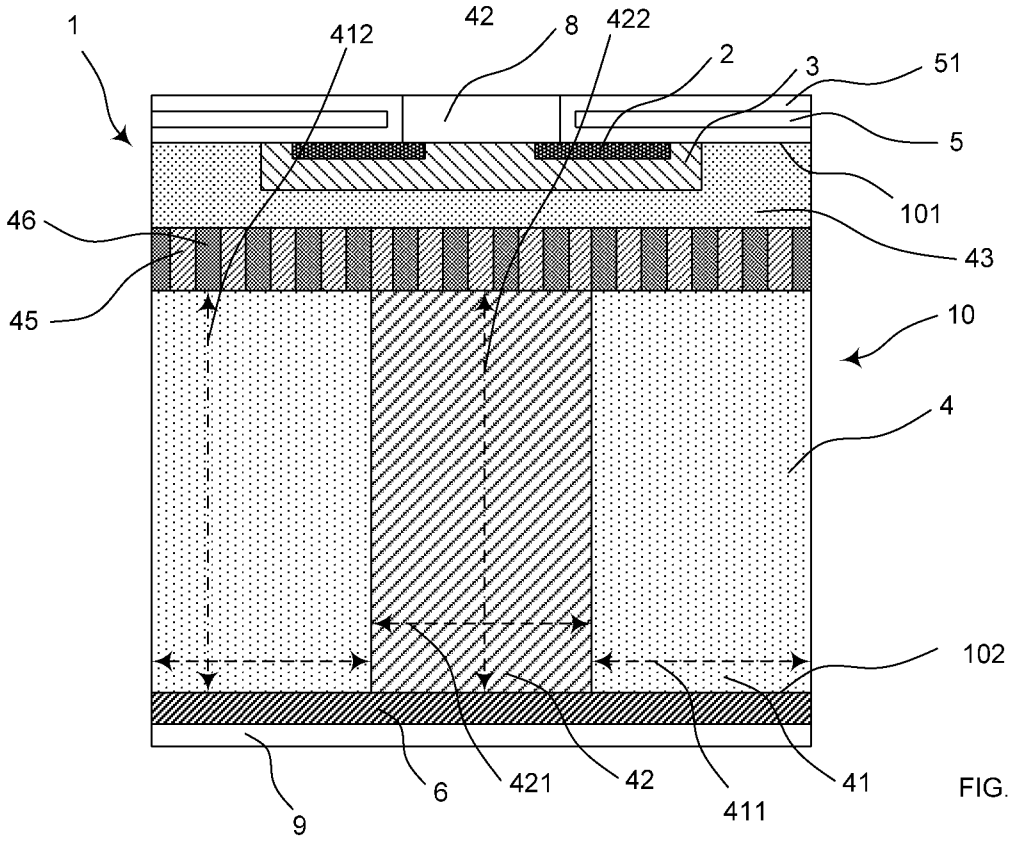
1
412
42
8
422
2
3
51
5
101
46
43
45
10
4
102
6
421
42
411
41
9

FIG. 11

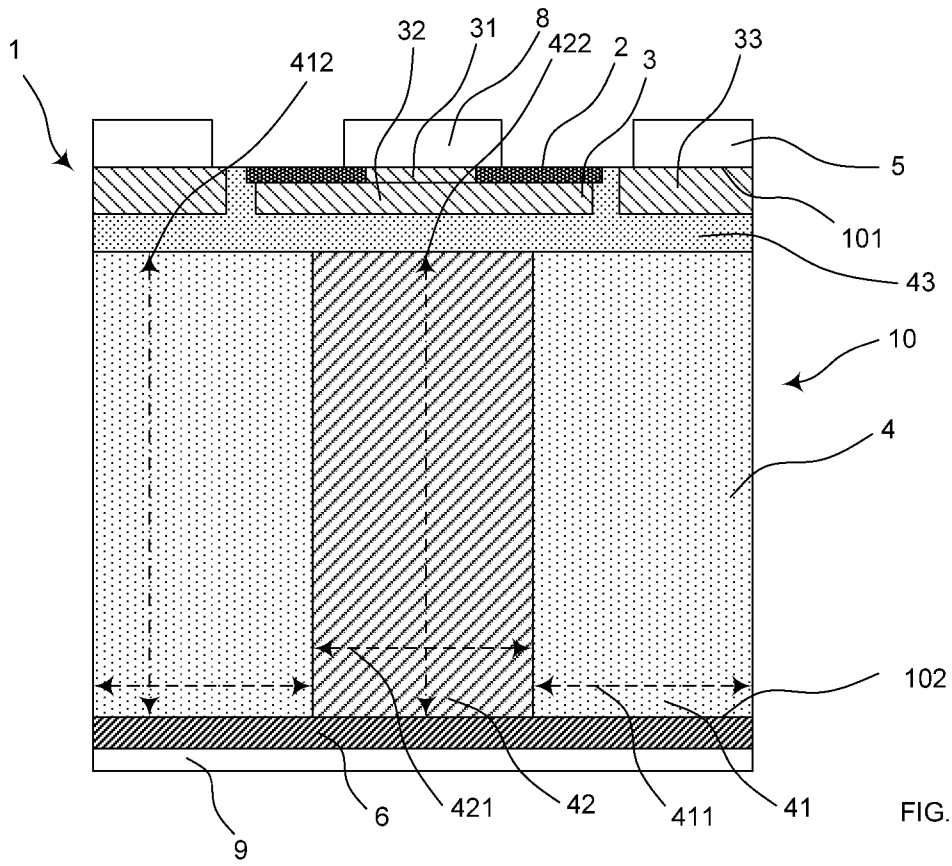
1
412
32
31
8
422
2
3
33
5
101
43
10
4
102
6
421
42
411
41
9

FIG. 12

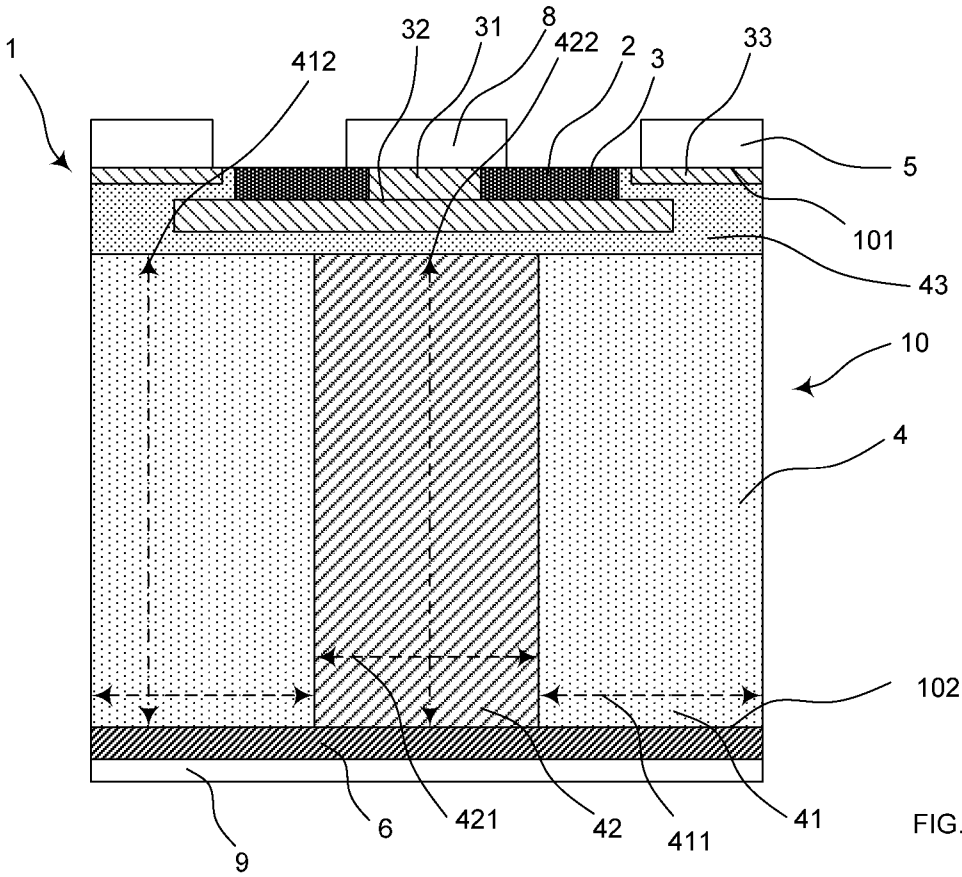
1
412
32
31
8
422
2
3
33
5
101
43
10
4
102
6
421
42
411
41
9

FIG. 13

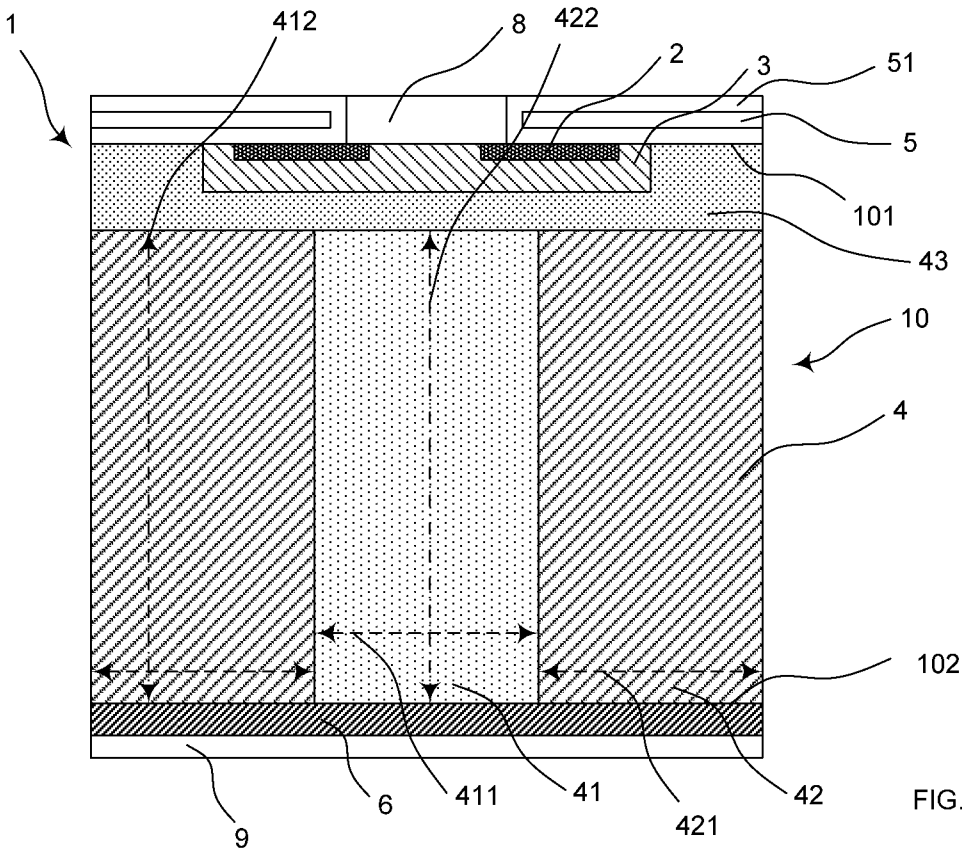
1
412
8
422
2
3
51
5
101
43
10
4
102
6
411
41
421
42
9

FIG. 14

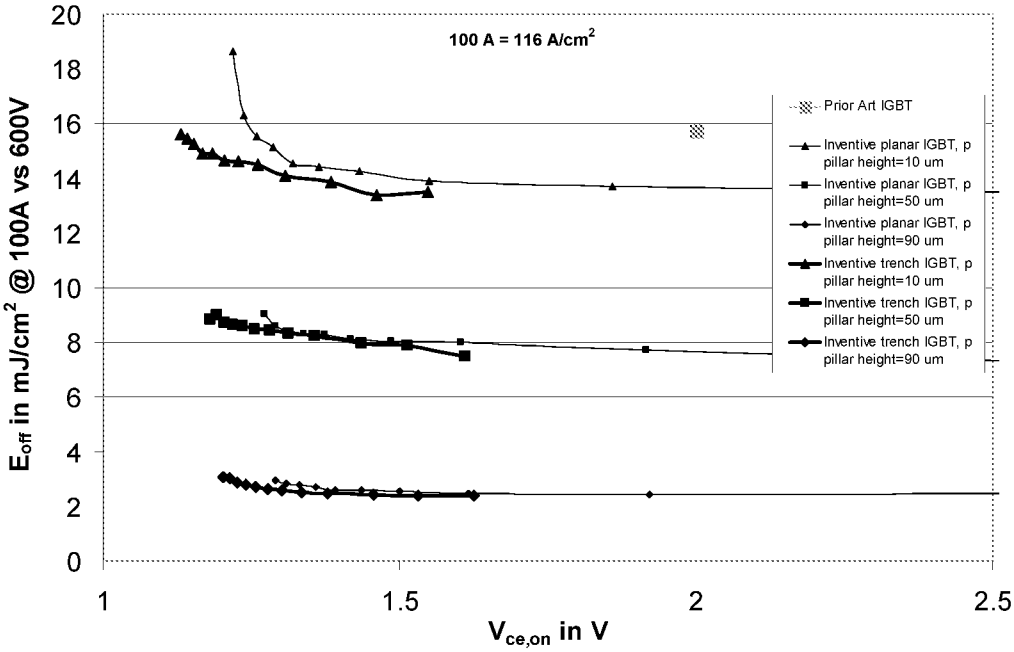
100 A = 116 A/cm2
Prior Art IGBT
Inventive planar IGBT, p pillar height=10 um
Inventive planar IGBT, p pillar height=50 um
Inventive planar IGBT, p pillar height=90 um
Inventive trench IGBT, p pillar height=10 um
Inventive trench IGBT, p pillar height=50 um
Inventive trench IGBT, p pillar height=90 um
Eoff in mJ/cm2 @ 100A vs 600V
Vce,on in V
0
2
4
6
8
10
12
14
16
18
20
1
1.5
2
2.5

FIG 15

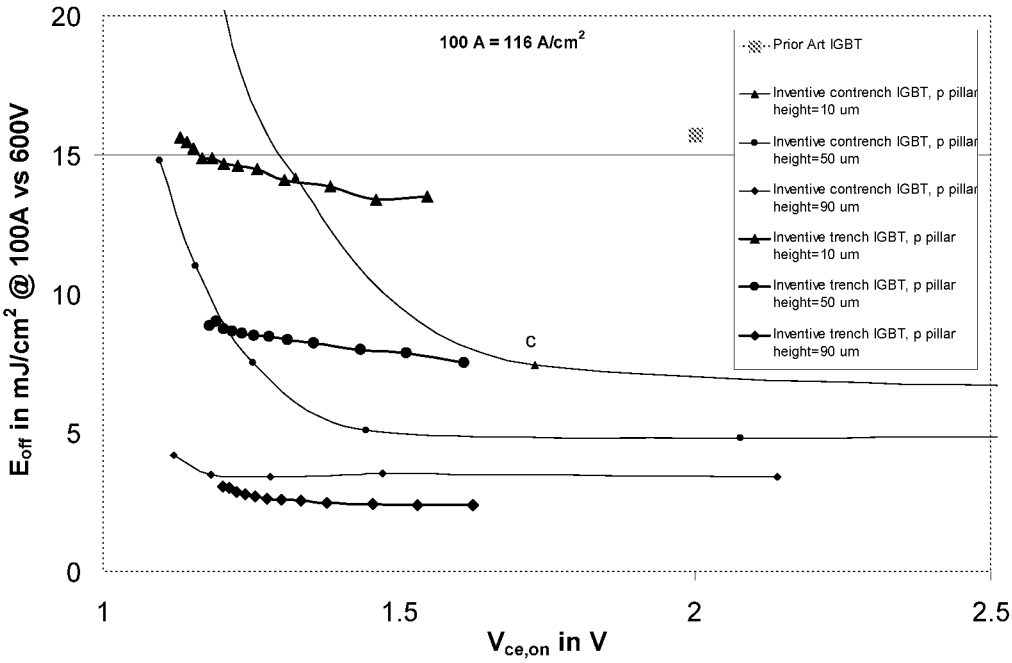
100 A = 116 A/cm2
Prior Art IGBT
Inventive contrench IGBT, p pillar height=10 um
Inventive contrench IGBT, p pillar height=50 um
Inventive contrench IGBT, p pillar height=90 um
Inventive trench IGBT, p pillar height=10 um
Inventive trench IGBT, p pillar height=50 um
Inventive trench IGBT, p pillar height=90 um
c
Eoff in mJ/cm2 @ 100A vs 600V
Vce,on in V
0
5
10
15
20
1
1.5
2
2.5

FIG 16

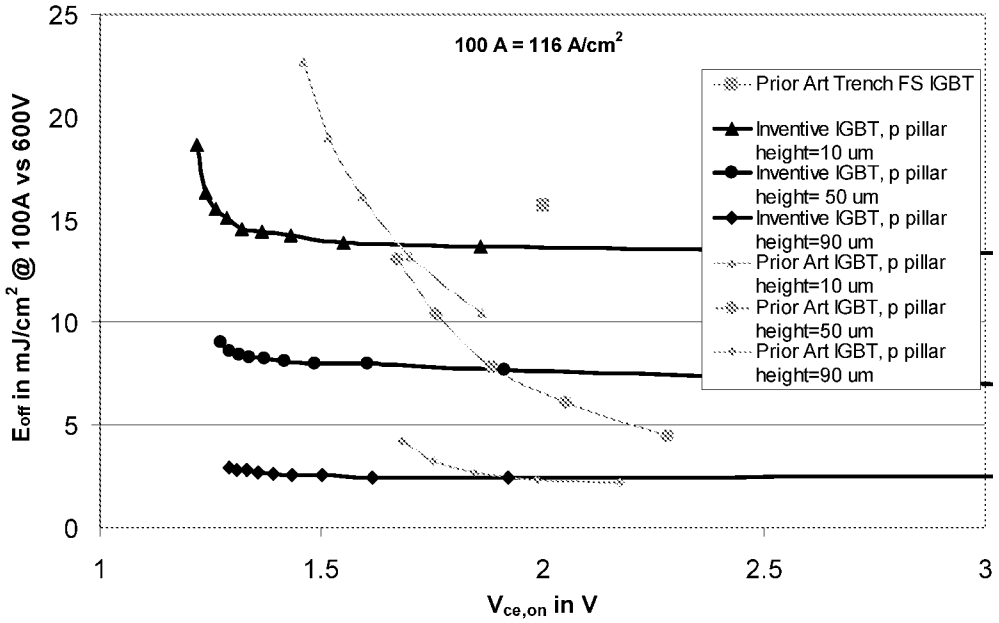
100 A = 116 A/cm2
Prior Art Trench FS IGBT
Inventive IGBT, p pillar height=10 um
Inventive IGBT, p pillar height= 50 um
Inventive IGBT, p pillar height=90 um
Prior Art IGBT, p pillar height=10 um
Prior Art IGBT, p pillar height=50 um
Prior Art IGBT, p pillar height=90 um
Eoff in mJ/cm2 @ 100A vs 600V
Vce,on in V
0
5
10
15
20
25
1
1.5
2
2.5
3

FIG 17

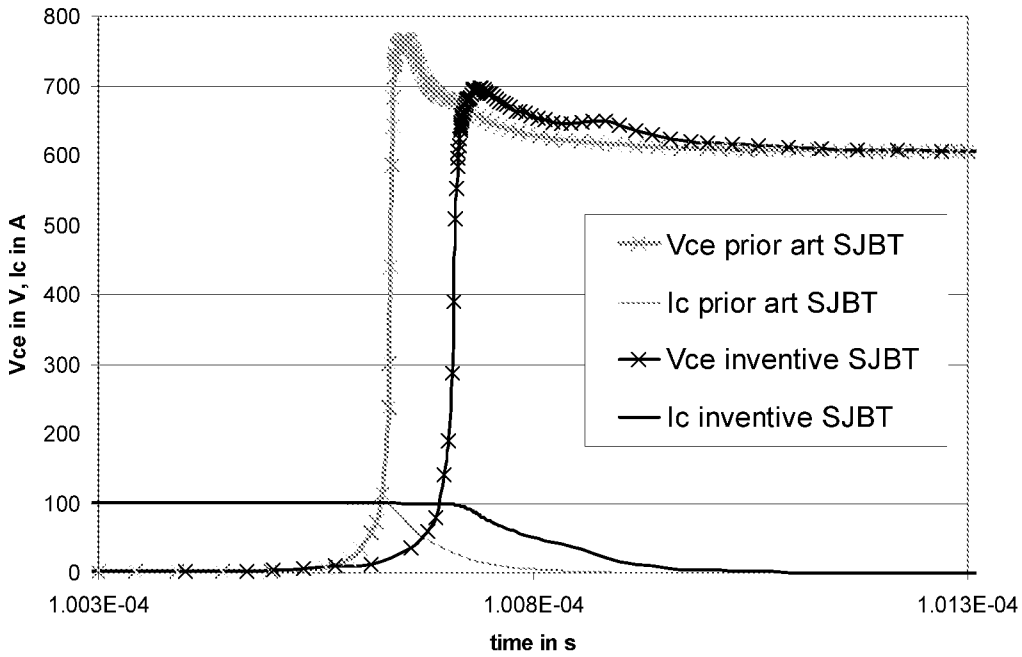
Vce prior art SJBT
Ic prior art SJBT
Vce inventive SJBT
Ic inventive SJBT
Vce in V, Ic in A
time in s
0
100
200
300
400
500
600
700
800
1.003E-04
1.008E-04
1.013E-04

FIG 18

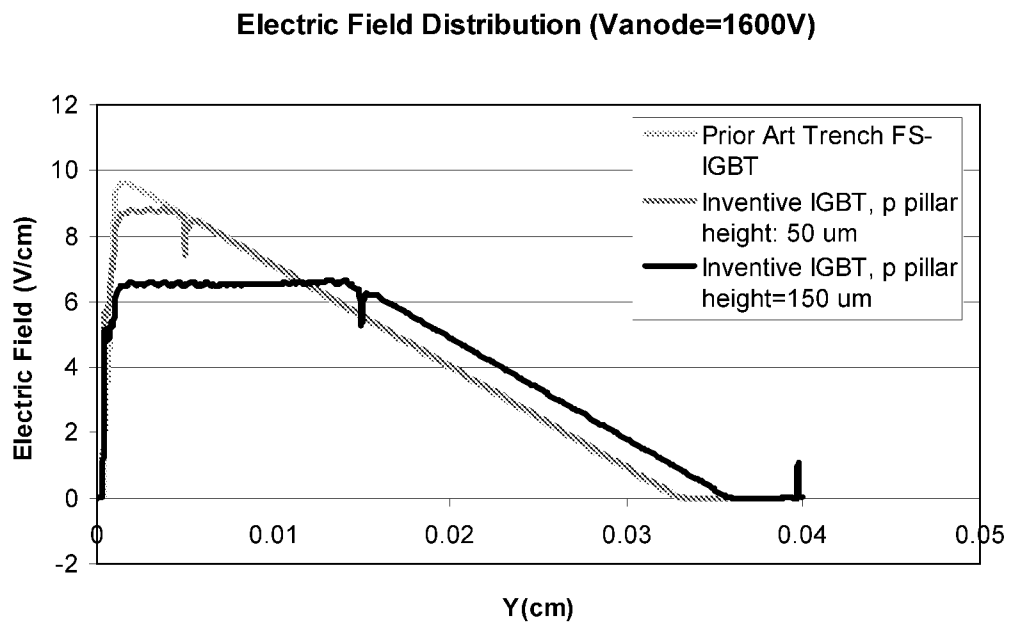
Electric Field Distribution (Vanode=1600V)
Electric Field (V/cm)
12
10
8
6
4
2
0
-2
0
0.01
0.02
0.03
0.04
0.05
Y(cm)
Prior Art Trench FS-IGBT
Inventive IGBT, p pillar height: 50 um
Inventive IGBT, p pillar height=150 um

FIG 19

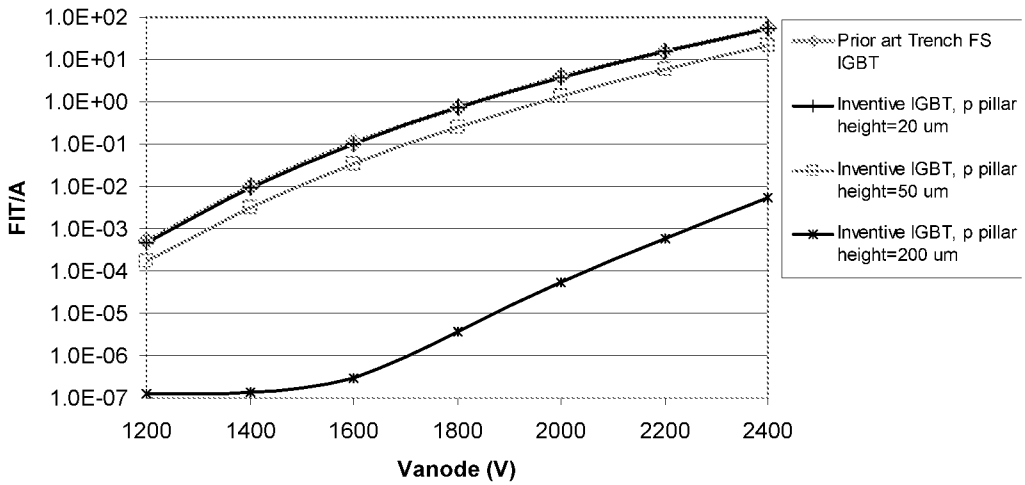
FIT/A
1.0E+02
1.0E+01
1.0E+00
1.0E-01
1.0E-02
1.0E-03
1.0E-04
1.0E-05
1.0E-06
1.0E-07
1200
1400
1600
1800
2000
2200
2400
Vanode (V)
Prior art Trench FS IGBT
Inventive IGBT, p pillar height=20 um
Inventive IGBT, p pillar height=50 um
Inventive IGBT, p pillar height=200 um

FIG 20

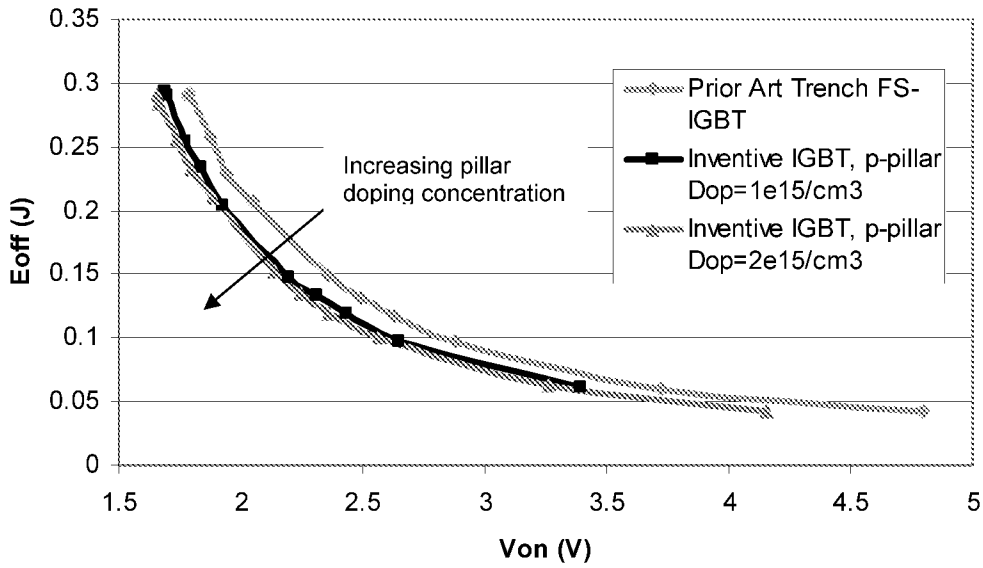
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
Eoff (J)
1.5
2
2.5
3
3.5
4
4.5
5
Von (V)
Increasing pillar doping concentration
Prior Art Trench FS-IGBT
Inventive IGBT, p-pillar Dop=1e15/cm3
Inventive IGBT, p-pillar Dop=2e15/cm3

FIG 21

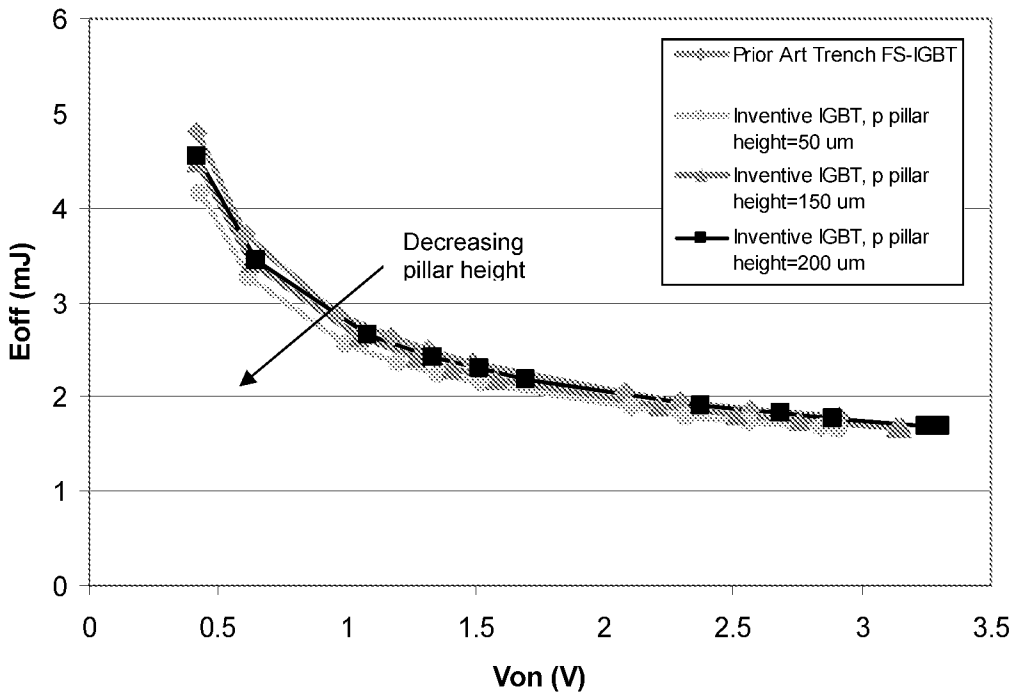
6
5
4
3
2
1
0
Eoff (mJ)
0
0.5
1
1.5
2
2.5
3
3.5
Von (V)
Decreasing pillar height
Prior Art Trench FS-IGBT
Inventive IGBT, p pillar height=50 um
Inventive IGBT, p pillar height=150 um
Inventive IGBT, p pillar height=200 um

FIG 22

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2009/057261

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L29/739 H01L29/06
ADD. H01L29/08 H01L29/10

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 184 555 B1 (TIHANYI JENO [DE] ET AL) 6 February 2001 (2001-02-06) * Fig.1 and corresponding text *	1-14
X	DE 196 04 043 A1 (SIEMENS AG [DE]) 7 August 1997 (1997-08-07) * Fig.1 and corresponding text *	1-14
A	B.JAYANT BALIGA: "Power Semiconductor Devices" 1995, PWS PUBLISHING COMPANY , XP002542146 * Figs. 8.53 and corresponding text *	1-14
A	EP 0 578 973 A (TOKYO SHIBAURA ELECTRIC CO [JP]) 19 January 1994 (1994-01-19) * Fig.5 and corresponding text *	1-14

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 August 2009	18/11/2009

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Fax: (+31–70) 340–3016	Kusztelan, Leonard

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2009/057261

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	KWANG-HOON OH ET AL: "A simulation study on novel field stop IGBTs using superjunction" IEEE TRANSACTIONS ON ELECTRON DEVICES IEEE USA, vol. 53, no. 4, April 2006 (2006-04), pages 884-890, XP002542140 ISSN: 0018-9383 cited in the application * Fig.5 and corresponding text *	1-14
A	BAUER F D: "The super junction bipolar transistor: a new silicon power device concept for ultra low loss switching applications at medium to high voltages" SOLID STATE ELECTRONICS, ELSEVIER SCIENCE PUBLISHERS, BARKING, GB, vol. 48, no. 5, 1 May 2004 (2004-05-01), pages 705-714, XP004489875 ISSN: 0038-1101 cited in the application * Fig.1 and corresponding text *	1-14

INTERNATIONAL SEARCH REPORT

International application No.
PCT/EP2009/057261

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-14

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-14

   Vertical IGBT or DMOS device with isolated gate electrode in combination with a dual level base layer optimised superjunction

   ---

2. claims: 15-16

   Vertical JFET device with adapted base region in combination with a single level base layer optimised superjunction

   ---

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2009/057261

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6184555 B1	06-02-2001	WO 9729518 A1	14-08-1997
		EP 0879481 A1	25-11-1998
		JP 4047384 B2	13-02-2008
		JP 2000504879 T	18-04-2000
DE 19604043 A1	07-08-1997	NONE	
EP 0578973 A	19-01-1994	DE 69324074 D1	29-04-1999
		DE 69324074 T2	12-08-1999
		JP 5347413 A	27-12-1993
		US 5286655 A	15-02-1994