

[54] **ELEVATOR CONTROL FOR OPTIMIZING
ALLOTMENT OF INDIVIDUAL HALL
CALLS TO INDIVIDUAL CARS**

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[73] Assignee: **Reliance Electric Company, Euclid, Ohio**

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[21] Appl. No.: 151,778

[52] U.S. Cl..... 187/29 R

[51] Int. Cl..... B66b 1/18

[58] **Field of Search**..... 187/29

[56] **References Cited**

UNITED STATES PATENTS

3,443,668	5/1969	Hall et al.	187/29
3,511,342	5/1970	Hall et al.	187/29
3,589,474	6/1971	Wavre.....	187/29

Primary Examiner—Bernard A. Gilheany

Assistant Examiner—W. E. Duncanson, Jr.

Attorney—Wilson & Fraser

[57] ABSTRACT

A system for assigning individual hall calls to individual elevator cars on the basis of service requirements imposed on the cars wherein signals associated with calls are time multiplexed and service requirements are represented by predetermined numbers of signal pulses which can be correlated to the anticipated delay imposed on the car in reaching the landing of the call and/or in travel commitments beyond the landing of the call. Pulse series for the several service requirements such as distance of the car from the call landing, car calls and hall calls assigned the car between the car and the call landing, and car calls and hall calls assigned the car beyond the call landing, are sequenced on a per floor basis as by a car travel scanning means so that one floor is considered at a time as to calls and then as to car travel distance so that no overlap of pulses is generated. Pulse series for car status representing conditions imposed upon the car as degree of loading, car in slow-down, door open, and car in acceleration are also sequenced to avoid overlap of pulses for the several factors. Pulse counts are accumulated for each of a plurality of cars to indicate the car best suited to serve the call to be assigned as that having the pulse count representing the least service commitment.

69 Claims, 18 Drawing Figures

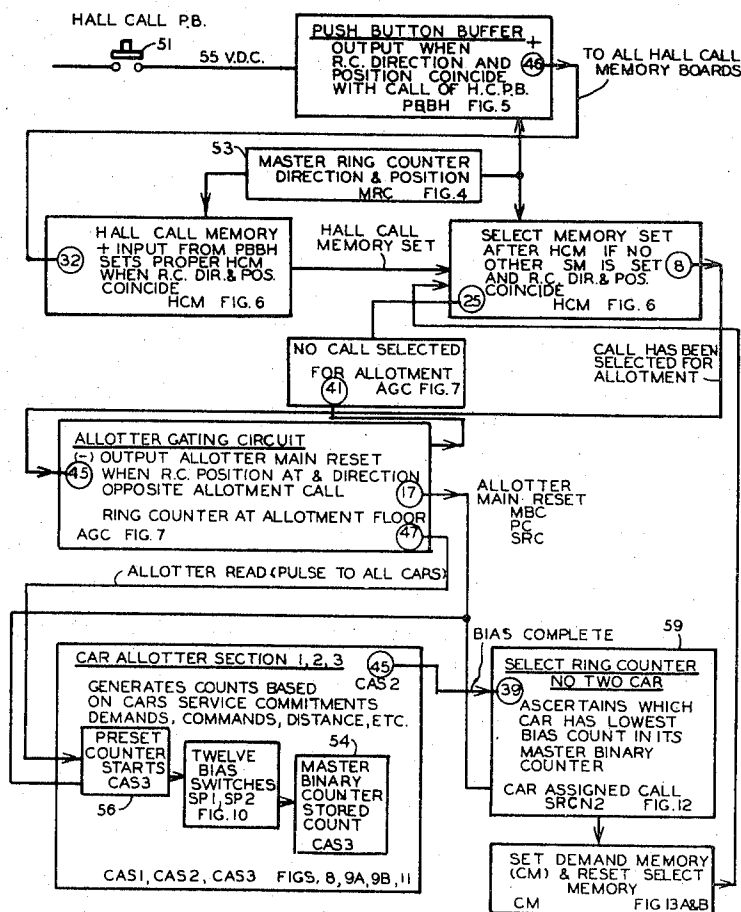


FIG. 2

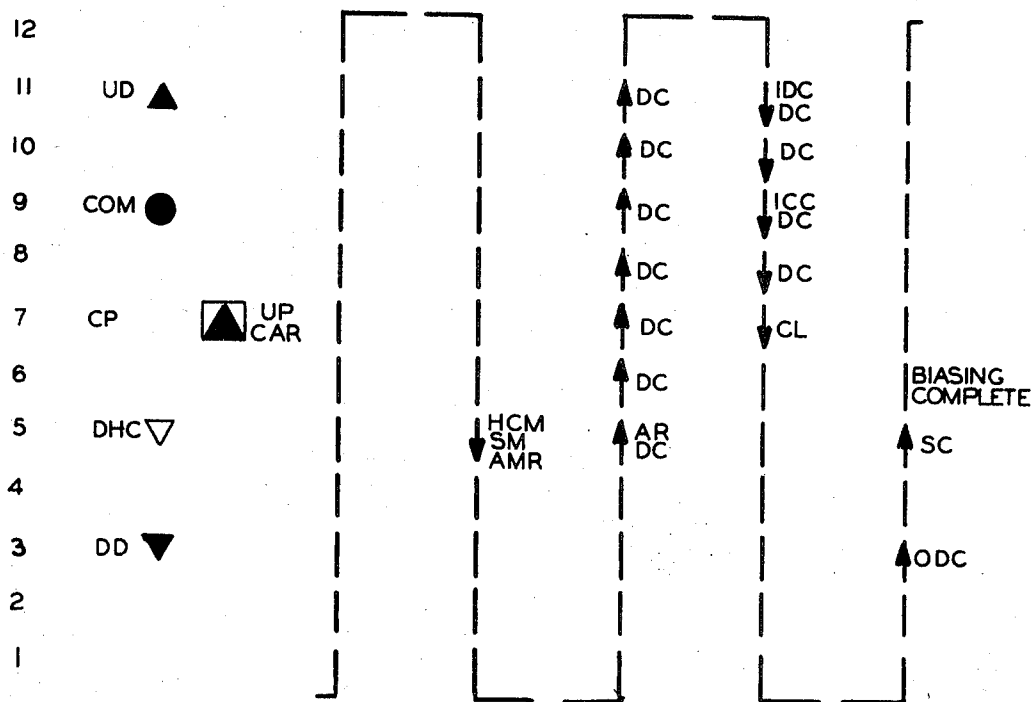
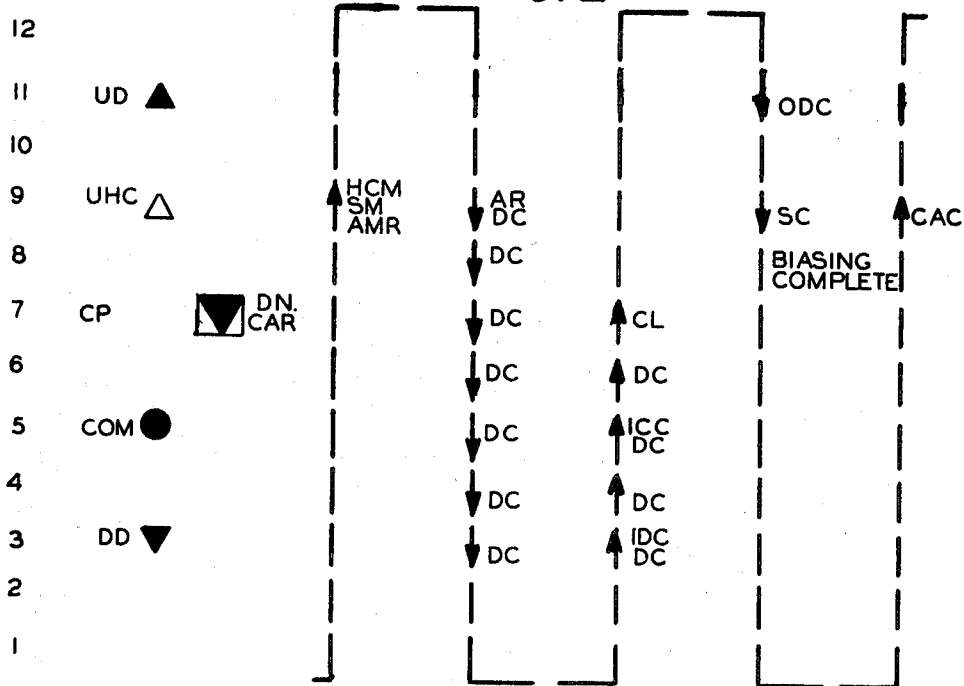


FIG. 3

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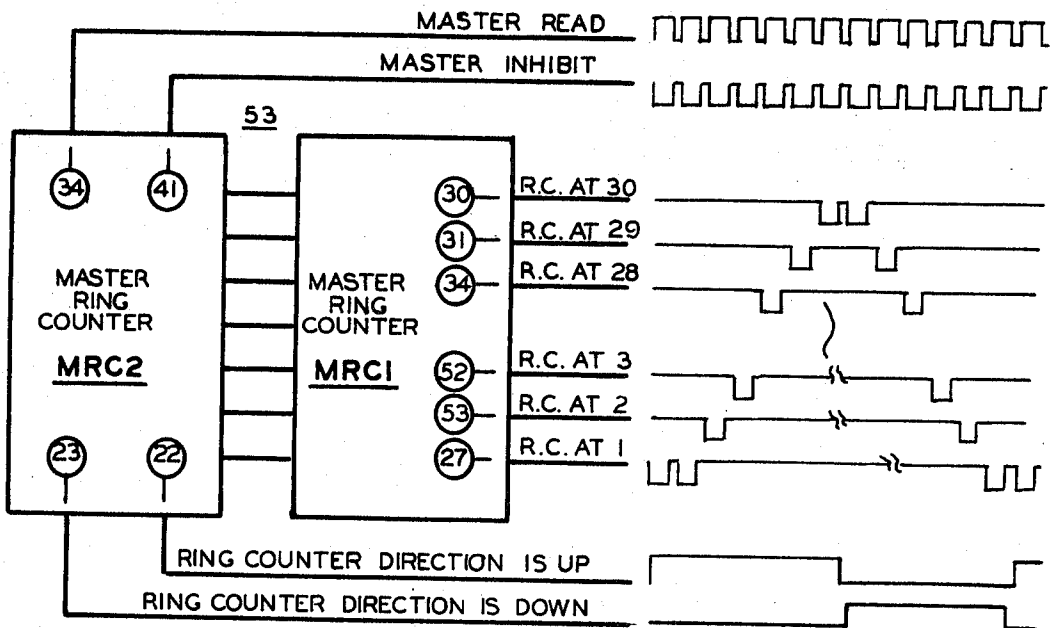
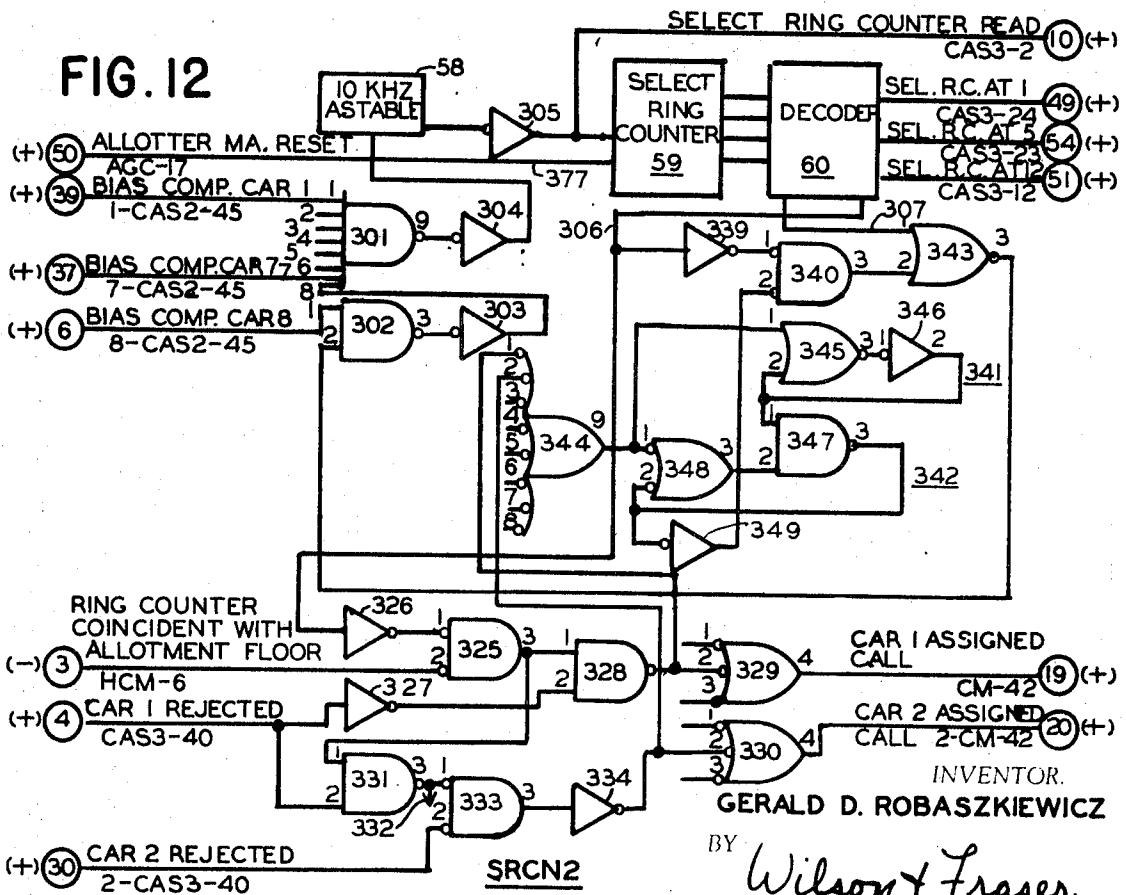
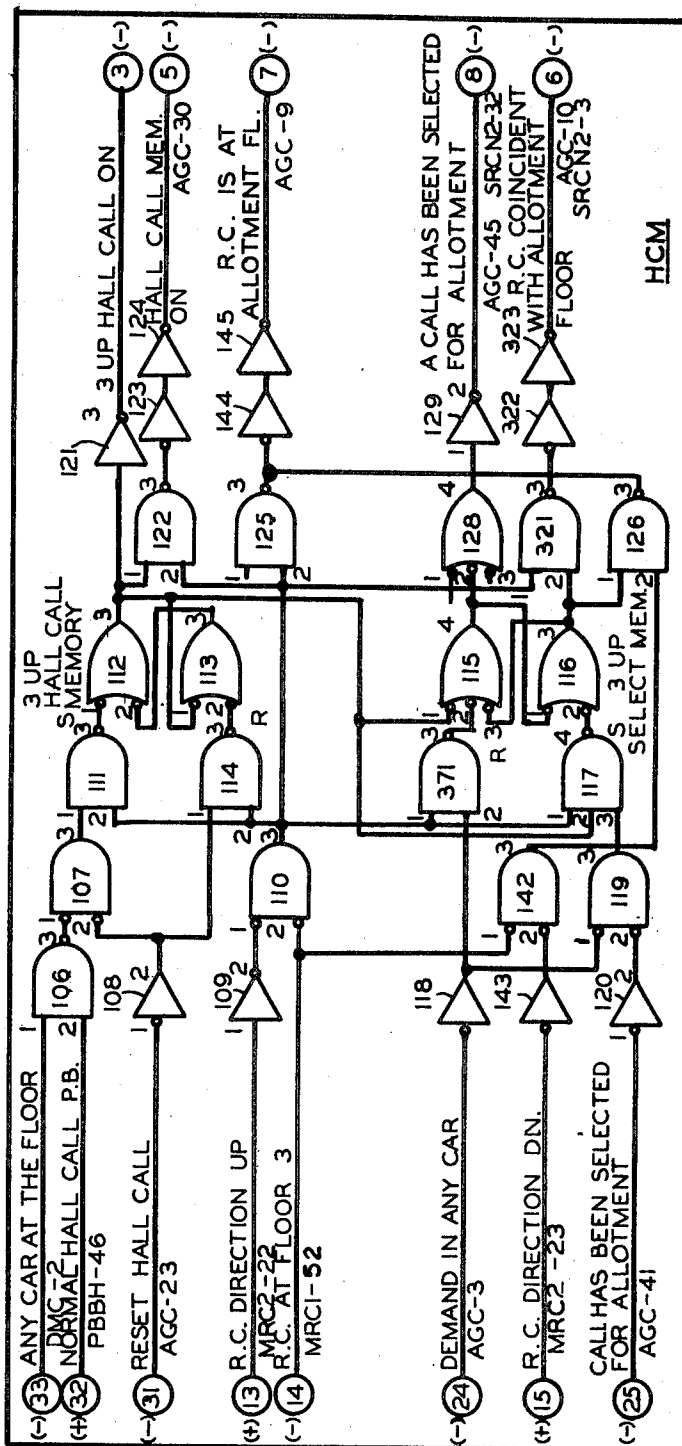
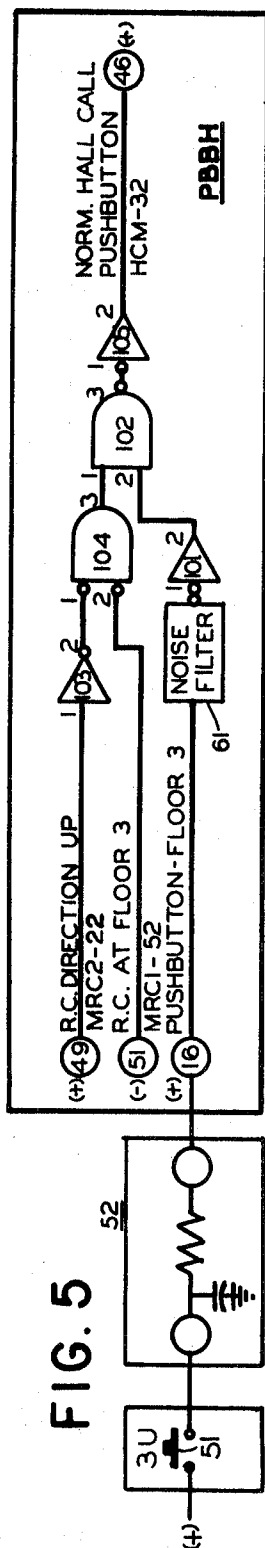


FIG. 4





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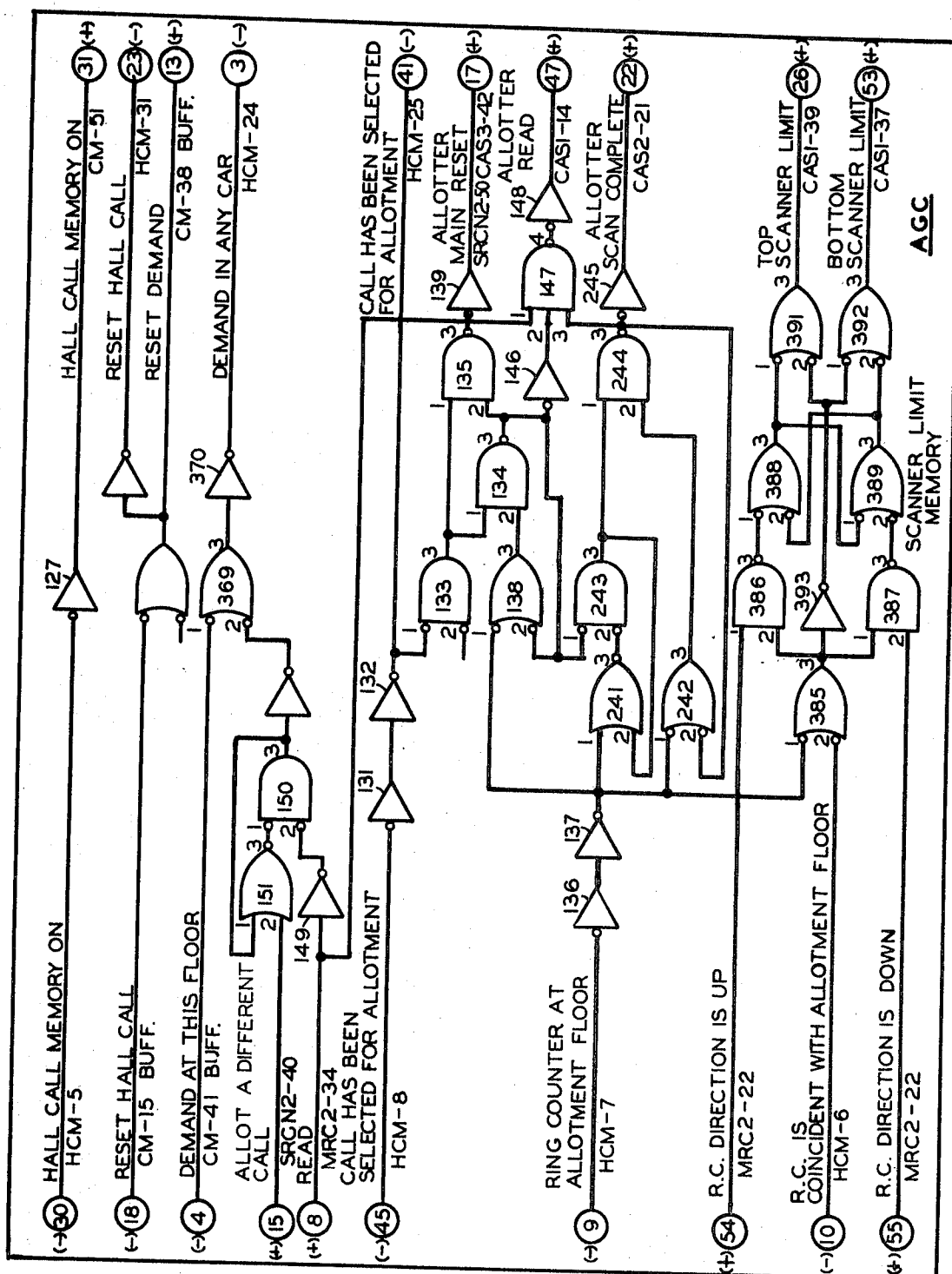
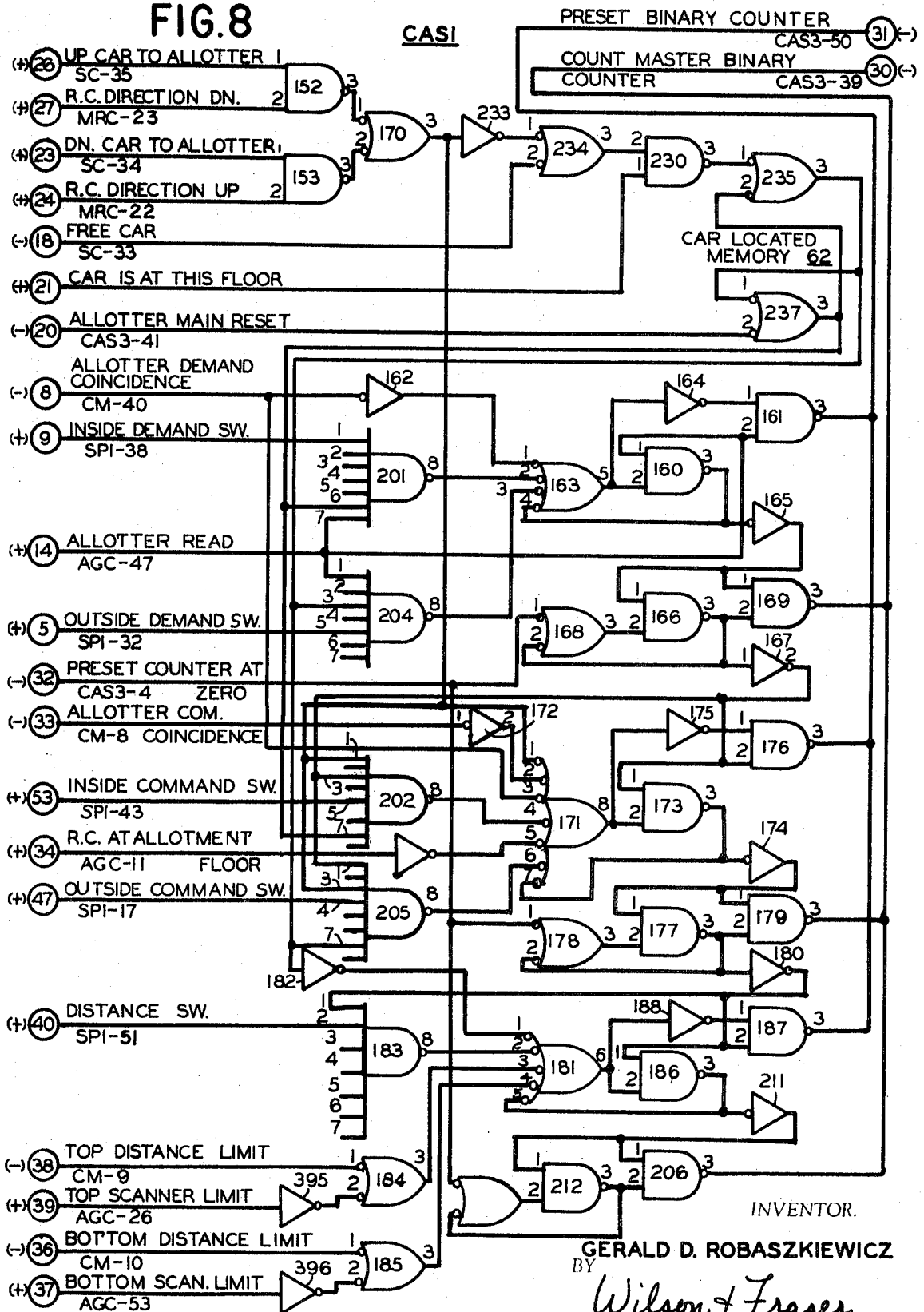


FIG. 7

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FIG. 8



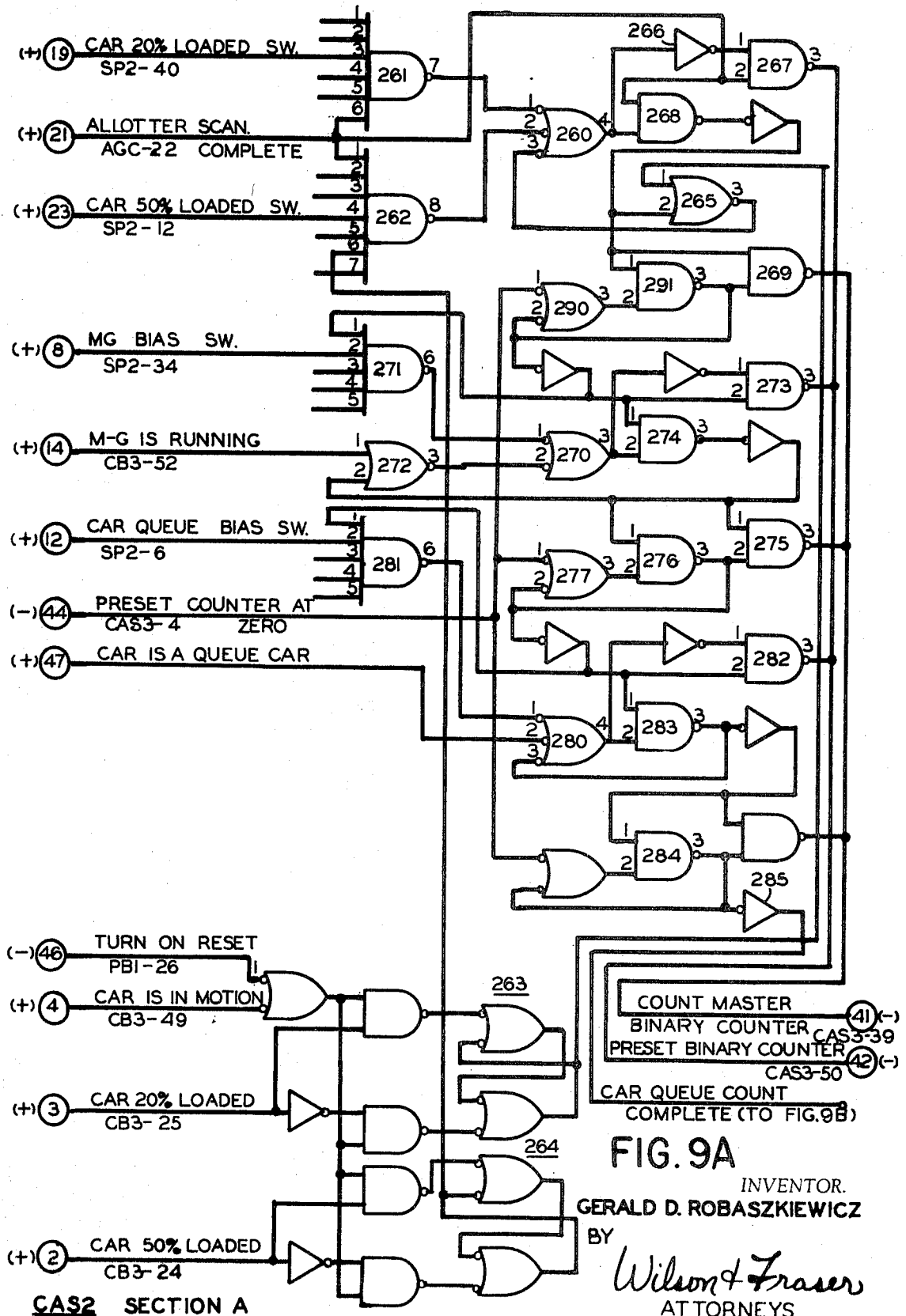
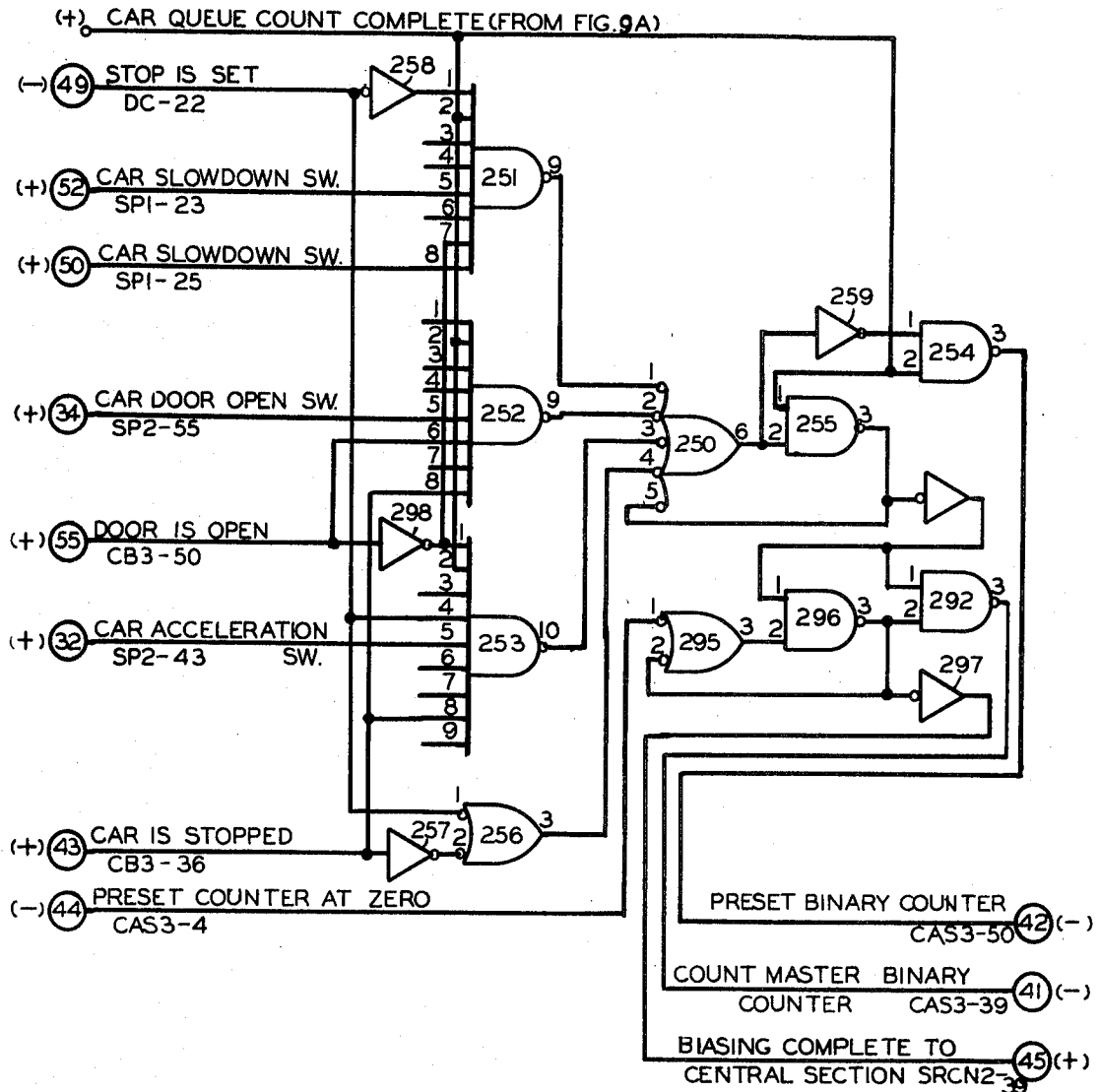


FIG. 9A

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FIG. 9B



CAS2
SECTION B

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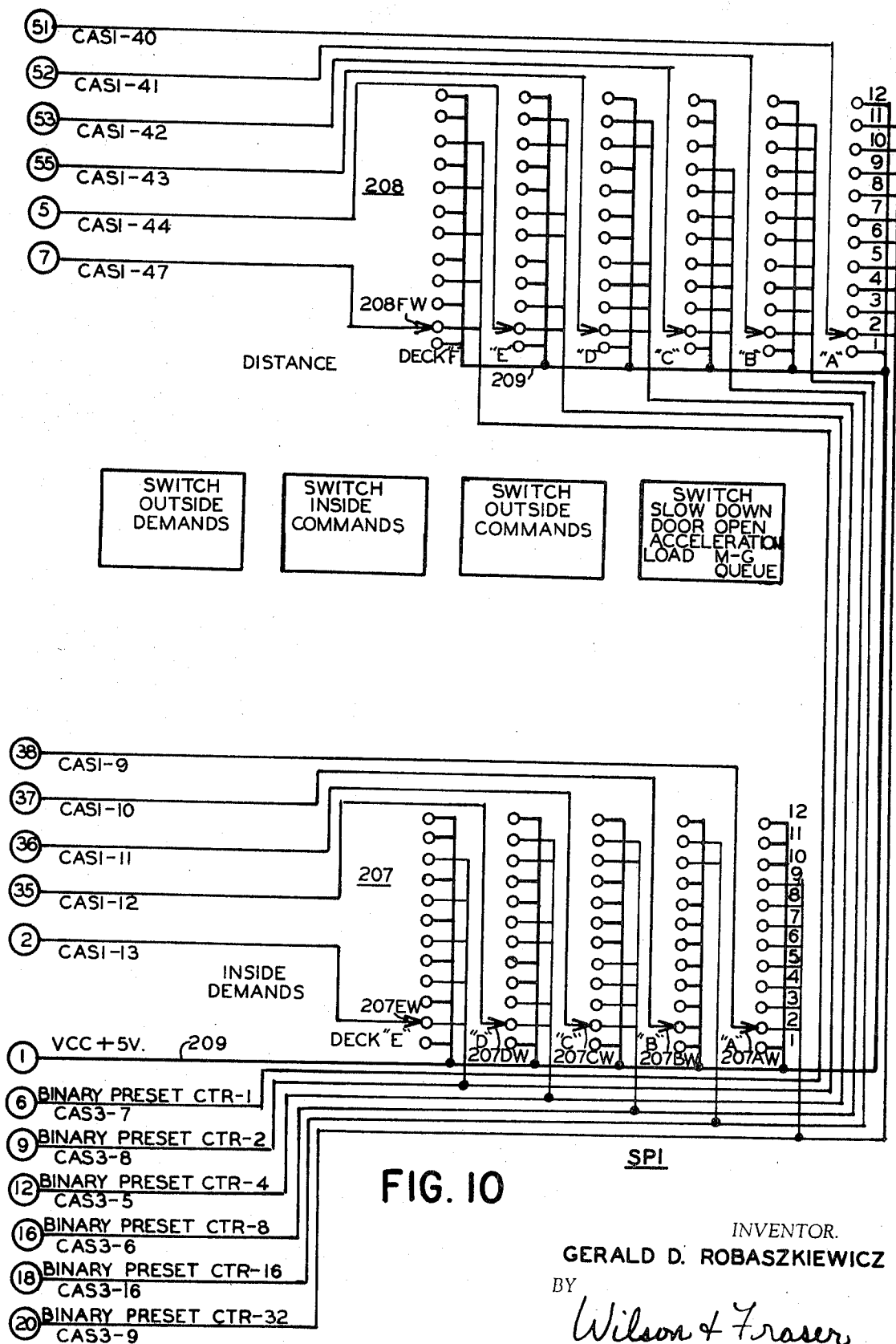


FIG. 10

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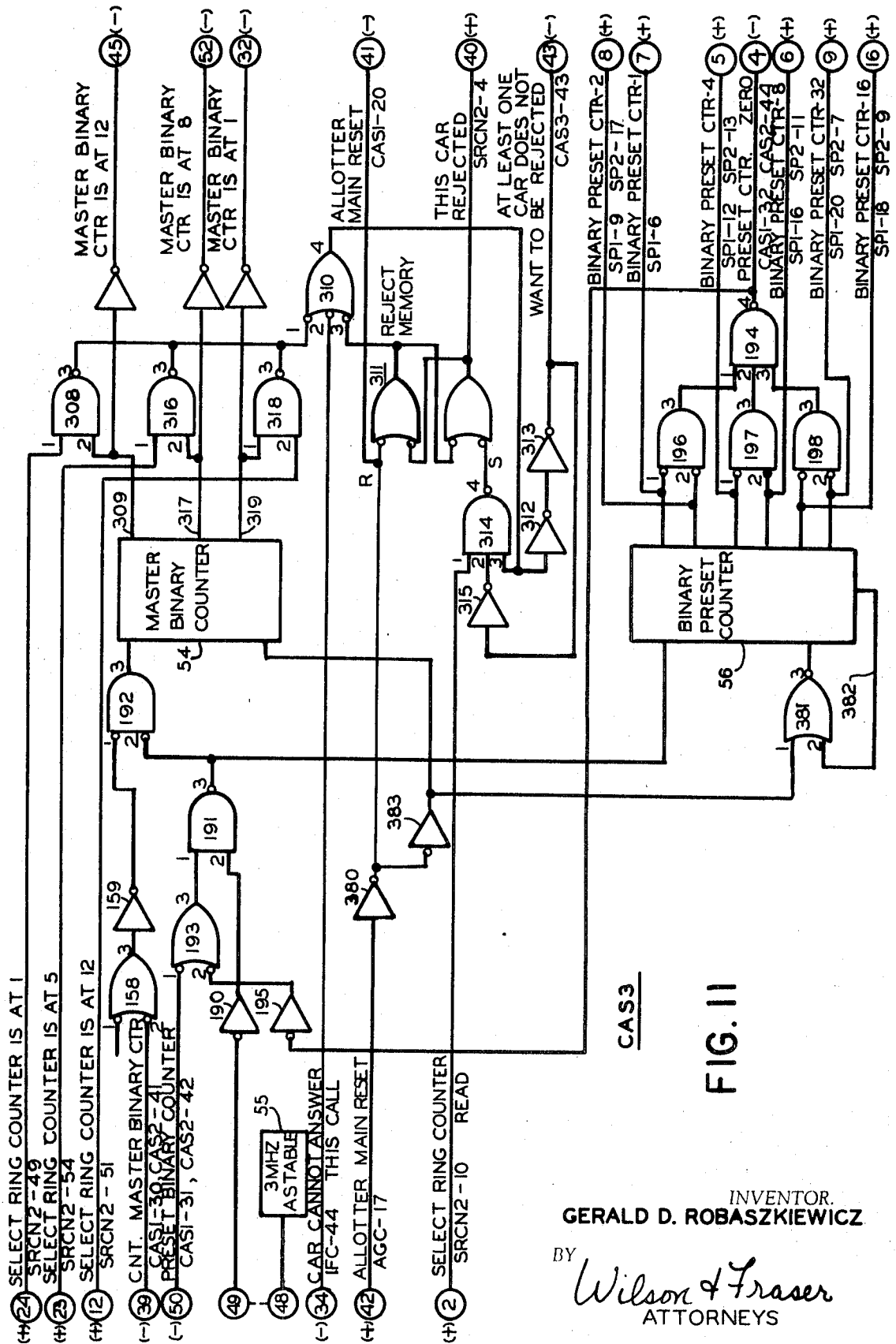


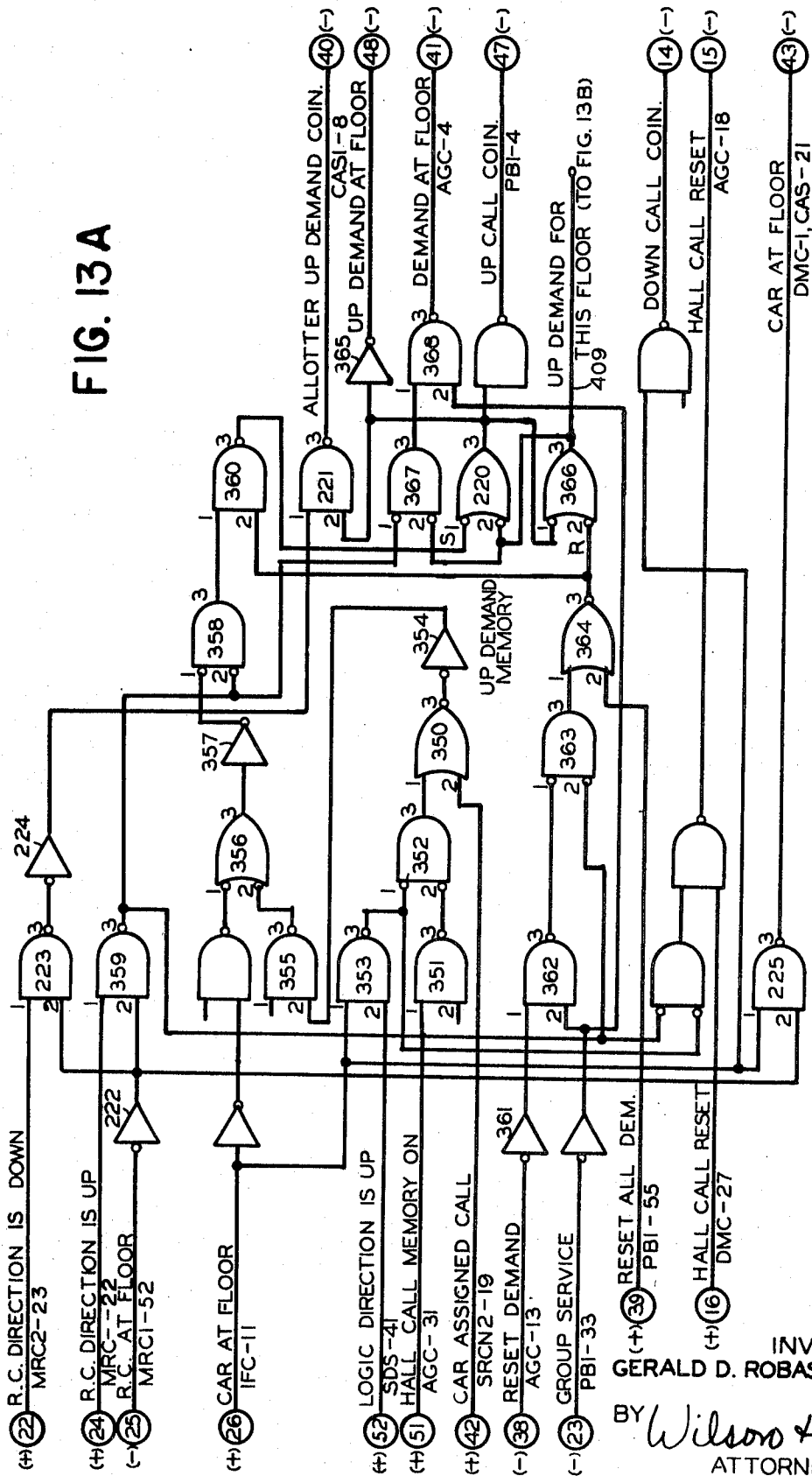
FIG. 11

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FIG. 13A



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CM
SECTION A

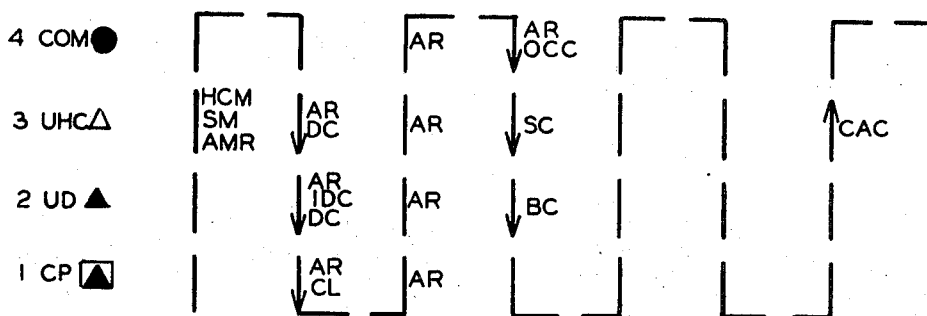
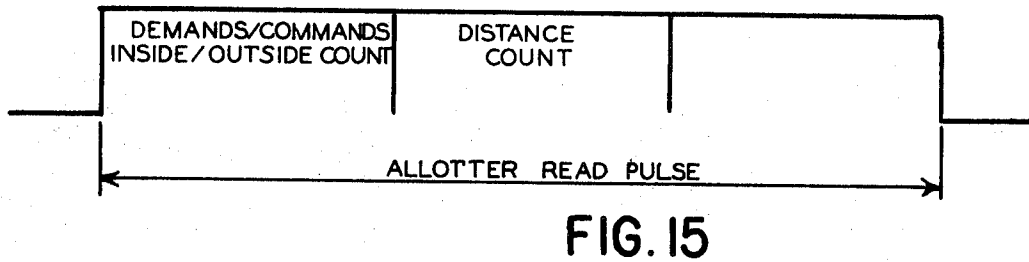
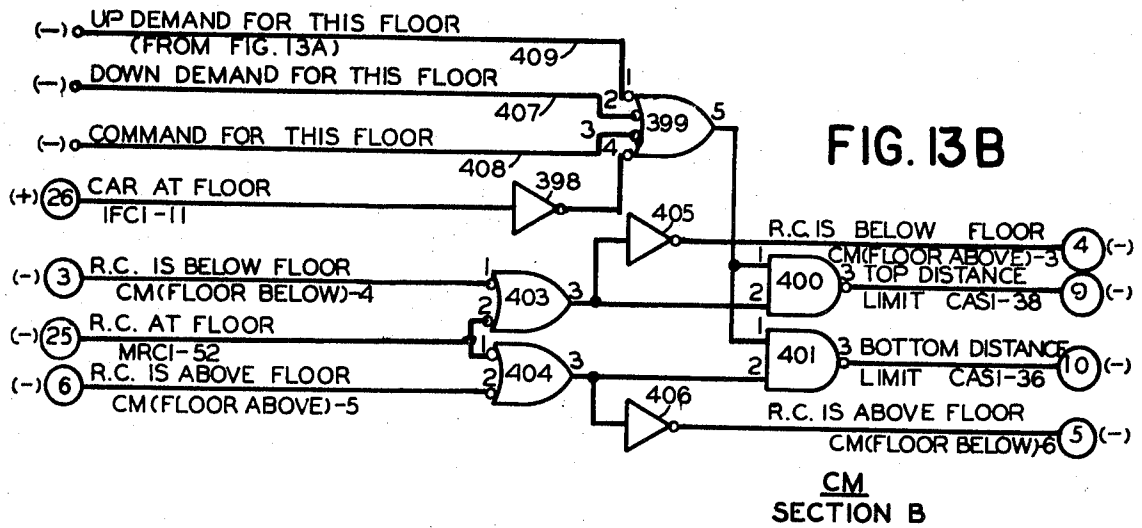


FIG. 14

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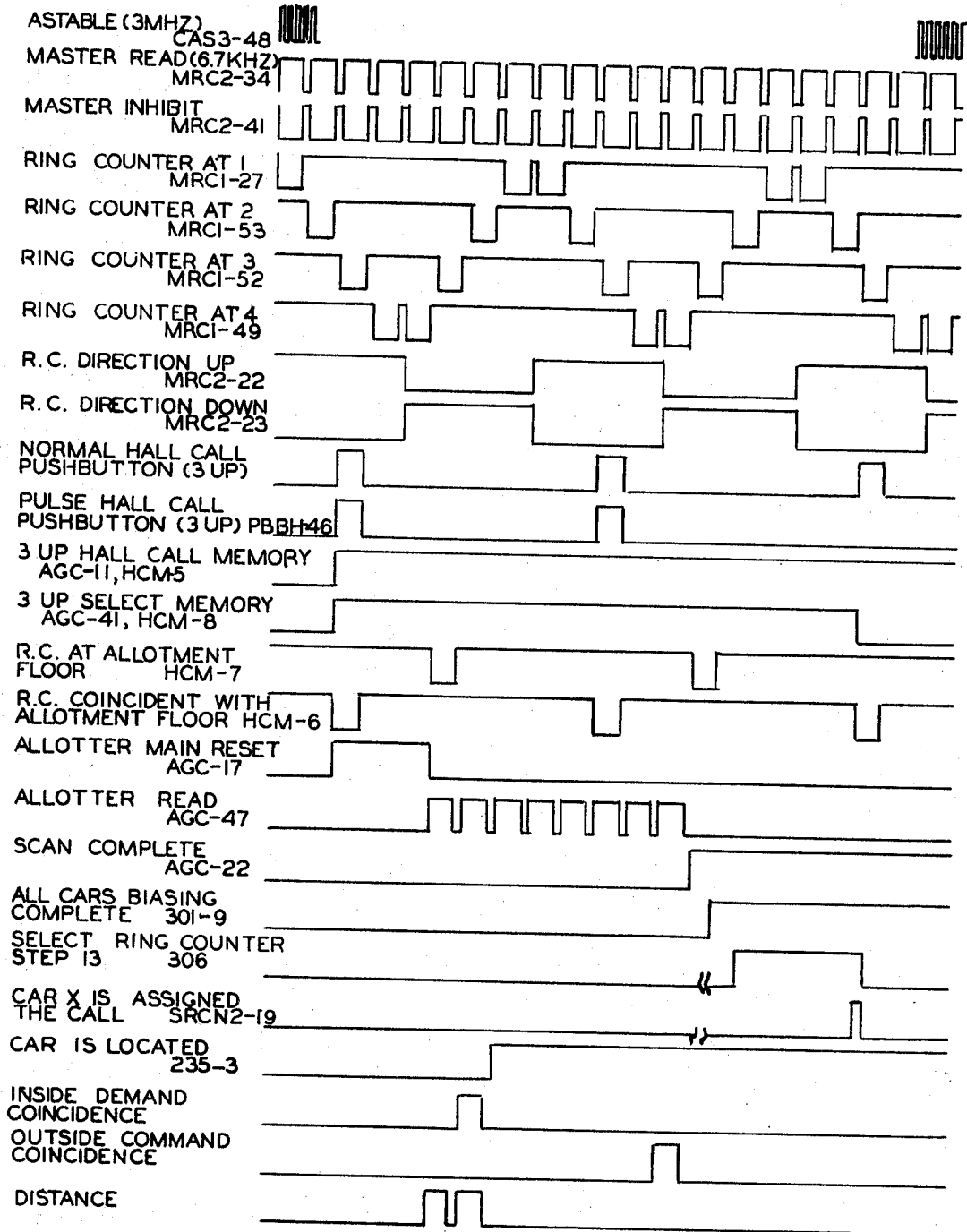


FIG. 16

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ELEVATOR CONTROL FOR OPTIMIZING ALLOTMENT OF INDIVIDUAL HALL CALLS TO INDIVIDUAL CARS

CROSS-REFERENCE TO RELATED APPLICATIONS

The elevator control of this invention is related to the control of United States patent application Ser. No. 151,697 entitled "Elevator Recall Control With Inter-floor Traffic Control" which was filed herewith in the names of Donovan L. Hall, Robert J. Lauer and Gerald D. Robaszkiewicz; Ser. No. 151,437 entitled "Multiple Digital Comparator" filed herewith in the name of Gerald D. Robaszkiewicz; and Ser. No. 151,861 entitled "Elevator Car Stopping Status Evaluating Means" filed herewith in the name of Robert J. Lauer.

BACKGROUND OF THE INVENTION

This invention relates to elevator controls and more particularly to means for translating service requirements to useful signals which can be combined to indicate a composite service burden. In one exemplary utilization the service burden is related to the capability of individual cars to serve individual hall calls and is utilized to optimize the assignment of individual hall calls to individual cars.

United States Pat. Nos. 3,443,668 which issued May 13, 1969, to Donovan L. Hall and William C. Susor for "Plural Car Elevator System for Developing Hall Call Assignments Between Individual Cars and Registered Hall Calls" and 3,511,342 which issued May 12, 1970 to Donovan L. Hall, William C. Susor and James H. Kuzara for "Elevator Control For Ascertaining the Capability of Cars to Serve Hall Calls" pertain to systems in which cars are assigned hall calls which may be many floors ahead of the usual call acceptance location of conventional elevator controls. These patented systems individually considered hall calls and established an assignment of each hall call, termed a "demand" after it was assigned. They ascertained the anticipated service burden imposed upon a car, as travel distance between the car and the landing of the hall call considered for assignment, the car calls registered on the car, the demands on the car, the car loading, and other factors which might delay its service, and summed those factors as an analogue signal value indicative of the car's service capability with respect to the hall call to be assigned. In some instances a count of the discrete factors as the number of floors to travel and the number of calls was converted to analogue values prior to summing. The summed signal for each car was then employed in ascertaining if the hall call under consideration should be assigned either by reference to fixed signal levels with assignment going to the closest car exhibiting a summed signal within the level or by reference to a ramp signal with assignment going to the car whose summed signal first matched the ramp signal.

Service capability of cars relative to hall calls, as ascertained above can be considered the equivalent of delay time. That is, a time interval can be specified for travel of a car one floor height at full speed, car call stops can be equated to time intervals as can demand stops, etc. so that rather precise service delays can be predicted for each car in reaching the floor of the call to be assigned and in concluding service beyond that floor to floors for which the car has calls. As the capability to predict has been refined, it has been found that

the analogue signal systems had shortcomings including instability of signal levels, and non-uniformity from system to system. Further, it has been found to be difficult to make adjustments requiring meter readings and precision potentiometers where factor values are to be changed for the circumstances of the individual systems. Further, where values of delay differ for different locations as for a distance to travel signal for short and long distances between adjacent landings the count of such floors or distance intervals followed by an analogue conversion of the total led to inaccuracies and offered no flexibility of adjustment.

The prior system of U.S. Pat. No. 3,443,668 employed a more cumbersome approach to the selection and allotting of hall calls than the present system in that a first scanner was placed in operation in response to the registration of a hall call to find the hall call as a call finder and then a second scanner was required to scan conditions from the selected hall call while inhibiting the call finder.

SUMMARY OF THE INVENTION

The present invention involves means for precisely defining service requirement values for elevator systems. More particularly, it is concerned with employing counts which may be pulse bursts of a number of pulses equated to the delay to be expected from imposed service requirements. These counts or pulse bursts are sequenced so they can be accumulated in a pulse counter to provide a precise service burden indication. Means can be provided in such a system to adjust the number of pulses indicative of any given value of a delay factor whereby the systems adaptability is enhanced.

It further involves a single continuously running scanner or master ring counter to time multiplex calls and signals associated with calls including the setting and resetting of memories associated therewith. The ring counter functions both as a call finder by setting a select memory corresponding to the hall call memory for a registered call and as an allotter scanner by scanning for the call of the set select memory from the location of the corresponding call. Upon assignment of a hall call to a car, termed an allotment, the select memory is reset, again by virtue of the scan coincidence with its floor. The master ring counter also defines read intervals for evaluation of service burdens imposed upon the individual cars for the several individual floors. This definition, for example as a read window of 125 microseconds for each floor separated by an inhibit read interval of 25 microseconds from the next floor's read window provides access to individual car allotment circuits which evaluate the burdens on a per floor basis. One such technique of evaluation is the issuance of higher frequency pulse trains during the window period for one or a plurality of burden factors to be accumulated on an individual car basis as a measure of service burden imposed on the car.

One illustrative embodiment of this invention is in an elevator control system for allotting hall calls to individual cars on the basis of an optimized allotment whereby the car having the best service capability with respect to the call to be allotted receives the allotment. In the illustrative system, the hall call selection and allotment is performed employing time sharing techniques. However, it is to be appreciated that service requirement evaluation of one or a combination of service factors for other types of elevator control systems

including individual car controls or plural car controls as where programs of operation are established and terminated by service conditions can utilize certain of the aspects of this invention.

In the illustrative system, service requirement factors for each of a plurality of cars relative to a hall call to be allotted are summed as a total pulse count for each car considering: the distance the car must travel, based on direction and service requirements, from its present location to the landing of the allotment call; the number of inside demands, hall calls that have already been allotted to the car for landings between its present position and the landing of the allotment call; the number of outside demands, hall calls that have already been allotted to the car for landings beyond the allotment call; the number of inside commands, car calls in the car for landings between its present position and the landing of the allotment call; the number of outside commands, car calls in the car for landings beyond the allotment call; the degree of loading of the car; the stopping status of car operation (if it is in a stopping mode) as accelerating, decelerating or standing with its door open; the state of its operating equipment, as motor set not running; and its assignment for special service, as at a lobby awaiting load in the manner of a queue car as disclosed in U.S. Pat. No. 3,474,885 of Oct. 28, 1969 by D. L. Hall et al. entitled "Queueing Controls For a Group of Elevators".

The influence for each factor as a service requirement represented by a number of pulses is adjustable. Further, since many of the factors were duplicated, as on a per floor basis, the system lends itself to applying different values to a given factor depending on special circumstances as for example a distance bias of six pulses for a normal floor height and a greater bias, proportioned to the time required for a car to travel the distance, for greater floor heights as a bias of 12 pulses on a floor having a floor height twice normal.

In the illustrative system the above factors are developed by operation of a pulse generator for each car having means to apply its output pulses to a binary preset counter and a master binary counter. Gating to the master binary counter is controlled in part by the binary preset counter for the per floor factors and by car status sequencing means for other factors. Since car status is a relatively static consideration, the count for the factors comprising car status can be sequenced as a preset count preceding the per floor scan for dynamic factor pulse trains or the status factors can be sequenced as pulse trains either before or following the consideration of the dynamic factors. The binary preset counter has sequencing controls which enable it to control pulses admitted into the master binary counter without overlap and loss. It has selectively coupled preset means arranged to establish an initial count which is barred from the master binary counter and a preset counter capacity count complement to that initial count which is admitted to the master binary counter as representative of the imposed service requirement then under consideration. The length of the applied pulse series is adjusted by adjustment of the preset to change the initially barred pulse train count.

Sequencing of the pulse trains is on a per floor basis beginning from the landing position of the allotment call and proceeding therefrom in the direction opposite the service direction of the allotment call. As each landing is scanned, service for that landing is read in an

allotter read interval which initially reads a command in the car for that landing, e.g. a 24 pulse count, unless a dominant demand is also in the car for that floor in which case a greater count is imposed, e.g. a 28 pulse count. If only a demand is present at the floor, the demand count is imposed. Thereafter in the allotter read interval for the floor, a distance count is issued if the car is committed to traverse that floor prior to answering the allotment call. The scan and resultant allotter read intervals for the floors between the car and the landing of the allotment call follow in the order of the floors. Beyond the landing of the allotment call the allotter read intervals apply outside command or demand pulse series for those landings for which there are commands or demands, e.g. 10 pulses for outside commands or 14 pulses for outside demands, without applying a distance pulse series for the floor. Upon return of the scan to the landing of the allotment call, the car status pulse series are applied in sequence for each factor. Following completion of the car status signals, the car with the lowest count in its master binary counter is assigned the hall call subject to allotment.

Comparison of the counts in the several master binary counters is by the simultaneous consideration of all master binary counters in a sequence beginning with the most significant bit and proceeding toward the least significant bit whereby assignment is avoided by rejecting cars having the highest counts through operation of respective reject memories. The car with the lowest count is identified by maintaining its reject memory in a reset state. It receives the allotment call as a demand when the master ring counter returns to the floor of the allotment call. In the event two or more cars have the same count a preference of assignment is established arbitrarily according to the numbering assigned the cars.

The call finding and allotting sequence is accomplished in the exemplary embodiment in about 18 milliseconds employing a scanning frequency of 6.7 kilocycles per second over a standard 30 up and 30 down scan positions for two or three sweeps and a service requirement counter frequency of 3 megacycles per second. Hence the system essentially freezes conditions during an allotment evaluation. Its high speed also permits the system to maintain optimum hall call allotments by frequent up-dating, as by release of demands on a car for reallocation of all such demands when significant changes of service burden on the car occur, as when the load changes or a car call is registered. Reallocation is based upon the same factors as allotment of a newly registered hall call.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a functional block diagram illustrating the service evaluation means of this invention in a call finder-allotter for a plural car elevator system utilizing time sharing techniques;

FIG. 2 is a schematic representation of a scan for a twelve landing elevator system employing the system represented in FIG. 1 for a typical car service capability evaluation for a car set for down travel at the seventh landing and showing only the scans of the actual floors of the system;

FIG. 3 is a schematic representation corresponding to FIG. 2 for a car set for up travel at the seventh landing;

FIG. 4 is a block diagram of the first and second sections of the master ring counter showing typical wave forms from certain of their terminals;

FIG. 5 is a logic diagram of a typical hall call switch, filtered coupling means, and pushbutton buffer to provide hall call signals to the system of this invention;

FIG. 6 is an abbreviated logic diagram of a hall call memory and select memory for a typical floor to store signals from FIG. 5;

FIG. 7 is an abbreviated logic diagram of an allotter gating circuit for providing output signals ALLOTTER MAIN RESET, ALLOTTER READ, and ALLOTTER SCAN COMPLETE to a system utilizing this invention;

FIG. 8 is an abbreviated logic diagram of a first car allotter section board for sequencing the dynamic service factors associated with the several landings for a typical car according to this invention for a typical car;

FIG. 9A and 9B are an abbreviated logic diagram of a second car allotter section board for sequencing the static car status service factors for a typical car according to this invention for a typical car;

FIG. 10 is a schematic representation of a typical selector switch for setting the weighting to be assigned a service factor of the type sequenced in FIGS. 8, 9A and 9B for a typical car;

FIG. 11 is an abbreviated logic diagram of a third car allotter section board for accumulating the service burden evaluations sequenced in FIGS. 8, 9A and 9B to ascertain the total service commitment of a typical car and for a reject memory for that car employed in the optimizing of the allotment;

FIG. 12 is an abbreviated logic diagram of a select ring counter and no two car board common to all cars of the system for comparing the accumulated service burden of the cars to select that car best situated with respect to the allotment call to receive allotment of that call;

FIGS. 13A and 13B are an abbreviated car memory for a typical floor and a typical car for storing allotted hall calls and car calls for that floor and car;

FIG. 14 is a diagram of a scan sequence for an allotment function similar to those of FIGS. 2 and 3 but for only four landings so that it is correlated with the detailed description of a conveniently illustrated embodiment of the invention;

FIG. 15 is a diagram of a time based expanded allotter read interval of the scan of FIG. 14; and

FIG. 16 is a diagram showing on a time base various signals employed in an allotment function.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The form of the service requirement evaluation means and the call to car assignment means of this invention can be employed in a number of different types of systems. For illustrative purposes, they will be considered in a system in which time sharing of signals is employed whereby the signals for individual landings are gated in many instances only during the brief period a master ring counter is at the scan position corresponding to that landing, and in some instances, only when the master ring counter scan and scanning direction are correlated with the landing and the service direction associated with the call or with a car position.

The functional block diagram of FIG. 1 represents the call finding and allotting signal flow for a time sharing system including the service evaluation means and

car assignment means of this invention. The system selects a hall call which is to be assigned and allots that call to the car best suited to serve that call as viewed from a consideration of the current service capability of each car relative to the landing and service direction of the selected hall call.

A review of the general call finding and allotting functions will precede a more detailed consideration of an abbreviated system including only four landings so that a full cycle of the call finding and allotting can be illustrated conveniently.

In the discussion of the functional block diagram of FIG. 1 reference will be made to the logic diagrams of FIGS. 4 through 12 in which the functions are accomplished. Operation of the call finding functions requires registration of a hall call for a given direction of service from that landing.

The depressing of the up hall call push button 51 of FIGS. 1 and 5 begins the allotting sequence. This places a signal on the corresponding R-C filter board 52 to set the proper push button buffer board PBBH of FIG. 5. Where time sharing of signals is employed and the range of car travel is scanned as by a master ring counter 53 of FIG. 4, which scans in an ascending order of floors followed by a reversal to scan in a descending order of floors, the output signal from PBBH is present only when the ring counter direction and position coincide with the floor and direction of the operated hall call push button. The output is a PBBH terminal 46 as a (+) signal. This coded output signal is sent from PBBH to the corresponding hall call memory for the floor of the call on the hall call memory board HCM of FIG. 6 as at terminal 32 of HCM. Time sequencing of the master ring counter codes the input to set the hall call memory for the floor and service direction of the call.

If no other call is being allotted, as indicated in the hall call memories HCM by all select memories being off, the call is selected for allotment when ring counter position and direction correspond with the set hall call memory. This sets the select hall call memory, select memory of FIG. 6 to indicate, by a (-) signal at terminal 8 of HCM to terminal 45 of AGC, to the allotter gating control AGC, FIG. 7, that this hall call has been selected for allotment. All of this is coincident with ring counter scan position and direction.

Allotment is based upon the count accumulated in each car's master binary counter 54 as shown in FIG. 11 in the car allotter section board 3, CAS3. An initial step in each allotment, therefore, is to reset the allotter by applying to it an ALLOTTER MAIN RESET from terminal 17 of AGC as a (+) signal. In the time sharing type of control this occurs when the ring counter is at a scan position of the allotment floor in the direction of allotment call service. This reset signal resets the binary preset counter 56 and the master binary counter 54, and thus the count held in each car's master binary counter 54. It also resets the select ring counter 59 employed in each selection of a car to be assigned a call in SRCN2, FIG. 12.

When the master ring counter returns to the allotment floor with its direction opposite that of the service direction of the hall call to be allotted a signal RING COUNTER AT ALLOTMENT FLOOR is generated in FIG. 6. This results in turning off of ALLOTTER MAIN RESET and turning on ALLOTTER READ signal from the allotter gating circuit AGC, FIG. 7. An

ALLOTTER READ pulse is issued from terminal 47 as a (+) for each floor as the master ring counter scans the range of car travel and each pulse is sent to each car's car allotter section CAS1, FIG. 8.

During the allotter read interval for each floor, each car is checked for a demand and a command at the floor and if either is present a pulse series is gated into that car's master binary counter 54 to represent the service burden it imposes. A travel distance pulse for the floor is also inserted in the car's master binary counter if it must traverse the floor to reach the allotment call.

A pulse generator 55, FIG. 11, which can be an astable 55 operating at three megacycles constitutes a pulse source for the service requirement pulse series passed to each car's master binary counter 54. When ALLOTTER READ turns on, each car is checked for a demand at the floor in CAS1. The PRESET MASTER BINARY COUNTER signal is applied to binary preset counter 56 to count pulses generated by the 3MC astable 55 if there is a demand at the floor. If there is no demand, no demand count is permitted. If a demand exists, the preset counter 56, which has a count capacity of 64 before resetting, counts the preset counter capacity count complement of the demand pulse series as set by a biasing control typified by switch 207 FIG. 10. When the count in the preset counter 56 reaches the bias setting for demands, the signal COUNT MASTER BINARY COUNTER is turned on to admit the remaining pulses to the master binary counter 54. An inhibit signal is imposed on the pulse gate from the 3MC astable when preset counter 56 returns to zero at its 64th count.

If the floor of a demand which is subject to ALLOTTER READ is encountered subsequent in the scan of the master ring counter to the setting of car located memory, see FIG. 8, operated when the scan coincides with car location, the demand is identified as an outside demand and the pulse series is of the length set for outside demands.

Prior to setting of the car located memory an encountered demand is an inside demand.

Completion of the demand evaluation, or skip through if no demand is present, is signified by a DEMAND COUNT COMPLETE signal on CAS1 of each car to enable other service factors at the floor to be read by the allotter, see FIG. 8. If no command is present, the circuits skip through to the next bias. Presence of a command will cause a series of pulses to be gated from astable 55 to master binary counter 54 for the car provided no demand was indicated. Command pulsing is skipped if a demand was recorded during the same ALLOTTER READ pulse.

Following the demand and command consideration portion of the allotter reading interval for a floor a terminal portion of that interval is employed to apply a distance pulse series from astable 55 to master binary counter 54 by filling the preset counter 56 to its bias level adjustment. The complement count of that bias level is gated to master binary counter 54 by controls subject to counter 56 provided the car is committed to travel to that floor before reaching the floor of the allotment call. Thus, after the car is located memory of CAS1 has been set, the distance pulse series are inhibited.

In order to permit the reading of demand or command and distance pulse series into the binary counter, the allotter read interval is set at about 125 microseconds in the exemplary embodiment. A read inhibit in-

terval of about 25 microseconds separates each allotter read interval.

The car is located memory of CAS1 is set when the master ring counter position corresponds to the car position and ring counter direction opposes car direction. This causes the transfer of the pulse series for demands and commands from inside to outside and skips through all further distance biasing.

As the ring counter reaches the allotment floor following a complete scan for allotter read functions, the ALLOTTER READ pulses are discontinued from allotter gating circuit AGC and AGC issues a SCAN COMPLETE signal. This signal initiates a check of car status for each car through operations in CAS2, FIGS. 9A and 9B corresponding generally to an allotter read interval. Gating means are actuated in a sequence for various car conditions which are indicated as service burdens or requirements imposing prospective service delays as pulse series applied to master binary counter 54 to accumulate additional count in each car's counter. The static car status factors are loading at 20 percent and 50 percent of rated capacity, M-G set operating status, queue status wherein the car is held at a landing to receive passengers, and three phases of car stopping functions as car in slowdown mode, car is stopped mode (door open) and car is accelerating mode. Only one car stopping status is read for each car and all static car status factors are read without regard to read pulses of the master ring counter.

When all static car status factors have been scanned, a BIAS COMPLETE signal is issued by CAS2 of each car to select ring counter no two car board SRCN2, FIG. 12. Upon receipt of a BIAS COMPLETE signal for each car as a + signal from terminal 45 of CAS2 of each car to terminal 39 of SRCN2, SRCN2 starts the process of selecting the car having the lowest bias count in its master binary counter.

A pulse generator 58 which can be a 10 kilocycle astable actuates the car selection by driving select ring counter 59. Counter 59, through decoder 60 applies signals to each car's CAS3 to compare the outputs of the cars' master binary counter 54. Fourteen separate signals are employed in the comparison sequence to enable a comparison of output bits from master binary counters 54 in a sequence proceeding from the most significant bit to the least significant bit. The objective of selecting the car whose master binary counter has the lowest count and thus has the lowest service requirement is achieved by a process of elimination in which allotment is rejected by setting a reject memory in each car's CAS3 until one car remains with no reject memory set. The setting of a car's reject memory prevents its assignment to the allotment call.

Twelve of the select ring counter's counts are employed in the comparison for a typical system capable of evaluation of counts for a 12 stage counter. The 13th select ring counter count allows the unrejected car to be assigned the call by actuating suitable gating. If two or more cars contain the same master binary counter count, then the lowest numbered car is assigned the call.

In the example, the selection of the car in optimum service condition as evidenced by the lowest count is accomplished by a decoder as disclosed in greater detail in the above mentioned Robaszkiewicz patent application for "Multiple Digital Comparator". The steps in the comparator function are clocked by an astable

operating at 10 KH and thus at a frequency closely approximating that of the master ring counter. Allotment of the call to the selected car occurs when the scanner scan position and direction coincides with the call. Therefore, the master ring counter often will advance beyond the position and direction of the call while the select ring counter is selecting the car. This requires the advance of the scan through another cycle to return it to the scan position and direction of the call for completion of allotment. In the description which follows, a 12 scan position and a four scan position example are presented as though their respective master ring counters scanned only the floors of the system. In practice, it has been found convenient to permit the scanner to scan a greater number of positions than the number of landings. One arrangement is that of a 30 scan position master ring counter unit which can be expanded as by duplicating the scan position portions to make a unit of increased capacity in 30 position increments. Such a 30 scan unit will require scan steps beyond the actual floors of a 12 floor system and, therefore, call allotment at the end of the scan having the extra scan positions can be made upon the next coincidence of scan position and direction with the call since the car selection process proceeds while the master ring counter is scanning the extra floors. In view of the variants in the allotment floor locations, the call allotments, therefore, are completed in the examples in two scans for calls located a substantial distance along the scan path from the position at which the select ring counter is placed in operation and three scans where the location is close to the select ring counter start position.

When the master ring counter position and direction coincide with the hall call selected for allotment, the hall call memory HCM issues RING COUNTER OPPOSITE ALLOTMENT FLOOR to the SRCN2 board so that the unrejected car is issued a CAR ASSIGNED CALL signal to set its demand memory for that floor and direction in its car memory board CM for that floor.

The demand memory issues a DEMAND AT THIS FLOOR to the allotter gating control AGC to issue a THIS DEMAND IN ANY CAR signal which is decoded in the hall call memory HCM of that floor to reset the select memory for that allotment call and conclude the allotting sequence.

The scan sequences discussed above are illustrated in FIGS. 2 and 3 for a 12 landing system. Each vertical dash represents a master ring counter interval of scan at a landing in horizontal alignment therewith and as indexed on the left side of the drawing. In FIG. 2, the sequence is applied to a descending car at floor seven, CP (car position) represented in the index as a square containing a downward directed arrowhead. Its service capability is evaluated with respect to an up hall call UHC, represented by an unshaded upwardly pointing arrowhead, for the ninth landing and a car call or command COM represented by a solid circle, for the fifth landing. In FIG. 3, the sequence is for an ascending car at floor seven CP to evaluate its service capability with respect to a down hall call DHC for the fifth landing. In each sequence, the car has an eleven up demand UD (an assigned up hall call), as represented by the up-pointing solid arrow in its left marginal index opposite the eleventh landing, and a third down-demand DD as represented by the down-pointing solid arrow in its index opposite the third landing. In FIG. 2, the car has

a car call or command at floor five and in FIG. 3 it has a command at floor nine.

Master ring counter scanning is continuous. For convenience, it is assumed that it starts at the first landing and is set for scanning upward. In FIG. 2, the scan advances through the eighth landing without effect. At the ninth landing, the scan is coincident with the call assumed for allotment as to both position and direction, as represented by the arrowhead superimposed on the dash of the scan pulse and the designations HCM, SM and AMR to represent the setting of the hall call memory, the select memory and the allotter main reset respectively. The scan proceeds to the 12th landing as an up scan and then initiates down scanning from 12 until it reaches the landing of the allotment call, the hall call in select memory at nine. With the scan coincident with the landing of the allotment call and opposite the service direction of the allotment call, an allotter read signal is issued, as AR opposite nine, and a distance count DC is generated for that floor and in subsequent scan positions for the other floors to be traversed by the car in satisfying its current service commitments. Thus, a distance count issues for floors nine through three on the descending scan. The car need not travel beyond the lowest call, the down demand at three, hence no distance count is generated below three.

On the ascending scan of the master ring counter no service requirement counts are issued until the third landing is scanned. The car is committed by the down demand at three to serve floor three. Demands are read when scan direction opposes their service direction. An inside demand count IDC is generated during the up scan of three to take into consideration the car's down demand at three. A second distance count DC is generated for the third landing and for landings above as the scan advances until the landing at which the car is located and at which the car is set to travel opposite the scan direction is reached to generate a car located signal CL. During the upward scan of the fifth landing, the inside command ICC representing the car call for the fifth landing is counted. Commands are counted when the scan is coincident with the call and the scan direction opposes the direction the car is set run.

After the car is located scanning proceeds to the landing of the allotment call to permit outside demands and commands to be counted. In FIG. 2, the up demand at 11 is counted during the down scan of 11 as outside demand count ODC.

Scan is completed at the ninth landing by a signal SC. Thereafter, the static car status is ascertained as a sequence of evaluations of load bias at 20 or 50 percent of capacity, M-G set bias, queue status bias and operating mode bias in that order with counts for each. A biasing complete signal is then issued for all cars and the select ring counter 58 placed in operation.

FIG. 3 shows an allotter scan sequence for a five down hall call. Initiation of allotter read AR occurs on the up scan coincident with the allotment call landing, landing five. Inside calls and distance are counted until the descending scan is coincident with the floor of the car. Allotter read continues for an additional portion of half scan to the floor of the call to be allotted to complete the scan for outside demands and commands.

Only that portion of elevator system disclosing the means of establishing service burden levels, for typical positionally related and static factors, combining several such established levels for a typical car and evalu-

ating the combined levels for a plurality of elevator cars is illustrated. In illustrating these elements, the values ascertained are shown as the means of assigning or allotting a hall call to the elevator car of the plurality which is best suited to serve that call.

Much of the individual car controls and the central supervisory controls for a plural car system has been omitted. It is to be recognized that the elevator cars are provided with hoist motors, motor controls, means coordinating their position and movement with the motor controls and the system supervisory controls. Further, interfacing means and buffers must be provided between the system inputs and the supervisory controls and between the system outputs and those controls. The coupling of these various elements to start, stop and run the cars, to open and close their doors, and to actuate the external signals can be accomplished by apparatus of various known forms.

In order to illustrate the service requirement evaluation means and the means of optimizing the allotment of hall calls to individual cars best situated to serve them, the apparatus for registering a typical hall call and for operating upon that hall call and typical service requirements imposed on that car together with the apparatus for one car for allotting that hall call as a demand on the car is shown. Abbreviated logic diagrams are sectionalized as boards or chassis in which related functions are performed. The abbreviated printed circuit boards disclosed are designated by symbols and have titles generally indicating the functions they accommodate as follows:

SYMBOL	SHORT TITLE
AGC	Allotter Gating Circuit
CAS1	Car Allotter Section Board No. 1 (per car)
CAS2	Car Allotter Section Board No. 2 (per car)
CAS3	Car Allotter Section Board No. 3 (per car)
CM	Car Memory (per car per floor)
HCM	Hall Call Memory (typical per call)
MCR1	Master Ring Counter — position
MCR2	Master Ring Counter — read-inhibit and direction
PBBH	Hall Call Push Button Buffer (typical per button)
SP1	Switch Panel No. 1 (per car)
SRCN2	Select Ring Counter And No Two Car

A number of circuit boards are not shown although they supply input signals to those boards illustrated. Generally, the functional designations on the input leads are self-explanatory as to the purpose of those signals. Boards which are not shown include:

SYMBOL	
CB3	Contact Buffer — per car
DC	Door Control — per car
DMC	Door Mode Control — per car
SC	Start Control — per car
SDS	Stop and Direction Selection — per car
SP2	Bias Switches (corresponds to SP1) — per car
IFC	Interface Control (from floor selector)—per car

Each board except SP1 includes a number of integrated circuits which are represented by logic elements of their individual sections. These circuits are in transistor-transistor logic to provide NANDs and NORs. In order to facilitate an understanding of the logic and associate terminals with boards and logic ele-

ments, a system of identification will be followed wherein boards terminals will be numbered within the circles adjacent their margins representing those terminals and the board symbol will be placed within and in the lower right-hand corner of a rectangle encompassing that portion of the board illustrated. A label will be applied to each board input and output to designate the general logic function of the signal it transmits. The true signal will be designated parenthetically as "(+)" or "(-)" when the labled function is effective. In the discussion, the board terminals will be designated as PBBH-16+ to represent a positive going or logical 1 signal applied to terminal 16 at the lower left of the PBBH board in FIG. 5. A logical 1 on the output terminal 46 of board PBBH will be designated PBBH-46+ and conversely a logical 0 will be PBBH-46-. The individual logic elements can be one or more multiple input NAND gates in commercial integrated circuits as quadruple 2-input NAND gates, SN740N, triple 3-input NAND gates, SN7410N, dual 4-input NAND gates, SN7420N, 8-input NAND gate, SN7430N, and quadruple 2-input NAND gate with open collector output SN7401N all of which are available from Texas Instruments Incorporated, Post Office Box 5012, Dallas, Texas 75222. Further, dual 4-input NAND buffer units SN7440N, four bit binary counters SN7493N, and binary to decimal decoders SN7442N are available from Texas Instruments Incorporated.

The individual logic elements of the integrated circuits are designated in a numerical reference character sequence beginning with 101 and their terminals are designated numerically. Small circles on the terminals of the logic elements indicate the signal is of the opposite sense when passed through it. Thus, in FIG. 5, logic element 101 is a NOT or inverter gate which assumes the inverse of its input as a negative (-) signal 101-1- and results in a positive (+) signal 101-2+. Note that the terminal designation follows the element reference character and is separated therefrom by a dash while the signal is designated by a suffix minus or plus sign. NAND 102 of FIG. 5 upon coincidence of 102-1+ and 102-2+ issues a 102-3- while the presence of either a 102-1- or 102-2- issues a 102-3+. NANDs are also represented as NAND 115 of FIG. 6 where they perform OR logic to issue a 115-4+ when any of their inputs have a minus. NOR 104 of FIG. 4 will issue a 104-3- where any input receives a plus and a 104-3+ when both inputs are minus while NOR 241 of FIG. 7 is employed for a coincidence function where 241-1- and 241-2- produce a 243-3+ output.

With the above nomenclature in mind, the allotment of a hall call will be described for a system of four landings. In this description, the following assumptions are made for convenience:

1. The car to which the allotment will be made is at the first floor.
2. That car has a two-up-demand (an assigned 2-up hall call).
3. That car has a command at four (a fourth floor car call is registered in that car).
4. The car's doors are fully open.
5. That car's logic and destination direction are up.
6. That car's M-G set is running.
7. That car is in group service.
8. The three-up-hall call push button is pushed.
9. No other calls are being allotted.

The system employs time division multiplexing to reduce the wiring whereby certain signals, particularly those associated with the floors, including hall call set and reset, demand set and reset, car call set and reset, command set and reset, car position, select memory set and reset, and many allotter functions, are activated selectively as scan position is coincident with the associated floor while scanning in a given direction. A two section master ring counter is represented in FIG. 4 with typical wave forms. Conveniently, the first section MRC1 issues positional signals for its scan which correspond to floors scanned. Units having 30 scan positions have been employed, although it should be understood that it is only necessary to have a scan position for each floor. The wave forms opposite the ring counter scan position terminals "R.C at 1" through "R.C at 30" are fragmentarily illustrated for typical terminals MRC1-22, MRC1-53, MRC1-52, MRC1-34, MRC1-31 and MRC1-30. The second section of the master ring counter MRC2 issues read signals at MRC2-34 for multiplexing and defining the window in which service evaluation pulses can be admitted to each car's master binary counter 54. Signals at MRC2-41 are master inhibit controls to segregate the per floor read signals. Scan direction is defined as "up" at MRC2-22 and "down" at MRC2-23. Only the first four positional signals from MRC1 will be considered in the detailed discussion which follows, although additional scans of positions five through 30 would occur using this master ring counter. FIG. 14 illustrates the four positions while FIG. 15 shows a typical read pulse on an expanded time scale and FIG. 16 shows the wave forms on a common time base assuming no scans beyond the fourth position.

Registration of the hall call sets the hall call and select memory as the first step in the allotting sequence. Depressing up hall call push button 51 of FIG. 5 makes PBBH-16+ and after a double inversion from the noise filter 61 and inverter 101 makes 101-2+ and 102-2+. NAND 102 sets the No. 3 up hall call memory in the third HCM of FIG. 6 when the ring counter is at floor 3 and its direction is up.

RING COUNTER DIRECTION UP signal makes PBBH-49+ to 103-1+ whereby the 103-2 from inverter 103 partially satisfies NOR 104 as 104-1-. When the ring counter reaches 3 in its upward scan, the RING COUNTER AT FLOOR 3 signal makes PBBH-51- and 104-2- to make 104-3+ thereby satisfying both inputs of NAND 102 to make 102-3-. Inverter 105 makes 105-2+ and PBBH-46+ to issue a 3 UP NORMAL HALL CALL PUSH BUTTON signal to make HCM-32+ for the third floor hall call memory (see FIG. 6).

Allotment takes place only if no car is at the floor since NAND 106 is inhibited if HCM-33- for a signal ANY CAR AT THE FLOOR. With HCM-33+, 106-1+ and 106-2+ from HCM-32+, 106 causes 106-3- so that NOR 107 is gated to make 107-3+. This assumes no RESET HALL CALL signal so an HCM-31+ is inverted to make 108-2- and 107-2- with 107-1-. Again, ring counter position and scan direction must correspond to the hall call floor and service direction to make HCM-13+ and HCM-14- whereby inverter 109 makes 109-2- to provide coincident negative inputs 110-1- and 110-2- to NOR 110 so that 110-3+ enables NAND 111 to issue a set signal to the flip-flop of cross coupled NANDS 112 and 113

as 111-3-. NANDS 112 and 113 form the 3 up hall call memory.

At this time NAND 114 is inhibited since there is no RESET HALL CALL signal and HCM-31+ through inverter 108 holds 114-1- with 114-2+ to make 114-3+.

The several cross coupled NAND flip flops shown have their set and reset leads respectively labeled S and R. They are set and reset by negative signals on their respective leads. Initially, as when power is applied, the flip flops are biased to the reset condition whereby the NAND of the reset lead has at least one negative input and the NAND of the set lead has both inputs positive. Thus in the 3 up hall call memory 113-3+ applies 112-2+ while 112-1+ is present to cause 112-3- to latch 113-3+. In this condition, the signal at 113-2 has no effect.

When 111-3- is developed, it makes 112-1- to set the memory by 112-3+ making 113-1+ and 113-3-. This latches the set condition of the flip flop until NAND 114 makes 114-3- and 113-2- for reset. This will occur when a RESET HALL CALL signal, HCM-31-, a RING COUNTER DIRECTION UP signal, HCM-13+, and a RING COUNTER AT FLOOR 3 signal, HCM-14-, are coincident.

A hall call memory is provided for each hall call which can be registered. Therefore, while the allotment is made very rapidly and usually essentially instantaneously following operation of a hall call if simultaneous hall call registration occurred or if other hall calls were registered while a hall call was being allotted, the hall memories for those other hall calls would be set as the master ring counter scanned the system. As a result, a plurality of unassigned hall calls can have their hall call memories set. Further, the hall call memories remain set until their call has been served. This retention of the set hall call memory enables the release of the hall call button without its loss and its reallotment where a more optimum assignment can be made as where service burden on the several cars changes.

The next step in the allotting function is to select a hall call for allotment. This is random because it depends on the master ring counter direction and position at the time the selection is made. The third up select memory comprising flip flop connected NANDS 115 and 116 is set, assuming no other call is to be allotted and the 3 up hall call was not already a demand, when the 3 up hall call memory is set and ring counter floor and direction are coincident with the memory. Only one hall call is subject to allotment at a time, hence only one select memory can be set at a time. Ring counter coincidence makes 110-3+ to NAND 117 at 117-1+. The 3 up hall call memory makes 117-2+. Since there is no DEMAND IN ANY CAR signal for the third floor up call, HCM-24+ through inverter 118 makes 119-1- of NOR 119, and since there is no CALL HAS BEEN SELECTED FOR ALLOTMENT signal, HCM-25+ makes 119-2- through inverter 120, thereby making 119-3+ and 117-3+ so that 117-4- is a set signal as 116-2- for the third up select memory.

At this juncture, inverter 121 issues an HCM-3- for a 3 UP HALL CALL ON signal. NAND 122 issues through the double inverter 123 and 124 HALL CALL MEMORY ON as HCM-5- since 122-1+ from the memory and 122-2+ from master ring counter to hall call memory incidence gate 110 are coincident.

A CALL HAS BEEN SELECTED FOR ALLOTMENT signal appears as HCM-8- since 115-4- makes 128-4+ of NAND 128 and by inverter 129 makes 129-2-. The signal RING COUNTER IS AT ALLOTMENT FLOOR, HCM-7-, is not present at this time since it is issued only when the first half scan is complete and the counter opposes the direction of the set select memory. NAND 125 is inhibited since the three down select memory is not set and 125-1- controls while its counterpart 126 is inhibited since the ring counter direction is up and HCM-15- controls.

HALL CALL MEMORY ON as AGC-31+ (FIG. 7) is provided by inverter 127 from HCM-5- to AGC-30-.

It will be noted that certain logic element terminals are shown without input circuits as 125-1, 128-1 and 128-3. Such signals do not enter directly into the logic being discussed. Thus, it should be assumed that the signals on the unconnected leads are of a nature to enable the described function.

The allotment or assignment of a hall call to a particular car depends upon the service requirements of that car, which is represented by the count held in its master binary counter 54. These service requirements are continuously changing for all cars as changes occur in such factors as their position, door operation, calls imposed and load. Consequently, the master binary counter of each car must be reset to zero before each allotment. This reset is by an ALLOTTER MAIN RESET signal as AGC-17+ from the allotter gating control AGC of FIG. 6 which is maintained from the coincidence of the master ring counter and scan direction with the floor and direction of the allotment call (the call for which the select memory is set) until the ring counter is at the allotment floor and set in the opposite direction to the call.

Following the main reset, the master ring counter scans from coincidence of floor and direction with the allotment call to coincidence of floor of and an opposed direction to the allotment call at which point the allotter read signals are initiated. Initially, prior to the advance of scan to the floor and direction of the allotment call and the set of the select memory NOR 133 (FIG. 7) is inhibited by 133-1+ and 133-2- so that NAND 134 is inhibited by 134-1- and 134-2+. AGC-9+ from HCM-7+, as described, applied to NAND 138 holds 138-1+ through inverters 136 and 137 so that 138 stands gated with 138-3-.

Upon selection of the call for allotment, HCM-8- makes AGC-45- and through inverters 131 and 132 makes 133-1- to gate 133. With 133-3+ and 134-3+, NAND 135 is gated to make 135-3- whereby inverter 139 issues an ALLOTTER MAIN RESET signal as AGC-17+. At this time, inverters 131 and 132 also make AGC-41- for a CALL HAS BEEN SELECTED FOR ALLOTMENT signal.

The select memory for each floor and service direction and the time multiplexing features enable the master ring counter to perform an allotting scan function after its call finding scan function thereby eliminating the need for separate scanners.

ALLOTTER MAIN RESET signal as AGC-17+ and thereby SRCN2-50+ and CAS3-42+ resets the selecting ring counter 59 on SRCN2, FIG. 12, resets the master binary counter 54 of each car on its CAS3, FIG. 11, resets the binary preset counter 56 of each car on its CAS3, FIG. 11, and through inverter 139 on CAS3 to

CAS3-41- and thus CAS1-20- resets the car located memory 62 shown at the top of FIG. 8, and resets the reject memory 311 of FIG. 11.

The ALLOTTER MAIN RESET signal persists following selection of a call for allotment until the master ring counter reverses and is again coincident with the floor of the set select memory. This is indicated by gating NAND 126 for a three up select memory NAND 125 for a three down select memory. In the example, the set three up select memory imposes 126-1+ so that when the master ring counter returns to the third floor to make HCM-14- and its direction is down to make HCM-15+, NOR 142 will be gated to make 126-2+ and gate NAND 126. Inverter 143 inverts HCM-15+ to impose a 142-2- signal gating NOR 142. NAND 126 issues a 126-3- which is inverted twice by inverters 144 and 145 issue a RING COUNTER IS AT ALLOTMENT FLOOR signal as HCM-7-.

Termination of the ALLOTTER MAIN RESET signal occurs immediately prior to the advance of the master ring counter to the allotment floor while scanning in a direction opposite the service direction of the allotment call by application of HCM-7- as AGC -9- to the allotter gating control. Inverters 136 and 137 impose a 138-1- to inhibit NAND 138 causing it to issue 138-3+ to 134-2+ so that NAND 134 is gated to issue 134-3- to inhibit NAND 135. AGC-17- is generated by inverter 139 when 135-3+ issues to terminate the ALLOTTER MAIN RESET signal.

Allotter read pulses issue as the master ring counter advances from the allotment call floor in a direction opposite the service direction of the allotment floor until completion of a scan, as by a scan downward, upward and back down to the allotment floor, in the example. ALLOTTER READ pulse signals are issued as AGC-47+.

As shown in FIG. 16 four signals are issued from the master ring counter for counter scan direction, scan read and scan inhibit as labeled MASTER READ (6.7 KHZ) issuing from MRC2-34 as to AGC-8 of FIG. 6, MASTER INHIBIT as the inverse of MASTER READ, RING COUNTER DIRECTION IS UP from MRC2-23 as applied at HCM-13 of FIG. 6 and AGC-54 of FIG. 7, and RING COUNTER DIRECTION IS DOWN from MRC2-23 as applied at HCM-15 and AGC-35. A second portion of the master ring counter, MCR1, issues floor scan position signals. In the example, only four floor scan positions are illustrated as negative going pulses as RING COUNTER AT FLOOR 3 from MRC1-52 to HCM-14 of FIG. 6 with the first floor signals issued from MRC1-27, second floor from MRC1-53 and fourth floor issued from MRC1-49. The signal patterns indicate a scan between the first and fourth floors with the effective interval of the scan signal established by the MASTER READ. The logic sequence outlined above results in the 3 UP HALL CALL MEMORY signal shown until that call is answered and the memory reset (not shown) and a 3 UP SELECT MEMORY from the setting of the hall call memory until the call is allotted a car as a 3 up demand.

The scan in FIG. 16 is represented as in FIG. 14 beginning with the first floor in the up direction as an arbitrarily selected start. The hall call memory set HCM, select memory set SM, and allotter main reset AMR are all actuated on the up scan of the third floor. Allotter main reset is terminated and allotter scan AR is initiated on the down scan of the third floor.

Each occurrence of coincidence of the master ring counter scan with the allotment floor causes a pulse to issue as RING COUNTER IS AT ALLOTMENT FLOOR at HCM-7 when the scan direction opposes call service direction and RING COUNTER IS COINCIDENT WITH ALLOTMENT FLOOR as at HCM-6.

ALLOTTER MAIN RESET as from AGC-17 persists from the initial RING COUNTER IS COINCIDENT WITH ALLOTMENT FLOOR to the initial RING COUNTER IS AT ALLOTMENT FLOOR following the setting of the select memory. Upon termination of the reset, ALLOTTER READ signals issue as a pulse train at AGC-47 until the SCAN COMPLETE signal issues at AGC-22.

Thereafter, the static car service factors are imposed and, upon their completion, an ALL CARS BIASING COMPLETE signal is issued at 301-9 of FIG. 12 the select ring counter 59 functions through its decoder 60 to provide a signal SELECT RING COUNTER STEP 13 on lead 306 and the car assigning pulse issues as CAR "X" IS ASSIGNED THE CALL at SRCN2-19.

The remaining wave forms enter into the evaluation of the exemplary car's service capability during the allotter read including the CAR IS LOCATED signal from the car located memory of CAS1 FIG. 8 to segregate inside from outside demands and commands and to indicate the car distance from the allotment call. For example, a demand for a floor scanned before the car is located is signified by the signal INSIDE DEMAND COINCIDENCE while a command scanned after the car is located is signified by the signal OUTSIDE COMMAND COINCIDENCE. Each floor scanned between the initiation of ALLOTTER READ signals and the initiation of the CAR IS LOCATED signal is counted as DISTANCE provided the car is required to traverse that floor in serving the calls imposed upon it.

The logic of the allotter read sequence will be considered next with reference to the allotter gating control AGC of FIG. 7. As the signal AGC-9- terminates the ALLOTTER MAIN RESET, it also enables the ALLOTTER READ. 138-3+ from inhibited NAND 138 enables NAND 134 to issue at 134-3- which is inverted at 146 to supply NAND 147 a 147-2+. Assume 147-3+, then 147-4- depends on the read pulse being present from the master ring counter at AGC-8+ as shown in the time sequence drawing FIG. 16. Gating action in AGC through 147 corresponds directly with the master ring counter read pulses from the coincidence of scan in the direction opposite the call until a scan is completed by return to the allotment floor in a scan direction opposite the call direction. Pulses at 147-4 are inverted by 148 to issue as ALLOTTER READ at AGC-47+.

A distance count is established as a pulse series for each floor scanned from the allotment call floor to the floor at which the car is located and these pulse series are accumulated in the master binary counter 54 of each car. As shown in FIG. 15, representing on a much expanded time scale an allotter read pulse for a floor between the allotment call and the car, the car allotter sections CAS1 and CAS3 sequence the gating of a distance pulse series to the master binary counter 54 during a terminal portion of each allotter read interval and following the counting of any inside command or demand for the car for the floor of the scan. Since no command or demand is imposed for floor three, the demand and command logic circuitry is skipped by the

sequencing means and the distance count is applied to master binary counter.

READ pulses from the master ring counter 53 are applied from MRC2-34 to AGC-8 as AGC-8+ to establish a read pulse interval for each floor scanned at appropriate times through NAND 147. A failure to assign a car to an allotment call results in issuance of an artificial indication of assignment in order to reset the select memory and permit allotment of other hall calls. 10 ALLOT A DIFFERENT CALL provides this indication from SRCN2-40 (not shown) to AGC-15 as a (+initiated when the master ring counter position and direction are coincident with the call of the set select memory and cancelled when the select memory is reset by a DEMAND IN ANY CAR as AGC-3-. An AGC-15+ failure signal is latched by NORs 151 and 152 and the latch is released by AGC-8- during the inhibit READ interval. AGC-8+ by inverter 149 makes 150-2- and 150-3+ if 150-1- is present due to an AGC-15+ making 151-2+ and 151-3-. This makes 369-2- and 369-3+ to issue AGC-3-. When the select memory is reset, AGC-15- and AGC-8- release the latch since 150-3- makes 151-1- and 151-3+ to hold 150-3-. The DEMAND IN ANY CAR will be discussed with the termination of allotment. The gating of a count pulse series will be discussed generally.

Each of the service requirement factors are introduced into the master binary counter of the car upon which it is imposed by enabling a counting NAND gate exemplified by 163 FIG. 8 for a demand, 171 for a command and 181 for distance in CAS1. The counting NAND can be gated as its sequence is effective only if the service requirement is imposed. When gated, a preset NAND is enabled and an advance from preset NAND is inhibited. Preset NANDs are exemplified for demands by 161, for commands by 176, and for distance by 187, while advance from preset NAND is exemplified by 160 for demands, 173 for commands and 186 for distance.

The preset for a service requirement enables a binary preset counter 56 to receive counts from astable 55 (FIG. 11) and to apply signals from its outputs as they are accumulated therein to selector switches (FIG. 10) which link selected ones of the outputs to inputs of count NANDs (FIG. 8). The selector switches also supply permanent enabling signals selectively to inputs of the count NANDs so that a combination of the permanent signals and the binary preset counter outputs signals can satisfy the count NAND to cause it to inhibit the counting NAND and thereby inhibit the preset NAND while enabling the advance from preset NAND. Count NANDs are exemplified for demands by 201 and 204, for commands by 202 and 205 and for distance by 183.

Binary preset counter 56 employs six stages and has a capacity count of 64 so that any count of one to 64 can be issued by combinations of signals to its output leads and thence through the switches typified by those of FIG. 10 to the count NANDs. It counts to the binary preset counter capacity count complement for which the selector switch linking means to the count gate is set and then causes the balance of its capacity count to be inserted in the master binary counter by gating its master count NAND gate as typified by 169 for demands, 179 for commands and 206 for distance. When the binary preset counter attains its capacity count, it stops counting and actuates a counting completed

NAND to advance to the next sequence while inhibiting the master count NAND. Counting completed NANDs are typified by 166 for demands, 187 for commands and 212 for distance.

Two signals are issued from the CAS1 and CAS2 circuits to the CAS3 circuit. A PRESET BINARY COUNTER signal from CAS1-31 and CAS2-42 issued when a preset NAND is gated is applied to CAS3-50 as a (-) to inhibit NAND 193 and impose a 191-1+ as an enabling signal. With NAND 191 enabled, astable 55 applies pulses from CAS3-48 to CAS3-49 through inverter 190 as 191-2+ whereby 191-3- pulses advance binary preset counter 56 and impose 192-2- enabling pulses on NOR 192. The circuit is latched as binary preset counter advanced from zero to issue a 194-4+ inverted at 195 to inhibit 193 and latch 191-1+. Pulses are therefore passed from 191 until binary preset returns to zero on its capacity filling 64th count and makes 194-4- to enable 193 thereby inhibiting 191.

When a preset NAND of CAS1 or CAS2 is inhibited by the filling of its count NAND and the inhibiting of its counting NAND, its master count NAND issues a COUNT MASTER BINARY COUNTER as a (-) at CAS1-30 or CAS2-41 to CAS3-39. This inhibits NAND 158 by a 158-2- causing it to issue a 158-3+. Inverter 159 applies this as a 192-1- to gate NOR 192 each time a pulse from astable 55 makes 192-2- whereby the master binary counter count is advanced by the resultant 192-3+ pulses.

ALLOTTER READ as a CAS1-14+ input skips through the demand circuitry for the third down scan in the absence of a third down demand by gating advance from preset NAND 160 while preset demands NAND 161 is inhibited. NANDs 160 and 161 each derive an input from the car memory CM for the scan floor as CAS1-8- when there is ALLOTTER DEMAND COINCIDENCE. It is assumed no demand is at three, therefore CAS1-8+ inverted by 162 (FIG. 7) to terminal 163-1- of counting NAND 163 causes 163-5+ to impose, through inverter 164, an inhibiting 161-1- on preset NAND 161 and to impose directly an enabling 160-2+ on advance from preset NAND 160. Inhibited NAND 161 inhibits the preset counter by its 161-3+ signal making CAS1-31+. The resultant 160-3- imposes an inhibiting seal at 163-4- and through inverter 165 is passed on to the command circuitry by gating NAND 166 which causes inverter 167 to issue at 167-2+ a COUNTING DEMANDS COMPLETE to the inside command circuitry.

As previously discussed, the master binary counter 54 of each car is controlled by a binary preset counter 56 having a full count cycle of 64. The preset counter selectively controls the gating of the weighting or biasing applied to the several service burden factors considered so that the 64 count complement of the bias setting is admitted to the master binary counter. For example, if it is desired to treat a floor distance count as a count of six, its preset control is effective to pass counts zero through 58 into the preset counter, thereafter pass counts 59 through 64 into the master binary counter and return the preset counter to its starting count or zero. If no count is made when the service burden factor consideration is complete, the factor can be skipped.

In the assumed no demand condition a PRESET COUNTER AT ZERO signal is present as CAS1-32-

to cause latching NAND 168 to issue a 168-3+ thereby gating counting demands complete NAND 166 with a 166-2+ coincident with 166-1+. The 166-3- makes 169-2- so that 169-3+ inhibits the COUNT MASTER BINARY COUNTER as a CAS1-30+. It also provides a seal at 168-2- and causes inverter 167 to have 167-2+ to skip the demand count sequence and consider if a command count should proceed.

A command count is admitted when scan direction opposes car travel. NAND 152 is gated by a coincidence of UP CAR TO ALLOTTER, as CAS1-26+, and RING COUNTER DIRECTION IS DOWN, as CAS1-27+. NAND 153 is gated by a coincidence of DOWN CAR TO ALLOTTER as CAS1-23+, and RING COUNTER DIRECTION IS UP, as CAS1-24+. When either 152 or 153 is gated a (-) signal on one of the inputs to NAND 170 indicates the car travel opposes the scan, as signified by a 170-3+ as a first enabling signal to NAND 171 as 171-1+. This condition is satisfied. However, it was assumed there was no command at three hence CAS1-33+ indicates an absence of ALLOTTER COMMAND COINCIDENCE which by inverter 172 applies its 172-2- signal as 171-2- to hold 171-8+ and inhibit any command count. This inhibit is coupled with a skip through of command count as in the case of demand count for floor three.

The 167-2+ signal from the demand count circuits in coincidence with the 171-8+ from the command count gate gates NAND 173 to issue a 173-3- latch signal as 171-7- and enables the second sequence phase including the gates for COUNT MASTER BINARY COUNTER through the inverter 174 to NAND 177 and NAND 179 to impose a CAS1-30+ signal. PRESET BINARY COUNTER is inhibit as CAS1-31+ at this time since 171-8+ is inverted at 175 to cause NAND 176 to issue a 176-3+. Since a zero count is maintained NAND 178 gates 177 to inhibit 179 and the COUNT MASTER BINARY COUNTER signal.

Distance count is enabled with the command count inhibit for the master binary counter since NAND 177 is gated to issue 177-3- and thereby latch the passing of command counts by NAND 178, cause NAND 179 to hold CAS1-30+ and thereby inhibit COUNT MASTER BINARY COUNTER and enable the distance count through issuance of a positive COUNTING COMMANDS COMPLETE signal from inverter 180.

As in the case of gate 163 for demand counts and 171 for command counts, gate 181 issues a negative signal to admit counts into the preset binary counter as a prerequisite to admitting the complement of a 64 count to the master binary counter. The prerequisites are: the car has not been located so that inverter 182 from the car located memory 62 makes 181-1+, the preset count has not been achieved so that NAND 183 is not gated and, therefore, issues a 183-8+, the car top and bottom travel limits have not been exceeded, so that NAND 184 and 185 respectively issue a 184-3+ and a 185-3+, and count completed NAND 186 is not issuing a 186-3- as a seal for 181.

Upon completion of the counting of command pulses 183-1+, 186-1+ and 187-2+ signal are imposed. At this time, a coincidence of positive inputs on 181 causes it to have 181-6- whereby NAND 186 is inhibited by 186-2- and inverter 188 makes 187-1+ to cause NAND 187 to issue a 187-3- and thus a PRESET BINARY COUNTER, as CAS1-31-. Thus, the presence of an inside demand coincidence gates

NAND 161, the presence of an inside command coincidence gates NAND 176 and the presence of a distance count gates NAND 187 each to enable the preset binary counter to count and establish the complement of 64 to be admitted to the master binary counter. This enables a count by imposing a CAS3-50- in the third car allotter section CAS3 of FIG. 11.

The pulses to be counted are generated by a 3 megacycle astable 55 and issue from CAS3-48 to CAS3-49 and inverter 190 from which they are gated by NAND 191 to binary preset counter 56 and, selectively for the capacity count complement of the bias count in the binary preset counter through NAND 192, to master binary counter 54. Gate 191 passes pulses only when 191-1+ and thus only when one input to NAND 193 is minus. Initially, binary preset counter is at zero so that 194-4- of NAND 194 is inverted at 195 to impose 193-2+. When CAS1-31- makes CAS3-50-, 193 makes 193-3+ so that each negative pulse from astable 55 causes a 191-3- pulse to advance binary preset counter 56 one count.

A six stage binary counter will provide a 64 count cycle on six outputs representing counts of one, two, four, eight, 16 and 32 respectively at CAS3-7+, CAS3-8+, CAS3-5+, CAS3-6+, CAS3-16+ and CAS3-9+. A check for zero which indicates no other count output is made by the NANDing of NORS 196, for neither of counts one or two, 197 for neither of counts four or eight, and 198 for neither of counts 16 or 32, all to NAND 194 to issue PRESET COUNTER AT ZERO as CAS3-4-.

Each car has a binary preset counter output which is employed in establishing the several bias levels which are selectively connected in its service requirement evaluation means of this invention. The preset or bias counts are effective until a count is established which imposes coincidence on the count NAND associated with the service factor present and currently effective in the allotter read sequence as NANDs 201, 202 and 183 for inside demands, inside commands and distance and after the scan has located the car, NANDs 204 and 205 for outside demands and outside commands respectively. Each of these gated NANDs inhibit either directly or through other logic the NANDs which control the passing of pulses from 55 to preset counter as 161, 176 and 187 respectively for demands, commands and distance and enable the NANDs which control the admission of the complement of the preset count into the master binary counter for the car as NANDs 169, 179 and 206 respectively for demands, commands and distance.

Gating of the bias count NANDs 201, 202, 204, 205 and 183 is controlled from selected output connections from the preset binary counter, so that upon the preset binary counter 56 achieving the selected count all inputs to the NAND under consideration are satisfied and it is gated to transfer the balance of the count of 64 to the master binary counter 54 for the car.

Such connections are established through multi-decked selector switches 207 and 208 as represented for inside demands and distance in FIG. 10 and are passed through those switch decks to the individual inputs of the service factor count NANDs. Thus for all counts involving an odd number CAS3-7+ will be imposed. Where two is a portion of the count CAS3-8+ will be imposed and so forth.

A five deck inside demand bias switch 207 and a six deck distance bias switch 208 are illustrated to respectively provide links from the preset counter outputs for counts of two, four, eight, 16 and 32 respectively as decks E, D, C, B and A from switch panel terminals SP1-9, SP1-12, SP1-16, SP1-18 and SP1-20 respectively and for a count of one for deck F as 208 F from SP1-6. These links are coupled to the count NANDs 201 and 183 respectively through switch panel output terminals coupled to suitable switch wipers. Both switches are illustrated in the second position with their wipers in that position so that in the case of a distance bias one count is entered into the car's master binary counter since the bias setting is for a count of 63 and the 64th count terminates the admission of additional counts through NAND 191 (FIG. 11). Assume the wipers were moved to the fourth position for distance bias switch 208. Wiper 208 EW would be engaged with a contact coupled to the continuous positive bias on SP1-1 and lead 209 (FIG. 10) thereby eliminating a two count from distance bias by imposing a positive signal through SP1-5- to CAS1-44 and 183-6 (FIG. 7). In this condition 183 would be gated when counter 56 reached a count of 61 and a count of three would be applied to master binary counter 54. This will be appreciated by considering the inputs to NAND 183 which will have positive coincidence when a count of one at CAS1-45, four at CAS1-43, eight at CAS1-42, 16 at CAS1-41 and 32 at CAS1-40, the constant positive at CAS1-44 and an enabling counting commands complete signal as 183-1+.

A count of three is admitted to the master binary counter 54 of the car by inhibiting NAND 181 at the 61 count of preset counter 56. 183-8- causes NAND 181 to be inhibited and issue 181-6+ to inverter 188 and 187-1- so that 187-3+ removes the PRESET BINARY COUNTER signal and makes CAS1-31+. At this time 186-3- occurs by coincidence of 186-1+ and 186-2+. This makes 206-1+ through inverter 211 and since 206-2+ from 212-3+, NAND 206 issues 206-3- to establish the signal COUNT MASTER BINARY COUNTER or CAS1-30-.

If a demand count has been entered for an allotter read interval, the command count is skipped even if a command is registered since the service burden of or delay imposed by the demand will not be appreciably increased by the command. However, if no demand is present for the floor, the demand count is skipped since coincidence gate 163 would be inhibited and the gating of demand counting completed gate 166 would enable the command counting controls. If a command is present, the gate 176 is gated to institute the count cycle, if no command is present, the gate 173 is gated and when this occurs, with the preset counter count at zero, the read sequence advances to the next factor, a distance count.

Distance count is sequenced in the same manner as demand and command counts. If the car located memory has not yet been set, then the terminal portion of each allotter read interval is available for a distance count provided the car is required to transverse the floor of the allotter read interval in serving the calls currently imposed upon it or in serving the allotment call.

The second allotter read pulse in the illustration is for floor two scanning downward. An up demand is assumed for the car under consideration. Consequently,

during this read interval an inside demand count followed by a distance count will be imposed on the car's master binary counter 54.

A demand is stored in a memory such as shown in the typical car memory CM of FIG. 13 A. A car memory CM is provided for each car and each floor except the terminal floors wherein a single car memory is provided for each car. Each car memory includes an up demand memory, a down demand memory (not shown) and a command memory (not shown) together with circuits for relating the relative locations of the memories to the car position, the ring counter scan position relative to the floor, and the top and bottom distance limits. For illustrative purposes, only the up demand memory is shown. Down demand memory functions as an up demand memory. While command memory enters into the service demand aspect of allotment, it is not an allotted call, hence it also was deleted from this disclosure. The illustrated car memory is for the allotment floor of the example and is typical in logic functions to the car memory for floor two. It will be discussed as a floor two memory in the consideration of the allotting treatment of a second up demand.

Assume the No. 2 up demand memory is set so that NAND 220 issues 220-3+ to enable NAND 221 with 221-2+. Since the ring counter is at the floor, a RING COUNTER AT FLOOR 2 signal makes CM-25- and through inverter 222 applies 223-2+ to NAND 223 and since the direction of scan causes a RING COUNTER DIRECTION DOWN signal to be present as CM-22+ and 223-1+ so that NAND 223 is gated to issue 223-2-. Inverter 224 applies that signal as 221-1+ to gate NAND 221 to 221-3- providing an ALLOTTER UP DEMAND COINCIDENCE signal as CM-40-, and CAS1-8-.

Coincidence of a demand institutes an inside demand count in FIG. 8. Inverter 162 enables demand counting gate, NAND 163 since CAS1-8- is applied as 163-1+ and initially all other inputs to NAND 163 are positive. NAND 160 is therefore inhibited by 160-2- while inverter 164 gates NAND 161 with a 161-1+ coincident with the ALLOTTER READ signal CAS1-14+ applied as 161-2+. This applies an enabling signal to the controls for the preset binary counter 56 as PRESET BINARY COUNTER, CAS1-31-. The demand count is thus entered into the master binary counter 54 as the preset counter capacity count complement of the selected count established by inside demand switch 207 in the same manner as described for distance count.

NAND 201 is gated for the illustrated second position of inside demand bias switch 207 when counter 56 has a count of 46 whereby a count of 18 is admitted to the car's master binary counter 54. This 46 count is composed of the coincidence on NAND 201 of a 32 count signal from CAS3-9+9+ to SP1-20+ to 207 AW to SP1-38+ to CAS1-9+ and 201-1+, a constant positive signal from bus 209 to 207 BW SP1-37+ resulting in a 201-2+, an eight count through 207 CW resulting in a 201-3+, a four count through 207 DW resulting in a 201-4+ and a two count through 207 EW resulting in a 201-5+. Since the car located memory has not been set, 201-6+ enables the gate and the ALLOTTER READ signal, a 201-7+, also enables it so it is gated by the count. With 201-8-, demand counting gate 163 is inhibited by 163-2- making 163-5+ so that inverter 164 applies 161-1- to inhibit gate 161 and remove PRESET BINARY COUNTER signal CAS1-31- while

160-2+ enables NAND 169 to issue a COUNT MASTER BINARY COUNTER as a CAS1-30-.

In the normal sequence, the demand coincidence inhibits the command count sequence by 171-3- from CAS1-8- and directly institutes the distance count sequence by a counting command complete signal as 177-3- to the distance count sequence control.

Distance count for floor two is entered into the car's master binary counter in the same manner it was entered for floor three. The master ring counter, thereafter terminates the allotter read for floor two and institutes an allotter read for floor one.

Floor one is interrogated by allotter read pulse three. Again, consider the typical car memory of FIG. 13 as representative of the car memory for floor one. The output signal CAR AT FLOOR ONE will be present as CM-43-. Input signals RING COUNTER AT FLOOR ONE will exist as CM-25- and CAR AT FLOOR ONE as CM-26+ to gate NAND 225 by a coincidence of 225-1+ and 225-2+ and issue a 225-3-. CM-43- is inverted by a buffer (not shown) and imposed as CAS1-21+ and 230-1+ of NAND 230 in the car located memory 62. It has been assumed that the car is at the first floor, its logic direction is up and it, therefore, appears as an up car in the allotter functions by having a signal UP CAR TO ALLOTTER (by means not shown) as CAS1-26+ and 152-1+. RING COUNTER DIRECTION DOWN condition is indicated as CAS1-27+ to 152-2+ so that NAND 152 gates a 152-3- to NAND 170 so it issues a 170-3+ inverted by 233 to a 234-1- on NAND 234. Since the car under consideration has a call, it is not a free car and 234-1- results in 234-3+ so that 230 is gated to issue 230-3- to set the car located memory 62 at set input 235-1.

It is to be recognized that if the car appears as a DOWN CAR TO ALLOTTER imposing a CAS1-23, NAND 153 is gated when the ring counter is set RING COUNTER DIRECTION UP as CAS1-24+ and the car located memory is set when the car is at the allotter read floor to make CAS1-21+ and gate 230.

When the car located memory is set, distance counting is inhibited by 235-3+ to inverter 182 and 181-1- on the distance count gate 181, outside demand counting is enabled by 235-3+ to 204-3+ thereby enabling outside demand count gate 204, inside demand counting is inhibited by 237-3-, of the second NAND 237 of the car located memory, to 201-6- inhibiting inside demand count gate 201, outside command counts are enabled by 235-3+ as 205-7+, and inside command counts are inhibited by 237-3- as 202-7-.

Allotter read pulses four, five, six and seven for up scanning of floors one, two, three and four respectively add no counts to the master binary counter of the car since there are no outside demands to be counted and outside commands as inside commands are counted only when the scan direction opposes the car direction.

Allotter read pulse eight is a downward scan of the master ring counter for the fourth floor. RING COUNTER DIRECTION DOWN signal, CAS1-27+ and UP CAR TO ALLOTTER signal, CAS1-26+ are again coincident to gate NAND 152 thereby inhibiting NAND 170 to issue a 170-3+ signal to the command counting gate 171 and command count gates 202 and 205 at 171-1+, 202-1+ and 205-3+. This enables 171 for a command counting operation and outside command count gate 205. No demand is present for the fourth floor, hence, at the initiation of the allotter read

interval a counting demands complete signal issues as 166-3- to 176-2+.

The assumed command for floor four imposes an ALLOTTER COMMAND COINCIDENCE signal as CAS1-33- (by means not shown) to gate NAND 171 through inverter 172 whereby NAND 176 issues a 176-3- as a PRESET BINARY COUNTER signal. When the binary preset counter 56 satisfies NAND 205, gate 171 is inhibited to gate NAND 173 and inhibit NAND 176. The capacity count complement of the partial count in the binary preset counter 56 is thus admitted to the master binary counter by gating NAND 179 to produce a CAS1-30- COUNT MASTER BINARY COUNTER signal.

Since the distance counting logic is inhibited by the set car located memory 62, no distance count is made during the eighth allotter read pulse.

At the beginning of the ninth allotter read pulse with the allotter at floor three and scanning downward a signal RING COUNTER AT ALLOTMENT FLOOR issues as a signal HCM-7- from FIG. 6 to terminate the allotter read logic. HCM-14- makes 142-1- and HCM-15+ through inverter 143 makes 142-2- to make 142-3+. 142-3+ makes 126-2+ and the set 3 up select memory makes 126-1+ so that 126-3- through inverters 144 and 146 makes HCM-7-. HCM-7- at AGC-9- (FIG. 7) through inverters 136 and 137 makes 241-1-, 242-1- and 138-1-.

Three latches are utilized in the allotter gating control AGC to remember the succession of coincidence of the ring counter scan position with the allotment floor in the direction of scan opposite the service direction of the allotment floor as signified by AGC-9- for RING COUNTER AT ALLOTMENT FLOOR. These latches comprise NANDs 134 and 148 set to issue a 134-3- when AGC-9- first appears following the setting of the select memory identifying the allotment floor (at the next coincidence of scan with that floor), NORs 243 and 241 set to issue a 243-3+ when AGC-9+ first appears following the latch of 134-3-, and NANDs 244 and 242 set to issue a 244-3- when AGC-9- first appears following the latch of 242-3+. All of these latches are reset when the allotment is completed to reset the select memory of the allotment call and make AGC-45+ since 133-1+ makes 134-1- to make 134-3+ to make 243-3- thus and make 244-3+.

As described above, 134 was cocked by 134-1+ when the select memory was set. When next the ring counter scanned the allotment floor (as at floor 3 scanning downward in the first down scan of FIG. 14) AGC-9- made 138-1- to make 138-3+ thereby making 134-3- since 134-1 was (+). With 134-3-, the circuit is sealed by 138-2- holding 134-2+. At this time, AGC-9- has no effect on 243 since 241-1 and 241-2- hold 241-3+ and 243-2+. When the ring counter advances from the allotment floor and AGC-9 goes (+) (as at floor 2 scanning downward in the first down scan of FIG. 14), 241-1+ makes 241-3-. 243-2- with 243-1- makes 243-3+ to make 144-1+ and 241-2+. 241-2+ holds 241-3- by 243-2- coincident with 243-1-. At this time 242-1+ and 242-2+ hold 242-3-. The next time AGC-9- appears (as at floor 3 scanning downward in the second down scan of FIG. 14) 242-1- makes 242-3+ to make 244-2+ coincident with latched 244-1+ making 244-3-. 244-3- latches 243-2- to latch 242-3+. When the ring counter completes the allotter read signal and imposes AGC-9-,

244-3- inhibits the ALLOTTER READ by inhibiting NAND 147 with a 147-3-. 244-3- also issued through inverter 245 an ALLOTTER SCAN COMPLETE signal as AGC-22+.

The ALLOTTER SCAN COMPLETE signal is passed from AGC-22 to CAS2-21 (FIG. 9A) as CAS-2-21+ to initiate the generation of the static service requirement factors imposed upon the car as pulse trains added to the count accumulated in the master binary counter of the car during the per floor allotter read pulses.

Car status for the static service factors imposed on the car can be inserted as pulse series each scaled to the delay imposed by the factor represented in much the same manner as discussed above for the dynamic per floor factors or they can be inserted as a preset count into the reset master binary counter 54 prior to the per floor scan (by means not shown). Combinations of presets preceding the allotter read pulses and pulse counts either preceding or following the allotter read pulses can also be employed. For purposes of illustration, the car status factors will all be inserted as pulse series immediately following the allotter scan and read of the per floor factors. The static car status factors include the car stopping status as either in its slowdown phase as where it has initiated a stop, a door open phase where it is stopped, or an acceleration phase where it is starting from a stop. Only one stopping status is imposed on a car for any instant of allotment. A single stopping status pulse train of a relatively long length is applied for the long delay of a car in its deceleration mode, a relatively short length is applied for the brief delay of a car in its acceleration mode or an intermediate length is applied for a car with its doors open. If the car is running with no stop set, the sequencing control skips through the car stopping status count. A load factor can be inserted where the car is loaded to a predetermined level, for example a selectively short pulse group for a load of 20 percent of rated capacity or more up to 50 percent of rated capacity and a longer pulse group for a load of 50 percent of rated capacity or more up to some limit such as 80 percent of rated capacity at which loading the car accepts no further allotments. Additional factors can be for the delay in starting the car's motor-generator set or the corresponding transfer of its operating equipment to fully operational status where it is shutdown, and special assigned status for the car as the queue status each of which are represented by pulse groupings.

FIGS. 9A and B show that portion CAS2 of the car allotter section which controls the sequencing of the several static service factor pulse series. The logic sequences are similar to those discussed with respect to CAS1 and the allotter read intervals. When a factor is to be considered, its counting NAND gate is satisfied to issue a PRESET BINARY COUNTER signal from CAS2-42 to CAS3-50 until its count NAND gate is satisfied. When its count NAND gate is satisfied a COUNT MASTER BINARY COUNTER signal from CAS2-41 is passed to CAS3-39 so that the binary preset counter capacity count complement of the count which gated the count gate is introduced into the master binary counter of the car. Upon completion of the capacity count the logic of the next factor in the sequence is activated.

Counting NANDs 250 for car stopping status, 260 for car loading, 270 for car shutdown, and 280 for car

queue assignment control the sequencing. Stopping status count is controlled for a car in the slowdown mode by NAND 251, for a car in the door open mode by NAND 252, and for a car in the acceleration mode by NAND 253 each of which can inhibit 250. Load count is controlled by NAND 261 for a car which is 20 percent loaded and by NAND 262 for a car which is 50 percent loaded. A car shutdown count is controlled by NAND 271 and inhibited by NOR 272. Queue bias count is controlled by NAND 281.

Bias switches (not shown) of the type illustrated in FIG. 10 are employed to establish the appropriate number of pulses from preset counter 56 required to satisfy NAND count gates 251, 252, 253, 261, 262, 271 and 281. As in the dynamic factor logic, the complement of the binary preset counter capacity gating count is applied to the master binary counter 54 of the car. A first section of the logic establishes either a PRESET BINARY COUNTER signal or an advance logic signal and the second section establishes either a COUNT MASTER BINARY COUNTER signal or an advance logic signal signifying the counting of the factor is completed.

When the allotter completes scanning the floors for dynamic factors, an ALLOTTER SCAN COMPLETE signal appears as CAS2-21+ for each car to initiate car load consideration. If the car is loaded 20 percent of capacity, signals appear at CAS2-3+ for at least 20 percent load and CAS2-2+ for at least 50 percent load to respectively set flip flops 263 and 264. Inertia effects on load are avoided by inhibiting the setting of the flip flops while the car is moving by a signal CAR IS IN MOTION as CAS2-4+.

A 20 percent load satisfies NAND 260 through NOR 265 by imposing 265-1- to apply 265-3+ to 260-3+. 260-4- through inverter 166 imposes 167-1+ on load preset count NAND 267 while 267-2+ from CAS2-21+ is coincident to make 267-3- and issue PRESET BINARY COUNTER at CAS2-42- to CAS3-50. If the load is 20 percent and less than 50 percent, gate 261 is satisfied at the count for 20 percent. Since a 20 percent load imposes less delay than a 50 percent load, the pulse group for 20 percent is less than for 50 percent and therefor its complement pulse count is greater than for 50 percent. Accordingly, NAND 262 achieves its full count before NAND 261 and must be inhibited when less than 50 percent load is present by a signal from 50 percent load flip flop 264 as 262-6-. Conversely, when a 50 percent load is imposed, 262-6+ enables the earlier filling of the count for 262 to gate 262 before 261, and thereby control the inhibiting of 260 to admit the longer pulse series of the capacity complement controlled by 262 to the master binary counter.

When 260 is inhibited, the sequence is advanced to issue a COUNT MASTER BINARY COUNTER as CAS2-41- by gating NAND 268 to gate 269 while inhibiting 267 and latching NOR 265. The balance of the capacity count for binary preset counter 56 is applied to the master binary counter 54 and then CAS3-4- signifies PRESET COUNTER AT ZERO to gate the latch NAND 290 and issue from advance NAND 291 a counting load complete signal to the M-G bias logic as a 273-2+ on NAND 273, a 274-1+ on NAND 274 and a 271-1+.

If the car is conditioned for immediate operation, an M-G IS RUNNING signal CAS2-14+ gates NAND 270 by a 272-3+ to 270-2+ so that car shutdown preset ad-

vance NAND 274 issues 274-3- to advance the logic through NANDs 275 and 276 by a 275-1+ and 276-1+. The zero count gates NAND 277 to apply 276-2+ to issue a count M-G bias complete to the car queue bias at NANDs 282 and 283. Alternatively, an M-G count is applied for a shutdown car by gating 270, counting to fill 271, and then imposing an M-G bias count on the master binary counter.

When queue bias counting is complete, NAND 284 is gated by a zero count to issue 284-3- which is inverted by 285 to enable car stopping status logic at NANDs 254 and 255 by 254-2+ and 255-1+ and to enable each of the count gates 251 at 251-2+, 252 at 252-2+ and 253 at 253-2+. Car stopping status is counted only when the car is responding to a call pickup and either has a stop set or is stopped at the time the allotment occurs. If a stop is set and the car is, therefore, in its slowdown mode, slowdown count gate is enabled by a STOP IS SET signal, as CAS2-49-, (by means not shown). If the car is stopped, door open count gate 252 and car acceleration count gate 253 are enabled by a CAR IS STOPPED signal as CAS2-43+. These signals also enable counting NAND 250 since CAS2-49+ to NAND 256 makes 250-4+ and CAS2-43+ through inverter 257 and NAND 256 makes 250-4+.

A car committed to stop is delayed for a significant interval with respect to other calls. This interval is of such length that it is a material factor where car service capability is evaluated with the precision of the allotment evaluation under discussion. If the car is in its slowdown mode between the pickup of the call and its door open state (door open is usually indicated when the door is essentially full open as two inches from full open), the delay in its service to other calls may be up to several seconds longer than if it is in its door open mode or its acceleration mode since it may require a full deceleration interval of several floors of travel to bring the car to the door open position if the allotment is made as the car picks up a slowdown signal and it has been running at full speed. Similarly, a car in its door open mode when the allotment occurs will be delayed several seconds longer than a car which has started to close its doors and is in the acceleration mode. For these reasons, the lowest count to the master binary counter is for the least delay mode, car acceleration, while the door open mode is the next longest count and slowdown mode is the longest count.

First consider a car slowdown count. When a stop is set for a running car, CAS2-49- inhibits 253 with a 253-4- and when inverted by 258 enables 251 with a 251-1+. Since the DOOR IS OPEN signal at CAS2-55 is off at this time, CAS2-55- inhibits 252 at 252-6-. Counting NAND 250 is gated by 256-3+ from 256-1- to apply 250-6- through inverter 259 to gate NAND 254 and develop PRESET BINARY COUNTER signal as CAS2-42-. The count as set on the bias selector switches for car slowdown (not shown) satisfies 251 to inhibit 250 and gate advance NAND 255 so the complement count is admitted to master binary counter when NAND 292 is gated and COUNT MASTER BINARY COUNTER issues as CAS2-41-. At zero count, latching NAND 295 gates NAND 296 to inhibit 292 by 296-3+, and to seal 295, and through inverter 297, to issue BIASING COMPLETE TO CENTRAL SECTION as CAS2-45+.

If a car is in the door open mode when allotment occurs, NAND 252 is enabled by the CAR IS STOPPED signal CAS2-43+ and DOOR IS OPEN signal CAS-2-55+. Termination of the DOOR IS OPEN signal as a car receives a start signal (by means not shown) inhibits 252 by CAS2-55-. It also causes a CAS2-55- 5 inverted by inverter 298 to apply 253-1+ coincident with CAS2-43+ at 253-8+ for a car acceleration count thereby enabling 253. A start signal removes CAS-2-49- so that 253-4+ is imposed. When the car is conditioned to move, the capacity to impose an acceleration count is inhibited at NAND 253 and NAND 250 by a CAS2-43-.

A BIASING COMPLETE TO CENTRAL SECTION signal is issued as CAS2-45+ upon completion of entry 15 of any car stopping status count.

A BIASING COMPLETE TO CENTRAL SECTION as CAS2-45+ also is issued immediately after the queue bias counting complete signal from 284 where the car is in full operation since 250 is inhibited to skip the car stopping status by gating 255, advancing the logic to gate 296 since the count is zero.

The BIASING COMPLETE TO CENTRAL SECTION from each car is passed from the car's CAS2-45 to an appropriate input for the select ring counter no two car board SRCN2 (FIG. 12) as exemplified by a SRCN2-39+ for car No. 1. NAND 301 responds to a coincidence of BIASING COMPLETE signals from all cars as by direct inputs for cars one through seven and through resetting NAND 302 for car eight. Reset input 302-2 normally is (+) from decoder 60 so that an SRCN2-6+ for car eight gates a 302-3- which is inverted by 303 to 301-8+. When the bias for all cars are complete, NAND 301 is gated and 301-9- inverted by 304 starts astable 58 to run the select ring counter 59 35 and the binary to decimal decoder 60. The decoder block provides 14 separate signals for the comparison sequence.

As the pulses enter select ring counter through inverter 305, counts one through 12 from the decoder make simultaneous comparisons of all master binary counter counts starting with the most significant bit and proceeding with successively less significant bits to the last significant bit. As these comparisons proceed, cars will be encountered with bits registered indicating counts of at least a certain magnitude and thus service burden of a corresponding magnitude while other cars have a smaller service burden. Accordingly, the more heavily burdened cars, those with the higher counts can be eliminated from consideration in the allotment by setting reject memories in their respective car allotter sections CAS3 (FIG. 11). Assuming no car has achieved a master binary count of 2048, no 12th master binary counter bits will be (+) and none will be rejected. However, as the comparison proceeds in accordance with the decoder 60 advance by select ring counter position, some cars will have a (+) bit and their reject memories will be set. The setting of the reject memory for a car prevents the assignment of the hall call under allotment to that car. On the 13th count issued on lead 306 from the decoder 60 and select ring counter 59 the assignment of the allotment call is made. Count 14 on lead 307 stops the select ring counter by resetting or inhibiting NANDs 302 and 301. 65

Comparison of the several master ring counter twelfth bits is undertaken for a one count for select ring counter 59 by an SRCN2-49+ to CAS3-24+ to NAND

308 as 308-1+. Since it is assumed that no car has accumulated a count of 2048 in its master binary counter, the 12th bit output from 54 at lead 309 is (-) to impose 308-2+ coincident with 308-1+ and make 308-3+ gating NAND 310 by 310-1+. It is assumed 310-2+ since the car can answer this call and its Reject Memory 311 has not been set so 310-3+. 310-4- twice inverted at 312 and 313 issues a CAR DOES NOT WANT TO BE REJECTED as CAS3-43-. Reject memory setting 10 NAND 314 has 314-3- and issues a 314-4+ so the reject memory 311 cannot be set at this time.

In the assumed eight car system, a wired OR is provided coupling all car's CAS3-43 terminals so that when any one is (-) or grounded all appear to be grounded. Thus, where one or more cars have positive signals for setting their reject memories as 314-3+ and at least one other car has a negative signal 314-3- and CAS3-43- so that inverter 315 for all cars provides a 314-2+ signal, the cars with the 314-3+ signal will set their reject memories 311.

Consider that cars one through eight each have a count in their master binary counters 54 of at least 128 and less than 256. Each master binary counter will have a (-) for their 11th, 10th, and ninth bit outputs (not shown) and a (+) for their eight bit outputs to issue a CAS3-52-. As NANDs corresponding to 308 are enabled in succession for the second, third and fourth select ring counter counts, the sequence outlined for NAND 308 is followed and none of the reject memories are set.

On the fifth select ring counter step SRCN2-54+ is applied as CAS3-23+ to NAND 316 as 316-1+ for each car. It was assumed that each car had a count in excess of 128 in its master binary counter 54 so that its lead 317 is + to issue a CAS3-52- and impose a 316-2+. NAND 316 is gated by the coincident (+) inputs and issues 316-3- inhibiting NAND 310 by 310-1- to issue a 310-4+ on every car. Every car, therefore, has 314-3+ however, since all cars have CAS3-43+ by inverters 312 and 313, their inverters 315 impose a 314-2- to inhibit their reject memory set NANDs 314.

Next consider one car has its seventh bit for its master binary counter set and the remaining cars do not. The coincidence of the sixth select ring counter count as a (+) signal with the (+) from the seventh bit of the master binary counter for the one car will gate a signal to that car's NAND 310 as 310-1- in the manner described for NAND 316 while all other cars will have a 310-1+ on their NAND 310 in the manner described for NAND 308. As a result, the one car sets its reject memory and the other cars remain in the scanning sequence of the select ring counter.

NAND 310 for the one car issues a 310-4+ to 314-3+. Its signal is ineffective through inverters 312 and 313 since all other cars have made CAS3-43- by their 310-4- signals through their inverters 312 and 313. In this condition, the one car applies CAS3-43- through inverter 315 as 314-2+ to gate its NAND 314 and issue a 314-4- setting its reject memory 311 to issue a THIS CAR REJECTED at CAS3-40+. This eliminates this car from normal allotment of the hall call subject to allotment. Its control NAND 310 is inhibited by a 310-3- from reject memory 311 to avoid any effect on the reject sequences of other cars.

Assume next that in succeeding seventh through eleventh select ring counter steps all other cars but the

first and second are rejected by the above process of establishing coincidence of a select ring counter step with a master binary counter bit while other cars do not want to be rejected. Assume further that on the twelfth select ring counter step only cars one and two remain to be rejected and neither has the least significant bit on its master ring counter. The no two car feature of the SRCN2 circuit is effective to reject the higher numbered cars where a coincidence of two or more cars are simultaneously indicated as appropriate to receive assignment of the call.

The CAS3 circuitry of cars one and two each functions with SRCN2-51+ applied as CAS3-12+ to enable NAND 318 as 318-2-. Since neither master binary counter has a count of one and their leads 319 impose 318-1-, 310 is gated to issue 310-4- for both cars and both cars are not rejected since 314-3- inhibits the set of their reject memories 311.

During the elimination of those cars having higher counts in their master binary counters, the master ring counter MRC continues to scan the floors. As shown in FIG. 12, the car is assigned the call when the master ring counter advances to the allotment floor running in the call service direction. This occurs after the static service factor counts and the select ring counter operation to identify the one or more cars with the lowest count in their master ring counter. The signal RING COUNTER COINCIDENT WITH ALLOTMENT FLOOR actuates the CAR ASSIGNED CALL signal for the appropriate car in SRCN2.

Select ring counter 59 and decoder block 60 are arranged to insure coincidence of the RING COUNTER COINCIDENT WITH ALLOTMENT FLOOR signal SRCN2-3- and the 13th count from the decoder block 60. The select ring counter astable 58 is inhibited on the 13th count, then enabled when during the 13th count a CAR ASSIGNED CALL signal is issued, and terminated by a 14th count. The 13th select ring counter count as a (+) on lead 306 is inverted by inverter 339 to NOR 340 as 340-1-. At this time, first and second latches 341 and 342 are in a reset state so 340-2- enables a 340-3+ to NOR 343. A 343-2+ makes 343-3- to 302-2- inhibiting NAND 302 to inhibit astable 58 through inhibited NAND 301 and thereby holds the 13th count of select ring counter 59.

While the counter 59 is held at thirteen, one of the cars receives a CAR ASSIGNED CALL by virtue of a coincidence of the 13th count and RING COUNTER COINCIDENT WITH ALLOTMENT FLOOR as SRCN2-3-, and the absence of a CAR REJECTED signal from its reject memory. This assignment signal inhibits NAND 344 by imposing a (-) input as, for car No. 1, 344-1- while all other inputs are (+). 344-9+ establishes the first seal 341 as 345-1+ to NOR 345 at a time while 345-2+ enabled the NOR to issue 345-3- which is inverted at 346 to hold 345-2+. 346-2- is also applied as 347-1+ to NAND 347. Thus latch 341 remembers that the CAR ASSIGNED CALL pulse came on.

As is more fully disclosed in the copending application entitled "Multiple Digital Comparator", the assignment of a call to a car cancels allotment floor identification to make SRCN2-3+ and after a short delay resets latches 341 and 342 (by means not shown). When 344-1 goes (+) it issues 344-9- to NAND 348 making 348-1- and 348-3+. Coincidence of 347-1+ and 347-2+ makes 347-3- thereby sealing 348 with

348-2-. This latch 342 remembers the completion of assignment. It applies 347-3- to inverter 349 applying 340-2+ coincident with 340-1+ representing the 13 count of the select ring counter 59. 340-3- gates NOR 343 passing 343-3+ to NAND 302 so that the astable 58 pulses the select ring counter 59 to a 14 count.

The 14 count on lead 307 from 60 to 343 as 343-1+ inhibits NOR 343. This issues a 343-3- to NAND 302 to again inhibit it and the astable 58.

The car selection occurs when the RING COUNTER COINCIDENT WITH ALLOTMENT FLOOR signal is present. As shown in FIG. 6, HCM-13+, HCM-14- make 110-1- and 110-2- so that 110-3+ and 321-1+ for NAND 321. The No. 3 up select memory remains set so 116-3+ imposes 321-2+ to make 321-3- and, through inverters 322 and 323, HCM-6- signifying RING COUNTER COINCIDENT WITH ALLOTMENT FLOOR. This makes SRCN2-3- (FIG. 12), 325-3- of NOR 325 in FIG. 12 and when the select ring counter reaches a count of 13 lead 306 is (+) to inverter 326 which applies 325-1- to gate NOR 325 and make 325-3+. For the moment, assume that the reject memory of car 1 was set while that of car 2 was not set so that CAS3-40+ for car 1 at SRCN2-4+ while 2-CAS3-40- for car 2 at SRCN2-30-. Inverter 327 imposes SRCN2-4+ as 328-2- on the NAND 328 having 328-1+ to issue 328-3+. If the No. 1 and No. 3 inputs are (+) to NANDs 329 and 330, 329 will be gated to issue a 329-4- and CAR No. 1 ASSIGNED CALL (not) as SRCN2-19-. In the case of car No. 2 however, selection order NAND 331 is enabled by interlocking circuit applying CAR No. 1 REJECTED SRCN2-4+ as 331-2+ and is sequenced after NOR 325 issues it a 331-1+ to issue a 331-3+. Lead 332 interlocks higher numbered cars thereby enabling those cars in the sequence after the lower numbered cars by enabling NAND or NOR gates corresponding to 331. Since 331-3- enabled NOR 333 at 333-1 and car No. 2 was assumed not rejected so SRCN2-30- makes 333-2-, 333-3+ is inverted by 334 to inhibit car No. 2 assigning NAND 330 with a 330-2-. The resultant 330-4+ represents a CAR No. 2 ASSIGNED CALL signal as SRCN2-20+ to the car memories of car No. 2 at CM-42.

If our assumption that neither of cars No. 1 nor No. 2 had their reject memories set existed, car No. 1 would have received the assignment first and would have inhibited assignment of the call to car No. 2. Both unrejected cars impose (-) as SRCN2-4- and SRCN2-30-. As outlined above, coincidence of 325-1+ and 325-2- makes 325-3+ and 328-1+. Inverter 327 makes 328-2+ hence 328-3 issues an inhibit signal to NAND 329 so that 329-4+ represents CAR No. 1 ASSIGNED CALL as SRCN2-19+. SRCN2-4- also imposes 331-2- to make 331-3+ thereby inhibiting NOR 333 even though SRCN2-30- is present. NOR 333 issues a 333-3- inverted by 334 to maintain NAND 330 gated so that 330-4- represents CAR No. 2 ASSIGNED CALL (not) as SRCN2-20-.

Completion of the assignment of the allotment call will be considered with reference to CAR No. 1. From SRCN2-19+ to CM-42+ (FIG. 13A) the CAR ASSIGNED CALL signal is applied to NOR 350 as 350-2+ making 350-3-. NOR 350 is inhibited if the HALL CALL MEMORY ON signal AGC-31+ to CM-51+ gates NAND 351 by 351-1+, assume 351-2+, and issues 351-3- gating NOR 352 when a car is at the allot-

ment floor and conditioned for the travel direction so that NAND 353 is gated to impose a 352-1- coincident with 352-2- to make 350-1+. These conditions were not assumed, hence NOR 350 is gated and its 350-3- inverted at 354 makes 355-2+ of NAND 355, assume 355-1+, making 355-3-. Assume NAND 356 has 356-1+ so that when 356-2- appears 356-3+ inverted at 357 makes 358-1- of NOR 358. With the ring counter position and direction corresponding to the allotment call, the call is assigned as a demand.

RING COUNTER DIRECTION UP, CM-24+, makes 359-1+ of NAND 359 and RING COUNTER AT FLOOR 3, CM-25-, through inverter 222 makes 359-2+ making 359-3- to 358-2-. NOR 358 issues 358-3+ to 360-1+ of NAND 360. Assuming no reset signals, CM-38+ and CM-39- the No. 3 up demand memory will be set when 360-1+ appears. Inverter 361 imposes a 362-1- on NAND 362 and the group service status makes 362-2+ so NAND 362 issues 362-3+ to inhibit NOR 363. 363-3- with CM-39- gates NOR 364 to issue 364-3+ to 360-2+ making 360-3- and 220-1- in the 3 up demand memory flip flop. Amplifying inverter 365 will actuate an illuminated indicator for UP DEMAND AT FLOOR 3 as CM-48-.

The allotting sequence is concluded by the setting of the 3 up demand memory and the resetting of the 3 up select memory so that the allotter is released for the next selected hall call. As the 3 up demand memory is set NAND 366 of FIG. 13A issues a 366-3- to NOR 367 as 367-2-. With the ring counter direction and floor coincident with the demand 367-1- is present, hence 367-3+ makes 368-1+. Group service status makes 368-2+ of NAND 368, hence 368-3- appears as DEMAND AT FLOOR 3, CM-41-, to FIG. 7, AGC-4-, 369-1- to NAND 369 and thus 369-3+ inverted by 370 as DEMAND IN ANY CAR, AGC-3- to HCM-24-. When this demand is thus indicated as entered, the select memory resets by HCM-24- inverted at 118 to reset NAND 371 at 371-2+. Again, master ring counter scan direction and position enable this reset imposing a 371-1+ to issue a 371-3- to 115-2- resetting the flip flop of the No. 3 up select memory and removing the A CALL HAS BEEN SELECTED FRO ALLOTMENT signal at HCM-8.

The system is conditioned to allot another hall call. It will upon coincidence of a hall call and a master ring counter scan position and scan direction set a new hall call memory, and new select memory. Reset signals are imposed on the select ring counter 59 and on a per car basis to the binary preset counter 56, the master binary counter 55, the reject memory 31 and the car located memory 62 of each car upon operation of the new select memory and the allotting scan of the master ring counter proceeds as previously described. It should be noted that the various counter resets are straight forward in that the signal ALLOTTER MAIN RESET, AGC-17+ (FIG. 7) is applied directly through SRCN2-50 to lead 377 and the reset input of select ring counter 59, and through suitable inversion and amplification to the paralleled car allotter sections of the several cars. Thus, AGC-17+ is applied to CAS3-42 for each car as a (+) signal and is inverted at 380 and applied to the reset reject memory 311 and as CAS-3-41- to CAS1-20- to reset with a 237- 2- the car located memory 62. NOR 381 (FIG 11) applies a (-) reset signal to the binary preset counter 56 as its count on lead 382 goes (+) in advancing from 63 to 64 in the

normal utilization of the counter, and as an assurance of an initial zero setting, inverter 383 imposes a 381-1+ to issue 381-3- and reset the counter.

In the example chosen for detailed discussion, the car was committed to serve the entire range of assumed travel by virtue of its presence at the bottom of travel and the registration of a command at the top of its travel. Thus all floors were read at least once as a distance count in the evaluation. Where the location of the calls imposed on the car, either commands (car calls) or demands (assigned hall calls), and/or the car position are such that the car need not run to the limits of travel before reversing, the distance count is confined to those landings actually to be traversed This concept is disclosed for an analogue system in Kuzara et al. United States Pat. No. 3,507,362 for "Apparatus for Measuring Elevator Car Travel" which issued Apr. 21, 1970. The present system embodies these concepts in the controls for the distance counting gate 181 of FIG. 8.

Distance counting gate 181 is enabled only when NAND 184 is inhibited indicating the scan is at or below the car's upper limit of travel commitment and NAND 185 is inhibited to indicate the scan is at or above the car's lower limit of travel. The car position, the allotment floor or an imposed call can set limits for reversal of the car short or its travel terminals.

Allotment floor as a limit is established in the allotter gating circuits AGC of FIG. 7, when the master ring counter is at the allotment floor and scanning in opposition to the direction of the allotment call. This is illustrated in FIG. 2 at floor 9 where on the first down scan, the top scan limit, bottom scan limit, and bottom distance limit are all effective. As explained with respect to the hall call memory, an AGC-9- will signify RING COUNTER AT ALLOTMENT FLOOR and through 136 and 137 impose 385-1- on NAND 385. In the opposite scan at the allotment floor AGC-10- for RING COUNTER IS COINCIDENT WITH ALLOTMENT FLOOR will impose 385-2-. Each signal will apply a (+) signal to a NAND to indicate coincidence with scan direction as NAND 386 for the setting of the top limit and NAND 387 for setting the bottom limit. RING COUNTER DIRECTION IS UP at AGC-54+ enables NAND 386 to be gated by 385-3+ so that 386-3- issues as a set signal for the top scanner limit to the flip flop comprising cross coupled NANDs 388 and 389. This 388-1- signal makes 388-3+ to impose a 391-1+ on the top scanner limit NAND 391. It also insures by a 389-1+ that 389-3- is applied to the bottom scanner limit NAND 392 as 392-2-. Whenever the scan is at the allotment floor scanning in either direction, 385 issues a 385-3+ to inverter 393 which imposes a (-) on both scanner limit NANDs 391 and 392. Thus, both limit NANDs 391 and 392 issue (+) signals as TOP SCANNER LIMIT and BOTTOM SCANNER LIMIT respectively AGC-26+ and AGC-53+.

After the ring counter passes the allotment floor the distance counting gate should no longer be gated by the allotment call for the direction of scan although the allotment call should provide a limit on the return direction of scan. Accordingly, on the next scan position beyond the allotment floor the scanner limit for the scan direction is cancelled while the scanner limit for the return direction is retained. Consider an ascending scan with a RING COUNTER DIRECTION UP to impose AGC-54+ and AGC-55- when both AGC-9+ and

AGC-10+ present. NAND 385 issues a 385-3- to inhibit any input to the direction flip flop comprising NAND 388 and 389 by making the flip flop control NAND 386 and 387 both issue (+) signals as 386-3+ and 387-3+. The set direction of the flip flop is "up" as established while the scan was at the allotment floor. Thus 388-3+ impose as 391-1+ is coincident with 391-1+ from inverter 393 and NAND 385 to make AGC-26- signifying TOP SCANNER LIMIT (not). However, 389-3- makes 392-2- so that 392-3+ is sustained as AGC-53+ signifying BOTTOM SCANNER LIMIT. When the scan direction reverses, this condition is maintained since NAND 385 will enable no change until the scan is again at the allotment floor.

When the ring counter scan is again coincident with the allotment floor to impose either AGC-9- or AGC-10- to 385 and RING COUNTER DIRECTION IS DOWN as AGC-55+, NAND 385 issues a scanner limit enabling signal 385-3+ through inverter 393 to both 391 and 392 whereby both limits are indicated. At the same time, the scanner limit memory is set for the top limit by gating NAND 387 to issue a 387-3- to 389-2. The resultant 389-3+ makes 388-3- as the seal so that at the next scan position 392-2+ and 392-1+ make 392-3- to remove the BOTTOM SCANNER LIMIT signal making AGC-53-. AGC-26+ remains since 383-3- at 391-1- holds 391-3+.

Either of the scanner limit signals provide distance counting NAND 181 of FIG. 8 with an enabling (+) signal since the top scanner limit signal AGC-26+ to CAS1-39+ inverted at 395 to 184-2- causes 184-3+ to appear as 181-3+. For a bottom scanner limit the signal 392-3+ as AGC-53+ appears as CAS1-37+ to inverter 396 which makes 185-2- to apply 185-3+ as 181-4+ enabling distance counting NAND 181. When the scan is at any floor but the allotment floor NAND 385 of FIG. 7 is gated to issue 385-3- and apply through inverter 393 a 391-2+ and a 392-1+ so that the top scanner limit signal will be turned off for the up scans above the allotment floor and the bottom scanner limit will be off for down scans below the allotment floor by the coincidence of a 391-2+ and a 391-1+ to issue a 391-3- TOP SCANNER LIMIT (not) as AGC-26- or coincidence of a 392-1+ and a 392-2+ to issue a 392-3- BOTTOM SCANNER LIMIT (not) as AGC-53-. Since the car is either above or below the allotment floor when at other floors, if it is below the allotment floor scanning upward its TOP SCANNER LIMIT is on by the scanner limit memory signal 391-1- coincidence with 391-2+ to issue 391-3+ and for down scanning above the allotment floor the BOTTOM SCANNER LIMIT is on by 392-1+ coincidence with 392-2- to issue 392-3+.

While both 184 and 185 have scanner limit signals to provide enable signals to distance counting gate 181 while the scan is at the allotment floor, at all other floors only one of NANDs 184 and 185 is so conditioned by scanner limit signals and if a distance count is to be made the other NAND must be gated either by virtue of car position or calls committed to the car. Such gating signals are supplied from the car memories for each floor as typified in FIG. 13B.

The relationship of the scan position to car position and calls is established on a per floor basis through top distance limit gate, NAND 400, and bottom distance limit gate, NAND 401. Considering FIG. 2, floor three is a bottom distance limit by virtue of the down demand

at three. Thus, the NAND 401 in the third command memory issues a 401-3- so long as the ring counter is at or above the third floor to cause NAND 404 to issue a 404-3+ and make 401-2+.

The ring counter scan position relative to the floor is indicated by the interconnection of the NAND 403 and 404 of each floor with those respective NANDs for all other floors. A RING COUNTER AT FLOOR SIGNAL is issued to both NANDs 403 and 404 for the floor being scanned. Thus, CM-25- to 403-2 and 404-1 make 403-3 and 404-3 for that floor (+). Inverter 405 passes a CM-4- to the NAND 403 of the car memories for all floors above at CM-3 to cause their NANDs 403 to issue 403-3+ due to the imposed 403-1-, thereby signifying to their following cascaded NANDs 403 RING COUNTER IS BELOW FLOOR. In a similar fashion a RING COUNTER IS ABOVE FLOOR is issued by each NAND 404 below the floor of the scan position since NAND 404 of the scan position issues a 404-3+ inverted by the inverter 406 to a CM-5- signal applied to the next lower floor's CM-6 terminal.

Car and call positions are related to the floor in the car memory for each floor by NAND 399. Any inhibiting signal on 399 results in a 399-5+ defining that floor as within a distance limit. Thus, an up demand at the floor makes lead 409 (-) from the up demand memory (FIG. 13A) to make 399-1-. A down demand for the floor makes 407 (-) to make 399-2-. A command for the floor makes 408 (-) to make 399-3-. The presence of the car at the floor makes CM-26+ from the car position means, such as a floor selector machine, so that inverter 398 imposes a 399-4-.

If a floor's NAND 399 issues a 399-5+ and the ring counter is at or below the floor so that its 403-3 issues a (+), then its top distance limit NAND 400 is gated to issue a 400-3-. The resultant TOP DISTANCE LIMIT signal CM-9- wire ORed to CAS1-36 imposes a 184-1- to provide a distance counting enable signal 181-3+. Similarly, if the ring counter is at or below the floor having a 399-5+ so that its 404-3 is (+), the coincident 401-1+ and 401-2+ issue a 401-3- wire ORed to CAS1-36. This imposes a 185-1- to provide a distance counting 181-4+ for a BOTTOM DISTANCE LIMIT.

The present elevator control assigns individual hall calls to individual elevator cars without restriction as to the location of the cars relative to the floors of the calls by continuously scanning the floors served by the elevators. A master ring counter 53 scans the floors upward and downward to locate registered hall calls and serialize them for allotment, to time division multiplex, per floor functions such as the setting and resetting of hall calls and car calls and memories associated therewith and locating the cars, and to actuate the per floor scanning of the allotment evaluation of each car's availability to serve the hall call selected for allotment.

A single scanner performs the multiple function by virtue of select memories which are provided for each hall call and are set to identify the hall call currently subject to allotment. In the example, the master ring counter scan when coincident in both floor position and scan direction with the floor and service direction of a registered hall call causes it push button buffer to set its hall call memory and, if no other select memory is set, to set its select memory. When a select memory is set, the allotter is reset for the allotment of the call

of the set select memory. This involves resetting counters and memories for each car which are employed in the allotment.

The exemplary system terminates the allotter reset and initiates allotment when the ring counter advances from coincidence of position and direction of scan to coincidence of position and opposed direction of scan with the floor and service direction of the select memory call. Allotment involves a per floor evaluation of service conditions imposed upon each car. A floor evaluation for all cars is performed simultaneously during an allotter read interval for the floor defined by the master ring counter. Allotter inhibit intervals are also defined between successive read intervals by the master ring counter. Pulse trains of lengths correlated to the delays experienced for the several service burdens are generated at a high frequency relative to the clocking frequency of the master ring counter and are admitted to individual car master binary counters 54 through the windows provided by the allotter read intervals.

The per floor factors imposed on the individual cars for which pulse trains are accumulated in their respective master binary counters include car calls imposed on the cars as "commands", hall calls assigned the cars as "demands", and distance to be traversed by the cars. The calls are further segregated into those calls to be served by the cars before they can serve the allotment call, inside commands and demands, and those calls to be served after the allotment call, outside commands and demands.

While all service burden factors are represented by pulse counts which are of an adjustable number of pulses, the system is arranged to correlate the number of pulses for each factor with the delay that factor imposes on the car in serving the allotment call. While a primary consideration in such service is the delay predicted until the car can reach the floor of the call some consideration is also given to the delays in responding to the car call which naturally follows as a passenger who registered a hall call enters the car at the floor of the hall call. This travel beyond the allotment call is represented by the outside demands and commands.

Ordinarily, the outside demands and commands are assigned about one-half the weight of the inside commands and demands. During a scan from the allotment call, each allotter read interval considers inside demands inside commands and distance in that order. If a demand is present and its count is imposed, it inhibits a command count. Distance count is made only for those floors the car is committed to traverse. When the car is located by the advance of the scan position to the car position while scan direction opposes car direction, the distance count is terminated for subsequent allotter read intervals and outside command and demand counts are accumulated until the scan is completed to the allotment call e.g. at the allotment floor with scan direction opposing allotment call service direction.

Static service conditions imposed on each car are then considered and pulse count representing the delays of those factors are added to each car's master binary counter. The completion of all count additions to the master binary counters of all cars, completion of biasing, is signaled to a multiple digital comparator which selects the counter having the lowest count. Upon the next coincidence of the master ring counter scan position and direction with the allotment call floor and direction, the car of that counter having the lowest

count is assigned the allotment call and the select memory of that call is reset to permit the allotment of other calls.

In the example, a scan interval from the coincidence of scan position and direction with the allotment call position and direction to a coincidence of scan position and direction with the allotment call position and opposite service direction is employed for allotter reset. When dynamic factors have been considered static factors are inserted as pulse trains. Evaluation of counts accumulated is performed step-by-step at about scan frequency. Assignment is completed on scan position and direction coincidence with the call position and direction. Thus, at least two and frequently three scan cycles are consumed in making an allotment.

It is to be understood that the system lends itself to modification both as to the individual elements thereof and their combination without departing from its spirit and scope. For example, the allotment can be performed in one scan cycle by setting the select memory resetting the allotter and inserting the static count of delay factors as a preset of the master ring counter of each car as the scan position is at the allotment floor and its direction opposes the call service direction. Allotment can then proceed immediately. The count comparator can be operated at higher frequencies and make the selection at the end of the allotment scan while the scanner is next at the scan position and its direction opposes the call service direction. Accordingly, it is to be appreciated that the detailed example set forth above is for illustrative purposes and is not to be read in a limiting sense.

I claim:

1. An elevator control for a plurality of cars serving a plurality of floors including a scanning means for scanning said floors; means for registering calls for service at the floors; call memory means for each of a plurality of calls for service to floors set in response to a coincidence of operation of said registering means for said floor and the scan of said scanning means with said floor; select memory means for each of a plurality of calls for service to floors set in response to a coincidence of a registered call for said floor and the scan of said scanning means with said floor; and means responsive to the setting of said select memory for evaluating the availability of each of a plurality of cars to serve the registered call of said select memory.

2. An elevator control according to claim 1 including means to assign the call of said set select memory to the car of said plurality having the optimum availability.

3. An elevator control according to claim 2 including demand memory means for each car for each of a plurality of calls for service to floors and means to set the demand memory of the car having the optimum availability in response to a coincidence of the scan of said scanning means with said floor.

4. An elevator control according to claim 2 including means to reset said select memory in response to a coincidence of an assignment of a car by said assigning means and the scan of said scanning means with said floor of said select memory.

5. A control according to claim 1 including means responsive to a set select memory to inhibit the setting of other select memories.

6. An elevator control for a plurality of cars serving a plurality of floors, means for registering calls common to said cars, means to select a call for allotment to

a car and means to scan the floors to allot the call to the car the improvement which comprises a single scanner for scanning the floors to select a call and to scan the floors to allot the call, a select memory for each of a plurality of said call means, means to set said select memory for a registered call in response to coincidence of the registered call and the scan of the floor of the call by said scanner; and means to evaluate service burden for floors on individual cars relative to said call of said set select memory in response to coincidence of the scan of said scanner with said other floors.

7. A control according to claim 6 wherein said scanner runs continuously.

8. A control according to claim 6 wherein said scanner runs upward and downward according to the floor sequence of the system.

9. A control according to claim 8 wherein said select memory is set upon coincidence of said scanner scan position with the floor of the call of said select memory and scan direction corresponding to the service direction of the call.

10. A control according to claim 8 including a read interval defining means for defining an interval for each of a plurality of scan positions actuated by said scanner; and means to actuate said read interval upon coincidence of said scanner scan position with the floor of the call of said select memory.

11. A control according to claim 10 wherein said read interval actuating means is effective while said scanner scan direction opposes the service direction of the call of said select memory.

12. A control according to claim 11 including means to inhibit said actuated read interval means upon completion of the scan of all floors.

13. A control according to claim 12 including means to assign the call of said set select memory to a car upon coincidence of said scanner scan position and direction with the floor and service direction of the call of said select memory following completion of the scan of all floors with said read interval means actuated.

14. A control according to claim 6 including a read interval defining means for defining an interval for each of a plurality of successive scan positions actuated by said scanner; and an inhibit interval defining means actuated between successive read intervals by said scanner.

15. A control according to claim 14 including a clocking means for said scanner defining a scanner frequency; means to generate a series of pulses of higher frequency than the frequency of said scanner clocking means, a pulse counter, and means coupling said pulse generating means to said pulse counter during a read interval.

16. A control according to claim 15 wherein said pulse counter is provided individually for each of a plurality of cars.

17. A control according to claim 6 including a clocking means for said scanner for defining a scan frequency; a read interval defining means for defining an interval for each scan position; a pulse generator for generating a plurality of pulses during a read interval; a pulse counter; means for selectively coupling said pulse generator to said pulse counter; and means to adjust the number of pulses issued by said pulse generator while coupled to said pulse counter.

18. A control according to claim 17 wherein certain of said scanner scan positions correspond to floors

served by said cars; and wherein said means responsive to service burden is responsive to service burden at the floor corresponding to the scanner scan position which is imposed upon the respective car.

19. A control according to claim 6 including a clocking means for said scanner for defining a scan frequency; a read interval defining means for defining a read interval for each of a plurality of scan positions; a pulse generator for generating a plurality of pulses during a read interval; a pulse counter for each car; means responsive to a predetermined service burden imposed on a car for selectively coupling said pulse generator to said pulse counter for said car.

20. A control according to claim 19 wherein certain of said scanner scan positions correspond to floors served by said cars; and wherein said means responsive to service burden is responsive to any of a plurality of service burdens at the floor corresponding to the scanner scan position which are imposed upon the respective car.

21. A control according to claim 19 including means to reset said pulse counter count for each car in response to the setting of said select memory.

22. A control according to claim 21 including a clocking means for said scanner for defining a scan frequency; a read interval defining means for defining a read interval for each of a plurality of scan positions; a pulse counter for each car; and means responsive to a predetermined service burden imposed upon a car and associated with a floor corresponding to the current scan position of said scanner to apply a predetermined number of pulses to said counter for said car during the read interval for said scan position.

23. A control according to claim 22 including means to define the floors which said car is required to traverse before it can serve the call of said set select memory; and wherein said pulse applying means is responsive while said scanner is at a scan position to said means defining floors to be traversed to apply a number of pulses correlated to the time required for the car to traverse the floor of that scan position.

24. A control according to claim 22 including means individual to each car for registering car calls for floors; means to define the presence of a car call for a floor having the scanner scan position coincident; and wherein said pulse applying means is responsive while said scanner is at a scan position to said means to define a car call for the floor of that scan position to apply a number of pulses correlated to the time required for the car to serve the car call for the floor of that scan position.

25. A control according to claim 22 including means to allot individual hall calls to individual cars in response to said service evaluation means; a demand memory set for each hall call assigned to a car; and wherein said pulse applying means is responsive to said demand memory while said scanner is at a scan position to apply a number of pulses for each demand memory set correlated to the time required to serve the set demand for the floor of that scan position.

26. A control according to claim 22 wherein said means responsive to a predetermined service burden includes a first means responsive to a first service burden imposed upon a car and associated with a floor corresponding to the current scan position to apply a first predetermined number of pulses to said counter, a second means responsive to a second burden imposed

upon a car and associated with a floor corresponding to the current scan position to apply a second predetermined number of pulses to said counter, and sequencing means to apply said first predetermined number of pulses ahead of said second predetermined number of pulses.

27. A control according to claim 26 including means to allot individual hall calls to individual cars as demands for the floors of the calls; means to define the floors which said car is required to traverse before it can serve the call of said set select memory; and wherein said first means is responsive to demands imposed upon said car for said floors and said second means is responsive to distance said car is required to traverse at said floors.

28. A control according to claim 26 including means individual to each car for registering car calls for floors, means to define the floors which said car is required to traverse before it can serve the call of said set select memory; and wherein said first means is responsive to car calls imposed upon said car for said floors and said second means is responsive to distance said car is required to traverse at said floors.

29. A control according to claim 6 including means responsive to a set select memory to inhibit the setting of other select memories.

30. A control according to claim 6 including a pulse counter for each car; means to sense a static service burden imposed upon any of a plurality of said cars and tending to delay its service to the call of said set select memory; and means to insert a pulse count in said counter of each of a plurality of cars subject to said static service burden correlated in number to the delay in service imposed upon said car by said burden.

31. A control according to claim 6 including a pulse counter for each car; means to sense a first static service burden imposed upon any of a plurality of said cars and tending to delay its service to the call of said select memory; means to sense a second static service burden imposed upon any of a plurality of said cars and tending to delay its service to the call of said select memory; and means to insert a pulse count in said counter of each of a plurality of cars subject to any of said first and second static service burdens correlated in number to the delay in service imposed upon said car by said burden.

32. A control according to claim 31 wherein said means to insert a count includes means to sequence a count insertion for said first service burden ahead of a count insertion for said second service burden.

33. An elevator control for a plurality of cars serving a plurality of floors including means for registering calls common to a plurality of said cars and means for assigning individual registered hall calls to individual cars the improvement comprising scanning means for scanning said floors; a pulse counter for each car; means effective for each scan position corresponding to a floor which a car is committed to traverse to generate a plurality of pulses for any of a plurality of service burdens imposed upon said car for said floor; a pulse counter for each car for accumulating pulses generated for service burdens imposed on said car; means to compare the number of pulses accumulated and means to select that car having the lowest number of accumulated pulses for assignment of a registered hall call.

34. An elevator control according to claim 38 including a select memory set upon coincidence of said scan-

ner scan position with the floor of a registered hall call; and means to assign the call of the set select memory to the car selected by said car selecting means.

35. An elevator control according to claim 34 including means to reset said counters for all cars upon setting a select memory.

36. In an elevator system, means for representing a first and second service factor comprising a pulse generator; control means to cause said pulse generator to issue a first series of pulses in response to said first service factor imposed on a car representative of said service factor; a second control means to cause said pulse generator to issue a second series of pulses in response to a second service factor imposed on said car and means to sequence said first and second means whereby the overlap of the pulses of the respective first and second pulse series is avoided.

37. A combination according to claim 36 including means to associate said control means with a given location along a path of travel for an elevator car.

38. A combination according to claim 36 including means to associate in sequence said control means with each of a plurality of locations along a path of travel for an elevator car.

39. A combination according to claim 38 including third control means to cause said pulse generator to issue a third series of pulses in response to a condition imposed upon an elevator car; and means to sequence said third control means with said first and second control means whereby the overlap of the pulses of the respective first, second and third pulse series is avoided.

40. Elevator service requirement evaluation means comprising first means responsive to a first service requirement for issuing a first predetermined plurality of pulses in response to the imposition of said requirement; second means responsive to a second service requirement of a type different from said first service requirement for issuing a second predetermined plurality of pulses in response to the imposition of said requirement; and means to accumulate said pulses from said generating means as an indication of combined imposed service requirements.

41. Elevator service requirement evaluation means according to claim 40 wherein said service requirements are for a given landing.

42. Elevator service requirement evaluation means according to claim 41 including means for registering calls for service at each of a plurality of landings wherein said service requirements are a call for service at said given landing and a distance to be traversed by an elevator car at said given landing.

43. Elevator service requirement evaluation means according to claim 41 including means for registering a car call for service at said given landing; means for registering a landing call for service at said given landing; and wherein said first means includes means responsive to a car call for said given landing to issue a car call series of pulses of a predetermined number, means responsive to a landing call for said given landing to issue a landing call series of pulses of a predetermined number, and means responsive to a coincidence of a car call and a landing call to render a selected one of said call responsive means ineffective.

44. Elevator service requirement evaluation means according to claim 43 wherein said selected one of said call responsive means is said means responsive to a car call.

45. Elevator service requirement evaluation means according to claim 40 including sequencing means to enable said second means following the completion of pulse issuance by said first means.

46. Elevator service requirement evaluation means according to claim 40 including means responsive to the absence of said first service requirement and sequencing means to enable said second means in response to the means responsive to an absence of said first service requirement.

47. Elevator service requirement evaluation means according to claim 40 including means to actuate said first and second means for a given landing; and means to sequence said first and second means for said given landing to enable said second means following the completion of pulse issuance by said first means.

48. Elevator service requirement evaluation means according to claim 40 including means for registering car calls for service at landings; means for registering landing calls for service at landings; and wherein said first means includes means responsive to a car call for a landing to generate a car call series of pulses of a predetermined number, and means responsive to a landing call for a landing to generate a landing call series of pulses of a predetermined number.

49. Elevator service requirement evaluation means according to claim 40 for an elevator system having a plurality of cars, wherein said means to accumulate pulses is individual to each of a plurality of said cars, whereby the accumulated pulse count for each car is an indication of combined imposed service requirements on said car.

50. Elevator service requirement evaluation means according to claim 40 including means to adjust the number of pulses generated by said first means.

51. Elevator service requirement evaluation means according to claim 40 for an elevator system having a plurality of cars, wherein said first, second and accumulating means are individual to each of a plurality of said cars whereby the accumulated pulse count for each car is an indication of combined imposed service requirements on said car.

52. Elevator service requirement evaluation means according to claim 51 including means individual to each of a plurality of said cars to adjust the number of pulses generated by said first means.

53. Elevator service requirement evaluation means according to claim 40 for an elevator system serving a plurality of landings including means to successively scan said landings; means responsive to said scanning means to actuate said first and second means to respond to respective first and second service requirements at scanned landings for each of a plurality of said landings.

54. Elevator service requirement evaluation means according to claim 40 for an elevator system having a plurality of cars serving a plurality of landings wherein said first, second and accumulating means are individual to each of a plurality of said cars; including means to successively scan said landings; and means responsive to said scanning means coincidence of scan with said landings to actuate said first and second means to respond to respective first and second service requirements imposed on individual cars for said landings for each of a plurality of said landings.

55. Elevator service requirement evaluation means comprising a pulse counter; means responsive to a

given service condition to insert a predetermined plural pulse count in said counter; and means responsive to a second service condition of a type different from said given service condition to insert a second predetermined plural pulse count in said counter whereby the total pulse count in said pulse counter indicates the combined service burden imposed by the conditions.

56. Elevator service requirement evaluation means for a system comprising a plurality of landings comprising means to register landing calls for said landings for each direction of travel from said landings; means to register car calls for service to said landings; a scanner to scan said landings upward and downward in their natural order; a landing call memory for each of a plurality of landings and service direction which is set in response to a coincidence of scanner scan position and direction with a registered landing call for the landing and service direction; a landing call select memory for each of a plurality of landings and service direction which is set in response to a coincidence of scanner scan position and direction with a set landing call memory for the landing and service direction and the absence of any other set landing call select memory; first means responsive to a first service requirement for issuing a first predetermined plurality of pulses in response to the imposition of said first requirement for each of a plurality of said landings when said scanner scan is coincident with said landings; enabling means for said first means actuated by coincidence of said scanner scan location with the landing of a set select memory and said scanner scan direction is opposed to the service direction of said set select memory and maintained actuated for an interval until a scanner scan of all landings in both directions is completed; and means to accumulate pulses issued by said first means while said enabling means is actuated as an indication of the imposed service requirement.

57. Elevator service requirement evaluation means according to claim 56 including second means responsive to a second service requirement for issuing a second predetermined plurality of pulses in response to the imposition of said second requirement for each of a plurality of said landings when said scanner scan is coincident with said landings; said enabling means when actuated enabling said second means; and said means to accumulate pulses accumulating pulses issued by said second means.

58. Elevator service requirement evaluation means according to claim 56 including a static service burden responsive means for imposing a pulse count on said pulse accumulating means representing a level of service burden imposed by the static service burden.

59. Elevator service requirement evaluation means according to claim 56 including means to reset said pulse accumulating means prior to the actuation of said enabling means.

60. Elevator service requirement evaluation means according to claim 59 including a static service requirement burden responsive means responsive subsequent to operation of said reset means for imposing a pulse count on said pulse accumulating means representing a level of service burden imposed by the static service burden.

61. Elevator service requirement evaluation means according to claim 56 wherein said reset means is responsive to a coincidence of scanner scan position and

direction with the landing and service direction of a set select memory.

62. Elevator service requirement evaluation means according to claim 56 including a static service burden responsive means effective subsequent to the termination of the actuated interval of said enabling means for imposing a pulse count on said pulse accumulating means representing a level of service burden imposed by the static service burden.

63. Elevator service requirement evaluation means for a system comprising a plurality of cars serving said landings according to claim 56 wherein said means to accumulate pulses is individual to each of a plurality of said cars whereby the accumulated pulse count for each car is an indication of combined imposed service requirements on said car.

64. Elevator service requirement evaluation means according to claim 63 including means responsive when said scan is coincident with the landing of a set select memory to allot the landing call of said select memory to the car having a certain pulse count in its accumulating means subsequent to the termination of the actuated interval of said enabling means.

65. Elevator service requirement evaluation means according to claim 64 wherein said certain pulse count is the least pulse count for any car.

66. Elevator service requirement evaluation means according to claim 64 including a demand memory for each of a plurality of cars for each of a plurality of landings and service directions of said landing calls; and wherein said allotting means sets the demand for the landing and service direction of the set select memory when said scan position and direction is coincident with said landing and service direction.

67. An elevator control responsive to an imposed service burden for producing a pulse count of a desired number corresponding to the delay imposed by said service burden comprising means to generate a given number of pulses; means to issue a signal when the given number complement of the desired number of pulses has been generated; and means responsive to said signal to issue the balance of the given number of pulses.

68. An elevator control for producing a first pulse count corresponding to the delay imposed by a service condition and for producing a second pulse count corresponding to the delay imposed by a second service condition comprising first means responsive to said first predetermined service condition; second means responsive to said second predetermined service condition, means to produce a given number of pulses; means responsive to said first means to issue a signal

when the given number complement of the first pulse count has been generated; means responsive to said second means to issue said signal when the given number complement of the second pulse count has been generated; and means responsive to said signal to issue the balance of the given number of pulses.

69. In an elevator control, means for generating a pulse train of a length corresponding to a delay anticipated for a service burden imposed comprising:

- a pulse issuing gate;
- a preset pulse counter having a predetermined count capacity;
- a plurality of outputs for said preset pulse count representative of binary count bits;
- a preset pulse gate coupled to said preset pulse counter;
- a pulse source coupled to said pulse issuing gate and said preset pulse gate;
- a count gate having a plurality of inputs;
- a bias signal source;
- a multiplicity of switching means for selectively coupling said outputs of said preset counter and said bias signal source to said count gate inputs in combinations to provide coincident gating inputs to said count gate at selected counts within the capacity count of said preset counter;
- a preset control gate for issuing a gating signal to said preset pulse gate;
- an advance from preset gate;
- a pulse issuing control gate for issuing a gating signal to said pulse issuing gate;
- a count is completed gate;
- means for applying a service burden evaluation enabling signal to said preset control gate and advance from preset gate;
- means for applying a service burden signal to gate said enabled preset control gate when said burden is imposed whereby said preset pulse gate admits pulses from said pulse source to said preset counter;
- means responsive to coincident inputs to said count gate from said preset counter outputs to gate said advance from preset gate to enable said pulse issuing control gate and said count is completed gate;
- means responsive to a count other than zero in said preset counter to gate said enabled pulse issuing control gate to gate said pulse issuing gate; and
- means responsive to a count of zero in said preset counter to inhibit said pulse issuing control gate and said pulse issuing gate while gating said count is completed gate.

* * * * *

UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 3,739,880
DATED : June 19, 1973
INVENTOR(S) : Gerald D. Robaszkiewicz

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 12, line 19,	"SN740N" should be - - SN7400N - - .
Column 15, line 64,	"ing" should be deleted.
Column 16, line 17,	after "145" insert - - to - - .
Column 19, line 60,	"count" should be - - counter - - .
Column 20, line 34,	"inhibit" should be - - inhibited - - .
Column 23, line 55,	"CAS3-9-9+" should be - - CAS3-9+ - - .
Column 25, line 26,	"146" should be - - 145 - -
Column 25, line 35,	"148" should be - - 138 - - .
Column 25, line 59,	"144-1+" should be - - 244-1+ - - .
Column 25, line 66,	"243-2-" should be - - 242-2- - -
Column 27, line 36,	"166" should be - - 266 - - , "167-1+" should be - - 267-1+ - - .
Column 28, line 24,	"49+" should be - - 49- - - .
Column 31, line 14,	"-2-" should be - - -2+ - - .
Column 33, line 44,	"FRO" should be - - FOR - - .
Column 35, line 8,	"391-1+" should be - - 391-2+ - - .
Column 40, line 67,	after "second" insert - - service - - .
Column 44, line 11,	"form" should be - - from - - .
Column 45, line 31,	after "demand" insert - - memory - - .

Signed and Sealed this

sixth Day of January 1976

[SEAL]

Attest:

RUTH C. MASON
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents and Trademarks

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