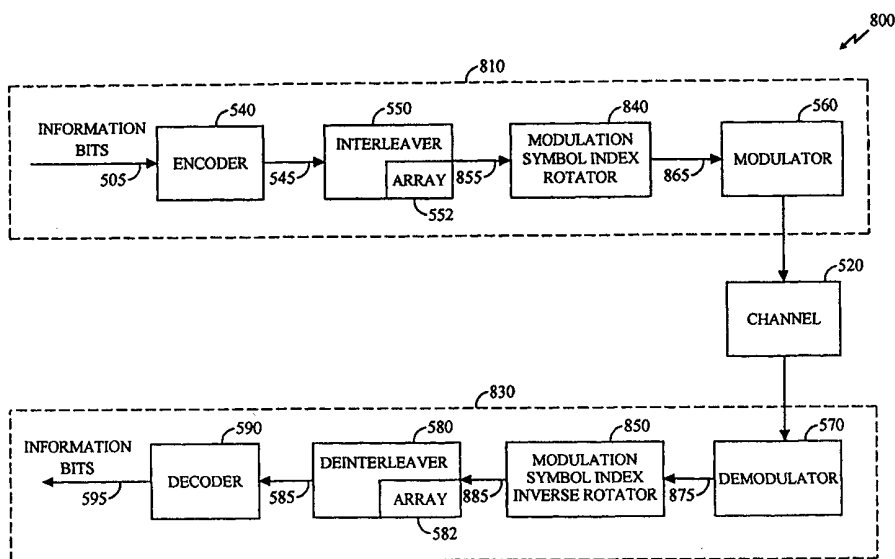




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(54) Title: METHOD AND APPARATUS FOR ROTATING MODULATION SYMBOL INDICES



(57) Abstract

A method and apparatus for improving the performance of a digital communications system (100) which uses a block interleaver (550) that writes data words into an array (552) by columns and reads modulation symbol indices from the array (552) by rows where the number of columns in the array of the block interleaver (550) is an integer multiple of the number of bits used to form each modulation symbol index. The method includes the steps of receiving from the array (552) a plurality of modulation symbol indices (855), modifying at least one of the modulation symbol indices (840, 906) in a predetermined manner to produce a modified modulation symbol index so that the most significant bit of the modified modulation symbol index does not occupy the same bit position as the most significant bit of adjacent modulation symbol indices, and sending the modified modulation symbol indices to a modulator (560, 908).

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METHOD AND APPARATUS FOR ROTATING MODULATION SYMBOL INDICES

BACKGROUND OF THE INVENTION

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I. Field of the Invention

The present invention relates generally to spread spectrum communication systems, and more specifically, to receiving a communication signal in the presence of large amounts of signal Doppler. The present invention further relates to a novel and improved method for rotating modulation symbol indices in an M-ary orthogonally encoded signal to compensate for this signal Doppler.

II. Description of the Related Art

Wireless communications systems are subject to errors introduced by interruptions in the signal path between the transmitter and receiver. In general, these errors are of two types: random errors and burst errors. Random errors are temporally distributed in the signal, and are caused by factors such as atmospheric phenomena. Burst errors are temporally concentrated in one particular portion of the signal, and are caused by such factors as complete blockage of the signal path. Modern wireless communications systems employ several strategies to mitigate these errors.

One such strategy is to use a convolutional coding mechanism, such as a Viterbi coder. These coders excel at compensating for random errors. Another such strategy is to use an interleaver. Interleavers excel at compensating for burst errors. Interleavers "shuffle" the bit stream prior to transmission by distributing consecutive information bits over a portion of the signal. When the received signal is deinterleaved, burst errors are distributed over a portion of the information signal, and so can be corrected by a convolutional encoder such as that mentioned above.

One common type of interleaver is known as a "block" interleaver. A block interleaver typically includes a memory array including rows and columns. In one scheme, data words to be interleaved are written to the array by column and are read out of the array by row. According to this

scheme, consecutive data bits are separated by $I-1$ bits, where I is the number of rows in the array.

In one common wireless communications scheme, information bits are first encoded and then interleaved before modulation and transmission to the receiver. At the receiver, the received signal is first demodulated, then deinterleaved, then decoded to reproduce the information bits. In one modulation scheme, the transmitted signal comprises modulation symbols. According to this scheme, the modulator matches each interleaved data word, referred to as a modulation symbol index, to a corresponding modulation symbol. The modulation symbol is then transmitted in place of the interleaved data word.

At the receiver, the demodulator correlates each received modulation symbol with all possible modulation symbols to produce correlation energies. The largest correlation energy indicates that the corresponding modulation symbol has been received. Therefore, the demodulator generates the modulation symbol index that corresponds to that modulation symbol. In wireless communications systems, this decision process is adversely affected by frequency changes, such as Doppler shifts, experienced by the signal between transmission and reception. Such frequency changes are often caused by relative motion between the receiver and transmitter, or between the receiver or transmitter and a relay station, such as a relay satellite.

In some correlation schemes, the bit of the modulation symbol index that is most likely to be determined incorrectly as a result of such a frequency error is the most significant bit (MSB). When the system uses a block interleaver having a number of columns that is an integer multiple of the number of bits used to form each modulation symbol index, the most significant bits of the modulation symbol index are read out of the interleaver consecutively as data words. When a frequency error causes the MSBs of several consecutive modulation symbol indices to be decided incorrectly, the erroneous bits are read out of the interleaver consecutively. The result resembles a burst error that the decoder is unable to mitigate.

SUMMARY OF THE INVENTION

The present invention is directed toward a system and method for improving the performance of a digital communications system which uses a block interleaver that writes data words into an array by columns and reads modulation symbol indices from the array by rows where the number of columns in the array of the block interleaver is an integer multiple of the number of bits used to form each modulation symbol index. Of course, the terms "row" and "column" are arbitrary references to the logical structure of the interleaver. Thus, the present invention also improves the performance of a digital communications system which uses a block interleaver that writes data words into an array by rows and reads modulation symbol indices from the array by columns where the number of rows in the array of the block interleaver is an integer multiple of the number of bits used to form each modulation symbol index.

The method includes the steps of receiving from the interleaver a plurality of modulation symbol indices, modifying at least one of the modulation symbol indices in a predetermined manner to produce a modified modulation symbol index so that the most significant bit of the modified modulation symbol index does not occupy the same bit position as the most significant bit of adjacent modulation symbol indices, and sending the modified modulation symbol indices to a modulator.

In a preferred embodiment, the modifying step includes the step of rotating the bits of the modulation symbol index. The rotating step includes the steps of rotating the bits of each modulation symbol index by a number of bit positions in accordance with the number of the row in the array occupied by that index.

A further embodiment includes the step of interleaving data words to produce the modulation symbol indices using a block interleaver where the number of columns of the block interleaver array is an integer multiple of the number of bits used to form each modulation symbol index.

A further embodiment includes the step of encoding information bits to produce the data words using an encoder that mitigates random channel errors. Preferably, the encoder is a Viterbi rate 1/3 convolutional encoder.

5 A further embodiment includes the step of generating modulation symbols based on the modulation symbol indices. Preferably, each of the modulation symbols is one of a set of orthogonal modulation functions. Preferably, the orthogonal modulation functions are Walsh functions or codes.

10 One advantage of the present invention is that it prevents the introduction of burst-type errors that could otherwise be introduced by the use of a block interleaver.

BRIEF DESCRIPTION OF THE DRAWINGS

15 The features, objects, and advantages of the present invention will become more apparent from the detailed description set forth below when taken in conjunction with the drawings in which like reference characters identify the same or similar elements throughout and wherein:

20 FIG. 1 illustrates a typical satellite communication system in which the present invention is used;

FIG. 2 illustrates an exemplary transceiver apparatus for use in a user terminal;

FIG. 3 illustrates an exemplary transmission and reception apparatus for use in a gateway;

25 FIG. 4 illustrates a forward link and a reverse link transmission between a gateway and a user terminal;

FIG. 5 is a block diagram of a conventional communications system;

FIG. 6 is a flowchart depicting the operation of a transmitter according to conventional methods;

30 FIG. 7 is a flowchart depicting the operation of a receiver according to conventional methods;

FIG. 8 is a block diagram of a communications system according to a preferred embodiment of the present invention;

FIG. 9 is a flowchart depicting the operation of a transmitter according to a preferred embodiment of the present invention; and

FIG. 10 is a flowchart depicting the operation of a receiver according to a preferred embodiment of the present invention.

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DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The preferred embodiment of the invention is discussed in detail below. While specific steps, configurations and arrangements are discussed, it should be understood that this is done for illustrative purposes only. A person skilled in the relevant art will recognize that other steps, configurations and arrangements can be used without departing from the spirit and scope of the present invention. The present invention could find use in a variety of wireless information and communication systems, including satellite and terrestrial cellular telephone systems. A preferred application is in code-division multiple access (CDMA) wireless spread spectrum communication systems for mobile or portable telephone service. One application of particular utility is in the reverse link of a CDMA satellite communications system. One CDMA communication system is specified in TIA/EIA/IS-95, "Mobile Station-Base Station Compatibility Standard for Dual-Mode Wideband Spread Spectrum Cellular System," July 1993, and similar systems are specified for satellite communication systems.

25 Introduction

The present invention is particularly suited for use in communications systems employing Low Earth Orbit satellites. However, as would be apparent to one skilled in the relevant arts, the concept of the present invention can also be applied to other types of satellite and terrestrial communications systems.

Typical satellite-based communications systems use base stations referred to as gateways, and one or more satellites to relay communications signals between the gateways and one or more user terminals. Gateways provide communication links from each user terminal to other user

terminals or users of other connected communications systems, such as a public telephone switching network. The user terminals can be fixed or mobile, such as a mobile telephone, and positioned near a gateway or remotely located.

5 Some satellite communications systems employ code division multiple access (CDMA) spread-spectrum signals, as disclosed in U.S. Patent No. 4,901,307, issued February 13, 1990, entitled "*Spread Spectrum Multiple Access Communication System Using Satellite or Terrestrial Repeaters*," and U.S. Patent Application Serial No. 08/368,570, filed January 4, 1995, entitled
10 "*Method and Apparatus for Using Full Spectrum Transmitted Power in a Spread Spectrum Communication System for Tracking Individual Recipient Phase Time and Energy*," both of which are assigned to the assignee of the present invention, and are incorporated herein by reference.

 In a typical spread spectrum communications system, one or more
15 preselected pseudonoise (PN) code sequences are used to modulate or "spread" information signals over a predetermined spectral band prior to modulation onto a carrier signal for transmission as communications signals. PN code spreading, a method of spread spectrum transmission that is well known in the art, produces a signal for transmission that has a
20 bandwidth much greater than that of the data signal. In a base station- or gateway-to-user communication link, PN spreading codes or binary sequences are used to discriminate between signals transmitted by different base stations or over different beams, as well as between multipath signals.

 In a typical CDMA spread spectrum system, channelizing codes are
25 used to discriminate between signals intended for different users within a cell or between user signals transmitted within a satellite sub-beam on a forward link (i.e., the signal path from the base station or gateway to the user terminal transceiver). Each user transceiver has its own orthogonal channel provided on the forward link by using a unique "channelizing" orthogonal
30 code. Signals transferred on these channels are generally referred to as "traffic signals." Additional channels are provided for "paging," "synchronization," and other signals transmitted to system users. Walsh functions are generally used to implement the channelizing codes.

CDMA spread-spectrum communications systems, such as disclosed in the above patent documents, contemplate the use of coherent modulation and demodulation for forward link user terminal communications. In communications systems using this approach, a "pilot" carrier signal, also referred to as a "pilot signal," is used as a coherent phase reference for forward link signals. That is, a signal which contains no data modulation is transmitted by a gateway throughout a region of coverage as a reference.

Pilot signals are used by user terminals to obtain initial system synchronization and time, frequency, and phase tracking of other signals transmitted by the gateway. Phase information obtained from tracking a pilot signal carrier is used as a carrier phase reference for coherent demodulation of other system signals or traffic (data) signals. This technique allows many traffic signals to share a common pilot signal as a phase reference, providing for a less costly and more efficient tracking mechanism. A single pilot signal is typically transmitted by each gateway for each frequency used, referred to as a CDMA channel or sub-beam, and shared by all user terminals receiving signals from that gateway on that frequency.

Gateways can convey information to user terminals using one or more signals known as paging signals or channels. For example, when a call has been placed to a particular mobile phone, the gateway alerts that mobile phone by means of a paging signal. Paging signals are used to designate the presence of a call, which traffic channel to use, and to also distribute system overhead information, along with subscriber unit specific messages. A communication system may have several paging signals. Synchronization signals can also be used to transfer system information useful to facilitate time synchronization. All of these signals act as shared resources in a manner similar to pilot signals.

User terminals can respond to a message on a paging signal by sending an access signal over a reverse link, (that is, the signal path from the user terminal to the base station or gateway transceiver). Access signals are also used by user terminals when they originate calls.

As with any communication system, the communication signals are received by the user terminal and downconverted into a baseband frequency

for further processing. Once downconverted, the signals are processed
digitally to detect the particular pilot signal or signals being received, and to
demodulate associated paging, synchronization, and traffic signals. During
demodulation, the PN spreading codes are applied to despread the signals
5 and the channelizing codes correlated with the signals to provide data.

An exemplary wireless communication system in which the present
invention is useful is illustrated in FIG. 1. It is contemplated that this
communication system uses CDMA type communication signals, but this is
not required by the present invention. In a portion of a communication
10 system 100 illustrated in FIG. 1, one base station 112, two satellites 116 and
118, and two associated gateways or hubs 120 and 122 are shown for effecting
communications with two remote user terminals 124 and 126. Typically, the
base stations and satellites/gateways are components of separate
communication systems, referred to as being terrestrial and satellite based,
15 although, this is not necessary. The total number of base stations, gateways,
and satellites in such systems depend on desired system capacity and other
factors well understood in the art.

User terminals 124 and 126 each have or comprise a wireless
communication device such as, but not limited to, a cellular telephone, a
20 data transceiver, or a paging or position determination receiver, and can be
hand-held or vehicle mounted as desired. Here, the user terminals are
illustrated as hand-held telephones and portable telephones, such as car
phones. However, it is also understood that the teachings of the invention
are applicable to fixed units where remote wireless service is desired,
25 including 'inside' as well as 'open air' locations.

Generally, beams from satellites 116 and 118 cover different
geographical areas in predefined patterns. Beams at different frequencies,
also referred to as CDMA channels or 'sub-beams,' can be directed to overlap
the same region. It is also readily understood by those skilled in the art that
30 beam coverage or service areas for multiple satellites, or antenna patterns for
multiple base stations, might be designed to overlap completely or partially
in a given region depending on the communication system design and the
type of service being offered, and whether space diversity is being achieved.

A variety of multi-satellite communication systems have been proposed with an exemplary system employing on the order of 48 or more satellites, traveling in eight different orbital planes in Low Earth Orbit (LEO) for servicing a large number of user terminals. However, those skilled in the art will readily understand how the teachings of the present invention are applicable to a variety of satellite system and gateway configurations, including other orbital distances and constellations. At the same time, the invention is equally applicable to terrestrial based systems of various base station configurations.

In FIG. 1, some possible signal paths are illustrated for communications being established between user terminals 124 and 126 and base station 112, or through satellites 116 and 118, with gateways 120 and 122. The base station-user terminal communication links are illustrated by lines 130 and 132. The satellite-user terminal communication links between satellites 116 and 118, and user terminals 124 and 126 are illustrated by lines 140, 142, and 144. The gateway-satellite communication links, between gateways 120 and 122 and satellites 116 and 118, are illustrated by lines 146, 148, 150, and 152. Gateways 120 and 122, and base station 112, may be used as part of one or two-way communication systems or simply to transfer messages or data to user terminals 124 and 126.

An exemplary transceiver 200 for use in a user terminal 106 is illustrated in FIG. 2. Transceiver 200 uses at least one antenna 210 for receiving communication signals which are transferred to an analog receiver 214, where they are downconverted, amplified, and digitized. A duplexer element 212 can be used to allow the same antenna to serve both transmit and receive functions. However, some systems employ separate antennas for operating at different transmit and receive frequencies.

The digital communication signals output by analog receiver 214 are transferred to at least one digital data receiver 216A and at least one searcher receiver 218. Additional digital data receivers 216B-216N can be used to obtain desired levels of signal diversity, depending on the acceptable level of unit complexity, as would be apparent to one skilled in the relevant art.

At least one user terminal control processor **220** is coupled to digital data receivers **216A-216N** and searcher receiver **218**. Control processor **220** provides, among other functions, basic signal processing, timing, power and handoff control or coordination, and selection of frequency used for signal carriers. Another basic control function often performed by control processor **220** is the selection or manipulation of PN code sequences or orthogonal functions to be used for processing communication signal waveforms. Signal processing by control processor **220** can include a determination of relative signal strength and computation of various related signal parameters. Computations of signal parameters, such as timing and frequency, may include the use of additional or separate dedicated circuitry to provide increased efficiency or speed in measurements or improved allocation of control processing resources.

The outputs of digital data receivers **216A-216N** are coupled to digital baseband circuitry **222** within the user terminal. User digital baseband circuitry **222** comprises processing and presentation elements used to transfer information to and from a user terminal. That is, signal or data storage elements, such as transient or long term digital memory; input and output devices such as display screens, speakers, keypad terminals, and handsets; A/D elements, vocoders and other voice and analog signal processing elements; and the like, all form parts of the subscriber baseband circuitry using elements well known in the art. If diversity signal processing is employed, user digital baseband circuitry **222** can comprise a diversity combiner and decoder. Some of these elements may also operate under the control of, or in communication with, control processor **220**.

When voice or other data is prepared as an output message or communications signal originating with the user terminal, user digital baseband circuitry **222** is used to receive, store, process, and otherwise prepare the desired data for transmission. User digital baseband circuitry **222** provides this data to a transmit modulator **226** operating under the control of control processor **220**. The output of transmit modulator **226** is transferred to a power controller **228** which provides output power control

to a transmit power amplifier **230** for final transmission of the output signal from antenna **210** to a gateway.

As discussed in further detail below, user terminal **200** can also employ a precorrection element **232** in the transmission path to adjust the
5 frequency of the outgoing signal. This can be accomplished using well known techniques of up- or down-conversion of the transmission waveform. In the alternative, a precorrection element **232** can form part of a frequency selection or control mechanism for the analog up-conversion and modulation stage (**230**) of the user terminal so that an appropriately adjusted
10 frequency is used to convert the digital signal to a desired transmission frequency in one step.

Information or data corresponding to one or more measured signal parameters for received communication signals, or one or more shared resource signals, can be sent to the gateway using a variety of techniques
15 known in the art. For example, the information can be transferred as a separate information signal or be appended to other messages prepared by user digital baseband circuitry **222**. Alternatively, the information can be inserted as predetermined control bits by transmit modulator **226** or transmit power controller **228** under the control of control processor **220**.

Digital receivers **216A-N** and searcher receiver **218** are configured with
20 signal correlation elements to demodulate and track specific signals. Searcher receiver **218** is used to search for pilot signals, or other relatively fixed pattern strong signals, while digital receivers **216A-N** are used to demodulate other signals associated with detected pilot signals. Therefore,
25 the outputs of these units can be monitored to determine the energy in or frequency of the pilot signal or other signals. These receivers also employ frequency tracking elements that can be monitored to provide current frequency and timing information to control processor **220** for signals being demodulated.

An exemplary transmission and reception apparatus **300** for use in
30 gateways **120** and **122** is illustrated in FIG. 3. The portion of gateway **120**, **122** illustrated in FIG. 3 has one or more analog receivers **314** connected to an antenna **310** for receiving communication signals which are then

downconverted, amplified, and digitized using various schemes well known in the art. Multiple antennas 310 are used in some communication systems. Digitized signals output by analog receiver 314 are provided as inputs to at least one digital receiver module, indicated by dashed lines generally at 324.

5 Each digital receiver module 324 corresponds to signal processing elements used to manage communications between a gateway 120, 122 and one user terminal 124, 126, although certain variations are known in the art. One analog receiver 314 can provide inputs for many digital receiver modules 324, and a number of such modules are typically used in gateways
10 102 to accommodate all of the satellite beams and possible diversity mode signals being handled at any given time. Each digital receiver module 324 has one or more digital data receivers 316 and a searcher receiver 318. Searcher receiver 318 generally searches for appropriate diversity modes of signals other than pilot signals. Where implemented in the communication
15 system, multiple digital data receivers 316A-316N are used for diversity signal reception.

The outputs of digital data receivers 316 are provided to subsequent baseband processing elements 322 comprising apparatus well known in the art and not illustrated in further detail here. Exemplary baseband apparatus
20 includes diversity combiners and decoders to combine multipath signals into one output for each subscriber. Exemplary baseband apparatus also includes interface circuits for providing output data, typically to a digital switch or network. A variety of other known elements such as, but not limited to, vocoders, data modems, and digital data switching and storage
25 components may form a part of baseband processing elements 322. These elements operate to control or direct the transfer of data signals to one or more transmit modules 334.

Signals to be transmitted to user terminals are each coupled to one or more appropriate transmit modules 334. A typical gateway uses a number of
30 such transmit modules 334 to provide service to many user terminals 124, 126 at a time, and for several satellites and beams at a time. A base station may also use a number of such modules, although base stations tend to group transmit and receive functions more closely together in modem

structures. The number of transmission modules 334 used by gateway 120, 122 is determined by factors well known in the art, including system complexity, number of satellites in view, subscriber capacity, degree of diversity chosen, and the like.

5 Each transmit module 334 includes a transmit modulator 326 which spread spectrum modulates data for transmission. Transmit modulator 326 has an output coupled to a digital transmit power controller 328, which controls the transmission power used for the outgoing digital signal. Digital transmit power controller 328 applies a minimum level of power for purposes of interference reduction and resource allocation, but applies appropriate levels of power when needed to compensate for attenuation in the transmission path and other path transfer characteristics. At least one PN generator 332 is used by transmit modulator 326 in spreading the signals. This code generation can also form a functional part of one or more control processors or storage elements used in gateway 122, 124.

10 The output of transmit power controller 328 is transferred to a summer 336 where it is summed with the outputs from other transmit power control circuits. Those outputs are signals for transmission to other user terminals 124, 126 at the same frequency and within the same beam as the output of transmit power controller 328. The output of summer 336 is provided to an analog transmitter 338 for digital-to-analog conversion, conversion to the appropriate RF carrier frequency, further amplification and output to one or more antennas 340 for radiating to user terminals 124, 126. Antennas 310 and 340 may be the same antennas depending on the complexity and configuration of the system.

25 At least one gateway control processor 320 is coupled to receiver modules 324, transmit modules 334, and baseband circuitry 322; these units may be physically separated from each other. Control processor 320 provides command and control signals to effect functions such as, but not limited to, signal processing, timing signal generation, power control, handoff control, diversity combining, and system interfacing. In addition, control processor 320 assigns PN spreading codes, orthogonal code sequences, and specific transmitters and receivers for use in subscriber communications.

Control processor 320 also controls the generation and power of pilot, synchronization, and paging channel signals and their coupling to transmit power controller 328. The pilot channel is simply a signal that is not modulated by data, and may use a constant-value (pattern) or tone-type input to transmit modulator 326, effectively transmitting only the PN spreading codes applied from PN generator 332.

While control processor 320 can be coupled directly to the elements of a module, such as transmit module 324 or receive module 334, each module generally comprises a module-specific processor, such as transmit processor 330 or receive processor 321, which controls the elements of that module. Thus, in a preferred embodiment, control processor 320 is coupled to transmit processor 330 and receive processor 321, as shown in FIG. 3. In this manner, a single control processor 320 can control the operations of a large number of modules and resources more efficiently. Transmit processor 330 controls generation of, and signal power for, pilot, synchronization, paging signals, and traffic channel signals, and their respective coupling to power controller 328. Receiver processor 321 controls searching, PN spreading codes and timing for demodulation, and monitoring received power.

FIG. 4 illustrates the various signals transmitted in communication system 100. Gateway 120 transmits a forward link signal 410 to user terminal 124 via satellite repeater 116. Forward link signal 410 is comprised of an uplink portion 412 from gateway 120 to satellite repeater 116 and a downlink portion 414 from satellite repeater 116 to user terminal 124. User terminal 124 transmits a reverse link signal 420 to gateway 120 via satellite repeater 116. Reverse link signal 420 is comprised of an uplink portion 422 from user terminal 124 to satellite repeater 116 and a downlink portion 424 from satellite repeater 116 to gateway 120.

When user terminal 124 transmits reverse link signal 420 to gateway 120 via satellite repeater 116, uplink portion 422 experiences frequency Doppler as a result of the relative motion between user terminal 124 and satellite repeater 116 (that is, as satellite repeater 116 moves), and downlink portion 424 experiences frequency Doppler as a result of the relative motion between gateway 120 and satellite repeater 116. This Doppler can cause the

demodulation errors described above because it creates a frequency shift that shifts the location of energy in the correlation process.

Modulation Symbol Index Rotation

5 FIG. 5 is a block diagram of a conventional communications system 500. System 500 includes a transmitter 510 and a receiver 530 connected by a channel 520. Channel 520 can be any link that is subject to burst and random errors, including air link, fiber optic, microwave, guided wave, and wireline. The invention compensates for frequency shifts or other error processes that
10 can adversely impact the proper detection of data due to changes in the MSB stored in an Interleaver/Deinterleaver array.

 Transmitter 510 includes an encoder 540, an interleaver 550, and a modulator 560. Receiver 530 includes a demodulator 570, a deinterleaver 580, and a decoder 590. Encoder 540 and decoder 590 employ a coding scheme
15 that compensates for random errors introduced by channel 520. Interleaver 550 and deinterleaver 580 are of the block interleaver type.

 FIG. 6 is a flowchart depicting the operation of transmitter 510 according to conventional methods. Encoder 540 receives information bits 505. Information bits 505 can represent any sort of data, such as a digitized
20 voice signal. Encoder 540 encodes information bits 505 to produce data words 545 using a coding scheme such as Viterbi 1/3 rate coding, as shown in step 602. Interleaver 550 interleaves data words 545 using a well-known block interleaving scheme to produce modulation symbol indices 555, as shown in step 604.

25 Specifically, interleaver 550 includes an array 552 having a number of rows and columns, such as that shown in Table 1. In the described embodiment, each modulation symbol index 555 has 6 bits and Table 1 has 16 rows and 6 columns, yielding 96 cells. Significantly, the number of columns in array 552 is an integer multiple of the number of bits used to
30 form each modulation symbol index 555. Interleaver 550 writes a frame of 96 data word bits into array 552 by column, as is well-known in the relevant arts. Table 1 depicts the locations of the 96 consecutive bits, numbered 1 through 96, immediately after being written to array 552.

Of course, the length of the modulation symbol indices and the dimensions of the array can vary in other embodiments. In those embodiments, the present invention improves performance when data words are written into the array by columns and modulation symbol indices are read from the array by rows where the number of columns in the array of the block interleaver is an integer multiple of the number of bits used to form each modulation symbol index. In those embodiments, the present invention also improves the performance of a digital communications system which uses a block interleaver that writes data words into an array by rows and reads modulation symbol indices from the array by columns where the number of rows in the array of the block interleaver is an integer multiple of the number of bits used to form each modulation symbol index.

	c_0	c_1	c_2	c_3	c_4	c_5
r_0	1	17	33	49	65	81
r_1	2	18	34	50	66	82
r_2	3	19	35	51	67	83
r_3	4	20	36	52	68	84
r_4	5	21	37	53	69	85
r_5	6	22	38	54	70	86
r_6	7	23	39	55	71	87
r_7	8	24	40	56	72	88
r_8	9	25	41	57	73	89
r_9	10	26	42	58	74	90
r_{10}	11	27	43	59	75	91
r_{11}	12	28	44	60	76	92
r_{12}	13	29	45	61	77	93
r_{13}	14	30	46	62	78	94
r_{14}	15	31	47	63	79	95
r_{15}	16	32	48	64	80	96

In one embodiment, interleaver 550 and deinterleaver 580 are block interleavers of the bit-reverse type. Such an interleaver shuffles the rows of the array before the array is read, so that the rows are read out in a different order. According to the bit-reverse technique, the rows are reordered by reversing the order of the bits in the binary row number. For example, row r_3 (binary 0011) becomes row r_{12} (binary 1100). This bit-reverse technique is not required by the present invention. Thus, in other embodiments, interleaver 550 and deinterleaver 580 are not of the bit-reverse type. Table 2 depicts the state of array 552 in interleaver 550 when the bit-reverse operation is complete.

In a preferred embodiment, each modulation symbol index 555 has 6 bits. Thus, interleaver 550 generates each modulation symbol index 555 by reading a row from array 552 depicted in Table 2. Modulator 560 generates modulation symbols 565 based on the modulation symbol indices, as shown in step 608. Modulation symbols 565 are then transmitted over channel 520.

TABLE 2 - Array after Bit Reversal						
	c ₀	c ₁	c ₂	c ₃	c ₄	c ₅
r ₀	1	17	33	49	65	81
r ₁	9	25	41	57	73	89
r ₂	5	21	37	53	69	85
r ₃	13	29	45	61	77	93
r ₄	3	19	35	51	67	83
r ₅	11	27	43	59	75	91
r ₆	7	23	39	55	71	87
r ₇	15	31	47	63	79	95
r ₈	2	18	34	50	66	82
r ₉	10	26	42	58	74	90
r ₁₀	6	22	38	54	70	86
r ₁₁	4	20	36	52	68	84
r ₁₂	12	28	44	60	76	92
r ₁₃	14	30	46	62	78	94
r ₁₄	8	24	40	56	72	88
r ₁₅	16	32	48	64	80	96

For each modulation symbol index 555, modulator 560 generates a modulation symbol 565, as shown in step 608. Each modulation symbol is transmitted across channel 520 to receiver 530. Channel 520 may introduce frequency errors into the signal so that a received modulation symbol 525 may differ from the corresponding transmitted modulation symbol 565 in frequency. Such frequency errors can be introduced due to the relative motion of transmitter 510 and receiver 530, or by the motion of a relay station, such as a relay satellite, with respect to transmitter 510 or receiver 530.

FIG. 7 is a flowchart depicting the operation of receiver 530 according to conventional methods. Demodulator 570 receives modulation symbols 525 from channel 520. As described above, received modulation symbols 520 may be affected by frequency errors introduced by channel 520. Demodulator

570 generates modulation symbol indices 575 based on the received modulation symbols 525, as shown in step 702. The frequency errors introduced by channel 520 may cause demodulator 570 to generate a series of modulation symbol indices 575 that have erroneous MSBs. Deinterleaver 580 then deinterleaves indices 575 to produce data words 585, as shown in step 706.

Indices 575 are written into array 582 of deinterleaver 580. The bit order of the data in array 582 after this operation is as shown in Table 2. The rows are then shuffled to reverse the bit-reverse operation described above. The bit order of the data in array 582 after this operation is as shown in Table 1. Deinterleaver 580 produces data words 585 by reading array 582 by row. From Table 1, it is clear that the MSBs of the modulation symbol indices 575 that were written into array 582 will be read out consecutively. If several of these MSBs are erroneous, data words 585 will contain a burst-type error that decoder 590 will be unable to correct. For purposes of discussion, this problem will be referred to as "modulation symbol MSB alignment," or simply "MSB alignment." Finally, data words 585 are decoded by decoder 570 to produce information bits 595. Because decoder 570 is unable to correct for the burst-type errors introduced by the MSB alignment problem, the corresponding information bits 595 contain errors.

FIG. 8 is a block diagram of a communications system 800 according to a preferred embodiment of the present invention. System 800 operates to prevent the MSB alignment problem described above. System 800 includes a transmitter 810 and a receiver 830 connected by a channel 520. Channel 520 can be any link that is subject to burst and random errors, such as an air link. Transmitter 810 includes an encoder 540, an interleaver 550, a modulation symbol index rotator 840 and a modulator 560. Receiver 830 includes a demodulator 570, a modulation symbol index inverse rotator 850, a deinterleaver 580, and a decoder 590. Encoder 540 and decoder 590 employ a coding scheme that compensates for random errors introduced by channel 520, as described above. Interleaver 550 and deinterleaver 580 are of the block interleaver type, also as described above. Modulation symbol index rotator 840 and modulation symbol index inverse rotator 850 manipulate

modulation symbol indices as described below to mitigate the modulation symbol MSB alignment problem described above.

FIG. 9 is a flowchart depicting the operation of transmitter 810 according to a preferred embodiment of the present invention. Encoder 540 receives information bits 505. Information bits 505 can represent any sort of data, such as a digitized voice signal. Encoder 540 encodes information bits 505 to produce data words 545 using Viterbi 1/3 rate coding, as shown in step 902. Other coding schemes can be used with the present invention, as would be apparent to one skilled in the relevant arts.

Interleaver 550 interleaves data words 545 using bit-reverse block interleaving to produce modulation symbol indices 855, as shown in step 904, and as described above. In a preferred embodiment, the modulation symbols are Walsh symbols, each having 64 chips. Other symbol lengths are usable depending on system designs, as is well known. The chip duration is selected according to considerations well-known in the relevant arts.

Specifically, interleaver 550 includes an array 552 having a number of rows and columns, such as that shown in Table 1 above. Table 1 has 16 rows and 6 columns, yielding 96 cells. Significantly, the number of columns in array 552 is an integer multiple of the number of bits used to form each modulation symbol index 855. Interleaver 550 writes a frame of 96 data word bits into array 552 by column, as is well-known in the relevant arts. Table 1 depicts the locations of the 96 consecutive bits, numbered 1 through 96, immediately after being written to array 552.

As described above, interleaver 550 and deinterleaver 580 are block interleavers of the bit-reverse type. Table 2, shown above, depicts the state of array 552 in interleaver 550 when the bit-reverse operation is complete. In system 800, each modulation symbol index 855 has 6 bits. Thus, interleaver 550 generates each modulation symbol index 855 by reading a row from array 552 depicted in Table 2.

Modulation symbol index rotator 840 receives modulation symbol indices 855 and manipulates at least some of the indices in a predetermined manner, as shown in step 906. This manipulation is performed to prevent the alignment of the MSBs of the demodulated modulation symbol indices

in deinterleaver 580. In a preferred embodiment, this manipulation includes rotating the bits of each modulation symbol index by the a number of bit positions in accordance with the row number that index occupied in array 552 of interleaver 550. For example, referring to Table 2, the modulation symbol index in row r_0 is rotated zero bit positions; that is, the index is not rotated. The modulation symbol index in row r_1 is rotated by one bit position to the right, the modulation symbol index in row r_2 is rotated by two bit positions to the right, and so on. Of course, equivalent rotations to the left can be used, as is well-known. Because each modulation symbol index has six bits, the rotation of row r_6 by six bit positions has no effect, and can be omitted. Similarly, the rotation of row r_7 by seven bits has the same effect as a one-bit rotation. Therefore, row r_7 need only be rotated to the right by one bit. These concepts are easily extended to indices of different bit lengths and tables of different dimensions, as would be apparent to one skilled in the relevant arts. In addition, other types of manipulations can be employed to prevent MSB alignment without departing from the spirit and scope of the present invention.

In one embodiment, modulation symbol index rotator 840 is not a separate unit, but rather is included within interleaver 550. In this embodiment, the modulation symbol indices are manipulated within interleaver 550. Table 3 depicts the state of array 552 within interleaver 550 following the rotation operation.

TABLE 3 - Array after modulation symbol Rotation						
	c_0	c_1	c_2	c_3	c_4	c_5
r_0	1	17	33	49	65	81
r_1	89	9	25	41	57	73
r_2	69	85	5	21	37	53
r_3	61	77	93	13	29	45
r_4	35	51	67	83	3	19
r_5	27	43	59	75	91	11
r_6	7	23	39	55	71	87
r_7	95	15	31	47	63	79
r_8	66	82	2	18	34	50
r_9	58	74	90	10	26	42
r_{10}	38	54	70	86	6	22
r_{11}	20	36	52	68	84	4
r_{12}	12	28	44	60	76	92
r_{13}	94	14	30	46	62	78
r_{14}	72	88	8	24	40	56
r_{15}	64	80	96	16	32	48

Modulator 560 generates modulation symbols based on the modulation symbol indices, as shown in step 908. For each six-bit modulation symbol index, modulator 560 generates one of 64 64-bit modulation symbols. These modulation symbols are then transmitted over channel 520.

FIG. 10 is a flowchart depicting the operation of receiver 830 according to a preferred embodiment of the present invention. Demodulator 570 receives modulation symbols from channel 520 and generates modulation symbol indices 875 based on the received modulation symbols, as shown in step 1002. Demodulator 570 decides which modulation symbol has been received by simultaneously correlating the received modulation symbol

with all 64 possible modulation symbols. This correlation produces 64 energies: one for each correlation. The correlation energy having the highest energy level indicates the most likely correlation.

Modulation symbol index inverse rotator 850 receives modulation
5 symbol indices 875 and performs an inverse rotation operation that reverses the effects of the rotation operation performed by modulation symbol index rotator 840, as shown in step 1004. The results are written to deinterleaver 580. The state of array 552 within interleaver 580 at this point is as shown in Table 2. Deinterleaver 580 deinterleaves the modulation symbol indices to
10 produce data words 585, as shown in step 1006. Decoder 590 decodes data words 585 to produce information bits 595, as shown in step 1008.

In the embodiment described above, nearly all of the modulation symbol indices are rotated. However, in other embodiments, fewer modulation symbol indices may be rotated, and by different amounts. For
15 example, only one preselected index, or every second or third index, or even a pseudo random selection of indices from among the indices may be rotated. Other rotation patterns are also possible depending on the amount of rotation desired to provide the advantages of the invention. Of course, complementary inverse rotation patterns are applied in these embodiments
20 in the receiver.

The previous description of the preferred embodiments is provided to enable any person skilled in the art to make or use the present invention. The various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be
25 applied to other embodiments without the use of the inventive faculty. Thus, the present invention is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

30 What is Claimed is:

CLAIMS

1. An apparatus for improving the performance of a digital
2 communications system which uses a block interleaver that writes data
words into an array by columns and reads modulation symbol indices from
4 the array by rows where the number of columns in the array of the block
interleaver is an integer multiple of the number of bits used to form each
6 modulation symbol index, comprising:

means for receiving from the array a plurality of modulation symbol
8 indices;

means for modifying one of said modulation symbol indices in a
10 predetermined manner to produce a modified modulation symbol index so
that the most significant bit of said modified modulation symbol index does
12 not occupy the same bit position as the most significant bit of adjacent ones
of said modulation symbol indices; and

14 means for sending said modified modulation symbol index to a
modulator.

2. The apparatus of claim 1, further comprising means for
2 modifying at least a further one of said modulation symbol indices in a
predetermined manner to produce at least one further modified modulation
4 symbol index so that the most significant bit of said at least one further
modified modulation symbol index does not occupy the same bit position as
6 the most significant bit of adjacent ones of said modulation symbol indices.

3. The apparatus of claim 1, wherein said means for modifying
2 comprises means for rotating the bits of said one of said modulation symbol
indices.

4. The apparatus of claim 3, wherein said means for rotating
2 comprises means for rotating the bits of said one of said modulation symbol
indices by a number of bit positions in accordance with the row number in
4 the array occupied by said one of said modulation symbol indices.

5. The apparatus of claim 1, further comprising a block interleaver
2 that writes data words into an array by columns and reads modulation
symbol indices from said array by rows where the number of columns in
4 said array is an integer multiple of the number of bits used to form each
modulation symbol index.

6. The apparatus of claim 5, further comprising an encoder that
2 encodes information bits to produce said data words where said encoder
mitigates random channel errors.

7. The apparatus of claim 6, wherein said encoder is a Viterbi rate
2 1/3 convolutional encoder.

8. The apparatus of claim 6, further comprising a modulator that
2 generates modulation symbols based on said modulation symbol indices.

9. The apparatus of claim 8, wherein each of said modulation
2 symbols is one of a set of orthogonal modulation functions.

10. The apparatus of claim 9, wherein said orthogonal modulation
2 functions are Walsh functions.

11. An apparatus for improving the performance of a digital
2 communications system which uses a block deinterleaver that writes
modulation symbol indices into an array by rows and reads data words from
4 the array by columns where the number of columns in the array of the block
interleaver is an integer multiple of the number of bits used to form each
6 modulation symbol index, comprising:

means for receiving from a demodulator a plurality of modulation
8 symbol indices where the most significant bits of adjacent ones of said
modulations symbol indices do not occupy the same bit position;

10 means for modifying one of said modulation symbol indices in a
predetermined manner to produce a modified modulation symbol index so
12 that the most significant bit of said modified modulation symbol index
occupies the same bit position as the most significant bit of adjacent ones of
14 said modulation symbol indices; and

means for sending said modified modulation symbol index to the
16 array.

12. The apparatus of claim 11, further comprising means for
2 modifying at least a further one of said modulation symbol indices in a
predetermined manner to produce at least one further modified modulation
4 symbol index so that the most significant bit of said at least one further
modified modulation symbol index does not occupy the same bit position as
6 the most significant bit of adjacent ones of said modulation symbol indices.

13. The apparatus of claim 11, wherein said means for modifying
2 comprises means for rotating the bits of said one of said modulation symbol
indices.

14. The apparatus of claim 13, wherein said means for rotating
2 comprises means for rotating the bits of said one of said modulation symbol
indices by a number of bit positions in accordance with the row number in
4 the array to be occupied by said one of said modulation symbol indices.

15. The apparatus of claim 11, further comprising a block
2 deinterleaver that writes modulation symbol indices into an array by rows
and reads data words from said array by columns where the number of
4 columns in said array is an integer multiple of the number of bits used to
form each modulation symbol index.

16. The apparatus of claim 15, further comprising a decoder that
2 decodes said data words to produce information bits where said decoder
mitigates random channel errors.

17. The apparatus of claim 16, wherein said decoder is a Viterbi rate
2 1/3 convolutional decoder.

18. The apparatus of claim 16, further comprising a demodulator
2 that generates said modulation symbol indices based on modulation
symbols.

19. The apparatus of claim 18, wherein each of said modulation
2 symbols is one of a set of orthogonal modulation functions.

20. The apparatus of claim 19, wherein said orthogonal
2 modulation functions are Walsh functions.

21. A method for improving the performance of a digital
2 communications system which uses a block interleaver that writes data
words into an array by columns and reads modulation symbol indices from
4 the array by rows where the number of columns in the array of the block
interleaver is an integer multiple of the number of bits used to form each
6 modulation symbol index, comprising the steps of:
receiving from the array a plurality of modulation symbol indices;
8 modifying one of said modulation symbol indices in a predetermined
manner to produce a modified modulation symbol index so that the most
10 significant bit of said modified modulation symbol index does not occupy
the same bit position as the most significant bit of adjacent ones of said
12 modulation symbol indices; and
sending said modified modulation symbol index to a modulator.

22. The method of claim 21, further comprising the step of
2 modifying at least a further one of said modulation symbol indices in a
predetermined manner to produce at least one further modified modulation
4 symbol index so that the most significant bit of said at least one further

modified modulation symbol index does not occupy the same bit position as
6 the most significant bit of adjacent ones of said modulation symbol indices.

23. The method of claim 21, wherein said modifying step
2 comprises the step of rotating the bits of said one of said modulation symbol
indices.

24. The method of claim 23, wherein said rotating step comprises
2 the step of rotating the bits of said one of said modulation symbol indices by
a number of bit positions in accordance with the row number in the array
4 occupied by said one of said modulation symbol indices.

25. The method of claim 21, further comprising the step of
2 interleaving data words to produce said modulation symbol indices using a
block interleaver where the number of columns of said block interleaver is
4 an integer multiple of the number of bits used to form each of said
modulation symbol indices.

26. The method of claim 25, further comprising the step of
2 encoding information bits to produce said data words using an encoder that
mitigates random channel errors.

27. The method of claim 26, wherein said encoder is a Viterbi rate
2 1/3 convolutional encoder.

28. The method of claim 26, further comprising the step of
2 generating modulation symbols based on said modulation symbol indices.

29. The method of claim 28, wherein each of said modulation
2 symbols is one of a set of orthogonal modulation functions.

30. The method of claim 29, wherein said orthogonal modulation
2 functions are Walsh functions.

31. A method for improving the performance of a digital
2 communications system which uses a block deinterleaver that writes
modulation symbol indices into an array by rows and reads data words from
4 the array by columns where the number of columns in the array of the block
deinterleaver is an integer multiple of the number of bits used to form each
6 modulation symbol index, comprising the steps of:

receiving from a demodulator a plurality of modulation symbol
8 indices where the most significant bits of adjacent ones of said modulations
symbol indices do not occupy the same bit position;

10 modifying one of said modulation symbol indices in a predetermined
manner to produce a modified modulation symbol index so that the most
12 significant bit of said modified modulation symbol index occupies the same
bit position as the most significant bit of adjacent ones of said modulation
14 symbol indices; and

sending said modified modulation symbol index to the array.

32. The method of claim 31, further comprising the step of
2 modifying at least a further one of said modulation symbol indices in a
predetermined manner to produce at least one further modified modulation
4 symbol index so that the most significant bit of said at least one further
modified modulation symbol index occupies the same bit position as the
6 most significant bit of adjacent ones of said modulation symbol indices.

33. The method of claim 31, wherein said modifying step
2 comprises the step of rotating the bits of said one of said modulation symbol
indices.

34. The method of claim 33, wherein said rotating step comprises
2 the step of rotating the bits of said one of said modulation symbol indices by
a number of bit positions in accordance with the row number in the array to
4 be occupied by said one of said modulation symbol indices.

35. The method of claim 31, further comprising the step of
2 deinterleaving said modulation symbol indices to produce data words using
a block deinterleaver where the number of columns of said block
4 deinterleaver is an integer multiple of the number of bits used to form each
of said modulation symbol indices.

36. The method of claim 35, further comprising the step of
2 decoding said data words to produce information bits using a decoder that
mitigates random channel errors.

37. The method of claim 36, wherein said decoder is a Viterbi rate
2 1/3 convolutional decoder.

38. The method of claim 36, further comprising the step of
2 generating said modulation symbol indices based on modulation symbols.

39. The method of claim 38, wherein each of said modulation
2 symbols is one of a set of orthogonal modulation functions.

40. The method of claim 39, wherein said orthogonal modulation
2 functions are Walsh functions.

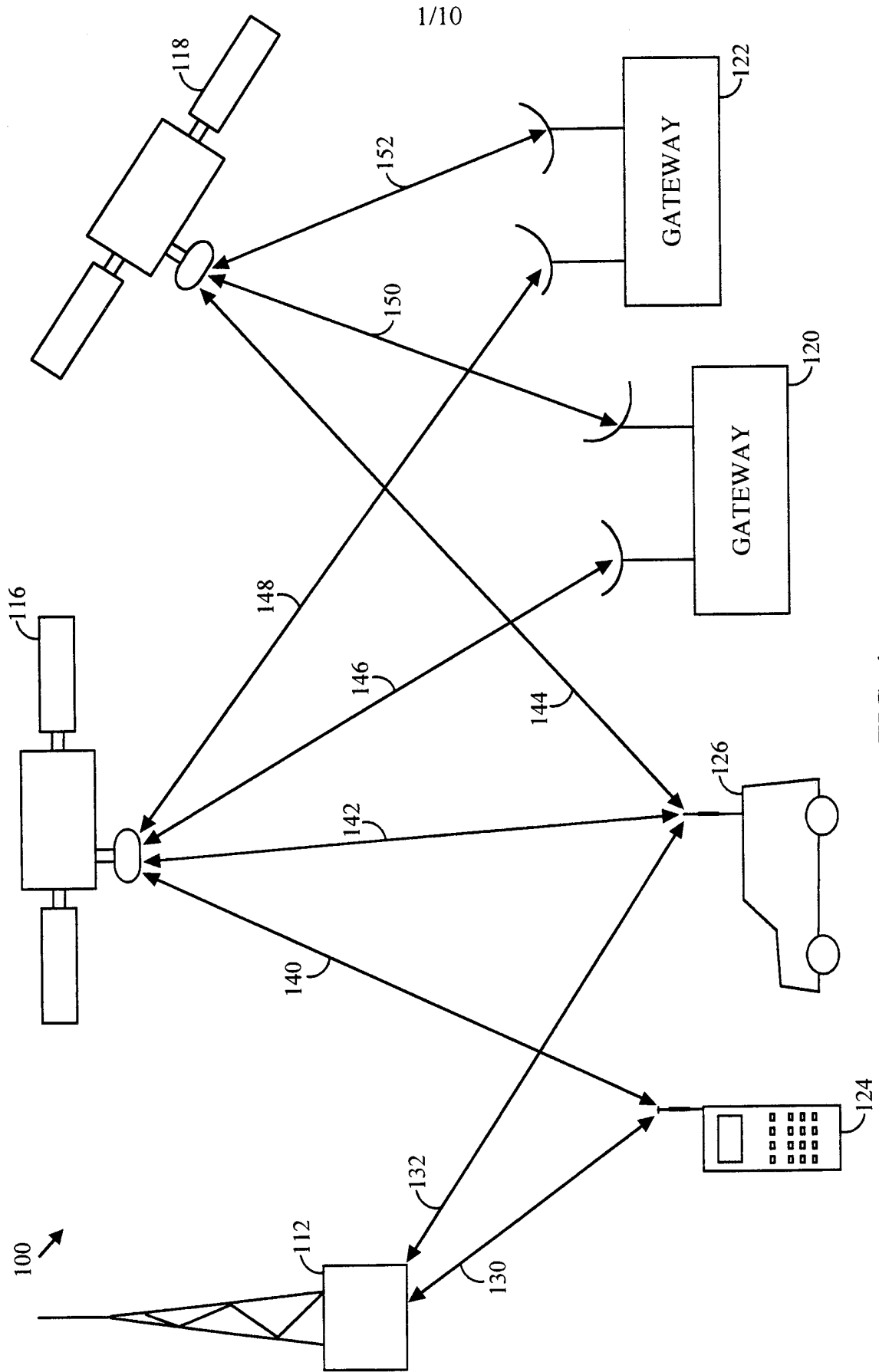


FIG. 1

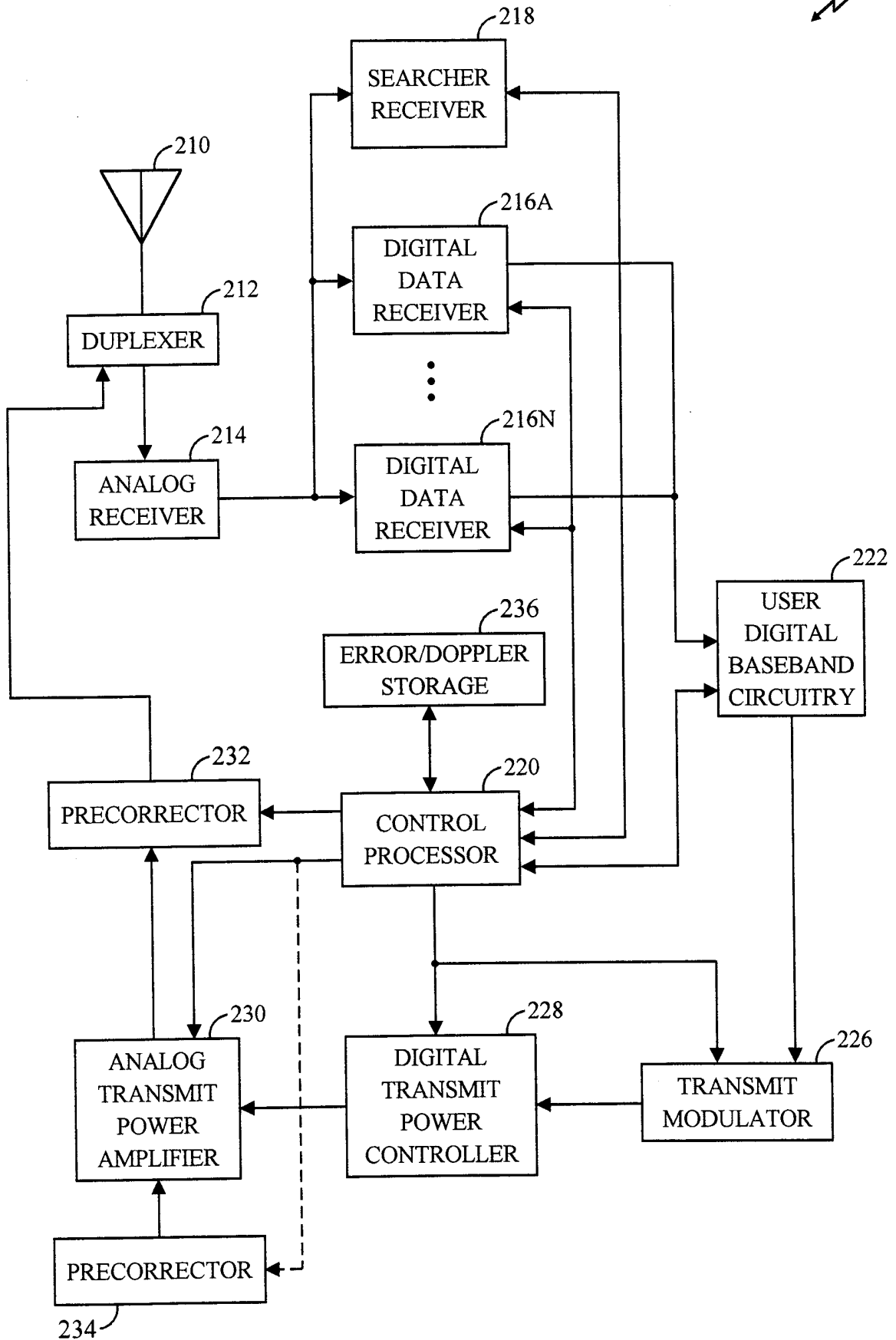


FIG. 2

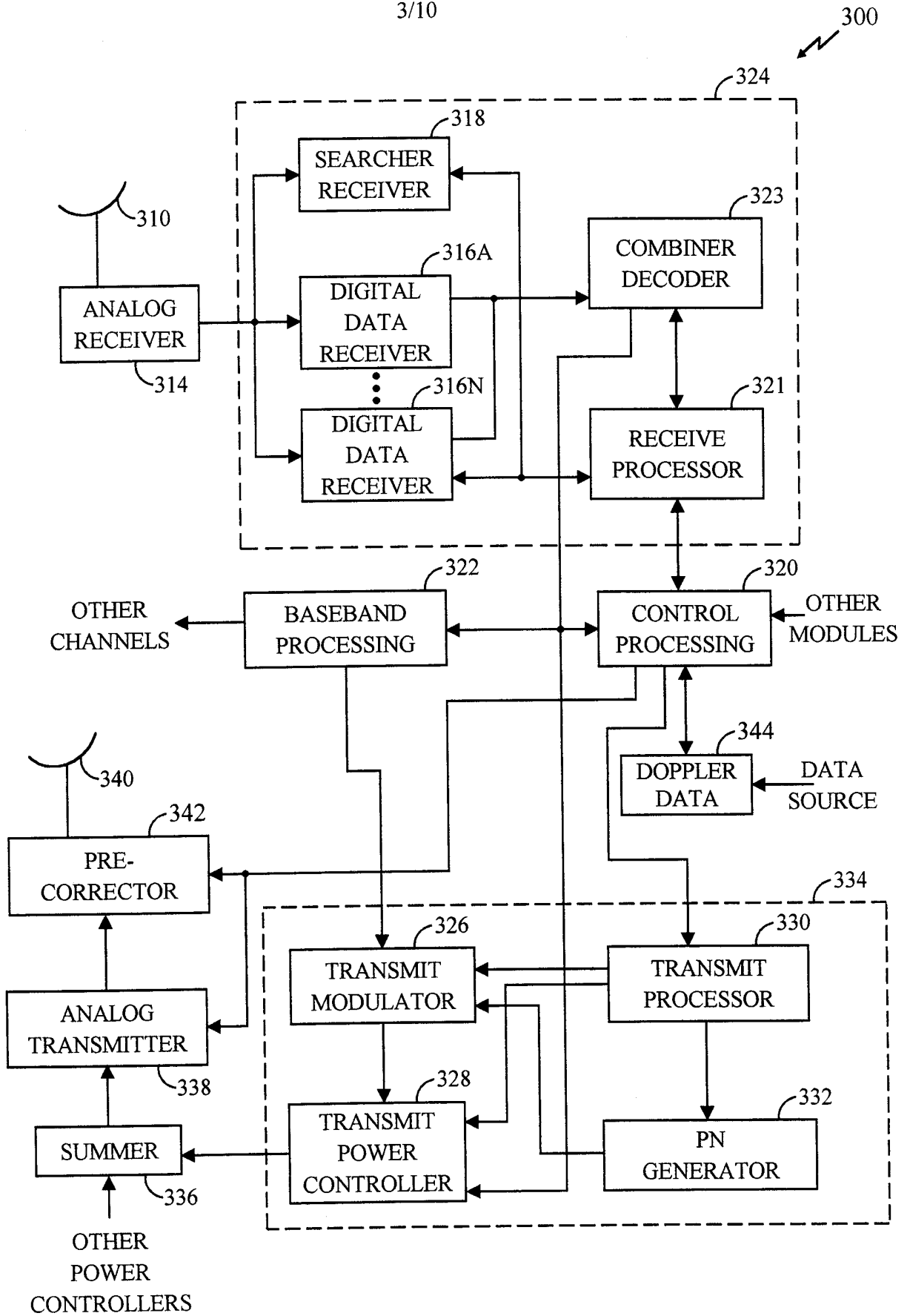


FIG. 3
SUBSTITUTE SHEET (RULE 26)

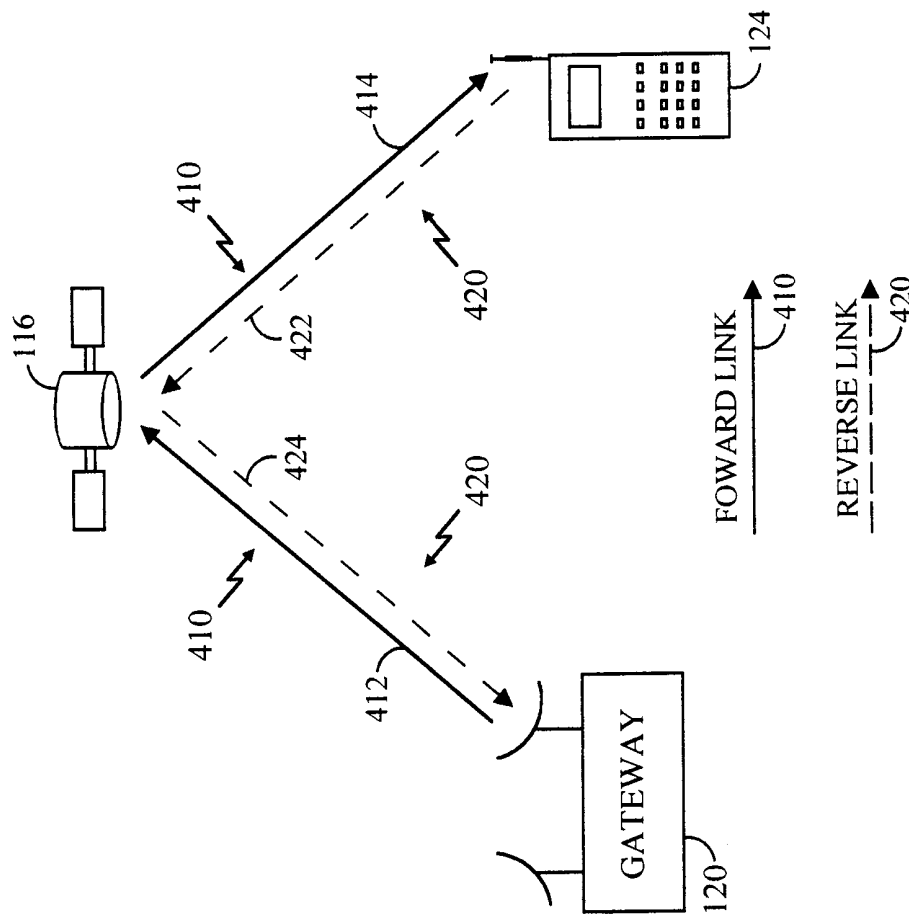


FIG. 4

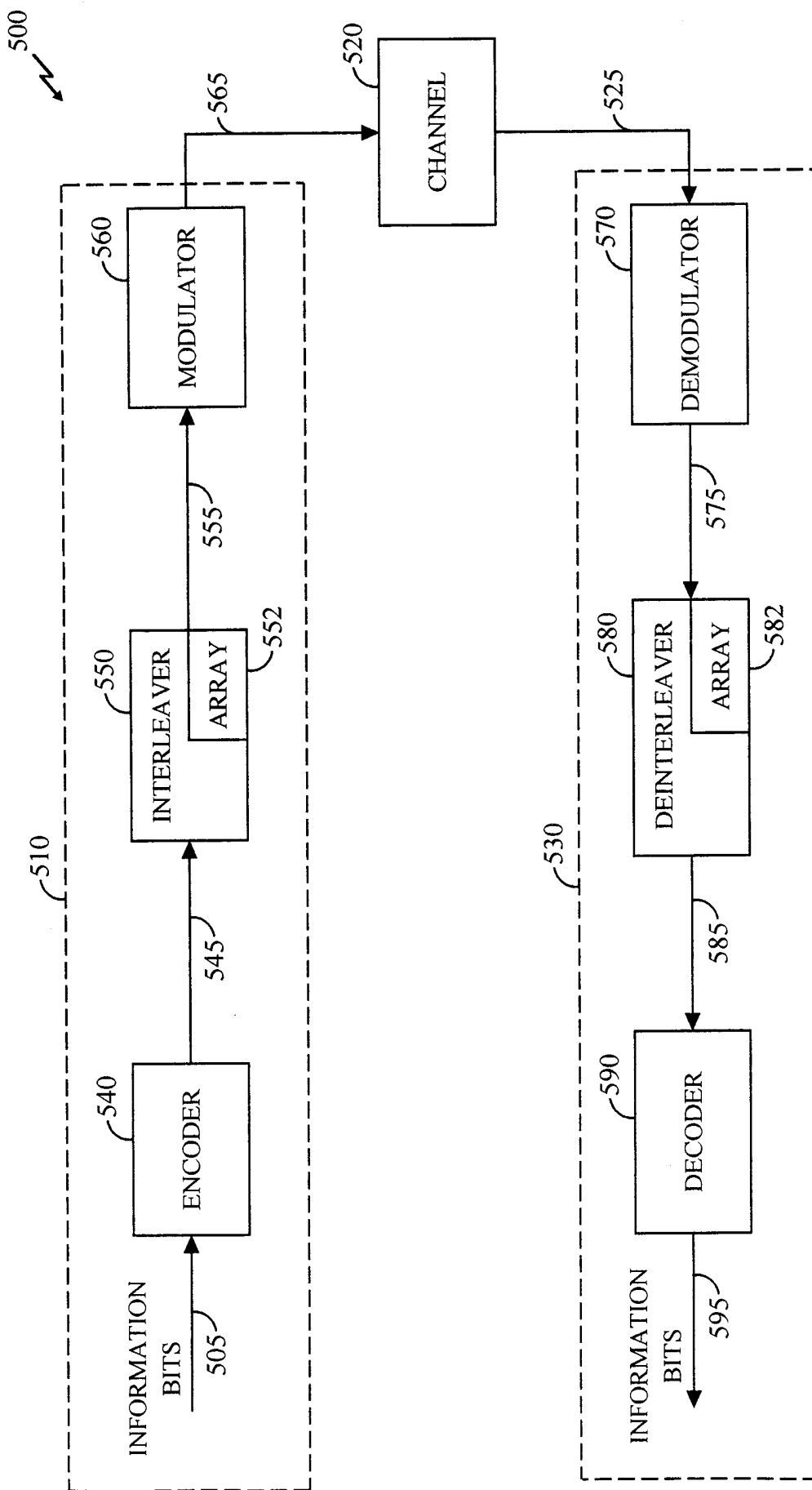


FIG. 5

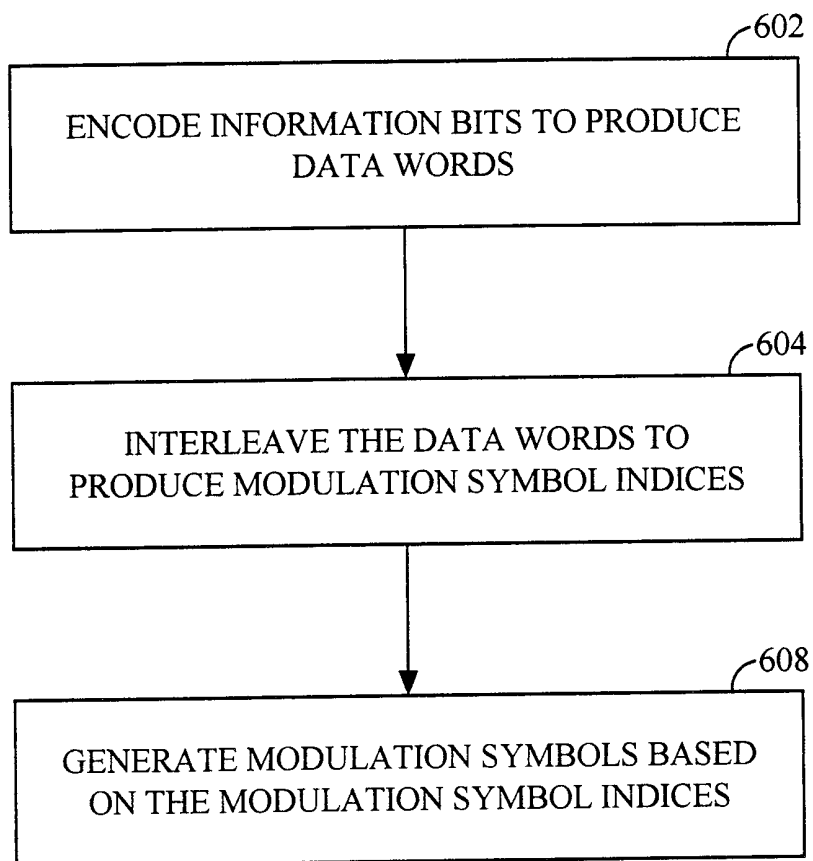


FIG. 6

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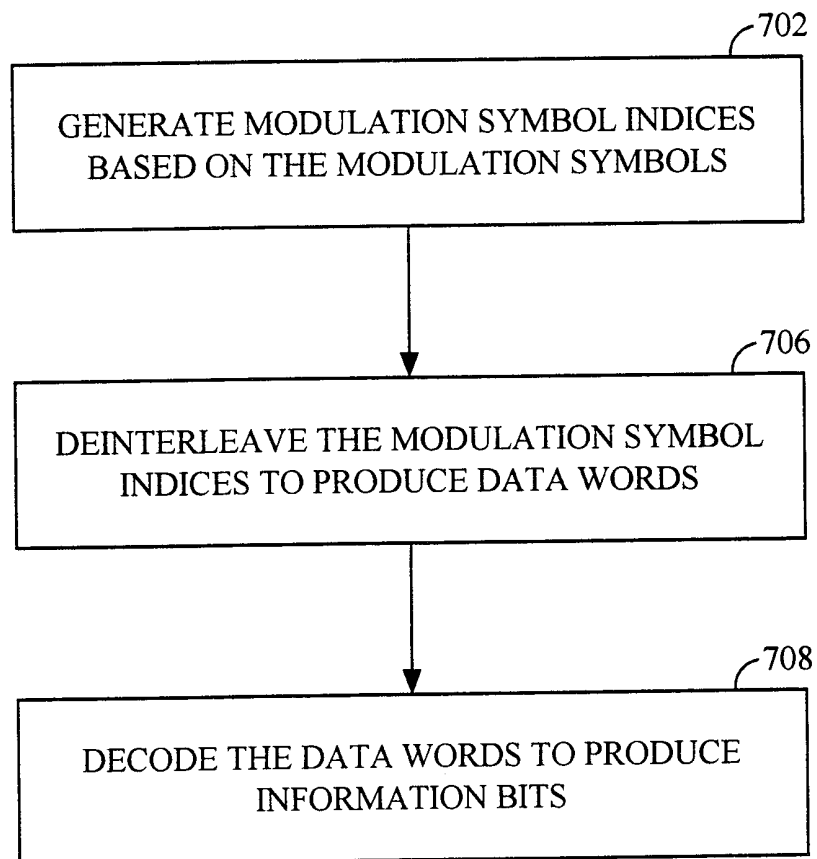


FIG. 7

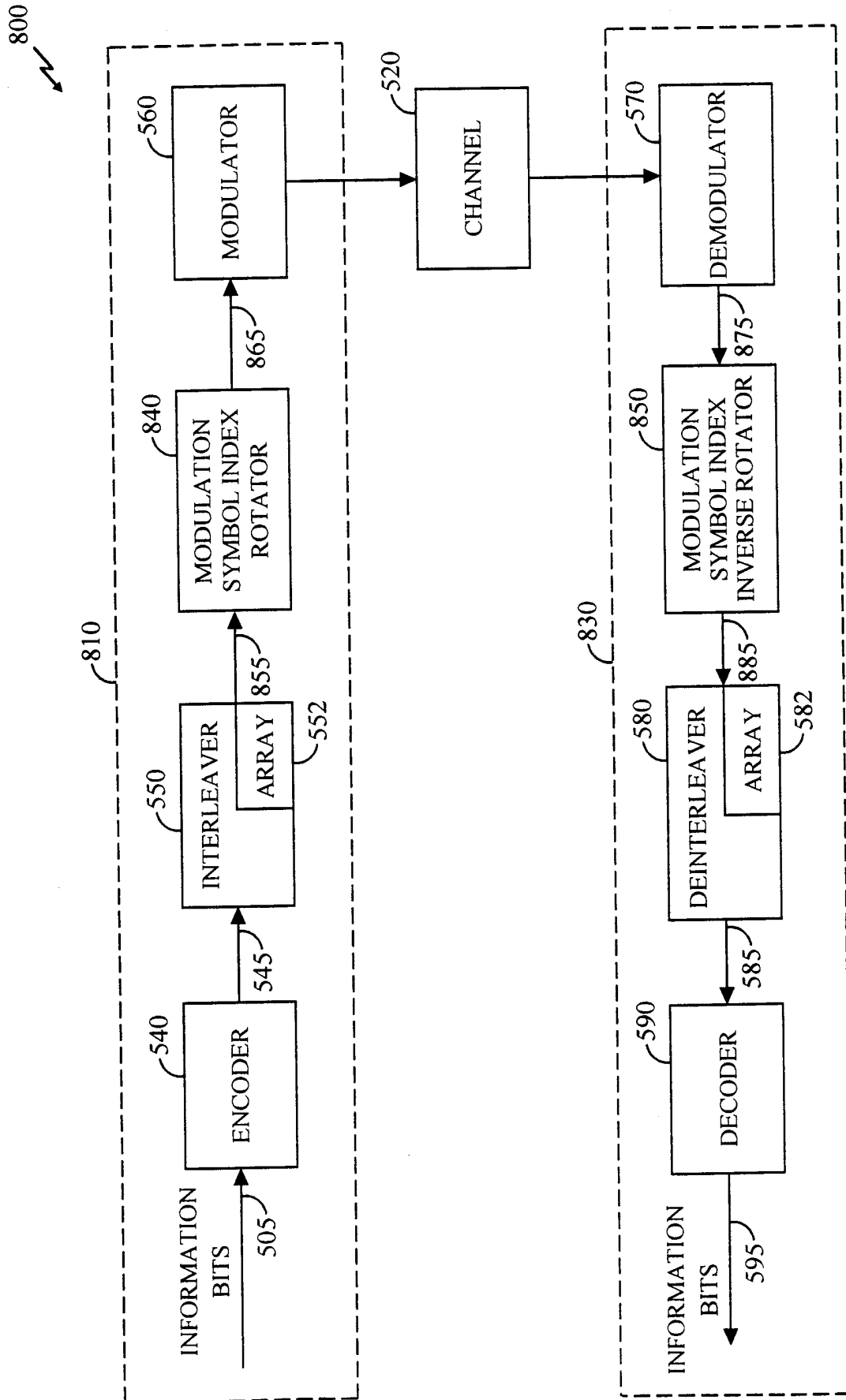


FIG. 8

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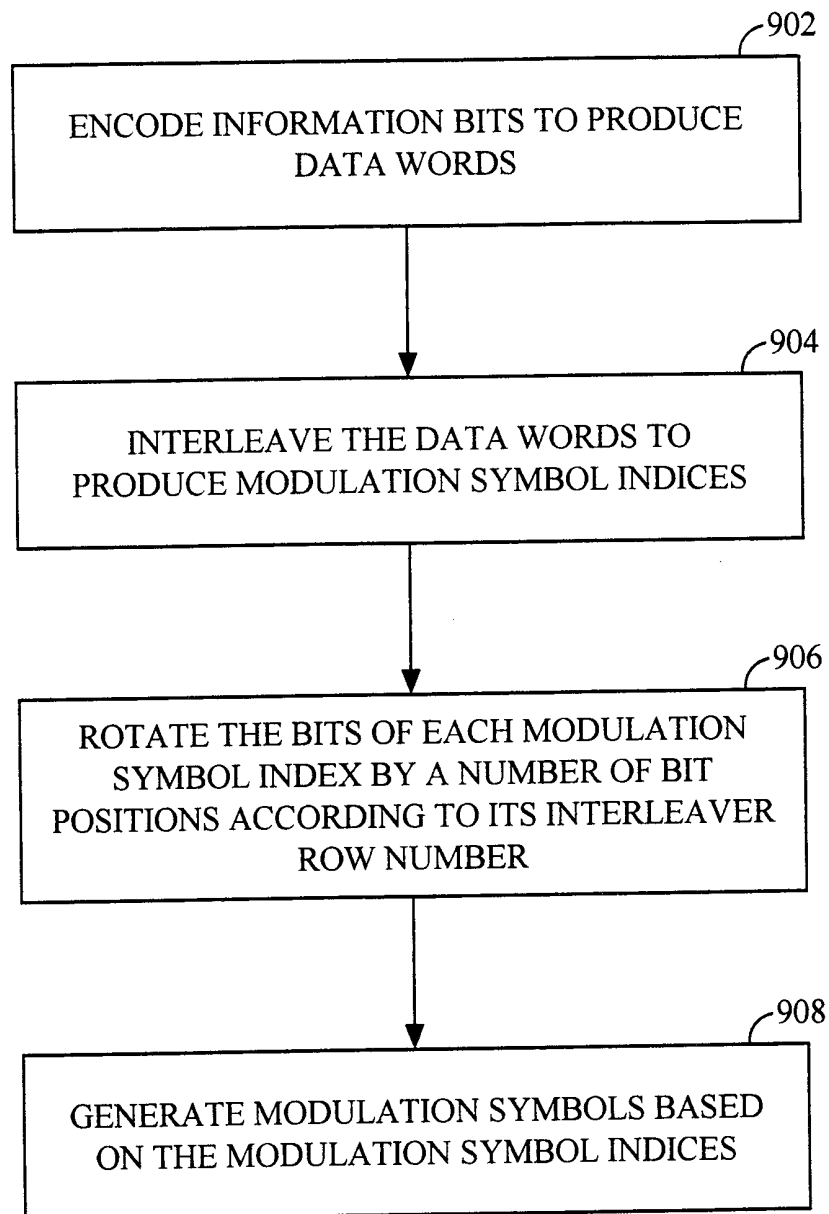


FIG. 9

10/10

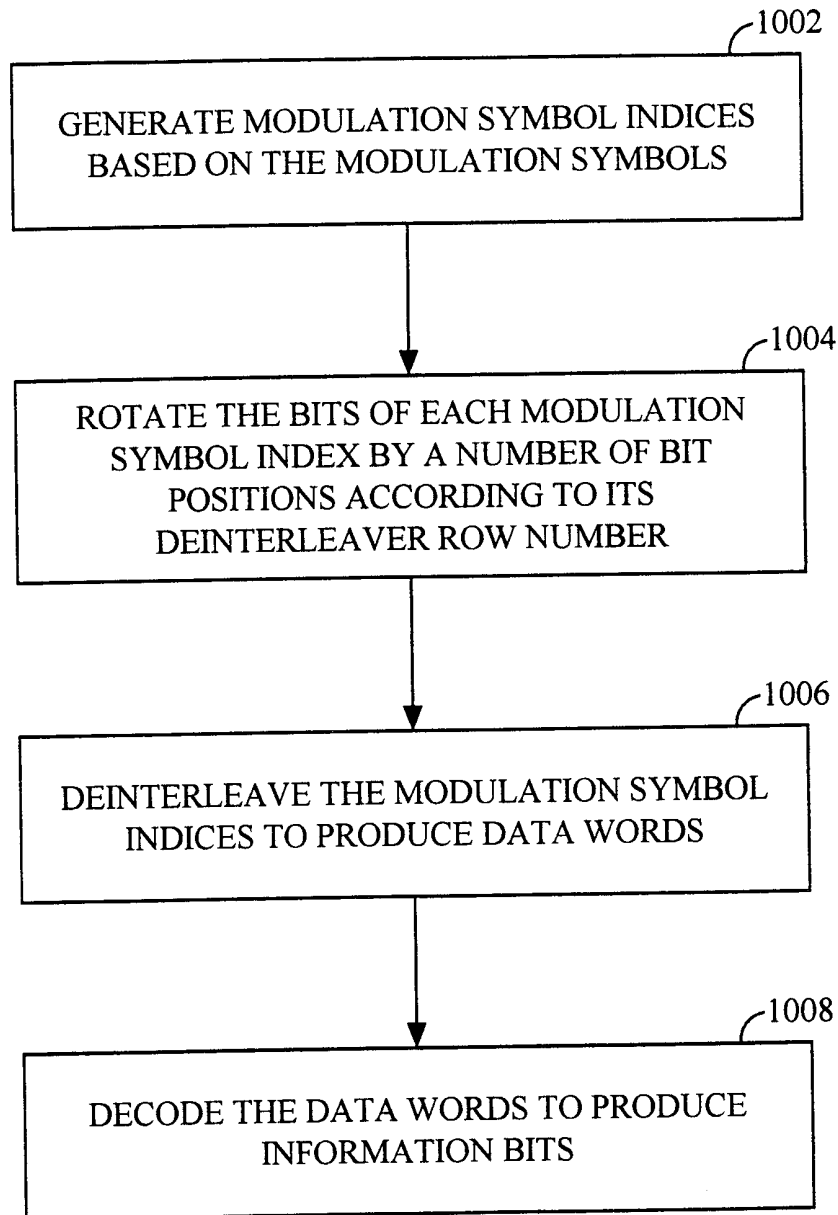


FIG. 10

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 99/17835

A. CLASSIFICATION OF SUBJECT MATTER IPC 7 H03M13/27 H04L5/02 H04B1/707 H03M13/00		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols) IPC 7 H03M H04L H04B		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practical, search terms used)		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 159 608 A (FALCONER DAVID D ET AL) 27 October 1992 (1992-10-27) the whole document	1-40
A	WO 95 18489 A (ZENITH ELECTRONICS CORP) 6 July 1995 (1995-07-06) page 12, line 24 -page 15, line 29; figures 5-8	1-3, 5, 6, 11-13, 15, 16, 21-23, 25, 26, 31-33, 35, 36
A	US 5 263 051 A (EYUBOGLU M VEDAT) 16 November 1993 (1993-11-16) -/-	
<input checked="" type="checkbox"/> Further documents are listed in the continuation of box C.		
<input checked="" type="checkbox"/> Patent family members are listed in annex.		
* Special categories of cited documents :		
"A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed		"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art. "&" document member of the same patent family
Date of the actual completion of the international search 25 November 1999		Date of mailing of the international search report 03/12/1999
Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016		Authorized officer Devergranne, C

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 99/17835

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 483 541 A (LINSKY STUART T) 9 January 1996 (1996-01-09) <hr/>	

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Information on patent family members

International Application No
PCT/US 99/17835

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