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(54) **DEVICE WITH SELF ALIGNED STRESSOR AND METHOD OF MAKING SAME**

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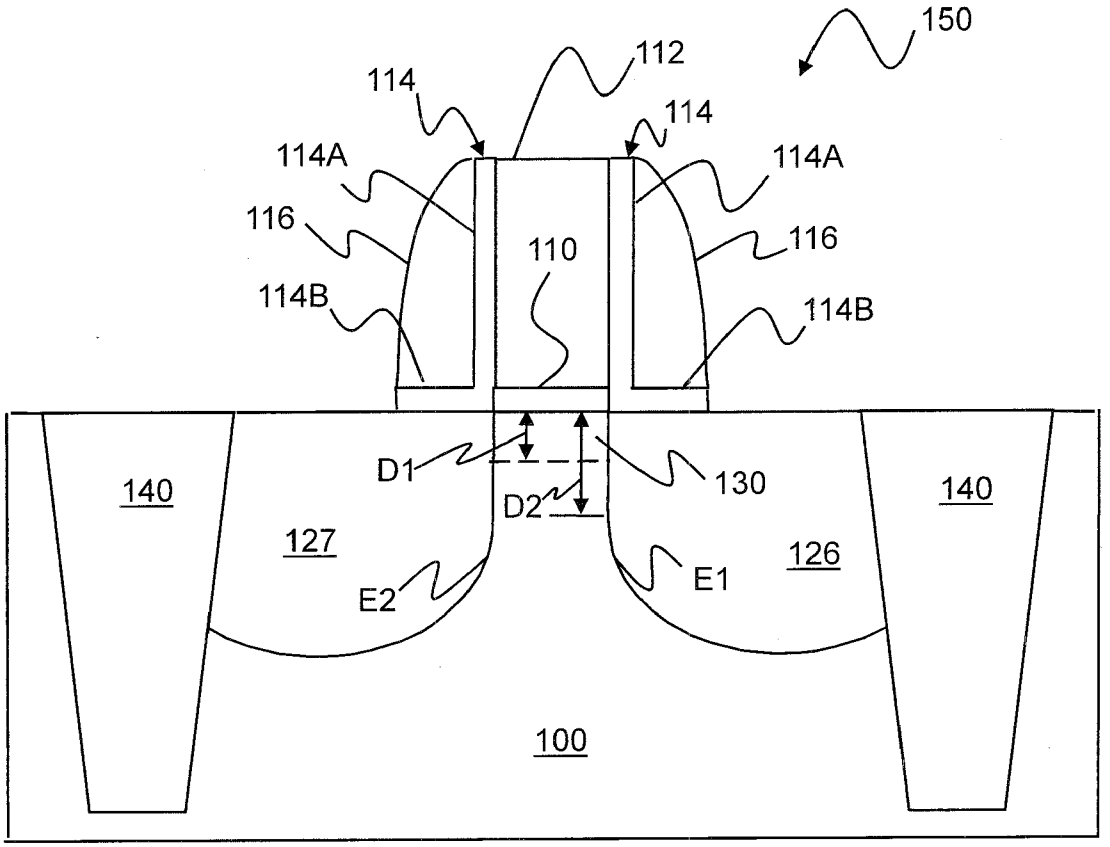
USPC **257/77**; 257/192

(57) **ABSTRACT**

A method includes providing a substrate comprising a substrate material, a gate dielectric film above the substrate, and a first spacer adjacent the gate dielectric film. The spacer has a first portion in contact with a surface of the substrate and a second portion in contact with a side of the gate dielectric film. A recess is formed in a region of the substrate adjacent to the spacer. The recess is defined by a first sidewall of the substrate material. At least a portion of the first sidewall underlies at least a portion of the spacer. The substrate material beneath the first portion of the spacer is reflowed, so that a top portion of the first sidewall of the substrate material defining the recess is substantially aligned with a boundary between the gate dielectric film and the spacer. The recess is filled with a stressor material.



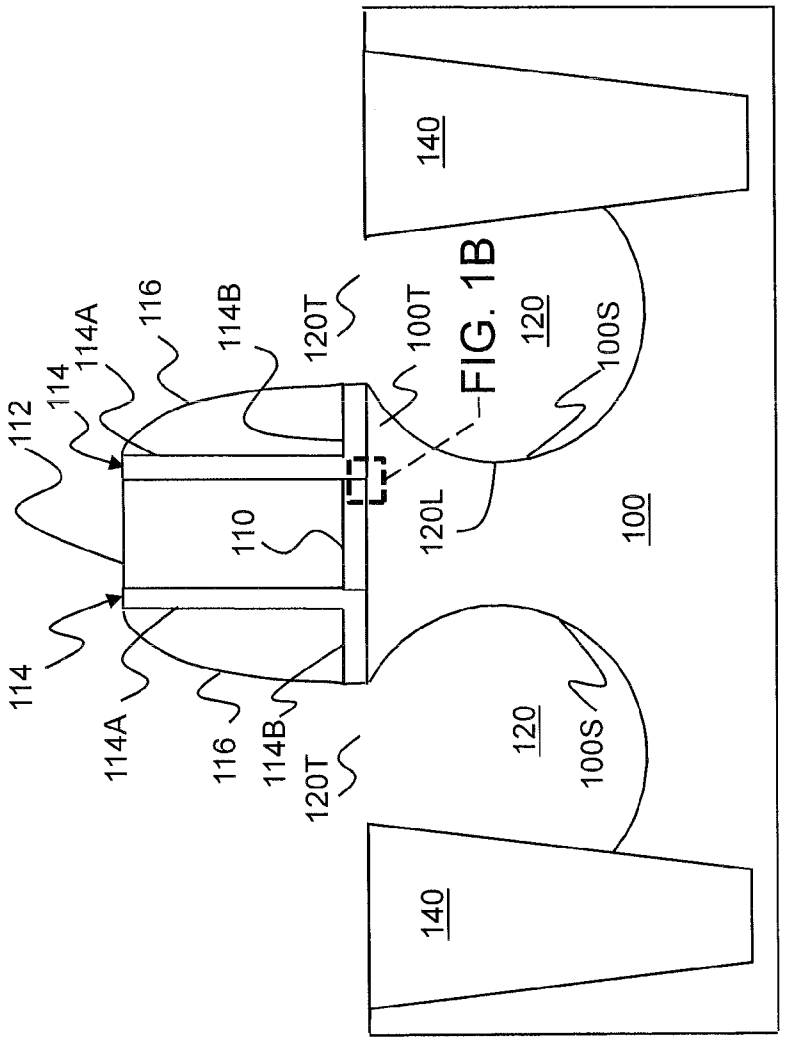

140
112
114
114A
116
114B
120T
100T
120
100S
110
120L
100
114
114A
116
114B
120T
120
100S
140

FIG. 1B

FIG. 1A

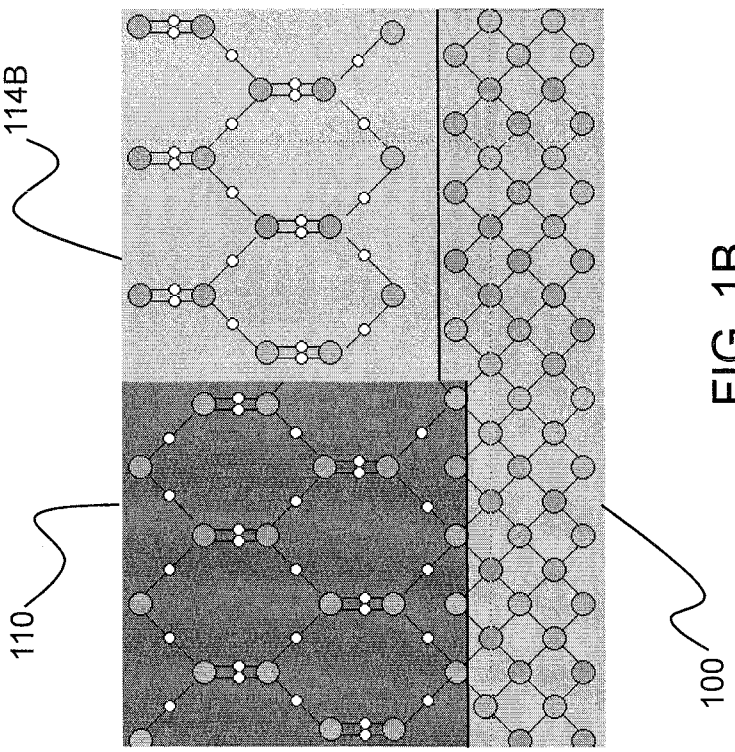


FIG. 1B

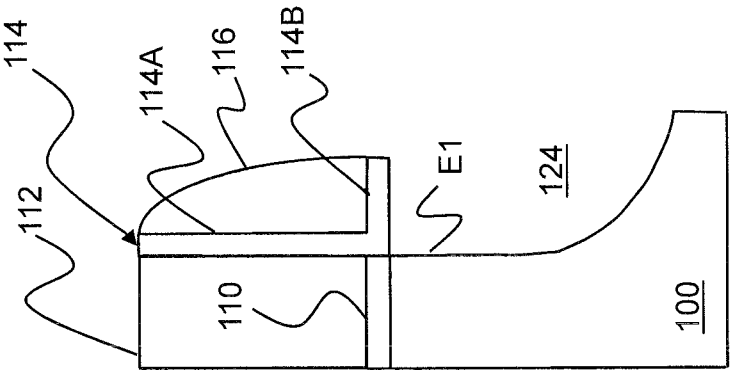

114
114A
116
114B
112
E1
124
110
100

FIG. 3

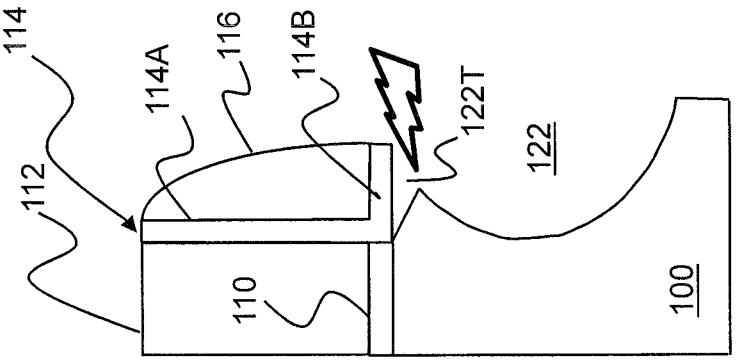

114
114A
116
114B
122T
112
122
110
100

FIG. 2

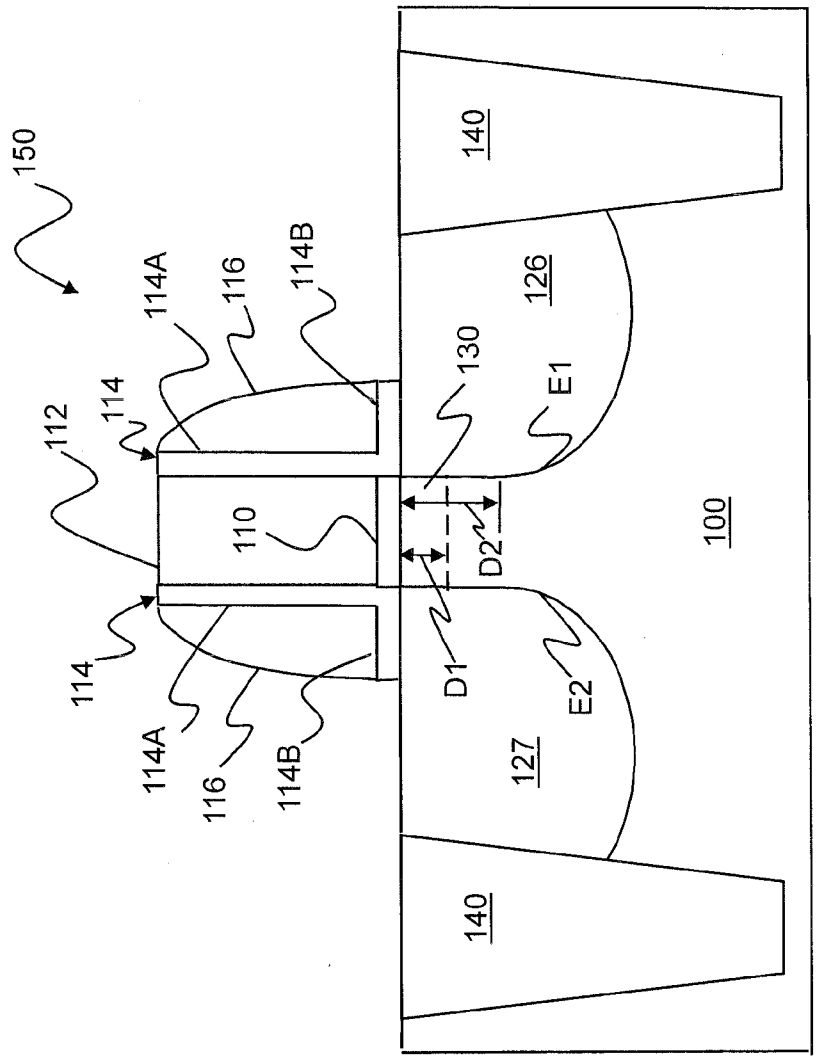


FIG. 4

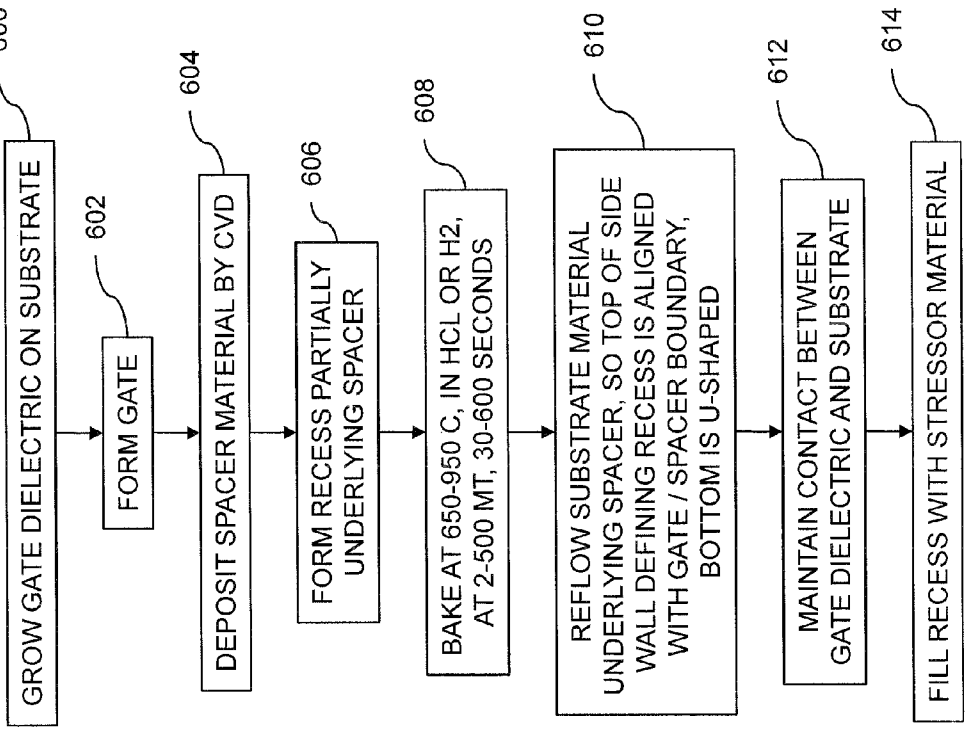

600
GROW GATE DIELECTRIC ON SUBSTRATE
602
FORM GATE
604
DEPOSIT SPACER MATERIAL BY CVD
606
FORM RECESS PARTIALLY UNDERLYING SPACER
608
BAKE AT 650-950 C, IN HCL OR H2, AT 2-500 MT, 30-600 SECONDS
610
REFLOW SUBSTRATE MATERIAL UNDERLYING SPACER, SO TOP OF SIDE WALL DEFINING RECESS IS ALIGNED WITH GATE / SPACER BOUNDARY, BOTTOM IS U-SHAPED
612
MAINTAIN CONTACT BETWEEN GATE DIELECTRIC AND SUBSTRATE
614
FILL RECESS WITH STRESSOR MATERIAL

FIG. 5

DEVICE WITH SELF ALIGNED STRESSOR AND METHOD OF MAKING SAME

[0001] This application is a division of U.S. patent application Ser. No. 12/572,743, filed Oct. 2, 2009, which is expressly incorporated by reference herein in its entirety.

FIELD OF THE INVENTION

[0002] The present disclosure relates to semiconductor fabrication generally, and more particularly to methods of making devices with stressors.

BACKGROUND

[0003] The continued development of metal-oxide-semiconductor field-effect transistors (MOSFET) has improved the speed, density, and cost per unit function of integrated circuits. One way to improve transistor performance is through selective application of stress to the transistor channel region. Stress distorts or strains the semiconductor crystal lattice, which affects the band alignment and charge transport properties of the semiconductor. By controlling the magnitude and distribution of stress in a finished device, manufacturers can increase carrier mobility and improve device performance. There are several existing approaches of introducing stress in the transistor channel region.

[0004] In U.S. Pat. No. 7,494,884, assigned to Taiwan Semiconductor Manufacturing Co., Ltd., MOS transistors have localized stressors for improving carrier mobility. A gate electrode is formed over a substrate. A carrier channel region is provided in the substrate under the gate electrode. Source/drain regions are provided on each side of the carrier channel region. The source/drain regions include an embedded stressor having a lattice spacing different from the substrate. The substrate is silicon and the embedded stressor is SiGe (for PMOS) or SiC (for NMOS). An epitaxy process that includes using HCl gas selectively forms a stressor layer within the crystalline source/drain regions and not on polycrystalline regions of the structure. In a PMOS transistor, the embedded SiGe stressor applies a compressive strain to channel region. In an NMOS transistor, the embedded stressor comprises SiC, and it applies a tensile strain to the transistor channel region.

[0005] The conventional process taught by U.S. Pat. No. 7,494,884 forms sidewall spacers on opposite sides of the gate electrode and gate dielectric. The sidewall spacers serve as self aligning masks for performing one or more ion implants within the source/drain regions. The embedded stressor regions are then positioned on either side of the sidewall spacers, and are thus separated from the channel.

[0006] An improved method for forming a device with an embedded stressor is desired.

SUMMARY OF THE INVENTION

[0007] In some embodiments, a method includes providing a substrate comprising a substrate material, a gate dielectric film above the substrate, and a first spacer adjacent to the gate dielectric film. The first spacer has a first portion in contact with a surface of the substrate and a second portion in contact with a side of the gate dielectric film. A recess is formed in a region of the substrate adjacent to the first spacer. The recess is defined by a first sidewall of the substrate material. At least a portion of the first sidewall underlies at least a portion of the first spacer. The substrate material beneath the first portion of the first spacer is reflowed, so that a top portion of the first sidewall of the substrate material defining the recess is substantially aligned with a boundary between the gate dielectric film and the first spacer. The recess is filled with a stressor material.

[0008] In some embodiments, a transistor includes a substrate comprising a substrate material, a gate dielectric film above the substrate, a gate above the gate dielectric film and first and second spacers adjacent to the gate dielectric film. The first spacer has a portion in contact with a first side of the gate dielectric film, and the second spacer has a portion in contact with a second side of the gate dielectric film. A source stressor region and a drain stressor region are provided in the substrate. The source stressor region has an edge substantially aligned with a boundary between the gate dielectric film and the first spacer. The drain stressor region has an edge substantially aligned with a boundary between the gate dielectric film and the second spacer. The source stressor region and drain stressor region are each filled with a stressor material that causes a stress in a channel between the source stressor region and drain stressor region.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIG. **1**A shows an intermediate stage of forming a transistor, after formation of a recess. Only one side of the transistor is shown for brevity.

[0010] FIG. **1**B is an enlarged detail of FIG. **1**A.

[0011] FIG. **2** shows the structure of FIG. **1**A, during baking.

[0012] FIG. **3** shows the structure of FIG. **2** after completion of baking

[0013] FIG. **4** shows the structure of FIG. **3**, after filling the recesses with a stressor material. Both sides of the transistor are shown.

[0014] FIG. **5** is a flow chart of an exemplary process.

DETAILED DESCRIPTION

[0015] This description of the exemplary embodiments is intended to be read in connection with the accompanying drawings, which are to be considered part of the entire written description. In the description, relative terms such as "lower," "upper," "horizontal," "vertical,", "above," "below," "up," "down," "top" and "bottom" as well as derivative thereof (e.g., "horizontally," "downwardly," "upwardly," etc.) should be construed to refer to the orientation as then described or as shown in the drawing under discussion. These relative terms are for convenience of description and do not require that the apparatus be constructed or operated in a particular orientation.

[0016] FIG. **4** shows a transistor **150** having self aligned stressor regions **126**, **127** immediately adjacent to the channel **130** of the transistor, throughout the height D**1** of the channel **130**.

[0017] The transistor **150** includes a substrate **100** comprising a substrate material. In some embodiments, the substrate material is silicon. In other embodiments, the substrate **110** may comprise bulk silicon, doped or undoped, or an active layer of a silicon on insulator (SOI) substrate. Generally, an SOI substrate comprises a layer of a semiconductor material, such as silicon, or germanium, or silicon germanium (SGOI) formed on an insulator layer. The insulator layer may be, for example, a buried oxide (BOX) layer or a silicon oxide layer. The insulator layer is provided on a substrate, typically a

silicon or glass substrate. Other substrates that may be used include multi-layered substrates, gradient substrates, or hybrid orientation substrates.

[0018] A gate dielectric film **110** is formed above the substrate **100**. The gate dielectric film **110** may be formed of SiO, SiO_2, or any other suitable material (e.g., high-k dielectrics such as Ta_2O_5, TiO_2, Al_2O_3, ZrO_2, HfO_2, Y_2O_3, L_2O_3, and their aluminates and silicates, hafnium-based materials such as HfO_2 , $HfSiO_x$, and $HfAlO_x$). In one embodiment, the gate dielectric **121** comprises an oxide layer, which may be formed by an oxidation process, such as wet or dry thermal oxidation in an ambient comprising an oxide, H_2O, NO, or a combination thereof.

[0019] A gate electrode **112** is formed above the gate dielectric film **110**. The gate electrode **112** may be formed of Ta, Ti, Mo, W, Pt, Al, Hf, Ru, suicides or nitrides thereof doped poly-crystalline silicon, other conductive materials, or a combination thereof, or other suitable conductive gate material. First and second spacers **114** are provided adjacent to the gate dielectric film **110**, on each side thereof. The first spacer **114** has a portion **114**A in contact with a first side of the gate dielectric film **110**, and the second spacer **114** has a portion **114**A in contact with a second side of the gate dielectric film. The sidewall spacers **114** serve as self aligning masks while performing ion implants within the source/drain regions, and allow formation of lightly doped drain (LDD) implants.

[0020] In some embodiments, the transistor **150** has L-shaped dummy spacers **114**, each dummy spacer having a first portion **114**A in contact with the gate dielectric film and a second portion **114**B in contact with the source/drain regions **126**. The dummy spacers **114** may be formed of a material such as SiO or TEOS, for example, and may have a thickness from about 20 Angstroms to about 200 Angstroms. Second spacers **116** are formed above the bottom portion **114**B of each dummy spacer and adjacent to the first portions **114**A. The second spacers **116** may be formed of Si_3N_4, Si_xN_y, SiO_xN_y, $SiO_xN_yH_z$, or SiO, for example, and may be between about 200 Angstroms and 700 Angstroms thick.

[0021] In other embodiments (not shown), the transistor may have a respective single unitary sidewall spacer on each side of the gate **112** and gate dielectric layer **110**. Unitary sidewall spacers may be formed of Si_3N_4, Si_xN_y, SiO_xN_y, $SiO_xN_yH_z$, for example.

[0022] A curved, substantially U-shaped source stressor region **126** and a curved, substantially U-shaped drain stressor region **127** are formed in the substrate **100**. One of ordinary skill in the art will understand that the depth of dopant implantation in the source and drain regions may differ from the depth of the stressor material in the regions **126** and **127**, and that the transistor may include LDD implant regions beneath the spacers **114**. The regions **126** and **127** in the drawings show the depth of the stressor material, and are not intended to illustrate dopant profiles.

[0023] The source stressor region **126** has an edge E**1** substantially aligned with a boundary between the gate dielectric film **110** and the first spacer **114**. The drain stressor region **127** has an edge E**2** which is substantially straight and substantially aligned with a boundary between the gate dielectric film **110** and the second spacer **114**. In some embodiments, the edges E**1** and E**2** are in line (along the same line or plane) with the boundary. In other embodiments, the edges E**1** and E**2** are parallel to the boundary, and offset from the boundary by only an insubstantial distance (e.g., 1 nanometer or less). The edges E**1** and E**2** have a depth D**2** that is at least as large as the depth D**1** of the channel region. In some embodiments, the depth D**2** is between 2 and 3 times the depth D**1**. For example, in one embodiment, the channel depth D**1** is 20 nanometers, and the straight, aligned edges E**1** and E**2** have a depth of 60 nanometers.

[0024] The source stressor region **126** and drain stressor region **127** are each filled with a stressor material that causes a stress in a channel between the source and drain regions. For a PMOS transistor, the stressor material is designed to place the channel region in compressive stress, so a material having a lattice larger than a lattice of silicon (e.g., SiGe) is used. For an NMOS transistor, the stressor material is designed to place the channel region in tensile stress, so a material having a lattice smaller than a lattice of silicon (e.g., SiC) is used. Thus, the stressor material in source/drain stressor regions **126**, **127** is close to the transistor channel **130** along the complete height of the channel. This results in improved carrier mobility, and a lower parasitic resistance of a lightly doped drain (LDD) region (not shown) to be formed beneath the spacer's sidewall **114**. In a test comparing a transistor with self aligned stressors as shown in FIG. **4** to a transistor with the stressors separated from the channel by the sidewall spacers, the device of FIG. **4** had a performance improvement of 10% (as determined by Ioff/Idsat), and Rsd was reduced by 15%.

[0025] The transistor **150** is located between a pair of field oxide (FOX) or shallow trench isolation (STI) regions **140**. Techniques for forming a FOX or STI region are known in the art. Any suitable technique may be used for forming the FOX or STI regions **140**.

[0026] FIG. **5** is a flow chart of an exemplary process, and FIGS. **1-3** show a cross section of one side of the transistor during the process.

[0027] At step **600** of FIG. **5**, the gate dielectric film **110** is grown on the substrate **100**, or otherwise formed on the substrate in a process that forms a relatively strong bond (such as, but not limited to, a covalent bond) between the gate dielectric material **110** and the underlying substrate material **100**.

[0028] At step **602**, the gate electrode **112** is formed on the gate dielectric film **110**. For example, in a typical process, after depositing the gate dielectric film layer, a layer of conductive gate material **112** (e.g., metal for an NMOS gate, or polysilicon for a PMOS gate) is deposited over the gate dielectric layer **110**, and an anisotropic etch, such as a dry etch, is performed.

[0029] At step **604**, the spacer material for dummy spacers **114** (or unitary spacers, not shown) is deposited by a process that forms a relatively weak bond between the material of spacer portion **114**B and the underlying substrate material **100**. That is, the bond between gate dielectric **110** and substrate **100** is stronger than the bond between the spacer material of spacer **114** and the substrate **100**. For example, a conformal layer of dummy spacer material for may be deposited over the gate **112** and adjacent regions by a chemical vapor deposition (CVD) process, so that the bond between spacers **114** and substrate **100** is provided by van der Waals force, or by other adhesion mechanism weaker than the particular bond between the gate dielectric film **110** and the substrate **100**. FIG. **1**B shows the respective covalent bonds of the gate dielectric layer **110** and weak bond of the dummy spacer **114**.

[0030] After depositing the layer of material for the dummy spacers **114**, the conformal layer of material for the second spacers **116** is deposited. Subsequent anisotropic etching

removes the dummy spacer material layer and second spacer material layer, except in the regions immediately adjacent to the gate dielectric layer **110** and gate electrode **112**, so as to form the dummy spacers **114** and spacers **116**.

[0031] In other embodiments (not shown), where unitary spacers are provided, a single thicker conformal layer of the spacer material is deposited over the gate and adjacent regions, and the anisotropic etch is performed, so that spacer material only remains adjacent to the gate dielectric film **110** and gate electrode **112**.

[0032] Depending on the specific process flow, the FOX or STI regions **140** may be formed at this time. In other embodiments, the FOX or STI regions **140** are formed after step **614**.

[0033] At step **606**, a recess **120** is formed in a region of the substrate **100** adjacent to the first spacers **114** on each side of the gate (only one side shown in FIGS. **1-3**). Each recess **120** is defined by a first sidewall **100**S of the substrate material **100**. At least a portion **100**T of the first sidewall **100**S underlies at least a portion of the first spacer **114**. The recesses **120** may be formed by an isotropic process. For example, a dry isotropic etch or a dry etch plus a wet etch may be performed. At this point, the substrate **100** appears as shown in FIG. **1**A. Each recess has a top portion **120**T at the surface of the substrate **100** and a lower portion **120**L, the top portion being narrower than the lower portion. Each recess **120** has an undercut, so that the lower portion **120**L of the recess extends under the spacers **114**, while the top **120**T of the recess stops at the end of the spacers **114** remote from the gate dielectric **110**.

[0034] Also, as shown in FIG. **1**A, at this point in the process, the substrate material **100** contacts an entire bottom surface of the first spacer **114** and an entire bottom surface of the second spacer **114**.

[0035] At step **608**, the substrate material is reflowed beneath the bottom portion **114**B of the first spacer **114**. For example, the substrate **100** may be baked at 650 to 950 degrees Celsius, in an atmosphere of hydrogen (H_2) or hydrochloric acid (HCl), at a pressure between 2 and 500 milliTorr, for a period between 30 seconds and 10 minutes. One of ordinary skill can readily adjust any of the three baking parameters (temperature, pressure and time) to accommodate the specific values of the other two parameters selected. As shown in FIG. **2**, the baking step **608** reflows the substrate material, and releases the silicon beneath the dummy spacers **114**, to form a modified recess **122**. However, the strong (e.g., covalent) bond between the gate dielectric material **110** and the substrate **100** is not overcome, so that the silicon is pinned at the boundary between the gate dielectric material **110** and the dummy spacer **114**.

[0036] At step **610**, the reflowing continues until the surface energy of the substrate material **100** migrates to a lower energy state, and the top of the side wall defining each recess is aligned with the boundary between the gate **112** and the spacer **114**. FIG. **3** shows the substrate **100** at the completion of step **610**. The material of substrate **100** beneath the spacers **114** has completely flowed downwards towards the bottom of the recess (now labeled **124**), so that the recess has a curved, substantially U-shaped or J-shaped profile. As shown in FIG. **3**, a top portion of the first sidewall of the substrate material defining the recess is substantially straight and aligned. The substrate material **100** is absent from substantially the entire bottom surface of the first spacer **114** and substantially the entire bottom surface of the second spacer **114**.

[0037] At step **612**, throughout the reflowing of substrate material **100** beneath the spacers **114**, contact is maintained between the gate dielectric layer **110** and the material of substrate **100**.

[0038] At step **614**, the recess is filled with the stressor material (e.g., SiGe for a PMOS or SiC for an NMOS), to form the structure shown in FIG. **4**.

[0039] Using a process as described above, the stressors can be self-aligned with the boundary between the gate and sidewall spacers, without requiring any additional photomasks.

[0040] Although the invention has been described in terms of exemplary embodiments, it is not limited thereto. Rather, the appended claims should be construed broadly, to include other variants and embodiments of the invention, which may be made by those skilled in the art without departing from the scope and range of equivalents of the invention.

What is claimed is:

1. A transistor comprising,

a substrate comprising a substrate material, a gate dielectric film above the substrate, a gate above the gate dielectric film and first and second spacers adjacent to the gate dielectric film, the first spacer having a portion in contact with a first side of the gate dielectric film, the second spacer having a portion in contact with a second side of the gate dielectric film;

a source stressor region and a drain stressor region in the substrate, the source stressor region having an edge substantially aligned with a boundary between the gate dielectric film and the first spacer, the drain stressor region having an edge substantially aligned with a boundary between the gate dielectric film and the second spacer, the source stressor region and drain stressor region each filled with a stressor material that causes a stress in a channel between the source stressor region and drain stressor region, the source stressor region and the drain stressor region each having a curved bottom edge.

2. The transistor of claim **1**, wherein the aligned edges of the source and drain stressor regions have straight portions extending deeper into the substrate than a depth of the channel.

3. The transistor of claim **1**, wherein the source and drain stressor regions are U shaped.

4. The transistor of claim **1**, wherein the transistor is a PMOS transistor, and the stressor material is SiGe.

5. The transistor of claim **1**, wherein the transistor is an NMOS transistor, and the stressor material is SiC.

6. The transistor of claim **1**, wherein the substantially aligned edges are in line with the boundaries between the gate dielectric film and the first and second spacers.

7. The transistor of claim **1**, wherein:

the first spacer has an L-shape comprising a first horizontal portion, and

the first horizontal portion and the portion in contact with the first side of the gate dielectric film are made of the same material as each other.

8. The transistor of claim **7**, wherein the first horizontal portion has a horizontal length substantially greater than a thickness of the first spacer, the first horizontal portion extending away from the gate dielectric film beyond a side edge of the portion in contact with the first side of the gate dielectric film opposite the gate dielectric film.

9. The transistor of claim **8**, wherein the source stressor region has a flat top surface contacting an entire bottom surface of the first horizontal portion.

10. The transistor of claim **8**, wherein the flat top surface of the stressor material extends from the first sidewall of the substrate material to an isolation region, and the first horizontal portion of the spacer extends only partially between the first vertical portion and the isolation region.

11. The transistor of claim **7**, wherein the substrate material is absent from substantially the entire bottom surface of the horizontal first portion of the first spacer.

12. The transistor of claim **1**, wherein a first bond between the gate dielectric film and the substrate material is a covalent bond.

13. A device comprising,

a semiconductor substrate;

a gate dielectric film above the substrate;

a gate above the gate dielectric film;

a first L-shaped spacer adjacent to the gate dielectric film, the first L-shaped spacer having a vertical portion in contact with a first side of the gate dielectric film and a horizontal portion extending away from the gate dielectric film beyond a side edge of the vertical portion opposite the gate dielectric film;

a drain stressor region in the substrate, the drain stressor region having an edge substantially aligned with a boundary between the gate dielectric film and the first L-shaped spacer, the drain stressor region filled with a stressor material that causes a stress in a channel adjacent the drain stressor region, the drain stressor material having a flat top surface contacting an entire bottom surface of the horizontal portion.

14. The device of claim **13**, wherein the vertical portion and the horizontal portion are made of the same material as each other.

15. The device of claim **13**, wherein the flat top surface of the stressor material extends from a sidewall of the substrate material contacting the edge of the drain stressor region to an isolation region, and the horizontal portion of the spacer extends only partially between the vertical portion and the isolation region.

16. The device of claim **13**, wherein the aligned edge of the drain stressor region has a straight portion extending deeper into the substrate than a depth of the channel.

17. The device of claim **13**, wherein the drain stressor region has a curved bottom edge.

18. The device of claim **13**, wherein:

the aligned edge of the drain region has a straight portion extending deeper into the substrate than a depth of the channel;

the first horizontal portion and the first vertical portion are made of the same material as each other;

the first horizontal portion has a horizontal length substantially greater than a thickness of the first spacer;

a bond between the gate dielectric film and the substrate material is a covalent bond;

the substrate material is absent from substantially the entire bottom surface of the first horizontal portion of the first spacer; and

the flat top surface of the stressor material extends from the first sidewall of the substrate material to an isolation region, and the first horizontal portion of the spacer extends only partially between the first vertical portion and the isolation region.

19. A device comprising,

a semiconductor substrate;

a gate dielectric film above the substrate;

a gate above the gate dielectric film;

a first L-shaped spacer and a second L-shaped spacer adjacent to the gate dielectric film, the first L-shaped spacer having a first vertical portion in contact with a first side of the gate dielectric film and a first horizontal portion extending away from the gate dielectric film beyond a side edge of the first vertical portion thereof opposite the gate dielectric film, the second L-shaped spacer having a second vertical portion in contact with a second side of the gate dielectric film and a second horizontal portion extending away from the gate dielectric film beyond a side edge of the second vertical portion thereof opposite the gate dielectric film;

a source stressor region and a drain stressor region in the substrate, the source stressor region having an edge substantially aligned with a boundary between the gate dielectric film and the first L-shaped spacer, the drain stressor region having an edge substantially aligned with a boundary between the gate dielectric film and the second L-shaped spacer, the source stressor region and the drain stressor region filled with a stressor material that causes a stress in a channel between the source stressor region and drain stressor region, the source stressor material having a flat top surface contacting an entire bottom surface of the horizontal portion of the first L-shaped spacer, the drain stressor material having a flat top surface contacting an entire bottom surface of the horizontal portion of the second L-shaped spacer.

20. The device of claim **19**, wherein:

the source stressor region and the drain stressor region each have a curved bottom edge;

the aligned edges of the source and drain regions have straight portions extending deeper into the substrate than a depth of the channel;

the first horizontal portion and the first vertical portion are made of the same material as each other;

the first horizontal portion has a horizontal length substantially greater than a thickness of the first spacer;

a bond between the gate dielectric film and the substrate material is a covalent bond;

the substrate material is absent from substantially the entire bottom surface of the first horizontal portion of the first spacer and the second horizontal portion of the second spacer; and

the flat top surface of the stressor material extends from the first sidewall of the substrate material to an isolation region, and the first horizontal portion of the spacer extends only partially between the first vertical portion and the isolation region.

* * * * *