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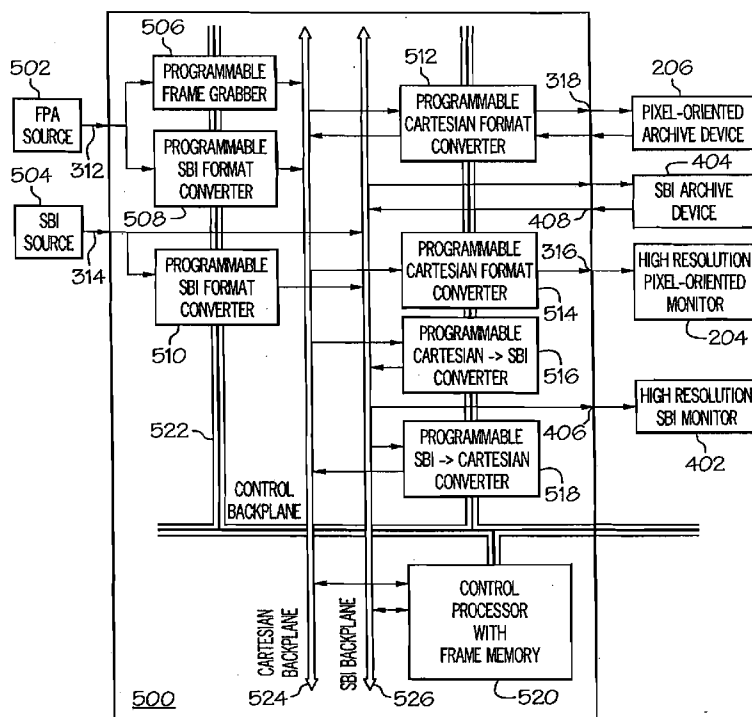


FIG. 5

(57) Abstract: An apparatus and method for allowing multiple high and low resolution SBI and conventional FPA imaging devices to use a common high resolution monitor and archive device without increasing or significantly changing the footprint of existing devices. This system and method uses a frame grabber for digitizing video from the legacy FPA devices, a frame mapper for rendering or mapping the FPA video into the SBI digital format, a converter for rasterizing SBI data streams into pixel-oriented FPA video frames, an input selector for selecting which FPA or SBI imaging device to display on a high resolution monitor, an processor for storing and manipulating frames of video, a video output encoder for converting the SBI frames into a video signal appropriate for display on the high resolution monitor, and an output means for connecting to a storage device for archiving video and images.

COMBINED SBI AND CONVENTIONAL IMAGE PROCESSOR

[0001] Technical Field

[0002] The present invention relates generally to systems, devices, and methods for rendering Scanned Beam Imager (SBI) and Focal Plane Array (FPA) image data into a common format for display on a high resolution monitor and storage on a common system.

[0003] Background of the Invention

[0004] Many medical devices have visual screens for providing real-time data. While some have simple backlit 80x25 text screens, others require television screens or video monitors for displaying video images. The space in hospital operating room environments is very tight and cannot accommodate much equipment, especially bulky video monitors. The space close to a patient, where one or more physicians might operate, is more or less constrained by the geometry of the patient and the need or desire to have certain medical instruments in fixed locations, e.g., anesthesia devices near the patient's head region. Usable space near a patient, especially that which is directly accessible by the operating physician, is at a premium. When multiple medical devices each require a video monitor, the situation presents both space and ergonomic challenges to the physician and support staff as they attempt to coordinate the use of multiple video monitors. In some cases, it might be impracticable to accommodate more than one monitor near the patient. There is therefore a need for a system and method to allow physicians and support staff to use, and coordinate the use of, multiple imaging devices on a common monitor and storage system.

[0005] Imaging devices can have different native resolutions and frame rates. Focal Plane Array (FPA) devices typically use Charge Coupled Device (CCD) technology to capture an entire image, or frame, all at once. Typically, these CCD-type imagers capture 30 frames

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per second (fps). As the frame is rendered to a suitable video format for display on a monitor, the frame may be split into two interlaced (every other line) 60 fps frames that combined make up one full frame on the monitor. This interlacing tends to result in image degradation, but does have the advantage that common inexpensive equipment that supports interlaced video is ubiquitously available and interconnections between various pieces of equipment are relatively simple and straightforward. Alternatively, the FPA may present a progressive scan video signal, whereby each frame is imaged line by line in its entirety resulting in better clarity video. Progressive scan FPA devices and monitors tend to be somewhat more expensive than interlaced devices.

[0006] Scanned Beam Imaging (SBI) devices, on the other hand, use a different, higher resolution technology. Instead of acquiring the entire frame at once, the area to be imaged is rapidly scanned point-by-point by an incident beam of light, the reflected light being picked up by sensors and translated into a native data stream representing a series of points and values. SBI technology is especially applicable to endoscopes because SBI devices have better image resolution and present higher quality images of small internal structures, use reduced power light sources, and can be put in very small package diameters for insertion into a human body.

[0007] Scanning beam imaging endoscopes using bi-sinusoidal and other scanning patterns are known in the art; see, for example U.S. Patent Application US 2005/0020926 A1 to Wikloff et al. An exemplary color SBI endoscope has a scanning element that uses dichroic mirrors to combine red, green, and blue laser light into a single beam of white light that is then deflected off a small mirror mounted on a scanning bi-axial MEMS (Micro Electro Mechanical System) device. The MEMS device scans a given area with the beam of white light in a pre-determined bi-sinusoidal or other comparable pattern and the reflected light is sampled for a large number of points by red, green, and blue sensors. Each sampled data point is then put in a native SBI data format and transmitted to an image processing device.

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- [0008] While reading data out from FPA/CCD devices is normally performed in an orderly line-by-line manner that makes conversion to a standard video signal relatively straightforward, MEMS-based scanners using bi-sinusoidal or other non-standard scanning patterns result in an ordering of the SBI data that would be incompatible for direct use with ordinary monitors. Also, the image may be scanned at frame rates that ordinary monitors are not capable of refreshing on their screens. To display on an ordinary monitor, the scanned image is therefore first reassembled from the SBI digital pixel image data into a full frame image. This reassembling process is sometimes referred to as rasterization, because a raster or frame is created from the raw data. The image processing device then uses the full frame image to render an appropriate video signal to be displayed on a video monitor at a suitable frame rate.
- [0009] A native SBI image has potentially superior digital pixel density and dynamic range than an FPA image. Preferentially, the SBI image should be displayed on a monitor suitable for directly displaying the SBI image from the SBI image data. Alternatively, the SBI image data should be converted to a format suitable for display on a high resolution video monitor. There is therefore a need for a system and method to allow physicians and support staff to use, and coordinate the use of, both FPA and SBI imaging devices on a common high resolution monitor and storage system.
- [0010] **Summary of the Invention**
- [0011] The present invention meets the above and other needs. An apparatus that is a combined SBI and FPA image processor comprises a frame grabber for digitizing video from the legacy FPA devices, a frame mapper for rendering or mapping the FPA video into the SBI digital format, an input selector for selecting which imaging device to display on the high resolution monitor, an SBI processor for storing and processing each frame of SBI video, and a video output encoder for converting the each digitized SBI frame into a video signal appropriate for display on the high resolution monitor. The apparatus allows multiple FPA and SBI imaging devices to use a common high resolution monitor and

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archive device without increasing or significantly changing the footprint of existing devices in the operating room environment.

[0012] The method of the invention involves using the combined SBI and FPA image processor to render both FPA and SBI inputs from imaging devices to a common high resolution format for display on a high resolution monitor and archiving in a storage means.

[0013] **Brief Description of the Drawings**

[0014] The accompanying figures depict multiple embodiments of the combined SBI and FPA image processor. A brief description of each figure is provided below. Elements with the same reference numbers in each figure indicate identical or functionally similar elements. Additionally, as a convenience, the left-most digit(s) of a reference number identifies the drawings in which the reference number first appears.

[0015] Fig. 1 is a schematic diagram of a prior art imaging system using a Focal Plane Array (FPA) imaging device, a television monitor, and a printer.

[0016] Fig. 2 is a schematic diagram of an embodiment of the invention where both an FPA imaging device and a Scanned Beam Imaging (SBI) imaging device connect to the combined SBI and FPA image processor, and the image processor provides outputs to the high resolution monitor and the archive device.

[0017] Fig. 3 is a schematic diagram of an embodiment of the combined SBI and FPA image processor showing an FPA frame grabber, an FPA-to-SBI frame mapper, an input selector, an SBI frame rasterizing element, and a video output encoder.

[0018] Fig. 4 is a schematic diagram of an alternate embodiment of the combined SBI and FPA image processor, where the selected SBI digital pixel input is sent to the monitor and archive device without rasterizing the frame.

[0019] Fig. 5 is a schematic diagram of an alternate embodiment of the combined SBI and FPA image processor, where the image processor is programmable and can support various

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Cartesian frame-based inputs and outputs as well as digital pixel stream inputs and outputs.

[0020] Fig. 6 is an illustration used to facilitate understanding the conversion process from the two-dimensional Cartesian space format typical of FPA devices to the pixel stream format used by SBI devices.

[0021] **Detailed Description**

[0022] Fig. 1 details the prior art imaging systems. Exemplary embodiments of the present invention are detailed in Figs. 2-5. Fig. 6 illustrates the SBI to FPA conversion process.

[0023] **Prior Art Imaging System**

[0024] Referring now to the schematic diagram of a prior art imaging system **100** depicted in Fig. 1, an FPA imaging device **102** connects to an FPA video processor **103** that connects to a monitor **104** that connects to a storage means **106**.

[0025] In a typical prior art imaging system **100**, like that found in a typical hospital operation room, an FPA imaging device **102**, usually a CCD-type camera, provides a video signal and, optionally, exchanges control signals or commands with a matching FPA video processor **103** that creates a variety of standard video outputs to the monitor **104**. The video signal supplied to the monitor can be a composite signal, an S-Video signal, a Digital Video Interface (DVI) signal, an HDMI signal, or more commonly a component RGB signal, with each of the Red, Green, and Blue signals carried on individual cables and having separate physical connectors for attaching to the monitor **104**. The monitor **104** displays the image seen by the FPA imaging device **102** to the physician. The storage means **106**, also receives the video signal and allows the physician to record the images the physician is seeing. Typically, the storage means **106** receives the video signal directly from the FPA video processor **103**. The storage means **106** can be a printer, an analog VCR, a DVD recorder, or any other recording means as would be known in the art.

[0026] Imaging System using the Combined SBI and FPA Image Processor

[0027] Referring now to the schematic diagram of an embodiment of an imaging system using the combined SBI and FPA Image Processor System **200** depicted in Fig. 2. An SBI imaging device **202** connects directly to the image processor **208** and an FPA imaging device **102** connects to the image processor **208** through an FPA video processor **103**. The image processor **208** connects to both the high resolution pixel-oriented monitor **204** and the pixel-oriented archive device **206**.

[0028] In the combined SBI and FPA Image Processor System **200**, the SBI imaging device **202** delivers SBI digital sample data to the image processor **208**, while the FPA imaging device **102** provides a traditional raster video signal through the FPA video processor **103** to the image processor **208**. The image processor **208** allows the physician to select which source to display on the high resolution pixel-oriented monitor **204**. The image processor **208** sends a separate output to the pixel-oriented archive device **206**. The output to the pixel-oriented archive device **206** is controlled by the physician. The physician uses a separate selection control on the endoscope to cause still images to be stored to the pixel-oriented archive device **206**, or to start and stop storage of video images to the pixel-oriented archive device **206**, allowing the physician the ability to record continuous video or discrete images from the previously selected source. The pixel-oriented archive device **206** can be storage system capable of storing analog data, such as a VCR, or DVD recorder, or it can be a digital device such as a printer or computer system, or any other recording means as would be known in the art.

[0029] In an alternate embodiment, the output to the pixel-oriented archive device **206** is a mirror copy of what the physician sees on the high resolution pixel-oriented monitor **204**. In another embodiment, the output to the pixel-oriented archive device **206** can be both the SBI imaging device **202** digital sample data and the SBI encoded FPA imaging device **102** video images, including a separate flag indicating which device was selected for viewing on the high resolution pixel-oriented monitor **204** by the physician at the time.

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In another embodiment, the image processor **208** is capable of multiple inputs from more than two different imaging devices. Various other arrangements are possible for the image processor **208**, the pixel-oriented archive device **206**, and different kinds of imaging devices, and would be apparent to one having ordinary skill in the art. The figures and descriptions represent merely exemplary embodiments of the invention, and are meant to be limited only by the claim scope.

[0030] SBI/FPA Image Processor with Analog and Digital Interfaces

[0031] Referring now to the schematic diagram of an SBI/FPA Image Processor with Analog and Digital Interfaces **300** depicted in Fig. 3, an FPA imaging device **102** is connected through an FPA video processor **103** to a pixel-oriented video input **312** which is connected to a video frame grabber **302**. The video frame grabber **302** connects to a frame mapper **304** which connects to an input selector **306**. The input selector **306** is also connected to the SBI input **314** that is connected to an SBI imaging device **202**. The input selector **306** connects to an SBI processor **308**. The SBI processor **308** connects to both the pixel-oriented storage means output **318** and the video output encoder **310**. The video output encoder **310** further connects to the pixel-oriented video monitor output **316**. The pixel-oriented video monitor output **316** connects to the high resolution pixel-oriented monitor **204**. The pixel-oriented storage means output **318** connects to the pixel-oriented archive device **206**.

[0032] An embodiment of the SBI/FPA Image Processor with Analog and Digital Interfaces **300** has inputs for accepting both analog and digital video devices. The pixel-oriented video input **312** accepts RGB video inputs from an FPA video processor **103** that is connected to an FPA imaging device **102**. The frame grabber **302** decodes the RGB video signal and digitizes each video frame. A frame mapper **304** uses the digitized video frame to encode a new SBI formatted digital sample data stream, thereby rendering or mapping the original video signal from the pixel-oriented video input **312** to the SBI format. The frame mapper **304** assigns each FPA pixel from the frame grabber **302** in a prescribed

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manner to create each sample of a synthesized SBI formatted digital sample stream. In this process a portion of each FPA pixel's color value is assigned to one or more SBI sample stream locations. The frame mapper **304** presents the SBI compatible digital sample data stream to the input selector **306**. The input selector **306** also receives an input from the SBI input **314**. The SBI input **314** accepts an SBI digital sample data stream from an SBI imaging device **202**.

[0033] The input selector **306** allows the physician to select which of the two devices to display on the high resolution pixel-oriented monitor **204**. The input selector **306** can be controlled using a switch on the image processor **208**. Based on the physician's device selection, the input selector **306** sends one of the two SBI digital sample data streams to the SBI processor **308**. The SBI processor **308** takes the SBI digital sample data stream and maps the individual pixel data points into an high resolution video frame. The SBI processor **308** performs color correction, contrast and gamma control, and other imaging enhancing algorithms on the video data. The SBI processor **308** can enhance the image differently depending upon whether the original image is from an FPA or an SBI imaging device.

[0034] The video output encoder **310** uses the mapped video frame in the SBI processor **308** to encode a suitable video output signal for driving the high resolution pixel-oriented monitor **204** and presents it to the pixel-oriented video monitor output **316**. The video output signal preferably uses either a progressive scan 720 HDMI (ITU-R BT.601) with a 60 fps refresh rate or an SVGA VESA-compatible output using at least 800x600 pixel resolution and 72 fps refresh rate, although both higher and lower resolutions and refresh rates are contemplated. Typically, a compatible commercially available medical grade display will be used, such as the Dynamic Displays' MD1518-101 display or any other suitable display as would be known by one having ordinary skill in the art. Pixel-oriented output from the SBI processor **308** sent to the pixel-oriented archive device **206** via the pixel-oriented storage means output **318** is controlled by the physician. The physician uses a selection control on the endoscope to select which images from the SBI processor

308 to store to the pixel-oriented archive device **206**, allowing the physician the ability to record continuous video or discrete images. The pixel-oriented archive device **206** can be storage system capable of storing analog data, such as a VCR, or DVD recorder, or it can be a digital device such as a printer or computer system, or any other recording means as would be known in the art.

[0035] The video frame grabber **302**, frame mapper **304**, input selector **306**, SBI processor **308**, and video output encoder **310** modules of the SBI/FPA Image Processor with Analog and Digital Interfaces **300** are implemented using one or more microcontroller processors (which may be independently applied or embedded in an ASIC or FPGA), and may also include one or more discrete electronic support chips. The actual circuit implementation necessary to perform the digital signal processing necessary for color correction, dynamic range control, data mapping and other pixel manipulation processes could be done in a variety of ways that would be obvious to one of ordinary skill in the art.

[0036] In another embodiment of the invention, the SBI digital sample data stream from the SBI processor **308** is sent to an SBI archive device **404** via an SBI digital storage means output **408**. In another embodiment of the invention, the analog video inputs from the FPA video processor **103** can be composite, S-Video, or other component interfaces including xVGA, and can be in NTSC, PAL, SECAM, VESA or other formats. In another embodiment of the invention, the video inputs from the FPA video processor **103** can be digital, including, but not limited to, the DVI, HDMI, or DV MPEG 4:2:2 standards. In these embodiments, the frame grabber **302** would be suitably adapted to handle the other formats, acquiring the video frame by digitizing if it is an analog video signal, or acquiring the video frame by capturing the digital data if it is a digital video signal. In another embodiment the high resolution pixel-oriented monitor **204** could be a heads up display worn by the physician.

[0037] SBI/FPA Image Processor with SBI Digital Sample Data Output

[0038] Referring now to the schematic diagram of an SBI/FPA Image Processor with SBI Digital Sample Data Output **400** depicted in Fig. 4, an FPA imaging device **102** is connected through an FPA video processor **103** to a pixel-oriented video input **312** which is connected to a video frame grabber **302**. The video frame grabber **302** connects to a frame mapper **304** which connects to an input selector **306**. The input selector **306** is also connected to the SBI input **314** that is connected to an SBI imaging device **202**. The input selector **306** connects to an SBI processor **308**. The SBI processor **308** connects to both the SBI video monitor output **406** and the storage means output **408**. The SBI storage means output **408** connects to the SBI archive device **404**. The SBI video monitor output **406** connects to the high resolution SBI monitor **402**.

[0039] An embodiment of the SBI/FPA Image Processor with SBI Digital Sample Data Output **400** has inputs for accepting both analog and digital video devices. The pixel-oriented video input **312** accepts RGB video inputs from an FPA video processor that is connected to an FPA imaging device **102**. The frame grabber **302** decodes the RGB video signal and digitizes each video frame. A frame mapper **304** uses the digitized video frame to encode a new SBI formatted digital sample data stream, thereby rendering or mapping the original video signal from the pixel-oriented video input **312** to the SBI format. The frame mapper **304** assigns each FPA pixel from the frame grabber **302** in a prescribed manner to create each sample of a synthesized SBI formatted digital sample stream. In this process a portion of each FPA pixel's color value is assigned to one or more SBI sample stream locations. The frame mapper **304** presents the SBI compatible digital sample data stream to the input selector **306**. The input selector **306** also receives an input from the SBI input **314**. The SBI input **314** accepts an SBI digital sample data stream from an SBI imaging device **202**. The input selector **306** allows the physician to control which of the two devices to display on the high resolution SBI monitor **402**. The input selector **306** can be controlled using a switch on the image processor **208**. Based on the physician's device selection, the input selector **306** sends one of the two SBI digital

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sample data streams to the SBI processor **308**. The SBI processor **308** performs color correction, contrast and gamma control, and other imaging enhancing algorithms on the video data. The SBI processor **308** can enhance the image differently depending upon whether the original image is from an FPA or an SBI imaging device.

- [0040] The SBI processor **308** presents the SBI digital sample data stream to the SBI video monitor output **316** which is connected to a high resolution SBI monitor **402** capable of accepting an SBI signal input. The output from the SBI processor **308** sent to the SBI archive device **404** via the SBI storage means output **408** is controlled by the physician. The physician uses a separate selection control on the endoscope to select which images from the SBI processor **308** to store to the SBI archive device **404**, allowing the physician the ability to record continuous video or discrete images. The SBI storage means output **408** is a digital device such as a printer or computer system, or any other recording means as would be known in the art.
- [0041] The video frame grabber **302**, frame mapper **304**, input selector **306**, SBI processor **308**, and video output encoder **310** modules of the SBI/FPA Image Processor with SBI Digital Sample Data Output **400** are implemented using one or more microcontroller processors (which may be independently applied or embedded in an ASIC or FPGA), and may also include one or more discrete electronic support chips. The actual circuit implementation necessary to perform the digital signal processing necessary for color correction, dynamic range control, data mapping and other pixel manipulation processes could be done in a variety of ways that would be obvious to one of ordinary skill in the art.
- [0042] In alternative embodiment of the invention, the analog video inputs from the FPA video processor **103** can be composite, S-Video, or other component interfaces including xVGA, and can be in NTSC, PAL, SECAM, VESA, or other formats. In another embodiment of the invention, the video inputs from the FPA video processor **103** can be digital, including, but not limited to, the DVI, HDMI, or DV MPEG 4:2:2 standards. In these embodiments, the frame grabber **302** would be suitably adapted to handle the other

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formats, acquiring the video frame by digitizing if it is an analog video signal, or acquiring the video frame by capturing the digital data if it is a digital video signal. In another embodiment the high resolution SBI monitor **402** could be a heads up display worn by the physician.

[0043] Programmable SBI/FPA Image Processor

[0044] Referring now to the schematic diagram of a programmable SBI/FPA Image Processor **500** depicted in Fig. 5, a pixel-oriented video input **312** connects an FPA source **502** to both a programmable frame grabber **506** and a programmable digital format converter **508** which connect internally to a Cartesian backplane **524**. The Cartesian backplane **524** connects to a programmable digital format converter **512** that connects to the pixel-oriented archive device **206** through the pixel-oriented storage means output **318**. The Cartesian backplane **524** further connects to a programmable Cartesian format converter **514** that connects to the high resolution pixel-oriented monitor **204** through the pixel-oriented video monitor output **316**. The Cartesian backplane **524** further connects to a control processor with frame memory **520**, a programmable Cartesian to SBI converter **516**, and a programmable SBI to Cartesian converter **518**. The control processor with frame memory **520**, the programmable Cartesian to SBI converter **516**, and the programmable SBI to Cartesian converter **518** also connect to an SBI backplane **526**. The SBI backplane **526** connects to an SBI source **504** through an SBI input **314**. The SBI backplane **526** also connects to the SBI input **314** through a programmable SBI format converter **510**. The SBI backplane **526** further connects to an SBI archive device **404** through an SBI storage means output **408**, and a high resolution SBI monitor **402** through an SBI video monitor output **406**. A control backplane **522** connects the control processor with frame memory **520** to the programmable frame grabber **506**, the programmable digital format converter **508**, the programmable SBI format converter **510**, the programmable digital format converter **512**, the programmable Cartesian format converter **514**, the programmable Cartesian to SBI converter **516**, and the programmable SBI to Cartesian converter **518**.

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- [0045] An embodiment of the Programmable SBI/FPA Image Processor **500** has inputs for accepting either or both analog and digital video devices. The pixel-oriented video input **312** accepts video inputs from an FPA source **502**. The FPA source **502** can be analog in which case the pixel-oriented video input **312** can be composite, S-Video, or other component interfaces including xVGA, and can be in NTSC, PAL, SECAM, VESA, or other formats. The pixel-oriented video input **312** can also be a digital interface for accepting DVI, HDMI, or DV MPEG 4:2:2 inputs from a digital FPA source **502**.
- [0046] The programmable frame grabber **506** acquires the analog video signal from an analog FPA source **502** by digitizing each video frame into an internal pixel-oriented format and transfers each frame of video to the control processor with frame memory **520** across the Cartesian backplane **524**. The programmable digital format converter similarly acquires a digital video signal from a digital FPA source **502** by converting the encoded frames of video into an internal pixel-oriented format and transfers each frame of video to the control processor with frame memory **520** across the Cartesian backplane **524**.
- [0047] The programmable SBI format converter **510** decodes an SBI source **504** input into an internal SBI format and transfers the digital data stream to the control processor with frame memory **520**. Alternatively, the SBI source **504** can transfer the SBI formatted digital sample data stream directly to the control processor with frame memory **520** if it is already in the internal SBI format.
- [0048] Once the pixel-oriented frame of video or SBI formatted digital sample data stream starts to transfer to the control processor with frame memory **520** it can start performing color correction, contrast and gamma control, and other imaging enhancing algorithms on the video data. Because SBI data samples can have greater resolution or include sampling of spectrum outside of the normal Red Green and Blue colorspace, the control processor with frame memory **520** may enhance the image differently depending upon whether the original image is from an FPA or an SBI imaging device. As an illustration only, if the SBI data samples include sampling of how much the imaged area fluoresced when an

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incident beam shone on it, the control processor with frame memory **520** may highlight the area in an normally absent color such as bright green, or it could utilize an edge detection algorithm and draw a flashing bright white line around the perimeter of the area. If the area being imaged by the SBI source **504** contained a greater depth of colors than could be displayed on a high resolution pixel-oriented monitor **204**, the control processor with frame memory **520** could scale the intensity linearly or non-linearly to optimal levels for display. The control processor with frame memory **520** can also use data from previous frames or scans in enhancing the current video data. These and other image enhancing algorithms known to those having ordinary skill in the art could be utilized.

[0049] The control processor with frame memory **520** uses the control backplane **524** to control which of the input devices, **502**, **504**, to use as input, and which type of high resolution monitor, **204**, **402**, to use for displaying the video. In an alternate embodiment the high resolution pixel-oriented monitor **204** or high resolution SBI monitor **402** could be a heads up display worn by the physician. The control processor with frame memory **520** also controls which images to send to the archive devices, **206**, **404** and whether the archive device is to record continuous video or discrete images. The archive devices, **206**, **404** can be either analog or digital storage devices.

[0050] The programmable SBI/FPA Image Processor **500** can run in four different modes: FPA source to SBI monitor mode; FPA source to pixel-oriented monitor mode, SBI source to pixel-oriented monitor mode; and SBI source to SBI monitor mode.

[0051] *FPA source to SBI monitor mode*

[0052] In FPA source to SBI monitor mode, the control processor with frame memory **520** forwards the pixel-oriented frame of video across the Cartesian backplane **524** to the programmable Cartesian to SBI converter **516**. The programmable Cartesian to SBI converter **516** converts the pixel-oriented video frame to an SBI formatted digital sample data stream, thereby rendering or mapping the original video signal from the FPA source

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502 to the SBI format. The programmable Cartesian to SBI converter **516** assigns each FPA pixel from the frame in a prescribed manner to create each new sample of the synthesized SBI formatted digital sample stream. In this process a portion of each FPA pixel's color value is assigned to one or more SBI sample stream locations. The control processor with frame memory **520** can then store the SBI formatted digital sample data stream back in memory, perform additional processing, or direct the SBI formatted digital sample data stream across the SBI backplane **526** to the high resolution SBI monitor **402** or the SBI archive device **404**.

[0053] ***FPA source to pixel-oriented monitor mode***

[0054] In FPA source to pixel-oriented monitor mode, the control processor with frame memory **520** forwards pixel-oriented frame of video across the Cartesian backplane **524** to the programmable Cartesian format converter **514**, which puts the frame of video into the appropriate analog or digital format for display on the high resolution pixel-oriented monitor **204**. If the high resolution pixel-oriented monitor **204** is analog, the pixel-oriented video monitor output **316** can be composite, S-Video, or other component interfaces including xVGA, and can be in NTSC, PAL, SECAM, VESA, or other formats. If the high resolution pixel-oriented monitor **204** is digital, the pixel-oriented video monitor output **316** can be a digital interface for accepting DVI, HDMI, DV or other digital connections. The control processor with frame memory **520** can also direct the programmable digital format converter **512** to send the current frame of video on the Cartesian backplane **524** to the pixel-oriented archive device **206**.

[0055] ***SBI source to pixel-oriented monitor mode***

[0056] In SBI source to pixel-oriented monitor mode, the control processor with frame memory **520** forwards the SBI digital sample data stream across the SBI backplane **526** to the programmable SBI to Cartesian converter **518**. The programmable Cartesian to SBI converter **518** converts the SBI digital sample data stream to a pixel-oriented video frame, thereby rendering or mapping the original video signal from the SBI source **504** to

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the pixel-oriented format. The programmable SBI to Cartesian converter **518** assigns each SBI formatted sample to one or more FPA pixels in a prescribed manner to create each new sample of the synthesized pixel-oriented frame. In this process a portion of each SBA data sample's color value is assigned to one or more FPA pixels. The control processor with frame memory **520** can then store the pixel-oriented frame of video back in memory, perform additional processing, or direct the pixel-oriented frame of video across the Cartesian backplane **524** to the programmable Cartesian format converter **514**, which puts the frame of video into the appropriate analog or digital format for display on the high resolution pixel-oriented monitor **204**. The control processor with frame memory **520** can also direct the programmable digital format converter **512** to send the current frame of video on the Cartesian backplane **524** to the pixel-oriented archive device **206**.

[0057] ***SBI source to SBI monitor mode***

[0058] In SBI source to SBI monitor mode, the control processor with frame memory **520** can have both the high resolution SBI monitor **402** and the SBI archive device **404** use the current SBI formatted digital sample stream from the SBI source **504** present on SBI backplane **526**. Alternatively, the control processor with frame memory **520** can store the SBI formatted digital sample data stream from the SBI source **504** in memory, perform additional processing, and then direct the modified SBI formatted digital sample stream back on the SBI backplane **526** to the high resolution SBI monitor **402** and the SBI archive device **404**.

[0059] ***Processor and Backplane Architecture***

[0060] The control processor with frame memory **520**, the programmable frame grabber **506**, the programmable digital format converter **508**, the programmable SBI format converter **510**, the programmable digital format converter **512**, the programmable Cartesian format converter **514**, the programmable Cartesian to SBI converter **516**, and the programmable SBI to Cartesian converter **518** modules of the programmable SBI/FPA Image Processor

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with SBI Digital Sample Data Output **500** are implemented using one or more microcontroller processors (which may be independently applied or embedded in an ASIC or FPGA), and may also include one or more discrete electronic support chips. The actual circuit implementation necessary to perform the digital signal processing necessary for color correction, dynamic range control, data mapping and other pixel manipulation processes could be implemented in circuitry and software in a variety of ways that would be obvious to one of ordinary skill in the art.

[0061] The control backplane **522**, the Cartesian backplane **524**, and the SBI backplane **526** can be discrete backplanes or they can be logical backplanes running on a common physical backplane. Backplane technology is a well developed art and the backplanes could be implemented in circuitry and software in a variety of ways that would be obvious to one of ordinary skill in the art.

[0062] **Converting between SBI formatted data streams and Pixel-Oriented video frames**

[0063] The dual resonant scanned beam imager is a class of MEMS oscillating mirror imagers with two orthogonal axis of rotation (labeled x and y) that operate in a resonant mode. By convention, the x-axis oscillation is referred to as the fast axis and the y-axis oscillation is referred to as the slow axis. When properly excited, the oscillating mirror causes a beam of light reflected from its surface to trace a geometric pattern known as a Lissajous figure or pattern. Based on the phase relationship of the slow and fast axis oscillation, the basic Lissajous pattern can precess. The number of slow axis cycles required to precess the pattern to an initial spatial point, is called the interleave factor.

$$x(t) = A \sin(w_f t + \phi_f)$$

$$y(t) = B \cos(w_s t + \phi_s)$$

[0064] The Lissajous pattern traced by an SBI is spatially repeated after a set number of oscillations on the slow axis (interleave factor). Once a reference point on the complete set of Lissajous patterns is identified, one can view the constant sample time, digital data stream captured at each optical detector as a vector of constant length, the SBI Data

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Vector (SDVi). The number of samples in the vector (N) is equal to the interleave factor times the period of the slow axis oscillation divided by the sample interval (ts).

$$SDV_i(j\Delta t) = [s(i, j)]_{j=0}^{N-1}$$

- [0065] If there are multiple optical detectors sampled coincidently, then the SBI data stream can be viewed as a matrix, the SBI Data Matrix (SDM), that has a row count equal to the number of sampled detectors (M) and a column count equal to the number of samples in each SDV (N). For example, a system of comprising RGB channels plus an additional Fluorescence channel would be as follows.

$$SDM = \begin{bmatrix} SDV_R \\ SDV_G \\ SDV_B \\ SDV_F \end{bmatrix}$$

- [0066] The pixel-oriented video frame is represented as a pixel data matrix (PDM), a two-dimensional matrix with row and column indices that represent the display space. A typical system might have 600 rows (Y) and 800 columns (X). Each point in the data set is a triple representing red (R), green (G), and blue (B) display intensities.

$$PDM = \begin{bmatrix} (r_{0,0}, g_{0,0}, b_{0,0}) & \cdot & \cdot & \cdot & (r_{0,799}, g_{0,799}, b_{0,799}) \\ \cdot & & & & \cdot \\ \cdot & & & & \cdot \\ \cdot & & & & \cdot \\ (r_{599,0}, g_{599,0}, b_{599,0}) & & & & (r_{799,599}, g_{799,599}, b_{799,599}) \end{bmatrix}$$

- [0067] In order to conveniently describe matrix operations, it is useful to define a view of the matrix, PDM, that is a vector of length XY, and define that vector as PDV.

- [0068] The transformation from matrix to vector representation can be achieved algorithmically. To transform data from the Lissajous SBI space SDM to the Cartesian pixel-oriented space PDM, a transformation matrix is defined. The transformation matrix is a N x XY matrix where N is the number of samples in the SDV; X is the number of horizontal

pixels in the Cartesian pixel-oriented space; Y is the number of vertical pixels in the Cartesian pixel-oriented space.

[0069] Referring now to Figure 6 provides a close-up look at the physical situation when converting from the Lissajous space SDM to the Cartesian space PDM. The grey crosses in the imaged area **600** represent the pixels in Cartesian Space mapped with the matrix origin located in the upper left hand corner. Each pixel is represented by conventional Cartesian coordinates (x,y). The solid line is the SBI beam path **602** and represents a portion of a specific trajectory of the dual resonant scanned beam through the imaged area **600**. The black diamonds indicate SBI samples **604** taken along that SBI beam path **602**. The SBI sample index (j) increases from the top left to bottom right in this depiction. The trajectory of the SBI beam path **602** (with increasing sample index) can be in any direction through a subset of the imaged area **600**. Note that in Figure 6 the SBI samples **604** at the top left and bottom right are closer together than the SBI samples **604** in the center of the figure. This difference is shown to reinforce the implications of a constant data-sampling rate applied to resonant (sinusoidal) beams.

[0070] *Conversion from Lissajous space SDM to Cartesian space PDM*

[0071] In general, conversion from Lissajous space SDM to the Cartesian space PDM can be represented as the matrix multiplication:

$$[SDV][T] = [PDV]$$

[0072] If the number of samples in the SDV matrix is N and the size of the Cartesian space is X by Y, then the matrix, SDV, is of dimension 1 x N, the transformation matrix, T, is of dimension N by (X*Y) and the matrix PDV, is of dimension 1 by X*Y. In Figure 6, we are converting from Lissajous space SDM to the Cartesian space PDM for every sample and pixel, but it is instructive for purposes of illustrating the algorithm to concentrate on a single SBI data sample (m) **606**.

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[0073] The object is to distribute the data from the imaged area **600** at sample **m 606** to the associated pixels **608** (those within the circle **610**) in the pixel space. The following steps can be used to populate the T matrix:

[0074] Step 1: Through precise knowledge of the path of the SBI beam (that knowledge is inherent in the scanner drive and positioning system) it is possible to identify the pixel data point closest to the SBI sample, **m 606**, at $t = m\Delta t_s$ from the start of the frame. We denote that pixel with the indices (k,l).

[0075] Step 2: Construct a circle **610** in Cartesian space of radius, r_d , over which the data from SBI sample, **m 606**, is going to be distributed to the associated pixels **608** contained within circle **610**.

[0076] Step 3: For each associated pixel **608** (k+s,l+t), where s and t are integers that describe points in Cartesian space located within the circle constructed in step 2:

[0077] a. Compute the length (in Cartesian space), l, of the vector from the Cartesian space location of the SBI sample, **m 606**, to the center of the associated pixel **608**, (k+s,l+t).

[0078] b. Calculate a weighting value, w, that is proportional to the length, of the vector, such as: $w = e^{-F \frac{s}{r_d}}$ where:

w	is the weighting factor,
s	is the length of the vector from the SBI data point (m) 606 to the associated pixel 608 of interest
F	is a controllable constant that sets how fast the effects of the SBI data falls off as the value of l increases.
r_d	is the radius of the circle 610 over which the data from the SBI sample is being distributed

Other weighting functions as would be known in the art could also be used.

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[0079] c. Record the value of w into the transformation matrix T at the x,y location of the subject pixel. The location in the matrix will be at the row m and the column which can be derived using the following mapping equations:

[0080] Define a $m \times n$ matrix A from which we wish to create a $1 \times mn$ vector B . Define the operation with the symbol \mapsto . Write the mapping as $A \mapsto B$. Conceptually, B is a concatenation of each row of A starting at row 0 and ending at row $m-1$.

[0081] (i) Mathematically, define a function for the conversion of a two-dimensional space to a one-dimensional space:

$$j = \Theta(x, y, m, n)$$

where j is an integer offset from the start of a vector ($j=0$);
 x is the traditional display space notion of the horizontal displacement from the origin
 y is the traditional display space notion of the vertical displacement from the origin.
 m is the number of rows in the matrix A
 n is the number of columns in the matrix A

Use the following instantiation of the function, Θ .

$$j = yn + x$$

where x is a positive integer less than m
 y is a positive integer less than n

[0082] (ii) Mathematically, define a set of functions for the conversion of a one-dimensional space into a two-dimensional space:

$$x = \Theta_x(j, m, n)$$

$$y = \Theta_y(j, m, n)$$

consistent with equation $j = yn + x$, use the following instantiation of the functions Θ_x, Θ_y :

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$$x = j \% n$$

$$y = \frac{j - (j \% n)}{n}$$

where % is the modulus operator.

[0083] Step 4(optional): It should be recognized that this method creates a sparse matrix, T. To improve computational efficiency, one can use various methods as are known in the art to create a banded matrix amenable to hardware acceleration or optimized software algorithms.

[0084] *Conversion from Cartesian space PDM to Lissajous space SDM*

[0085] In general, conversion from Cartesian space PDM to Lissajous space SDM can be represented as a matrix multiplication. In general, one can convert from a imaged area 600 in Cartesian space to a SBI sample vector, m , by solving the matrix equation:

$$[\text{SDV}] = \frac{[\text{PDV}]}{[\text{T}]}$$

[0086] The equation yields the multi-bit (analog) scan beam vector, SDV, which would result from a multi-bit (analog) Cartesian space matrix, PDM. Note that in cases where the transformation matrix, T, is not square, the creation of the inverse matrix (the result of $1/T$, being in the denominator) can be computationally challenging. As would be known in the art, linear algebra can be used to accomplish this inversion for rectangular matrices.

[0087] *Cartesian frames and FPA frames*

[0088] SBI imagers have a wider dynamic range per pixel and generally support more pixels than FPA devices. Therefore, there will not be a one-to-one mapping for each SBI data point to each Cartesian pixel. As would be well known in the art, the conversion process from SBI space to FPA space would therefore be lossy. To decrease loss, especially for image enhancement and storage of raw data purposes, the processor can internally use a much larger Cartesian frame with greater dynamic range than would be output to a monitor or received from an FPA or SBI device, and simply downsample and reduce the

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dynamic range appropriate to the monitor or storage device prior to outputting the video signal. Such a frame would facilitate a nearly lossless internal conversion between SBI and FPA spaces. It should be noted therefore, that this disclosure contemplates, and the claims should be read in light of, instances where the image processor uses an internal pixel frame that is both equal to, less than, or greater than that of an SBI or FPA pixel-oriented imaging device.

[0089] Conclusion

[0090] The numerous embodiments described above are applicable to a number of different applications. One particular application where the Combined SBI and FPA Image Processor is advantageous is in hospital operating room environments where space near a patient is at a premium and there is no room for multiple monitors, however there are many additional applications that would be apparent to one of ordinary skill in the art.

[0091] The embodiments of the invention shown in the drawings and described above are exemplary of numerous embodiments that may be made within the scope of the appended claims. It is contemplated that numerous other configurations of the disclosed system, process, and device for allowing different format imaging devices to use a common high resolution monitor may be created taking advantage of the disclosed approach. It is the applicant's intention that the scope of the patent issuing herefrom will be limited only by the scope of the appended claims.

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What is claimed is:

1. An FPA and SBI image processor for FPA and SBI imaging devices, the apparatus comprising:
 - a first input port adapted for accepting a first SBI formatted digital sample data stream;
 - a second input port adapted for accepting a video signal from an FPA video source;
 - an FPA processor for rendering the video signal from the FPA video source to a second SBI formatted digital sample data stream;
 - a selector for selecting an SBI formatted digital sample data stream from the first or second SBI formatted digital sample data streams for processing;
 - an SBI processor means for generating processed data by processing the selected SBI formatted digital sample data stream; and
 - an output port adapted for outputting the processed data.
2. The apparatus of claim 1 further comprising a high resolution monitor adapted to accept the processed data from the output port.
3. The apparatus of claim 2 wherein the high resolution monitor is selected from the group consisting of:
 - an SBI compatible monitor; and
 - a pixel-oriented FPA compatible monitor.

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4. The apparatus of claim 2 where the high resolution monitor is a wearable heads-up display.
5. The apparatus of claim 1 further comprising an archive adapted to accept the processed data from the output port.
6. The apparatus of claim 5 wherein the archive is selected from the group consisting of:
 - an SBI compatible archive; and
 - a pixel-oriented FPA compatible archive.
7. The apparatus of claim 1 where the FPA processor further comprises:
 - a frame grabber for acquiring an FPA video frame from the video signal; and
 - a frame mapper for rendering the FPA video frame into an SBI formatted digital sample data stream.
8. The apparatus of claim 1 where the FPA video source is one selected from the group consisting of:
 - the output of an FPA camera;
 - the output of a video recording device;
 - the output of an FPA video processor; and
 - a computer synthesized video stream.

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9. An FPA and SBI image processor that allows both FPA and SBI imaging devices to use a common high resolution monitor and archive, the apparatus comprising:
 - an input port adapted for accepting a first SBI formatted digital sample data stream;
 - an input port adapted for accepting a video signal comprised of a first series of pixel-oriented video frames from an FPA video source;
 - a processor capable of (a) converting the first series of pixel-oriented video frames in the video signal to a second SBI formatted digital sample data stream; (b) rasterizing the first SBI formatted digital sample data stream into a second series of pixel-oriented video frames; (c) selecting a first output from the first SBI formatted digital sample data stream, the second SBI formatted digital sample data streams, the first series of pixel-oriented video frames, and the second series of pixel-oriented video frames; and (d) rendering the first output to a suitable format for the high resolution monitor; and
 - an output port adapted for outputting the first output to the high resolution monitor.
10. The apparatus of claim 9 where the processor is capable of performing image enhancing algorithms on the first SBI formatted digital sample data stream, the second SBI formatted digital sample data streams, the first series of pixel-oriented video frames, and the second series of pixel-oriented video frames.
11. The apparatus of claim 9 where the output port includes circuitry and a physical connector for connecting to a high resolution pixel-oriented FPA monitor.

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12. The apparatus of claim 9 where the output port includes circuitry and a physical connector for connecting to a high resolution SBI monitor.
13. The apparatus of claim 9 where the processor is further capable of (e) selecting a second output from the first SBI formatted digital sample data stream, the second SBI formatted digital sample data streams, the first series of pixel-oriented video frames, and the second series of pixel-oriented video frames; and further comprising:
 - an archive output port adapted for outputting the second output to the archive device when triggered by a user.
14. The apparatus of claim 13 where the archive output port includes circuitry and a physical connector for connecting to a pixel-oriented archive device.
15. The apparatus of claim 13 where the archive output port includes circuitry and a physical connector for connecting to an SBI archive device.
16. The apparatus of claim 9 where the FPA video source is one selected from the group consisting of:
 - the output of an FPA camera;
 - the output of a video recording device;
 - the output of an FPA video processor; and
 - a computer synthesized video stream.

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17. A method for allowing both an FPA video source and an SBI imaging device to use a common high resolution monitor and archive, the method comprising the steps of:

acquiring, as a first source, a series of pixel-oriented frames of video from the FPA video source;

inputting, as a second source, an SBI formatted digital sample data stream from the SBI imaging device;

selecting, as an output selection, one of the first source and the second source;

outputting the output selection to the high resolution monitor; and

triggering the output selection to be sent to the archive.

18. The method of claim 17, the method further comprising the step:

performing image enhancement processes on the output selection prior to outputting.

19. The method of claim 17, the method further comprising the step:

converting the first source into an SBI format.

20. The method of claim 17, the method further comprising the steps:

rasterizing the second source into a pixel-oriented FPA format; and

rendering the output selection to a suitable high resolution FPA video signal for use with the high resolution monitor.

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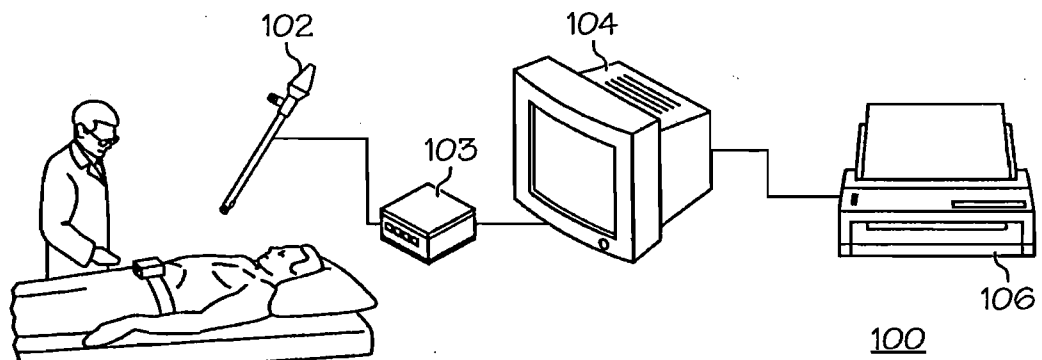


FIG. 1
(PRIOR ART)

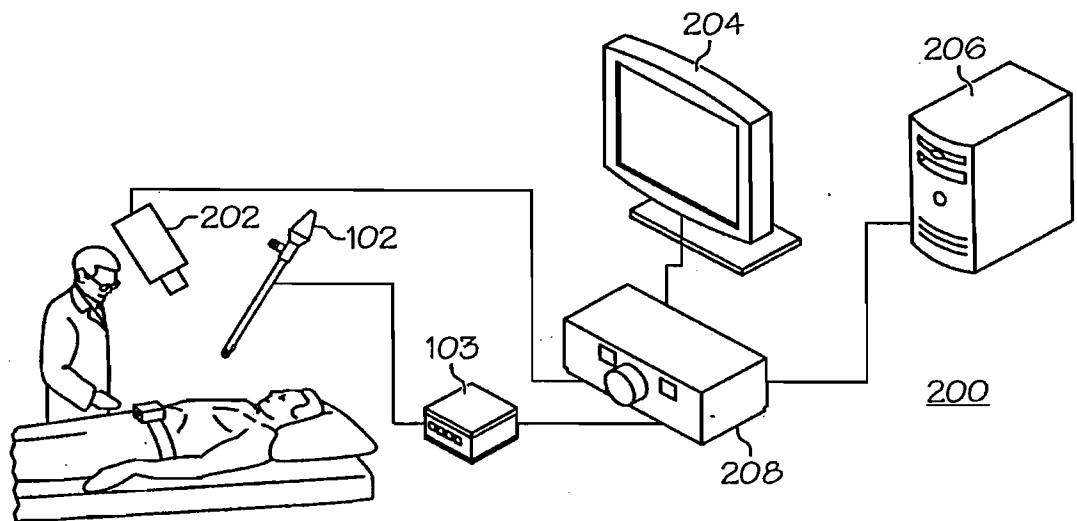


FIG. 2

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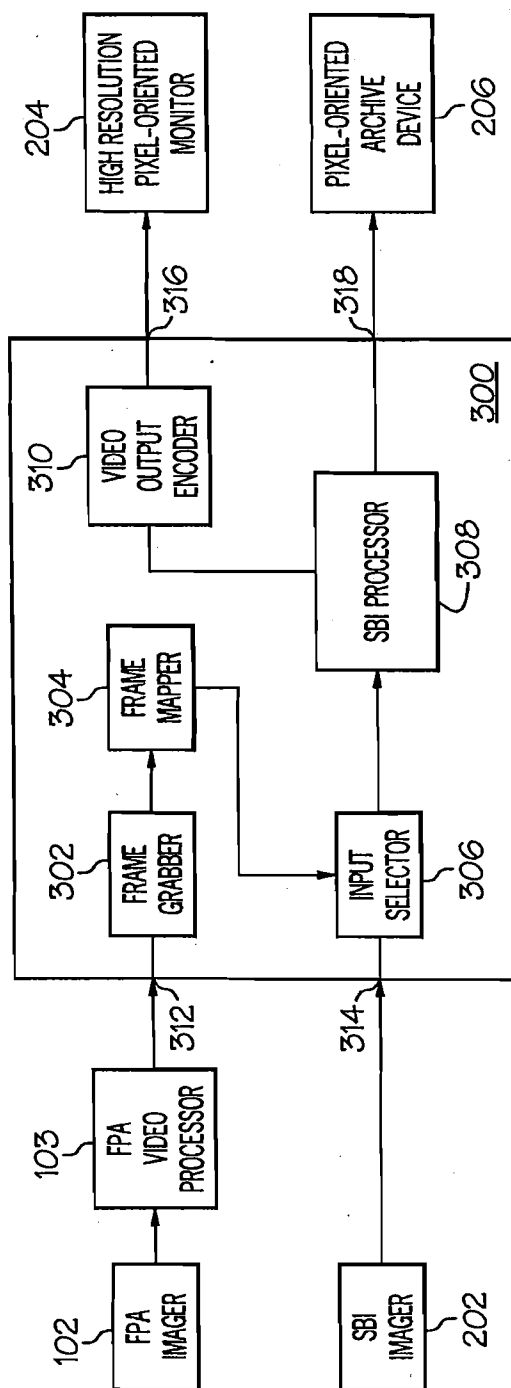


FIG. 3

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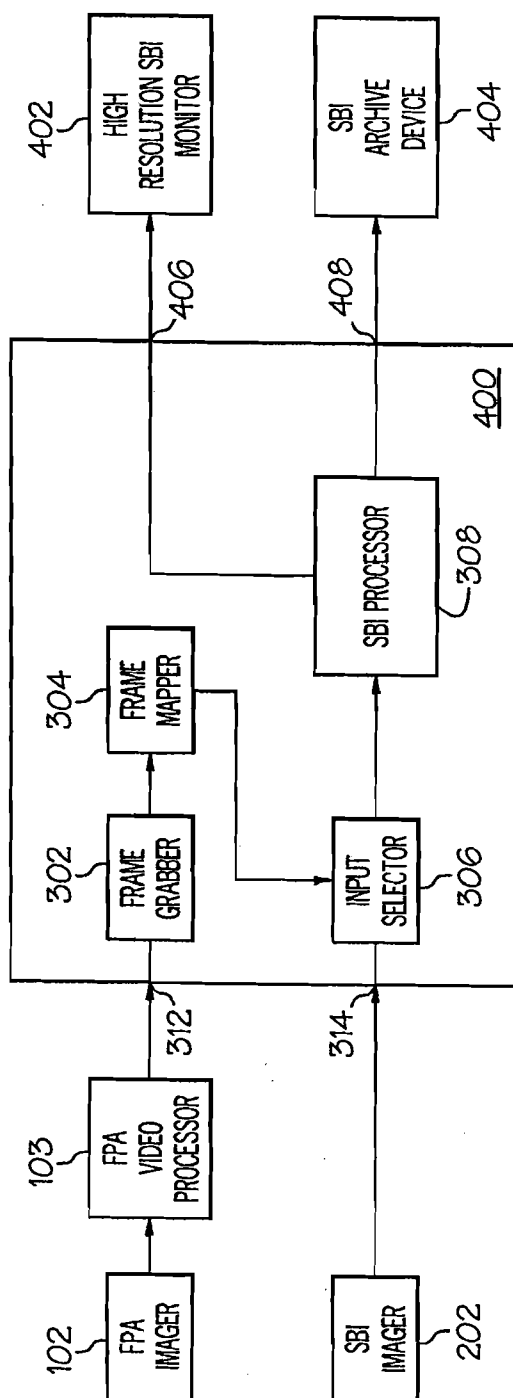


FIG. 4

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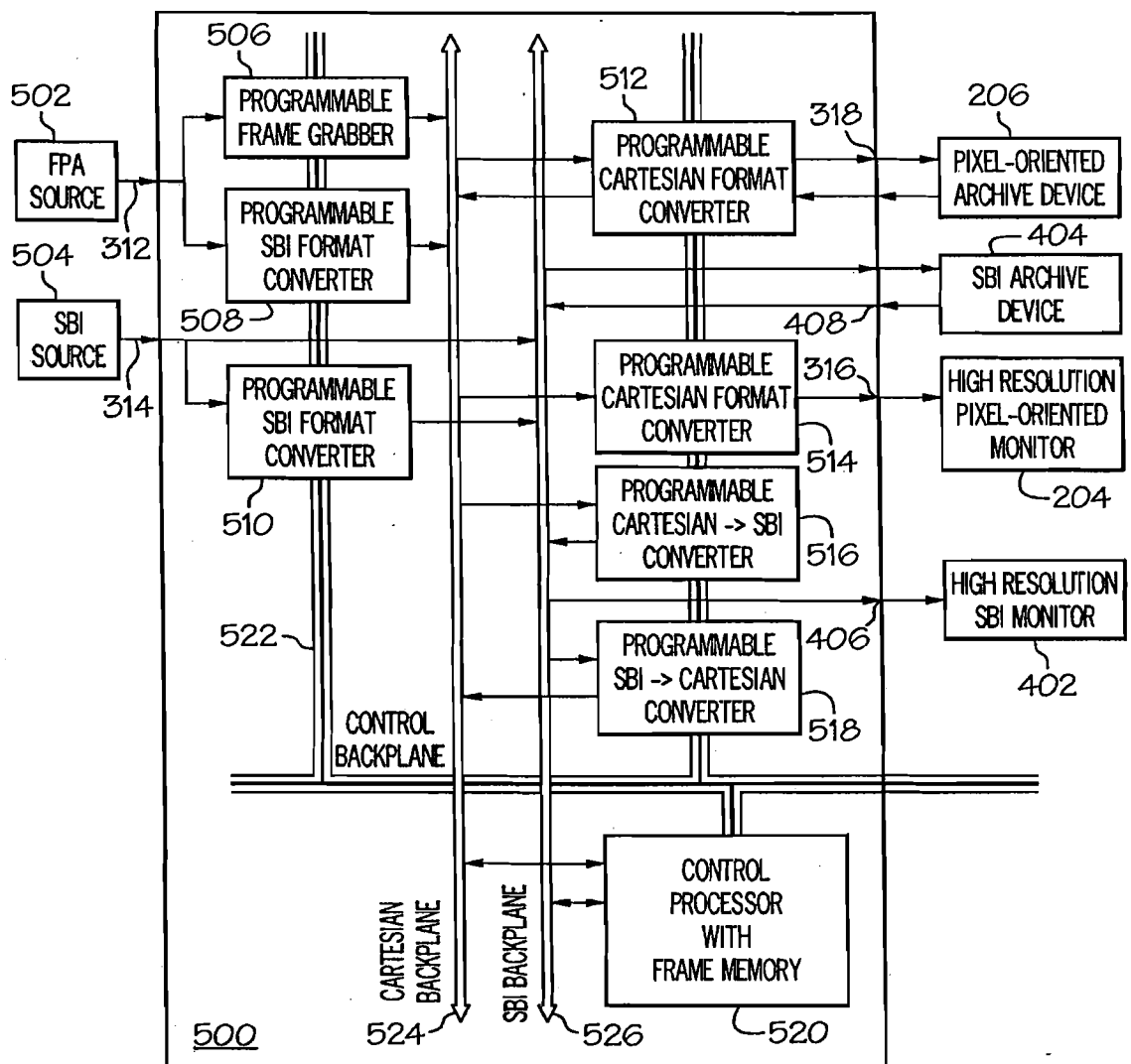


FIG. 5

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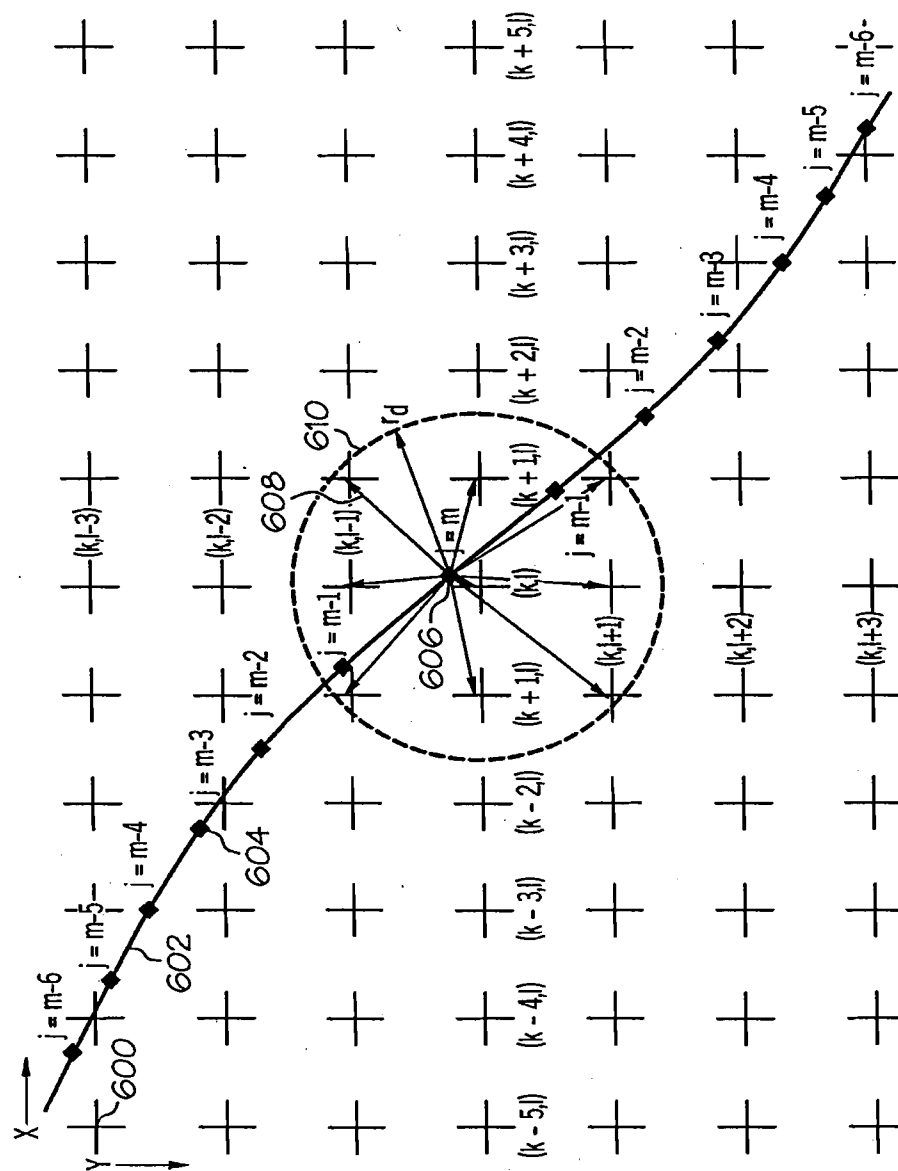


FIG. 6

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2008/059235

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04N3/30

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H04N G09G G06T

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2006/195014 A1 (SEIBEL ERIC J [US] ET AL) 31 August 2006 (2006-08-31) paragraph [0060] - paragraph [0064] paragraph [0100] - paragraph [0102] -----	1,9,17
A	WO 03/088643 A (MICROVISION INC [US]; BRIGHT GREGORY SCOTT [US]; STRAKA SCOTT W [US];) 23 October 2003 (2003-10-23) page 63, paragraph 15 - page 65, paragraph 2 figures 24A, 24B abstract ----- -/-	1,9,17

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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Date of the actual completion of the international search

4 July 2008

Date of mailing of the international search report

14/07/2008

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INTERNATIONAL SEARCH REPORT

International application No

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	<p>US 2005/116038 A1 (LEWIS JOHN R [US] ET AL LEWIS JOHN R [US] ET AL) 2 June 2005 (2005-06-02) paragraph [0008] - paragraph [0022] paragraph [0051] paragraph [0057] paragraph [0061] -----</p>	1,9,17

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Information on patent family members

International application No.

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