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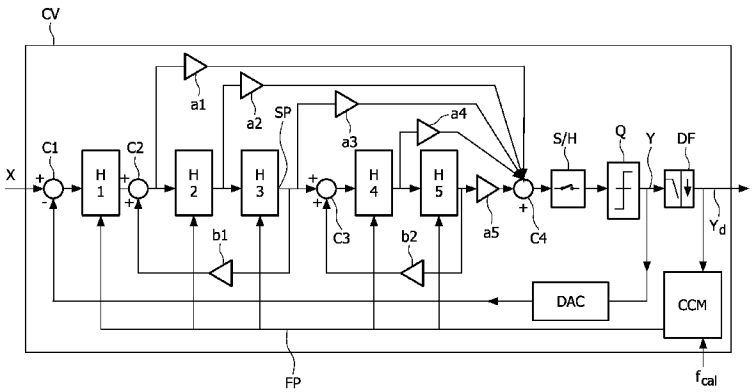
(54) **Title:** CONTINUOUS-TIME SIGMA-DELTA ANALOG-TO-DIGITAL CONVERTER WITH CAPACITOR AND/OR RESISTANCE DIGITAL SELF-CALIBRATION MEANS FOR RC SPREAD COMPENSATION



(57) **Abstract:** A continuous-time sigma-delta analog-to-digital converter (CV) comprises i) a signal path (SP) comprising at least one combiner (Cl) for combining analog signals to convert with feedback analog signals, at least two integrators (Hl, H5), mounted in series, to integrate the combined analog signals, a quantizer (Q) for converting the integrated signals into digital signals, and a decimation filter (DF) for filtering digital signals, and ii) a feedback path (FP) comprising at least a digital-to-analog converter (DAC) for converting the digital signals output by the quantizer (Q) into feedback analog signals intended for the combiner (Cl). Each integrator (Hl, H5) comprises variable capacitance means arranged to be set in chosen states define by the values of a digital word, to present chosen capacitances. The converter (CV) also comprises a self-calibration control means (CCM) arranged a) to generate a digital word with a chosen first value, b) to estimate an in-band noise IBN(n) from the filtered digital signals and to compare this IBN(n) to the preceding IBN(n-l), c) to modify the digital word value to decrease the capacitance of each integrator from a chosen decrement when IBN(n) is smaller than IBN(n-l), d) to iterate steps b) and c) till IBN(n) be greater than IBN(n-l), and to choose as calibration digital word value the value corresponding to IBN(n- 1) to set the calibration state of the variable capacitance means.

WO 2007/085997 A1

CONTINUOUS-TIME SIGMA-DELTA ANALOG-TO-DIGITAL CONVERTER WITH CAPACITOR AND/OR RESISTANCE DIGITAL SELF-CALIBRATION MEANS FOR RC SPREAD COMPENSATION

Field of the invention

The present invention relates to the domain of radio signal processing, and more precisely to continuous-time (CT) sigma-delta (ΣΔ) analog-to-digital converters (ADCs) used for converting analog radio signals.

Background of the invention

As is known to a person skilled in the art, CT ΣΔ ADCs are frequently used in numerous domains and especially in wireless radio receivers (or transceivers) used in radio communication equipment, such as mobile phones, where selected analog radio signals need to be converted into digital signals before being demodulated.

Such converters are notably described in the document by K.Philips et al "A 2mW 89 dB DR Continuous-Time ΣΔ ADC with Increased Immunity to Wide-Band Interferers", ISSCC Dig. Tech. Papers, pp 86-87, February 2004, and in the patent document WO 01/03312.

These converters offer some meaningful advantages over discrete-time (DT) implementations, and notably an implicit anti-aliasing filter, no front-end sample and hold S/H (there is a S/H but it is located after the loop filter which therefore is not discrete-time but continuous-time and enables to build anti-aliasing property in the ΣΔ ADC loop), the absence of kT/C noise and speed advantages, which all lead to a lower power consumption.

Nevertheless, in baseline deep-submicron CMOS technology (with low voltage supply: for instance 1.2 V in CMOS90LP), the continuous time loop filter of a CT ΣΔ ADC is built with RC integrators which are very sensitive to process variations and temperature spread of their analog components.

In fact the time constant, and hence the unity gain frequency, of these RC integrators depends on their RC product and therefore on the types of their resistances and capacitors (for instance P+ poly or N+ poly resistances and fringe capacitors in case of CMOS technology)

which are very sensitive to process variations and temperature spread. In CMOS technology, the process spread increases as the technology is scaling down. For instance, the worst case spread on the RC product is approximately +/-25% in 90 nm-CMOS technology, and approximately +/-40% in 65 nm-CMOS technology.

It can be shown that in the presence of a full-scale input signal, the RC time constant variations modify the CT ΣΔ ADC output spectrum in two different ways. Firstly, when the RC time constants of the integrators are too large, the quantization noise shifts to the bandwidth and reduces the signal-to-noise ratio (SNR) performance. Secondly, when the RC time constants of the integrators are too small, the loop filter becomes unstable because the noise transfer function is too aggressive. In both situations, the in-band noise (IBN) increases and consequently the signal-to-noise ratio decreases.

For instance, a 1-bit, single loop, feedforward CT ΣΔ ADC clocked at 288 MHz with 70 dB SNR in 4 MHz is suitable for highly digitized ZIF DVB H receiver. In this case, the simulated signal-to-quantization noise ratio (SQNR) is equal to 80 dB when the RC time constant is nominal, and if one takes into account the circuit noise (thermal noise, 1/f noise and clock jitter), then the nominal SNR is equal to 72 dB. Therefore, no more than +/-10% spread can be tolerated on the RC time constant. The spread on the RC product being +/-25% in the 90 nm-CMOS technology, this means that the RC time constant needs to be calibrated.

In the document of J.H. Shim et al, "A Hybrid Delta-Sigma Modulator with Adaptative Calibration", in proc. IEEE ISCAS, May 2003, pp.10251028, it has been proposed to use analog and digital integrators and to calibrate the digital integrators to match the analog integrators and then to keep good SNR performance. More precisely, the decimation filter output is monitored and the digital integrators are controlled, so that the SNR of the decimated output be maximized.

To simplify the SNR measurement during calibration, a special input pattern must be used. This input pattern is an impulse train whose fundamental frequency lies out-of-band. Because of this specific input pattern, the decimated output does not contain any signal component, so that the IBN must be estimated by calculating the variance of the output stream (a steepest descent algorithm updates the digital coefficients of the digital integrators to minimize the variance). Unfortunately this steepest descent algorithm has a very slow convergence. Approximately 400 iterations are necessary to converge to the calibration values, which takes too much time (for instance 91 ms for 400 iterations with 2^{16} samples at 288 MHz ($400*2^{16}/288.10^{6}$= 91 ms)) and then prohibits calibration before each use of the CT ΣΔ ADC.

Summary of the invention

So, the object of this invention is to improve the situation at least partly, and notably to provide a CT ΣΔ ADC with capacitance and/or resistance digital self-calibration means, which neither requires a dedicated test signal nor external calibration equipment.

For this purpose, it provides a continuous-time sigma-delta analog-to-digital converter (CT ΣΔ ADC), for converting analog signals into digital signals, comprising i) a (main) signal path comprising at least one combiner for combining analog signals to be converted with feedback analog signals, at least two integrators mounted in series and adapted to integrate the combined analog signals, a quantizer for converting the integrated signals into digital signals, and a decimation filter for filtering huge out-of band quantization noise and for reducing the bitstream data rate, and ii) a feedback path comprising at least a digital-to-analog converter (DAC) for converting the digital signals output by the quantizer into feedback analog signals intended for the combiner.

This converter (CT ΣΔ ADC) is characterized in that:

- at least one of its integrators comprises variable capacitance means and/or variable resistance means arranged to be set in chosen states depending on the values of a digital word in order to present chosen capacitances and/or chosen resistances, and
- it also comprises a self-calibration control means arranged :
  - a) to generate a digital word with a chosen first value,
  - b) then to estimate in-band noise IBN(n) from the filtered digital signals and to compare this in-band noise IBN(n) to the preceding in-band noise IBN(n-1),
  - c) then to modify the value of the digital word in order to decrease the capacitance and/or the resistance of each integrator concerned from a chosen decrement when IBN(n) is smaller than IBN(n-1),
  - d) then to iterate steps b) and c) till IBN(n) is equal to or greater than IBN(n-1), and to choose as a calibration digital word value the value corresponding to the preceding in-band noise IBN(n-1) in order to set the calibration state of the variable capacitance means and/or variable resistance means.

The converter (CT ΣΔ ADC) according to the invention may include additional characteristics considered separately or combined, and notably:

- each variable capacitance means may comprise a chosen number of banks of capacitors, with a chosen capacitance, mounted in series with a two-state switch (S), and controlled by

one bit value of the digital word;

- in step a) the self-calibration control means may be arranged to generate a digital word having a first value corresponding to a first capacitance equal to a chosen starting capacitance with a chosen increase step;
  - the starting capacitance may correspond to a given spread of the integrator RC product;
  - the chosen increase step may be equal to 33% of said starting capacitance, for instance;
  - the decrement may be equal to a chosen proportion of the starting capacitance, depending on a process variation value, a temperature spread and a final targeted accuracy;
  - the number of capacitors may be equal to 9, for instance. In this case, the nine capacitors offer together a maximum value equal to 4/3 of the starting capacitance, a first one of these nine capacitors having a value equal to 2/3 of the starting capacitance), each of the eight other capacitors having a value equal to 1/12 of the starting capacitance, and the decrement being equal to 1/12 of the starting capacitance;

- each variable resistance means may comprise a chosen number of resistors, connected in series and having chosen respective resistances, and a same chosen number of two-state switches each controlled by one bit value of the digital word and respectively controlling the accesses to these resistors;
  - in step a) the self-calibration control means may be arranged to generate a digital word having a first value corresponding to a first resistance equal to a chosen starting resistance with a chosen increase step;
    - the starting resistance may correspond to a chosen spread of the integrator RC product;
    - the chosen increase step may be equal to 33% of the starting resistance, for instance;
    - the decrement may be equal to a chosen proportion of the starting resistance;
    - the number of resistors may be equal to 9, for instance. In this case, the nine resistors offer together a maximum value equal to 4/3 of the starting resistance, a first one of these nine resistors having a value equal to 2/3 of the starting resistance, each of the eight other resistors having a value equal to 1/12 of the starting resistance, and the

decrement being equal to 1/12 of the starting resistance;

- it may be arranged to work in a differential mode. In this case, it may comprise two differential input nodes arranged to be fed with differential analog signals to be converted;
  - ➢ the two differential input nodes may be shortcut during the calibration steps a) to d);
- its signal path may comprise three, four or five (or else more than five) integrators mounted in series;
- the CT ΣΔ ADC filter loop can be a single filter loop or a cascaded filter loop (also called MASH) built with cascading several CT ΣΔ ADC stages, each being either a first order CT ΣΔ ADC or a second order CT ΣΔ ADC;
- it comprises high-frequency stabilization means (feedforward or feedback or a mixture of feedforward and feedback coefficient(s));
- the DAC and the quantizer may be single bit or multi-bit ones.

The invention also provides an integrated circuit (IC), and possibly a baseband integrated circuit, comprising a converter such as the one introduced above. Such a (baseband) integrated circuit may be part of a receiver or transceiver device.

The invention also provides mobile radio communication equipment comprising a converter or a (baseband) integrated circuit or a receiving or transceiver device such as the ones introduced above.

Brief description of the drawings

Other features and advantages of the invention will become apparent on examining the detailed specifications hereafter and the appended drawings, wherein:

- Fig.1 schematically illustrates an example of a receiver device according to the invention,
- Fig.2 schematically illustrates an example of embodiment of a **1**-bit, single-loop, feedforward continuous-time sigma-delta analog-to-digital converter (CT ΣΔ ADC) according to the invention,
- Fig.3 schematically illustrates an example of embodiment of the first integrator of the CT ΣΔ ADC illustrated in Fig.2, in a differential working mode,
- Fig.4 schematically illustrates an example of embodiment of the first integrator of the CT ΣΔ ADC illustrated in Fig.2, in a single-ended working mode,
- Fig.5 schematically illustrates an example of embodiment of the fifth (and last, if the CT ΣΔ ADC is a fifth order one) integrator of a 1-bit, single-loop, feedback CT ΣΔ ADC, variant of the CT ΣΔ ADC illustrated in Fig.2, in a differential working mode,

- Fig.6 schematically illustrates an example of embodiment of the fifth (and last, if the CT ΣΔ ADC is a fifth order one) integrator of a 1-bit, single-loop, feedback CT ΣΔ ADC, variant of the CT ΣΔ ADC illustrated in Fig.2, in a single-ended working mode,
- Fig.7 schematically illustrates an example of embodiment of a variable capacitance means for an integrator illustrated in Fig.3,
- Fig.8 schematically illustrates an example of embodiment of a variable resistance means for an integrator (except the first one H1) of a CT ΣΔ ADC according to the invention,
- Fig.9 schematically illustrates an example of embodiment of a self-calibration control module of a CT ΣΔ ADC according to the invention,
- Fig.10 schematically illustrates an example of evolution of the in-band noise (INB), in dB, as a function of the RC spread, in %, and the number of calibration iterations required when the starting capacitance (Ci) of the integrators is either equal to 0.8 Copt (where Copt is a nominal capacitance) or equal to 1.2 Copt,
- Fig.11 schematically illustrates an example of capacitance calibration algorithm intended to be implemented by a self-calibration control module.

The appended drawings may not only serve to complete the invention, but also to contribute to its definition, if need be.

Description of the preferred embodiments

Reference is initially made to Fig.1 to describe an example of receiver device R in which the invention may be applied. It is important to notice that the invention is not limited to receiver devices. Indeed it applies also to transceiver device, and more generally to any type of device adapted to receive analog radio signals to be converted into digital signals.

In the following description it will be considered that the receiver (or transceiver) device R is intended for mobile communication equipment such as a mobile phone, for instance a GSM or GPRS/EDGE or UMTS mobile phone, or Bluetooth or WLAN (Wireless Local Area Network) communication equipment. But it is important to notice that the invention is not limited to this type of radio communication equipment. For instance, it may also be used for television on mobile applications (DVB-H), and for all DVB standards (DVB-S, DVB-T or DVB-C, for instance). These examples of application are not exhaustive, and some other standards could also benefit from the invention.

As schematically illustrated in Fig.1, a receiver (device) R according to the invention notably comprises an antenna AN adapted to receive analog modulated signals and a

processing module PM fed with the received analog signals.

The processing module PM comprises a low noise amplifier LNA arranged to amplify the analog signals received by the antenna AN to feed a mixer MX which feeds a continuous-time sigma-delta analog-to-digital converter or CT ΣΔ ADC (hereafter named "converter") CV according to the invention, arranged to convert and filter the amplified analog signals into digital signals to feed a module M1 dedicated to channel filtering and noise-shaping digital filtering and feeding a digital demodulator DD arranged to demodulate the filtered digital signals.

Reference is now made to Fig.2 to describe an example of converter CV according to the invention.

As illustrated the converter CV comprises at least a signal path SP comprising at least one combiner C1 for combining the amplified analog signals to be converted with feedback analog signals, at least two integrators H1 and H2, mounted in series, for integrating the combined analog signals output by the combiner C1, a quantizer Q for converting the integrated signals output by the integrators H1 and H2 into digital signals Y, and a decimation filter DF for filtering the high-frequency quantization noise and reducing the bitstream data rate, and outputting filtered digital signals Y_d.

In the illustrated example of Fig.2 the converter CV comprises five integrators H1-H5 mounted in series in the signal path SP to define a 5-th order filter. But the number of integrators (and then the order of the filter) is not limited to this example. It may be equal to any value greater than 2 to define at least a 2nd order filter in the signal path SP.

Each integrator Hj (j = 1 to 5) is an active RC filter, such as an OTA-RC (Operational Transconductance Amplifier-RC), which achieves an excellent linearity performance.

The converter CV further comprises a feedback path FP comprising at least a digital-to-analog converter DAC arranged to convert the digital signals Y output by the quantizer Q into feedback analog signals intended for the combiner C1 (at least).

Although it is not illustrated in Fig.2, the feedback path FP could be provided with at least one analog weighting means arranged to apply a chosen weighting coefficient to the feedback analog signals output by the DAC to convert them into weighted feedback analog signals intended for the combiner C1. In fact the feedback path FP may be provided with as many analog weighting means (applying different weighting coefficients) as integrators Hj

(here j = 1 to 5). The analog weighting means may be transconductances or voltage attenuators, for instance. They are used to stabilize the ADC loop. In this case the signal path SP must comprise one combiner before each integrator in order to feed the latter with combined received analog signals and weighted feedback analog signals. Each combiner is then arranged to subtract the weighted feedback analog signals it receives from the associated analog weighting means from the analog signals it receives either from the mixer MX or from the preceding integrator Hj-1.

To offer a high-frequency filtering the converter CV may have a feedback and/or feedforward topology.

A non mandatory 1-bit, single-loop, feedforward topology is illustrated in Fig.2. More precisely in this example of embodiment the converter CV comprises two local resonator feedback means b1 and b2 mounted in parallel with the signal path SP. These local resonator feedback means may be transconductances or voltage attenuators, for instance. They are used to create notch(es) in the noise transfer function (NTF) to optimize the signal-to-quantization noise ratio (SQNR) in the bandwidth.

Each local resonator feedback means b1 or b2 is arranged to weight the integrated analog signals output by a chosen integrator H3 or H5 with a chosen coefficient to feed a combiner C2 or C4 with weighted analog signals, which combiner is located in the signal path SP before the integrator H2 or H4, itself located before this chosen integrator H3 or H5.

In this case each combiner (here C2 and C4) has an additional additive input to combine the integrated analog signals output by the preceding integrator (H1 or H3) with the weighted analog signals output by the local resonator feedback means b1 or b2 (and possibly with weighted feedback analog signals output by analog weighting means).

The converter CV may comprise only one local resonator feedback means (for instance b1 or b2) or more than two local resonator feedback means when the number of integrators Hj (or the filter order) is greater than or equal to 4.

In the non limiting example of embodiment illustrated in Fig.2, the converter CV further comprises four weighted feedforward summation path a1-a4 mounted in parallel with the signal path SP, respectively between the output of the first H1, second H2, third H3 and fourth H4 integrators and the fourth combiner C4, and another weighted feedforward summation means a5 mounted in series in the signal path SP between the output of the fifth integrator H5 and the fourth combiner C4.

Each weighted feedforward summation path or means aj is arranged to weight, with a

chosen coefficient, the integrated analog signals output by the preceding integrator (here Hj) to feed the fourth combiner C4 with weighted analog signals. For this purpose the fourth combiner C4 has as many additive inputs as weighted feedforward summation paths and means aj (here five) to feed the quantizer Q with the sum of all the weighted integrated analog signals output by the integrators H1-H5.

These weighted feedforward summation paths and means aj are also used to stabilize the ADC loop. Therefore, they may be mixed with the analog weighting means dj to maximize the advantages and minimize the drawbacks of the two topologies. But the cumulated number of weighted feedforward summation paths and means aj and analog weighting means must be equal to the filter order (L).

The invention proposes to integrate digital self-calibration means into the converter CV to allow calibration of the analog capacitors and/or resistors of at least one RC integrator Hj, to compensate process variations and temperature spread.

According to the invention at least one integrator Hj of the converter CV comprises variable capacitance means Cj and/or variable resistance means Rj. In the example illustrated in Figs.3 to 6 the integrators H1 and H5 (but this is also the case of integrators H2 to H4 of Fig.2) only comprise a variable capacitance means Cj arranged to be set in chosen states depending on the values of a digital word. So a specific capacitance value of each variable capacitor means Cj of each integrator Hj corresponds to each digital word value.

In practice all the capacitors are of the same type (for instance fringe or gate-oxyde capacitors), so the same correction is applied to each variable capacitor (as is described in the example of algorithm described below with reference to Fig.11).

In Fig.3, the feedforward coefficients Aj are implemented with resistors, but they could be also implemented with capacitors.

In Figs.3 and 5 the first H1 and last H5 integrators are illustrated in a differential working mode. So, each integrator Hj comprises a transconductance Tj with a differential input and a differential output.

Each differential input receives differential analog signals coming either from differential input nodes N1 and N2 of the converter CV (case of H1) or from a differential output of the preceding integrator Hj-1 (case of H2 to H5), through a resistor Rj (which can be variable and addressable by the digital word). A two-state control switch SW may be provided

between the first N1 and second N2 differential input nodes.

In Figs.4 and 6 the first H1 and last H5 integrators are illustrated in a single-ended working mode. So, each integrator Hj comprises a transconductance Tj with a single-ended input fed with analog signals and a single-ended output.

A non-limiting example of embodiment of a variable capacitance means Cj is illustrated in Fig.7. In this example, the variable capacitance means Cj consists of 9 couples connected in parallel and each comprising a capacitor, with a chosen capacitance, and a two-state switch S mounted in series with the capacitor. Each two-state switch S is controlled by one bit value of the digital word generated by a self-calibration control module CCM which will be described below.

For instance, and as illustrated in Fig.7, the number of couples may be equal to 9. In this case, the nine capacitors mounted in parallel offer together a maximum capacitance value equal to 4/3 of a starting capacitance Ci (4Ci/3).

A first one of the nine capacitors has a value equal to 2/3 of the starting capacitance Ci (2Ci/3), while each one of the eight other capacitors has a value equal to 1/12 of the starting capacitance Ci (Ci/12), for instance.

As illustrated, the switch S connected to the first capacitor (with the capacitance value equal to 2Ci/3) is preferably controlled by the digital word bit having the most significant weight (MSB), while the switch S connected to the last (or ninth) capacitor (with a capacitance value equal to Ci/12) is controlled by the digital word bit being the least significant bit (LSB).

With such an arrangement, it is possible to define first and second parts into a variable capacitance means Cj. The first part comprises the first to fifth couples and offers a maximum capacitance value equal to the starting capacitance Ci, while the second part comprises the sixth to ninth couples and offers a maximum capacitance value equal to 1/3 of the starting capacitance Ci (Ci/3).

Moreover, this arrangement allows to vary the capacitance value of each variable capacitance means Cj by a decrement (or increment) equal to 1/12 of the starting capacitance Ci (Ci/12).

A non-limiting example of embodiment of a variable resistance means Rj (with j≠1 as will be explained below) is illustrated in Fig.8. In this example, the variable resistance means Rj consists of nine resistors, connected in series and having chosen respective resistances, and nine two-state switches connected in parallel between the last resistor and two consecutive resistors, respectively.

Each two-state switch S is controlled by one bit value of the digital word generated by the self-calibration control module CCM.

For instance, and as illustrated in Fig.7, the number of couples may be equal to 9. In this case, the nine resistors mounted in series offer together a maximum resistance value equal to 4/3 of a starting resistance Ri (4Ri/3).

A first one of the nine resistors has a value equal to 2/3 of the starting resistance Ri (2Ri/3), while each one of the eight other resistors has a value equal to 1/12 of the starting resistance Ri (Ri/12), for instance.

As illustrated the switch S connected to the first resistor on the right side (to offer a cumulative resistance value equal to 4Ri/3) is preferably controlled by the digital word bit being the most significant bit (MSB), while the switch S connected to the last (or ninth) resistor on the left (to offer a resistance value equal to 2Ri/3) is controlled by the digital word bit being the least significant bit (LSB). With this arrangement, only one switch is "on" while all the others are off.

With such an arrangement, it is possible to define first and second parts into a variable resistance means Rj. The first part comprises the first to fifth resistors and offers a maximum resistance value equal to the starting resistance Ri, while the second part comprises the sixth to ninth resistors and offers a maximum resistance value equal to 1/3 of the starting resistance Ri (Ri/3).

Moreover, this arrangement allows to vary the resistance value of each variable resistance means Rj (with j≠1) by a decrement (or increment) equal to 1/12 of the starting resistance Ri (Ri/12).

In the differential working mode (Figs.3 and 5) the digital-to-analog converter DAC of the feedback path FP has one input connected to the signal path SP to be fed with digital signals Y and differential outputs connected to the differential inputs of the first integrator H1. Such a DAC may be a switched capacitor DAC, for instance.

In the single-ended working mode (Figs.4 and 6) the digital-to-analog converter DAC of the feedback path FP has one input connected to the signal path SP to be fed with

digital signals Y and one output connected to the single-ended input of the first integrator H1.

Moreover, in the differential working mode each integrator Hj comprises two banks of variable capacitors Cj respectively connected in series with resistances rj (not variable - each resistance "rj" helps to stabilize the OTA-RC structure and has preferably a different value for each integrator Hj) into a differential feedback path. In the single-ended working mode each integrator Hj comprises one bank of variable capacitors Cj respectively connected in series with resistances rj in a single-ended feedback path.

Still in the differential working mode the optional weighted feedforward summation paths and means a1-a5, but also the optional local resonator feedback means b1 and b2, are differential.

As illustrated in Figs.2 to 6, the converter CV according to the invention also comprises a self-calibration control module CCM having an input connected to the signal path SP after the decimation filter DF, to be fed with filtered digital signals Y_d, and coupled to each variable capacitor means Cj and/or each variable resistor means Rj, to provide it (them) with a chosen digital word to control its (their) capacitance and/or resistance.

This self-calibration control module CCM is arranged to implement a calibration algorithm comprising the following four main steps.

In a first main step a) the self-calibration control module CCM generates a digital word with a chosen first value. This value corresponds to a chosen first capacitance value and/or first resistance value of each variable capacitor means Cj and/or each variable resistor means Rj (with $j \neq 1$, i.e. R2 to R5).

For instance, if the converter CV comprises integrators Hj such as the one illustrated in Fig.3, the first value of the digital word corresponds to a first capacitance of each variable capacitor means Cj equal to a chosen starting capacitance Ci with a chosen increase step.

This starting capacitance Ci corresponds preferably to a chosen spread of the integrator RC product (or time constant). In analog integrated circuit (IC) design, the nominal value for a component (Ropt and Copt for instance) as well as the standard deviation from this nominal value due to process variations and temperature spread are well known inputs and are included in the modeling of the components. These inputs are used to set the starting capacitance Ci. In absence of any process variations and temperature spread Ci = Copt.

For instance and as illustrated in Fig.10, in the example of the evolution of the in-

band noise (IBN), in dB, as a function of the RC spread, the effective capacitance Ci can be Ci = 0.8 Copt, which corresponds to a capacitance spread of -20%, or Ci = 1.2 Copt, which corresponds to a C spread of +20%. However, the capacitance step must not only compensate for the capacitance variations but also for the resistance variations and temperature spread. The process variations and temperature spread depend on the technology (for instance they are different in CMOS 90 nm and CMOS 65 nm). Therefore, the Ci value must be chosen according to the CMOS technology used for the design.

The chosen increase step of the starting capacitance Ci may be equal to 33% (1/3) of this starting capacitance Ci, for nstance +Ci/3. So, in this case the first value of the digital word corresponds to a first capacitance of each variable capacitance means Cj equal to 4Ci/3 (Ci + Ci/3). This example of chosen increase step (+33%) is well adapted to the examples of variable capacitance means Cj and variable resistance means Rj described above with reference to Figs.7 and 8. These examples of embodiment of variable capacitance means Cj and variable resistance means Rj illustrated in Figs.7 and 8 allow a capacitance coverage corresponding to a RC spread comprised in the range [-25%; +33%].

A +33% increase step simplifies the algorithm and the calibration time. In fact, one does not try to solve an optimization problem (i.e. to optimize the IBN) with the risk of having a local optimum, but one just minimizes the IBN. As such one does not have to search for a gradient as in the state of the art, because one always knows the direction to take: one always decreases the capacitance and/or the resistance.

Other values of the chosen increase step of the starting capacitance Ci may be selected, if another CMOS technology is used for design and/or if an accuracy better than +/-10% is required.

In a second main step b) the self-calibration control module CCM estimates in-band noise IBN(n) (with n = 1) from the filtered digital signals Y_d currently output by the decimation filter DF and corresponding to the new values of the variable capacitance means Cj and/or variable resistance means Rj, defined by the generated digital word.

As illustrated in Fig.10, the IBN variations due to RC spread are not monotonic. The minimum of the IBN corresponds to the nominal RC value (no spread). Moreover, the absolute value of the IBN depends on the circuit noise. Since the circuit noise is temperature dependent, the absolute value of the IBN will vary depending on the die temperature during the calibration process. So, it is desirable to calibrate the RC product with a constant circuit noise.

If the calibration is achieved by triggering the resistance value Rj of each integrator Hj, the integrator noise will also change, because when optimizing the design for power consumption, resistor(s) R1 of the first integrator H1 is(are) usually the main noise contributor(s). So, it is not desirable to increase the resistance value of resistor(s) R1 and thus their thermal noise contribution because this would increase the total in-band noise (IBN) and reduce the signal-to-noise ratio (SNR). This situation happens as soon as the unity-gain frequencies of the integrators Hj are too high (i.e. when the RC product is smaller than the nominal one).

Therefore, it is preferable to calibrate the RC value by varying the capacitance value of the capacitors Cj of each integrator Hj. However, the loop filter topology being not sensitive to unity-gain variations of the first integrator H1, but very sensitive to the unity-gain frequency of the second to fifth integrators H2 to H5, a resistance calibration of the resistors Rj of each integrator Hj, except the first one H1, can be carried out. It is also possible to calibrate the capacitance value of the capacitors Cj of each integrator Hj and the resistance of the resistors Rj of each integrator Hj, except the first one H1.

For instance, the IBN is estimated by calculating the variance P_Q of the filtered digital signals Y_d, defined by the following relation:

$$P_Q = \frac{1}{N_S}\sum_{n=0}^{N_S-1}\left|y_d(n)\right|^2 - \left|\frac{1}{N_S}\sum_{n=0}^{N_S-1} y_d(n)\right|^2$$

where N_S is the number of samples used for estimation of IBN(n).

In order to implement such a variance computation, the self-calibration control module CCM may comprise an estimation module such as the one illustrated as an example in Fig.9.

In this example of embodiment, the upper branch (sub-modules SM1-SM4) determines the first member of the right part of the relation (P_Q) cited above, the lower branch (sub-modules SM5-SM8) determines the second member of the right part of the relation cited above, and the combiner SM9 subtracts the value provided by the sub-modules SM5-SM8 of the second branch from the value provided by the sub-modules SM1-SM4 of the first branch.

When the in-band noise IBN(n) is estimated, the self-calibration control module CCM stores it in a register A and compares it to the preceding estimated in-band noise

IBN(n-1), stored in a register B. When n = 1, IBN(1) is the first estimate. So one can set arbitrarily IBN(n-1) = IBN(0) to 0.

Then in a third main step c) the self-calibration control module CCM modifies the value of the digital word generated last in order to decrease the current capacitance value Ci of each variable capacitance means Cj of each integrator Hj from a chosen decrement Cstep and/or the resistance value of each variable resistance means Rj of each integrator Hj except the first one H1, when IBN(n) is smaller than IBN(n-1).

This decrement Cstep (or Rstep) may be equal to a chosen proportion of the starting capacitance Ci (or starting resistance Rj). It depends on the final accuracy.

For instance, the decrement Cstep (or Rstep) may be equal to Ci/12 (or Ri/12) when a +/-10% accuracy on the RC spread must be achieved. It is worth noting that the IBN must be predicted with less accuracy, which fixes the number of samples N_s required for the IBN estimation. This example of decrement is well adapted to the examples of variable capacitance means Cj and variable resistance means Rj described above with reference to Figs.7 and 8. These examples of embodiment of variable capacitance means Cj and variable resistance means Rj illustrated in Figs.7 and 8 allow to choose a decrement Cstep (or Rstep) situated in the range [Copt/15; Copt/10] (or [Ropt/15; Ropt/10]) when the accuracy is situated in the range [5%; 10%], for an initial capacitance (or resistance) increase step equal to 33%. So, the value of the decrement depends on the accuracy wanted.

Then in a fourth main step d) the self-calibration control module CCM iterates steps b) and c) till the currently estimated IBN(n) is equal to or greater than the previously estimated IBN(n-1). At most 9 iterations are necessary to converge to a final calibration value of the digital word. Thus the maximum calibration time t_{cal}, based on a number of samples $N_S = 2^{16}$ at a frequency f_S = 288 MHz, is given by the relation $t_{cal} = 9*(N_S/f_S) \approx 2$ ms.

When IBN(n) is equal to or greater than IBN(n-1), the self-calibration control module CCM chooses as the final calibration value of the digital word the value that corresponds to IBN(n-1). Then it generates this final calibration value in order to set the calibration state of each variable capacitance means Cj and/or each variable resistance means Rj.

Two examples of calibration are illustrated in Fig.10.

The first example corresponds to a RC spread of -25% (corresponding to Ci = 0.8 Copt). The calibration starts with a 33% increase of the starting capacitance Ci, and follows with a first iteration corresponding to a decrease of the Ci value by a decrement

Cstep = 6.66% Copt, and ends by an increase of the Ci value by an increment Cstep = 6.66% Copt. In this case the calibration time is approximately equal to 455 μs when $N_s = 2^{16}$ and $f_s = 288$ MHz.

The second example corresponds to a RC spread of +25% (corresponding to Ci = 1.2 Copt). The calibration starts with a 33% increase of the starting capacitance Ci, and follows with eight iterations each corresponding to a decrease of the current Ci value by a decrement Cstep = 10% Copt, and ends by an increase of the Ci value by an increment Cstep = 10% Copt.

A more detailed example of calibration algorithm dedicated to variable capacitance means Cj will be described now with reference to Fig.11.

In a preliminary starting step 10, one specifies in the self-calibration control module CCM the number N_S of samples to be used for estimating the IBN, and the length of two registers A and B respectively intended for storing the current IBN estimate (IBN(n)) and the preceding IBN estimate (IBN(n-1)).

In a step 20, the self-calibration control module CCM carries out a test to determine whether a calibration must be started or not.

If there is no need to start the calibration, then the calibration algorithm ends in a step 30 in which the self-calibration control module CCM may decide not to shortcut the differential input nodes N1 and N2 of the converter CV, for instance.

If the calibration must be started, then in a step 40, the self-calibration control module CCM may start by shortcutting the differential input nodes N1 and N2 of the converter CV by means of the control switch SW illustrated in Fig.3. This shortcutting operation is not mandatory because converter CV is self-biased due to the feedback mechanism. But this is preferable in order to avoid any distortion effect that could corrupt the IBN estimation.

Then the self-calibration control module CCM resets the value of registers A and B and the value of a counter (Count = 0), and generates a digital word with a chosen first value. For instance, this first value corresponds to a 33% increase of the starting capacitance Ci of each variable capacitance means Cj of each integrator Hj. So, the first value of the digital word sets the capacitance value of each variable capacitance means Cj to 4Ci/3 (Ci + Ci/3).

In a step 50, the self-calibration control module CCM stores the value of register A in register B, and increments the value of the counter by 1 (Count = Count + 1).

In a step 60, the self-calibration control module CCM estimates the in-band noise

IBN(n) (here n = 1) from the filtered digital signals Y_d.

In a step 70, the self-calibration control module CCM stores the estimated IBN value (IBN(1)) in register A.

In a step 80, the self-calibration control module CCM carries out a test to determine if the value of the counter is greater than 1 (Count > 1).

If this counter value is smaller than 1 (Count < 1), then the self-calibration control module CCM comes back to step 50.

If the counter value is greater than 1 (Count > 1), then the self-calibration control module CCM carries out another test in a step 90 to determine whether the value stored in register A is smaller than the value stored in register B.

If the A value is smaller than the B value (A < B, i.e. IBN(n) < IBN(n-1)), this means that the final calibration value has not been found yet. Then the self-calibration control module CCM carries out a step 100 in which it modifies the value of the digital word generated last in order to decrease the current capacitance value Ci of each variable capacitance means Cj of each integrator Hj from a chosen decrement Cstep. So each new capacitance value Ci becomes equal to Ci - Cstep (Ci = Ci - Cstep). Then the self-calibration control module CCM comes back to step 50 for a new iteration.

If the A value is greater than the B value (A > B, i.e. IBN(n) > IBN(n-1)), this means that the calibration value has just been passed. Then the self-calibration control module CCM carries out a step 110 in which it chooses the value that corresponds to IBN(n-1), stored in register B, as the final calibration value of the digital word. So it generates this final calibration value in order to set the calibration state of each variable capacitor means Cj. And the calibration algorithm ends in a final step 120.

It is important to notice that the digital-to-analog converter DAC and the quantizer Q illustrated in Figs.2-6 are of the single bit type. But the invention also applies to digital-to-analog converter DAC and quantizer Q of the multi-bit type.

Preferably, the converter CV is an integrated circuit IC, and possibly a baseband integrated circuit. Such an integrated circuit may be realized in CMOS technology or in any technology currently used in chip manufacture, and notably in AsGa or BiCMOS technology.

A converter CV according to the invention offers several advantages, and notably:

- it does not require any specific input pattern dedicated to calibration,
- it can be used to calibrate process and/or temperature variations,
- because of its very fast convergence (at most 9 iterations), it allows calibration each time it

needs to be used (for instance at each burst or at each time-slot),

- it can be arranged according to any topology, and not only to the feedforward topology.

The invention is not limited to the embodiments of continuous-time sigma-delta analog-to-digital converter, (baseband) integrated circuit, receiver device, transceiver device and radio communication equipment described above only by way of example, but it includes all alternative embodiments which may be considered by one skilled in the art to be within the scope of the claims hereafter.

CLAIMS

1. Continuous-time sigma-delta analog-to-digital converter (CV) for converting analog signals into digital signals, comprising i) a signal path (SP) comprising at least one combiner (C1) adapted to combine analog signals to be converted with feedback analog signals, at least two integrators (Hj) mounted in series and adapted to integrate said combined analog signals, a quantizer (Q) adapted to convert said integrated signals into digital signals, a decimation filter (DF) for filtering digital signals, and ii) a feedback path (FP) comprising at least a digital-to-analog converter (DAC) adapted to convert said digital signals output by said quantizer (Q) into feedback analog signals intended for said combiner (C1), characterized in that at least one of said integrators (Hj) comprises variable capacitance means (Cj) and/or variable resistance means (Rj) arranged to be set in chosen states depending on values of a digital word to present chosen capacitances and/or chosen resistances, and in that it also comprises a self-calibration control means (CCM) arranged a) to generate a digital word with a chosen first value, b) then to estimate in-band noise IBN(n) from said filtered digital signals and to compare said in-band noise IBN(n) to the preceding in-band noise IBN(n-1), c) then to modify the value of the digital word in order to decrease said capacitance and/or resistance of each concerned integrator (Hj) from a chosen decrement, when BN(n) is smaller than IBN(n-1), d) then to iterate steps b) and c) till IBN(n) ise equal to or greater than IBN(n-1), and to choose as calibration digital word value the value corresponding to the preceding in-band noise IBN(n-1) in order to set said calibration state.

2. Converter according to claim 1, characterized in that each variable capacitance means (Cj) comprises a chosen number of banks of capacitors, with a chosen capacitance, mounted in series with a two-state switch (S), controlled by one bit value of said digital word.

3. Converter according to claim 2, characterized in that in step a) said self-calibration control means (CCM) is arranged to generate a digital word having a first value corresponding to a first capacitance equal to a chosen starting capacitance (Ci) with a chosen increase step.

4. Converter according to claim 3, characterized in that said starting capacitance (Ci) corresponds to a given spread of the integrator RC product.

5. Converter according to any one of claims 3 and 4, characterized in that said chosen increase step is equal to 33% of said starting capacitance (Ci).

6. Converter according to any one of claims 3 to 5, characterized in that said decrement (Cstep) is equal to a chosen proportion of said starting capacitance (Ci), depending on a process variation value, a temperature spread and a final targeted accuracy.

7. Converter according to any one of claims 5 and 6, characterized in that said number of capacitors is equal to 9, said nine capacitors offer together a maximum value equal to 4/3 of said starting capacitance (Ci), a first one of said nine capacitors having a value equal to 2/3 of said starting capacitance (Ci), each of the eight other capacitors having a value equal to 1/12 of said starting capacitance (Ci), and said decrement being equal to 1/12 of said starting capacitance (Ci).

8. Converter according to any one of claims 1 to 7, characterized in that each variable resistance means (Rj) comprises a chosen number of resistors, connected in series and having chosen respective resistances, and a same chosen number of two-state switches (S), each controlled by one bit value of said digital word and respectively controlling the accesses to said resistors.

9. Converter according to claim 8, characterized in that in step a) said self-calibration control means (CCM) is arranged to generate a digital word having a first value corresponding to a first resistance equal to a chosen starting resistance (Ri) with a chosen increase step.

10. Converter according to claim 9, characterized in that said starting resistance (Ri) corresponds to a chosen spread of the integrator RC product.

11. Converter according to any one of claims 9 and 10, characterized in that said chosen increase step is equal to 33% of said starting resistance.

12. Converter according to any one of claims 9 to 11, characterized in that said decrement (Rstep) is equal to a chosen proportion of said starting resistance (Ri).

13. Converter according to any one of claims 11 and 12, characterized in that said number of resistors is equal to 9, said nine resistors together offering a maximum value equal to 4/3 of said starting resistance (Ri), one of said nine resistors having a value equal to 2/3 of said starting resistance (Ri), each of the eight other resistors having a value equal to 1/12 of said starting resistance (Ri), and said decrement (Rstep) being equal to 1/12 of said starting resistance (Ri).

14. Converter according to any one of claims 1 to 13, characterized in that it is arranged to work in a differential mode and comprises two differential input nodes (N1, N2) arranged to be fed with differential analog signals to be converted.

15. Converter according to claim 14, characterized in that said two differential input nodes (N1, N2) are shortcut during said calibration steps a) to d).

16. Converter according to any one of claims 1 to 15, characterized in that said signal path (SP) comprises five different integrators (H1-H5) mounted in series.

17. Converter according to any one of claims 1 to 16, characterized in that said digital-to-analog converter (DAC) and said quantizer (Q) are of the single-bit or multi-bit type.

18. Converter according to any one of claims 1 to 17, characterized in that it is built with one filter loop.

19. Converter according to any one of claims 1 to 17, characterized in that it is built by cascading several CT ΣΔ ADC stages, each being either a first-order CT ΣΔ ADC or a second-order CT ΣΔ ADC.

20. Converter according to any one of claims 1 to 19, characterized in that it comprises high-frequency stabilization means.

21. Integrated circuit, characterized in that it comprises a converter (CV) according to any one of the preceding claims.

22. Integrated circuit according to claim 21, characterized in that it defines a baseband integrated circuit.

23. Receiving device, characterized in that it comprises an integrated circuit according to any one of claims 21 and 22.

24. Transceiver device, characterized in that it comprises a converter (CV) according to any one of claims 1 to 20.

25. Mobile radio communication equipment, characterized in that it comprises a converter (CV) or an integrated circuit or a receiving device or a transceiver device according to any one of the preceding claims.

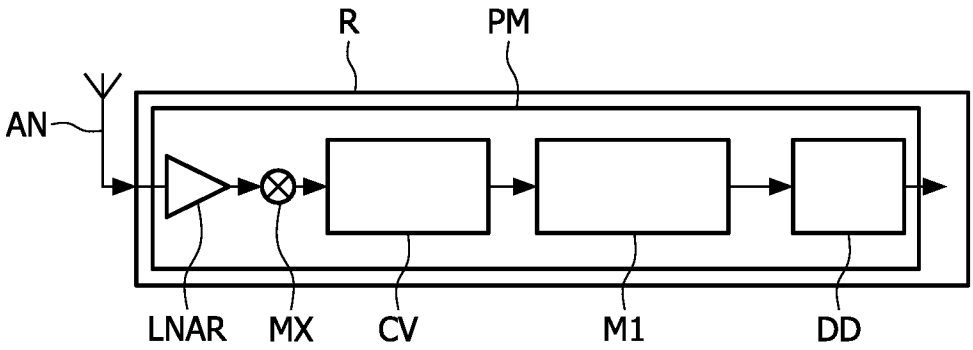


FIG. 1

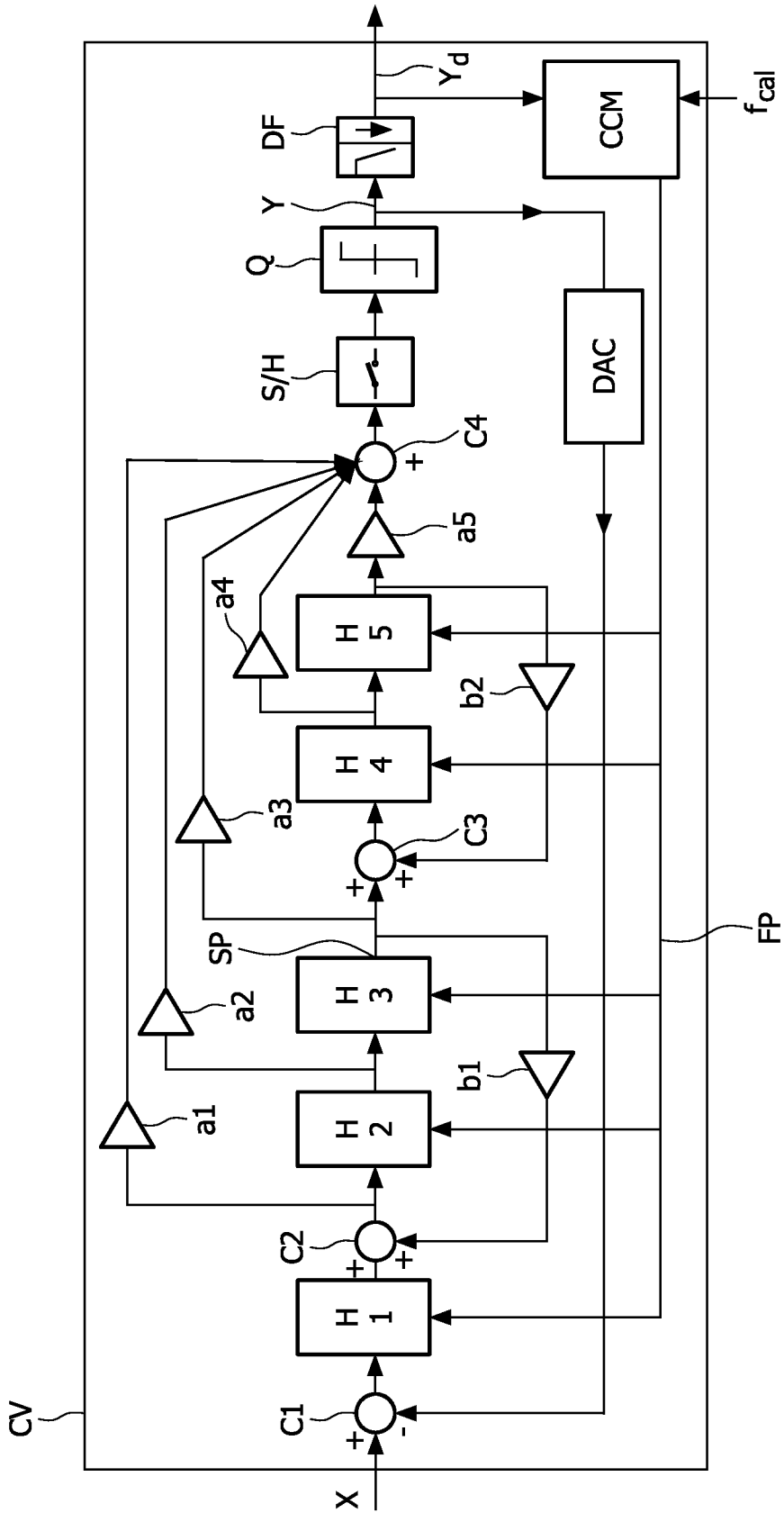

CV
X
C1
C2
C3
C4
H 1
H 2
H 3
H 4
H 5
a1
a2
a3
a4
a5
b1
b2
SP
FP
S/H
Q
Y
DF
Y_d
CCM
f_{cal}
DAC

FIG. 2

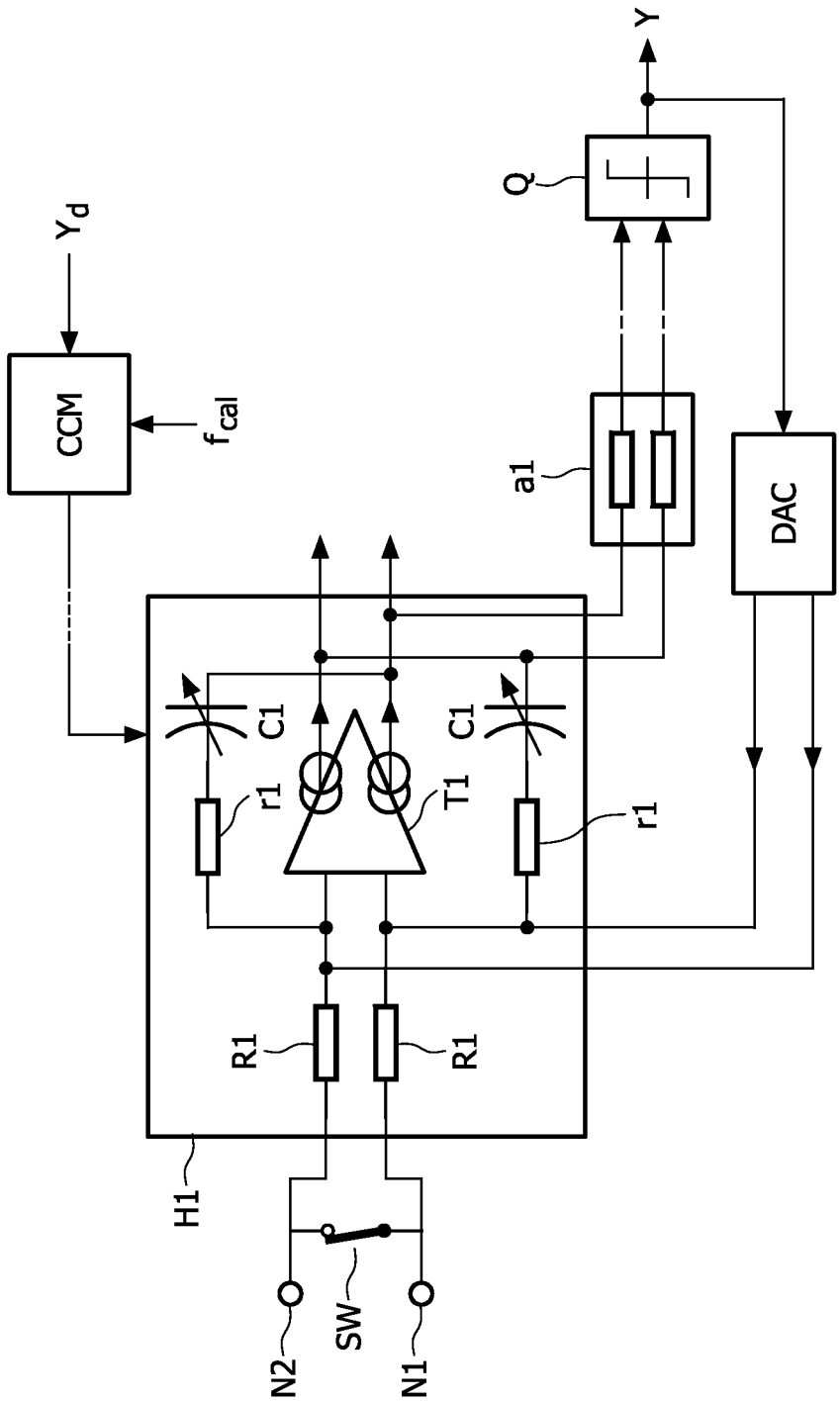


FIG. 3

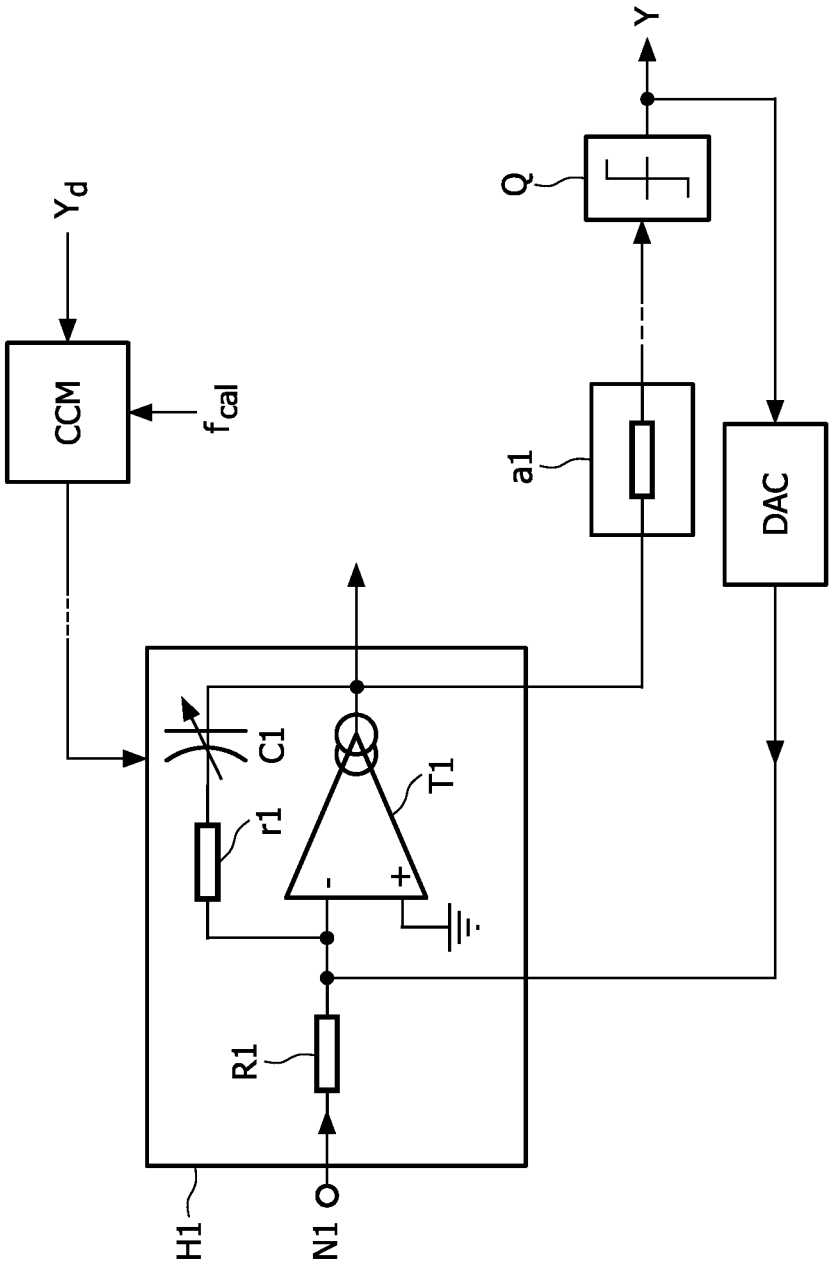


FIG. 4

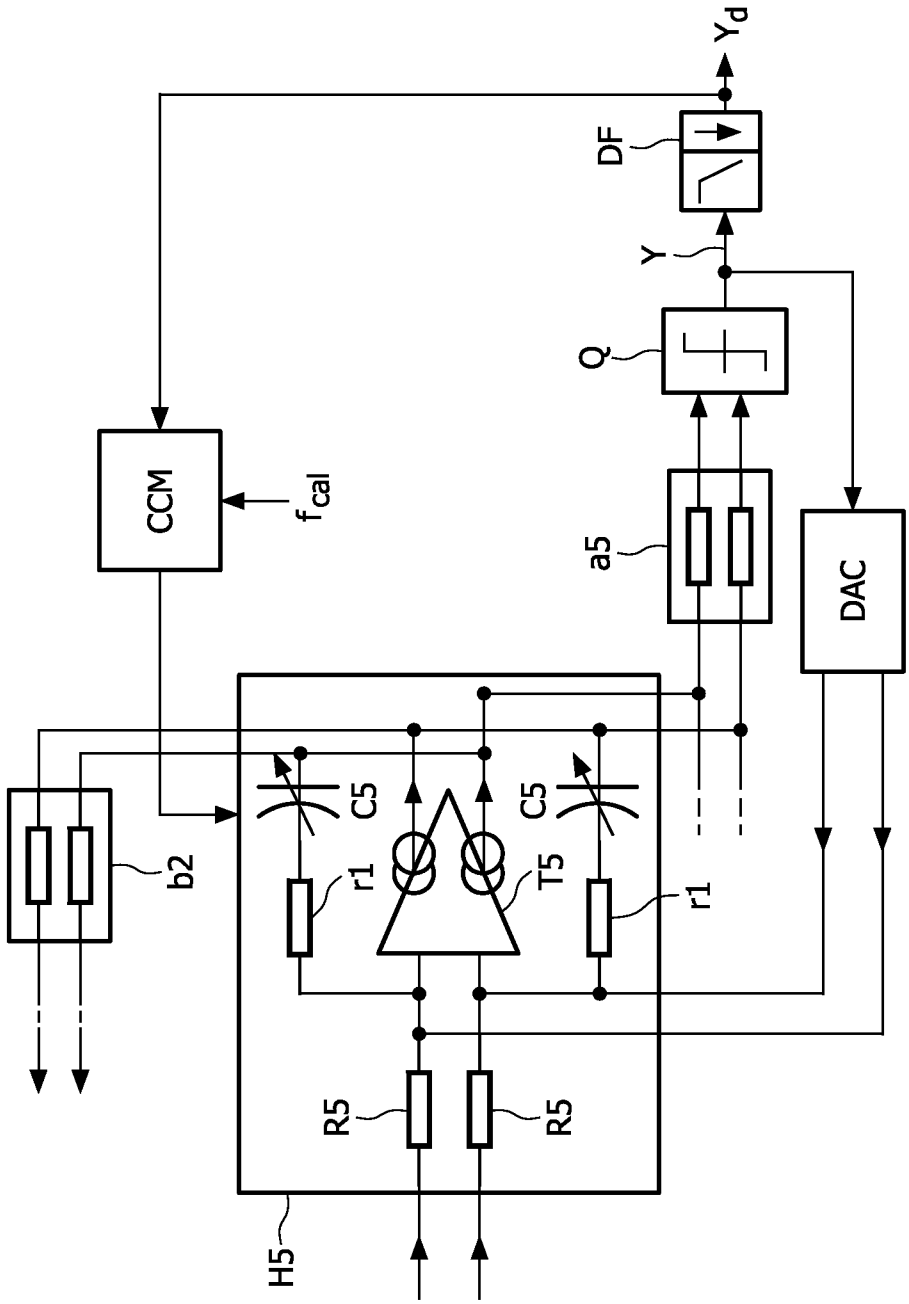


FIG. 5

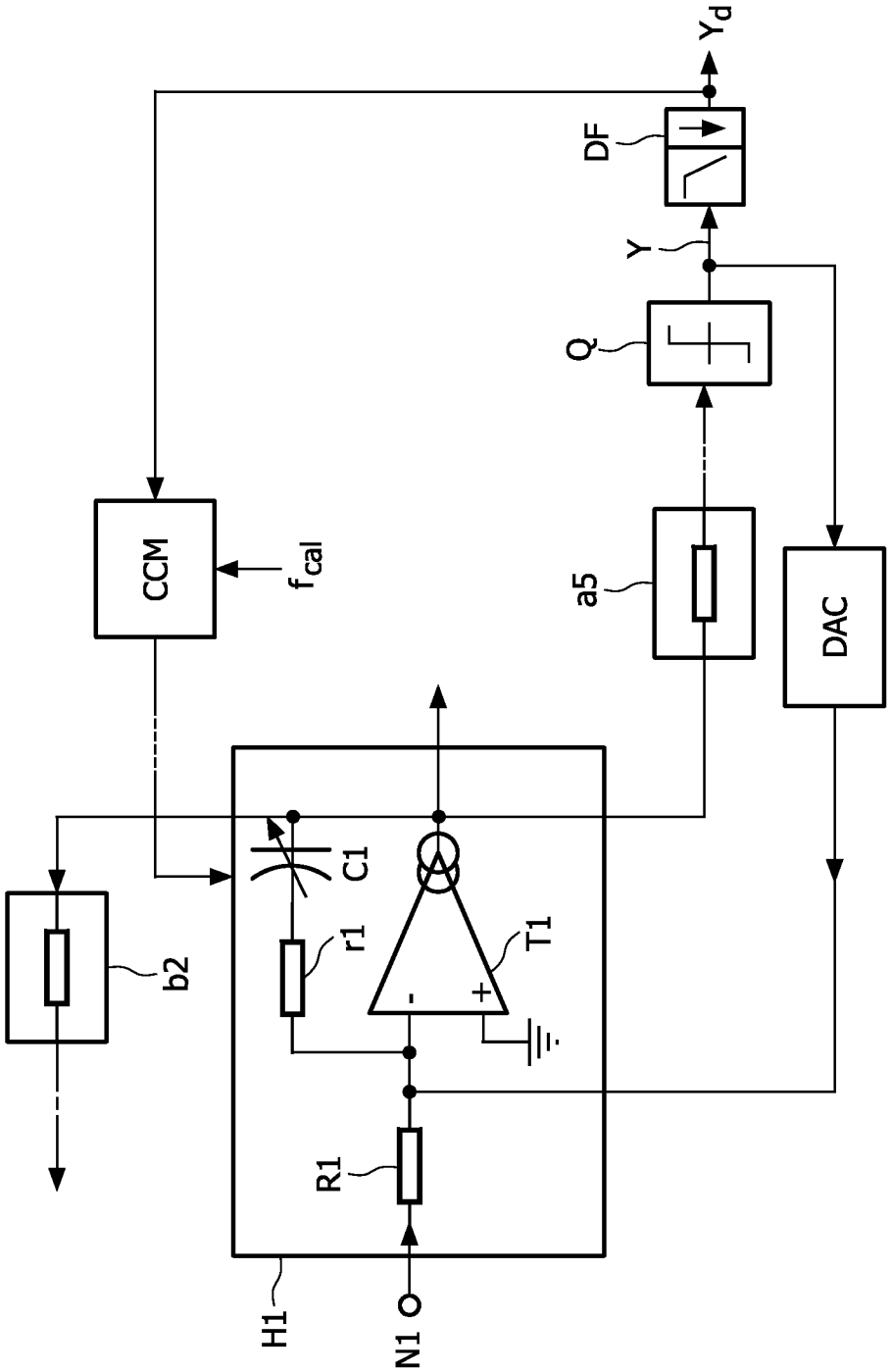


FIG. 6

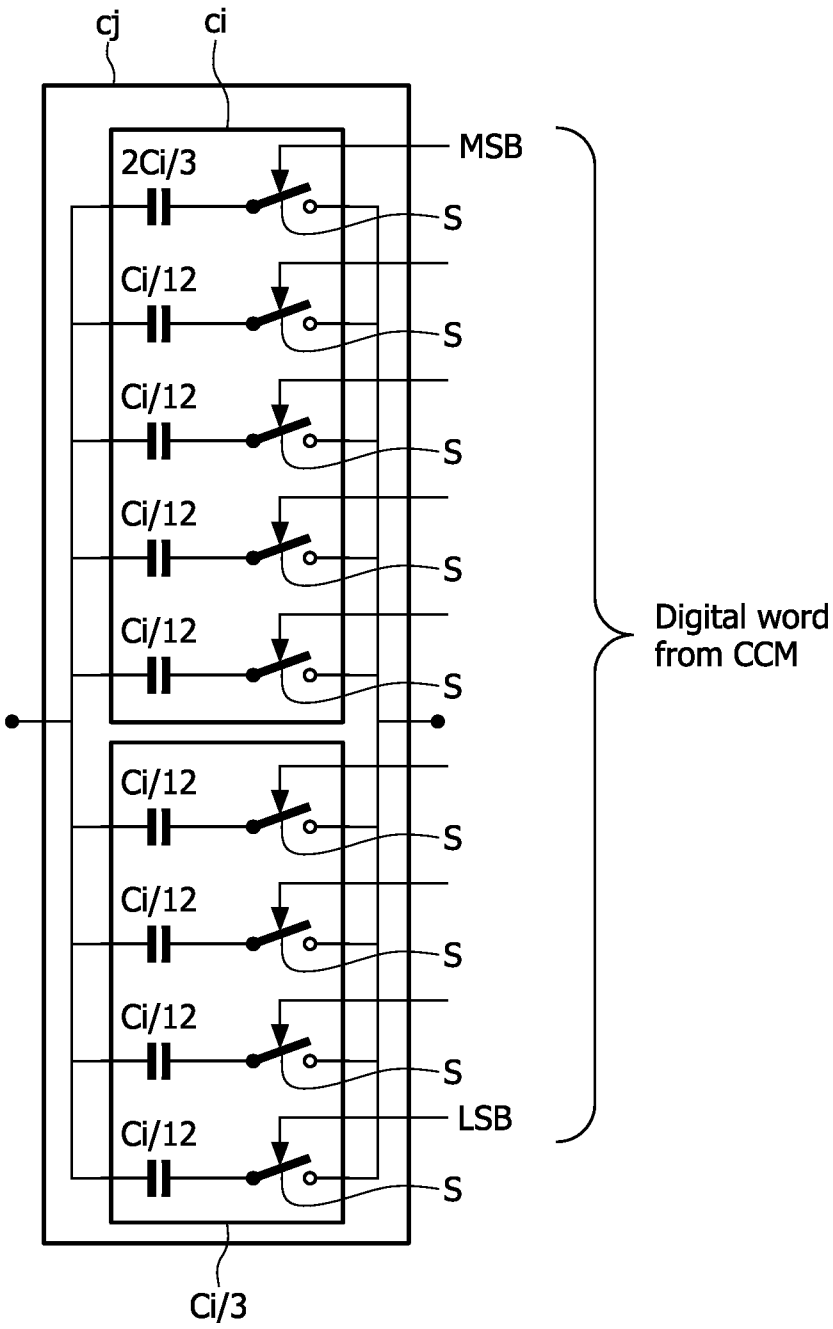

cj
ci
2Ci/3
Ci/12
Ci/12
Ci/12
Ci/12
Ci/12
Ci/12
Ci/12
Ci/12
Ci/12
S
MSB
LSB
Digital word
from CCM
Ci/3

FIG. 7

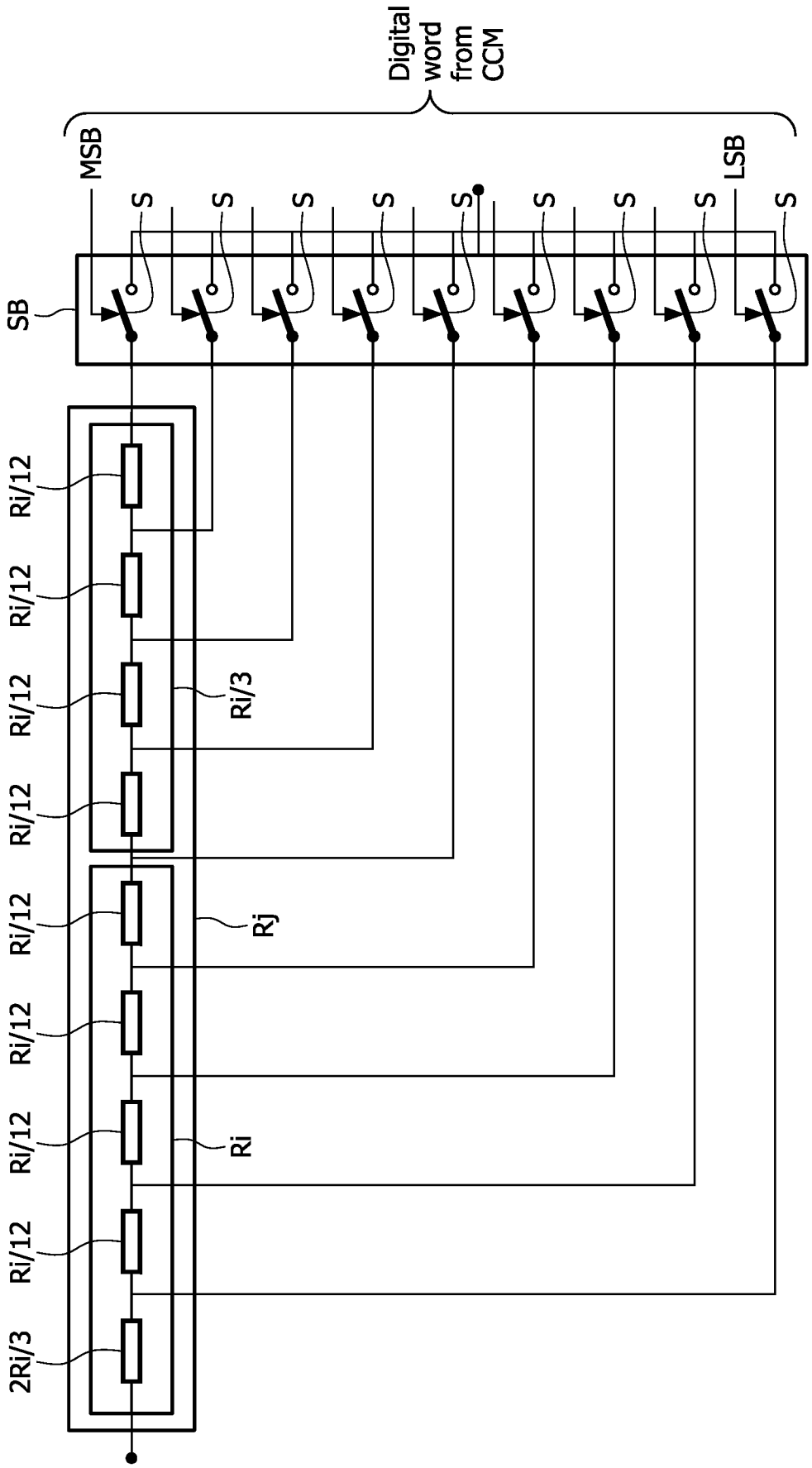


FIG. 8

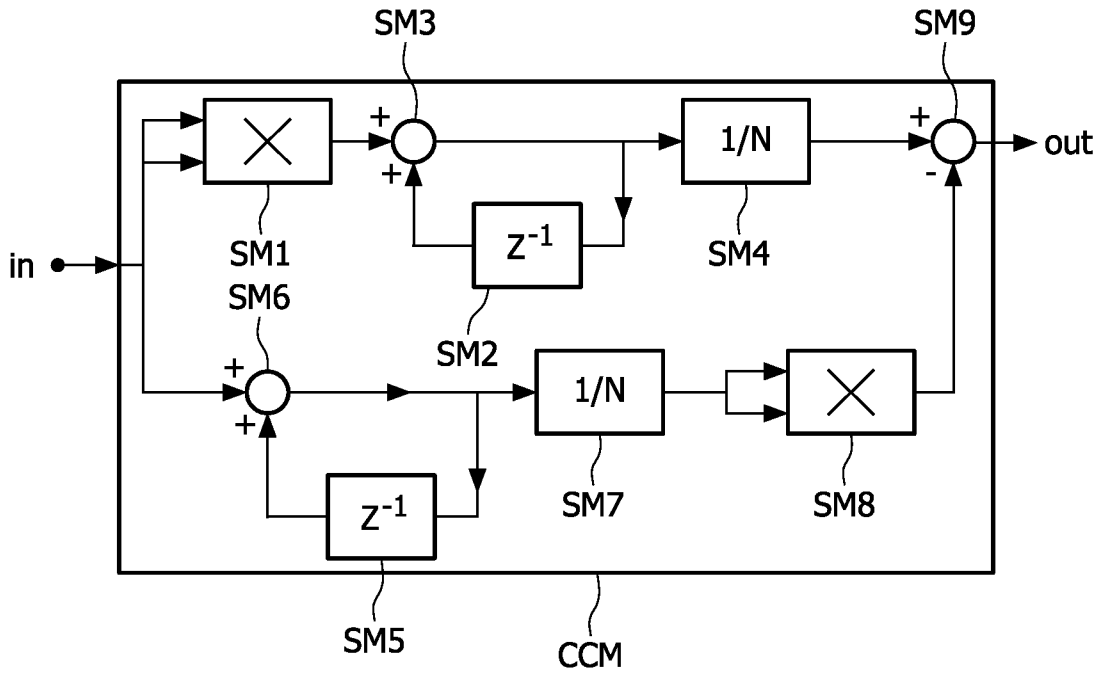


FIG. 9

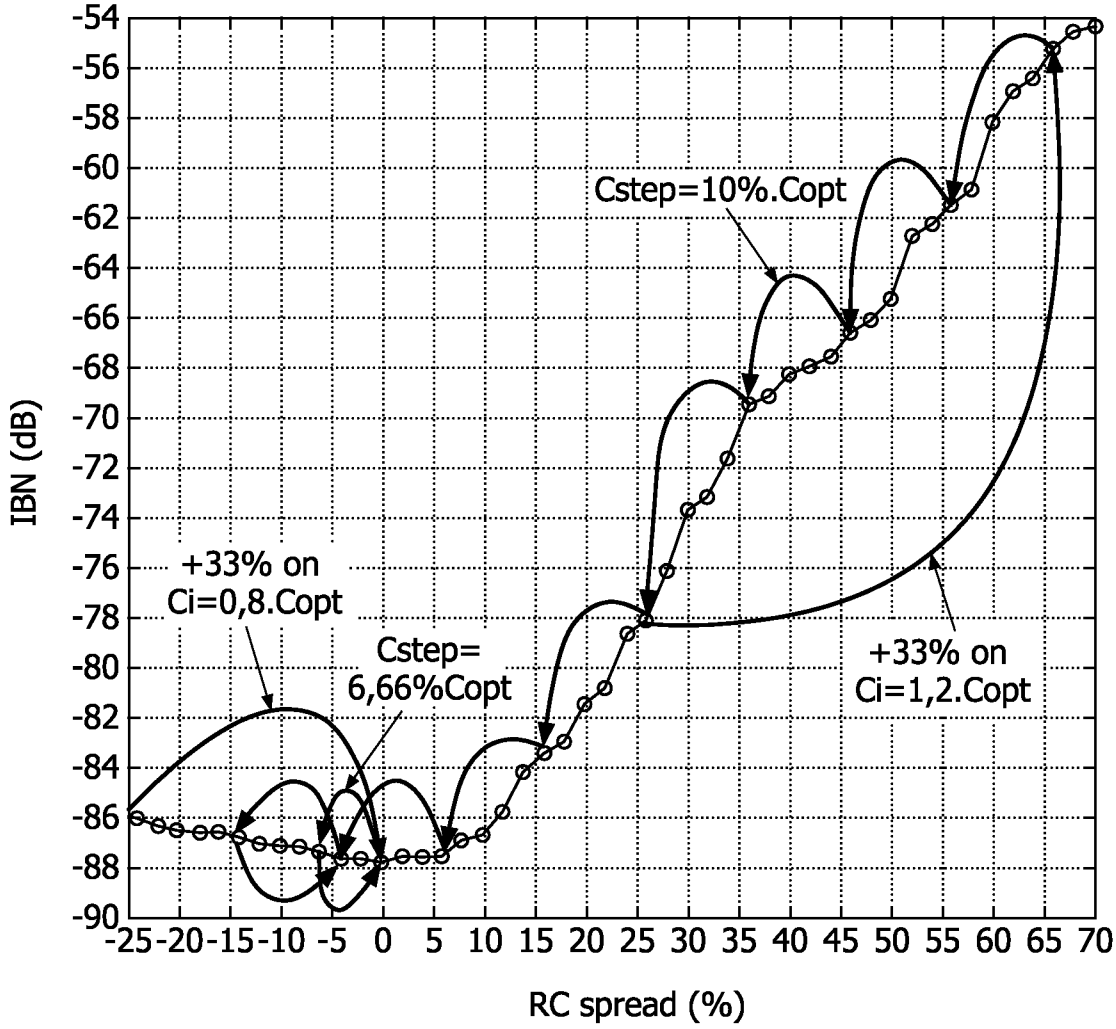

IBN (dB)
-54
-56
-58
-60
-62
-64
-66
-68
-70
-72
-74
-76
-78
-80
-82
-84
-86
-88
-90
-25 -20 -15 -10 -5 0 5 10 15 20 25 30 35 40 45 50 55 60 65 70
RC spread (%)
Cstep=10%.Copt
+33% on
Ci=0,8.Copt
Cstep=
6,66%Copt
+33% on
Ci=1,2.Copt

FIG. 10

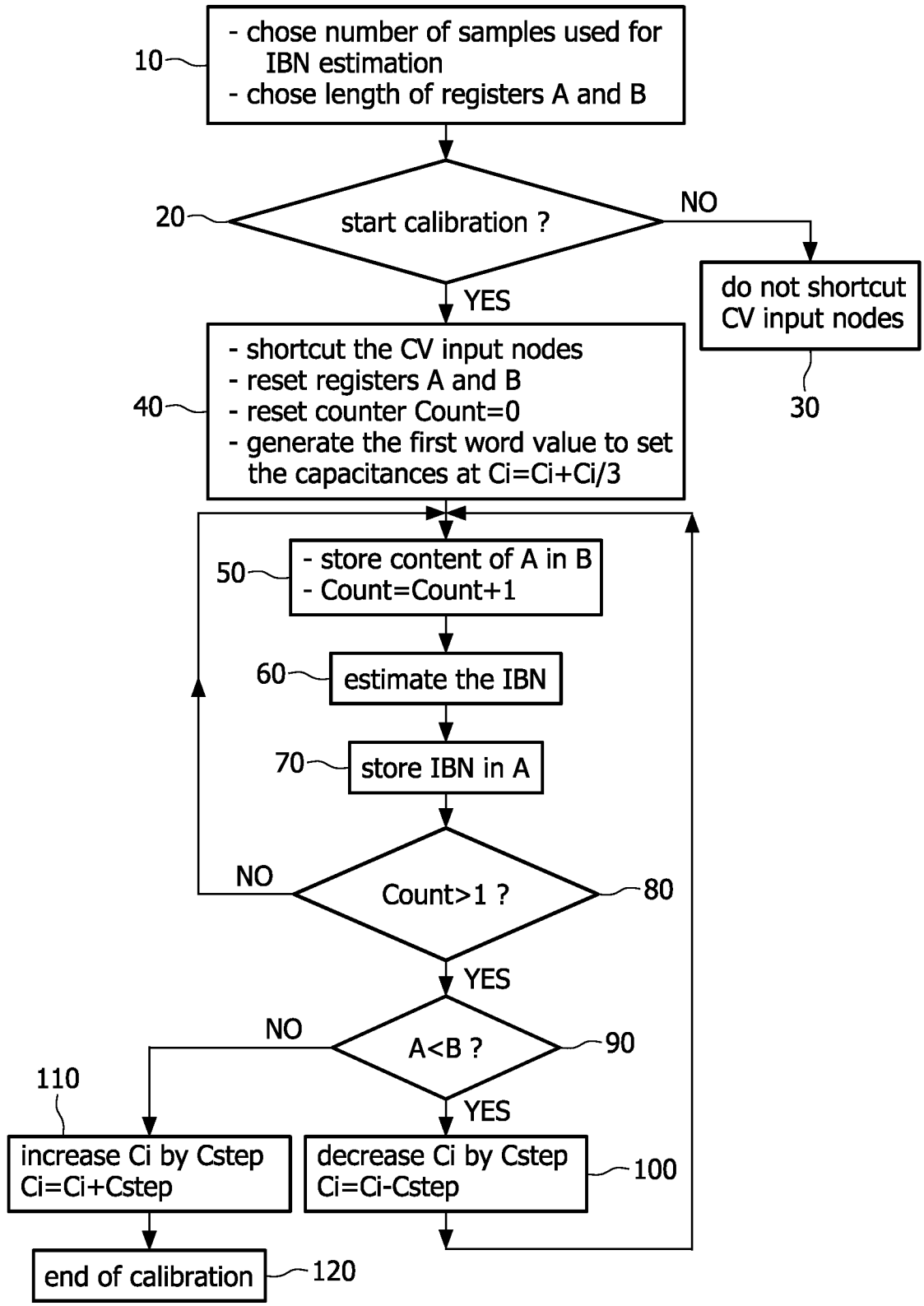

- chose number of samples used for IBN estimation
- chose length of registers A and B
10
start calibration ?
20
NO
YES
do not shortcut CV input nodes
30
- shortcut the CV input nodes
- reset registers A and B
- reset counter Count=0
- generate the first word value to set the capacitances at Ci=Ci+Ci/3
40
- store content of A in B
- Count=Count+1
50
estimate the IBN
60
store IBN in A
70
NO
Count>1 ?
80
YES
NO
A<B ?
90
YES
110
increase Ci by Cstep
Ci=Ci+Cstep
decrease Ci by Cstep
Ci=Ci-Cstep
100
end of calibration
120

FIG. 11

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2007/050213

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03M3/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, COMPENDEX, INSPEC, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2005/285763 A1 (NGUYEN KHIEM [US] ET AL) 29 December 2005 (2005-12-29) paragraphs [0030] - [0038]; figures 4-9	1

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
4 May 2007	11/05/2007

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Beindorff, Henk

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/IB2007/050213

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2005285763 A1	29-12-2005	EP 1766782 A1	28-03-2007
		WO 2006006993 A1	19-01-2006