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609737

FIRST SCHEDULE

FORM 1 Regulation 9

COMMONWEALTH OF AUSTRALIA

Patents Act 1952

CONVENTION APPLICATION FOR A STANDARD PATENT

Digital Equipment Corporation of 146 Main Street, Maynard, Massachusetts 01754-1418, United States of America, a corporation organised under the laws of the Commonwealth of Massachusetts hereby applies for the grant of a standard patent for an invention entitled PRINT ENGINE DRIVE INTERFACE which is described in the complete specification filed with the Australian Patents Office pursuant to the Paris Convention.

Details of basic application(s) -

Number of basic application - 900 057

Name of Convention country in which basic application was filed - United States of America

Date of basic application 25 August 1986

The address for service is FREEHILL HOLLINGDALE & PAGE, 32 Floor, BHP House, 140 William Street, Melbourne. Our Ref: MJW:WM:1310051

DATED this 23rd day of February, 1989.

Wayne McMaster

Digital Equipment Corporation
By its Solicitor Wayne McMaster
of Freehill, Hollingdale & Page

MOO68883 24/02/89 The Commissioner of Patents

APPLICATION ACCEPTED AND AMENDMENTS ALLOWED 18-2-91

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(CONVENTION - Company)

FORM 8 - REGULATION 12 (2)

COMMONWEALTH OF AUSTRALIA
Patents Act, 1952-1973

DECLARATION IN SUPPORT OF A CONVENTION APPLICATION FOR A PATENT

In support of the Convention Application No. 78774/87 made by DIGITAL EQUIPMENT CORPORATION, a corporation organized under the laws of the Commonwealth of Massachusetts, United States of America

(hereinafter referred to as "Applicant") for a patent for an invention entitled:

"Print Engine Drive Interface"

I, MARIETTA M. ETHIER, Assistant Secretary

of 146 Main Street, Maynard, MA 01754, United States of America

do solemnly and sincerely declare as follows:

1. I am authorised by Applicant to make this declaration on its behalf.

2. The basic Application(s) as defined by section 141 of the Act was/were made in the United States of America on August 25, 1986

by Charles Lai

3. Charles Lai of 355 Hosmer Street, Marlborough, Massachusetts 01752, U.S.A.

is/are the actual Inventor(s) of the invention and the facts upon which Applicant is entitled to make the Application are as follows:
Applicant is the Assignee of the said Inventor(s).

4. The basic Application(s) referred to in paragraph 2 of this Declaration was/were the first Application(s) made in a Convention country in respect of the invention, the subject of the Application.

DECLARED at Maynard, MA

this 7th day of February 1989.

DIGITAL EQUIPMENT CORPORATION

Marietta M. Ethier, Assistant Secretary
TO THE COMMISSIONER OF PATENTS.

(12) PATENT ABRIDGMENT (11) Document No. AU-B-78774/87
(19) AUSTRALIAN PATENT OFFICE (10) Acceptance No. 609737

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PRINT ENGINE DRIVE INTERFACE

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(57) Claim

1. A print engine data interface for reading pixel image data from a first full page bit map memory and serially transferring the read data to a print engine in response to signals from a horizontal line processor, a printer control and status interface and the print engine, comprising:

(a) a set of command and data registers for storing programmed page format and scan length data from said printer control and status interface;

(b) a scan offset adjustment circuit coupled to receive the page format and scan length data from the command and data registers;

(c) means for periodically generating a burst refresh signal;

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(d) an arbitration circuit coupled to detect whether the first full page bit map memory is to be read from/written to or refreshed, said arbitration circuit outputting refresh request signals in response to burst refresh signals to start the refresh cycle and outputting read/write request signals to start the memory cycle of each scan line;

(e) a bit map sequencer coupled to said arbitration circuit for generating read/write or refresh control signals for controlling said first full page bit map memory in dependence on the request signals output by said arbitration circuit;

(f) a bit map memory address counter coupled to said bit map sequencer and to said command and data registers for addressing said first full page bit map memory;

(g) a data conversion circuit coupled to receive data retrieved in parallel from said first full page bit map memory and converting the parallel data into a serial data stream for synchronous reception by the print engine in response to an enabling signal from said arbitration circuit; and

(h) a second full page bit memory which is loaded with pixel image data while said first full page bit map memory is being read.

whereby the pixel image data stored in said first full page bit map memory is periodically refreshed in response to said burst refresh signals when said print engine data interface is in the print mode.

2. The print engine data interface as defined in claim 1, wherein said second full page bit map memory is coupled to said bit map sequencer and to said data conversion circuit, pixel image data being read from said second full page bit map memory while said first full page bit map memory is being loaded with pixel image data.

PCT

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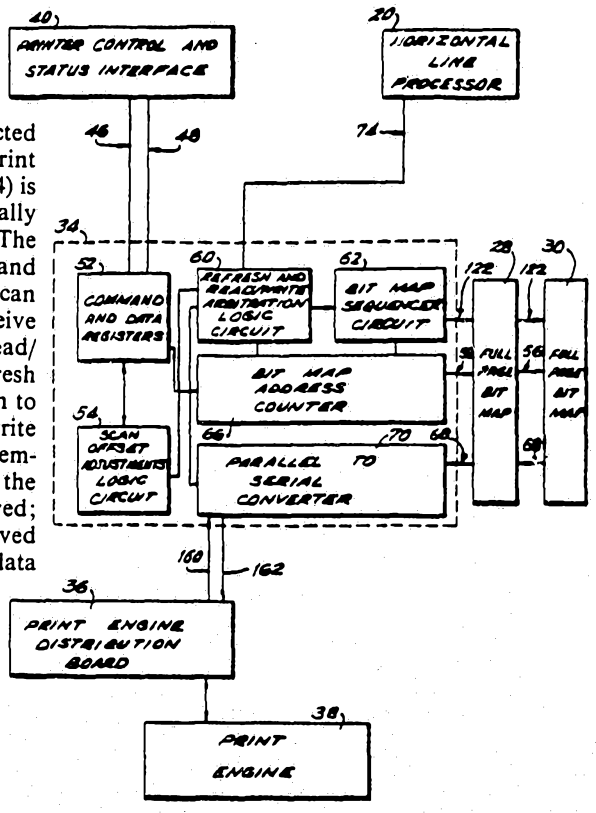
(54) Title: PRINT ENGINE DRIVE INTERFACE

(57) Abstract

A print engine data interface circuit (34) is selectively connected to one of a number of full page bit maps (28, 30) that provide a print engine (38) with command data. The print engine data interface (34) is designed to access one of the full page bit maps (28, 30) and serially transmit the pixel data contained therein to the print engine (38). The print engine data interface circuit (34) includes a set of command and data registers (52) for storing programmed page format and scan length data; a scan offset adjustment circuit (54) adapted to receive the data from the command and data registers; a refresh and read/write arbitration circuit (60) adapted to repeatedly generate a refresh signal when a portion of the full page bit map is not being written to or read from; a bit map sequencer (62) for generating either read/write or refresh commands to an address within the full page bit map memory; a bit map address counter (66) for pointing to an address in the full page bit map memory so the data at that address can be retrieved; and a data conversion circuit (70) for accepting the data retrieved from the full page bit map memory and converting it into a serial data stream for synchronous reception by the print engine.



PRINT ENGINE DRIVE INTERFACE

Field of the Invention

This invention relates to printer engine drive units such as those adapted to transmit control signals to a print engine from a data processing system. In particular, it relates to a print engine drive interface unit for transmitting print command data from a dynamic memory to a print engine, and for refreshing the command data stored in the memory.

Background of the Invention

Much work has been done in the recent years regarding the development of high-speed, high-quality data processing printers. A considerable fraction of this work has gone into the development of laser-type print engines. These print engines have a specially adapted laser with a beam that can be rapidly turned on and off to generate a raster type scan line composed of pixels, or dots, across a photoconductive surface. The adjacent scans of the laser beam are located within close proximity to each other so that when the surface is completely scanned a full, accurate depiction of the image to be produced is projected on the surface. A paper printout of the image may then be produced by conventional xerographic techniques.

The advantage of using a laser-type print engine is that the pixel density can be quite high. A laser-type print engine can produce 90,000 or more pixels per square inch of output image. This makes it possible to produce figures and characters of extremely high quality, equal to those produced by much slower conventional printers with typewriter type impacting keys. Another advantage laser printers have over conventional printers is that they are not limited to printing only the figures

contained on the type keys. The laser beam may be used to form a raster image of almost any combination of pixels desired. This is a desirable feature to have on a printer when printing either a business or technical document that includes irregularly shaped figures such as graph lines or scientific symbols.

One problem with laser printing technology is that large amounts of print command data must be processed by the printing system at a very high rate of speed. This is because it is necessary for the printing system to almost simultaneously receive the output data from the processor to be printed, convert the data into pixel image form readable by the print engine, and transmit the pixel print commands in the appropriate sequence to the print engine so the laser will be activated at the appropriate times as its beam scans along the photoconductive surface.

Thus, it is necessary to provide a data controller that can properly sequence the flow of data from the main processor, convert it to print engine-readable pixel form, and transmit the pixel data to the print engine.

Currently, there are two approaches to data controller design. One approach uses a band buffer where a block of data is received by the controller, converted into pixel form, and stored in a buffer where it can be read by the print engine. A disadvantage of this system is the storage buffer is too small to store all of the pixel data necessary for some complex graph and symbol imagery. Thus, these controllers are of limited utility.

Alternatively, the data controller may have a full page bit memory system. These controllers are provided with at least one full page bit memory map that is representative of the data to be retrieved and for scanning by the print engine. Processing circuitry

within the data controller analyzes the input from the main processor to determine if it is either format data, called font data, or actual image composition data. An image generator circuit analyzes the composition data by referring to the font data, and produces a pixel representation of the image to be generated. The pixel output is loaded into the full page bit map memory. The print engine is able to access the full page bit map memory and reproduce on the photoconductive surface the image stored therein. This makes it possible to generate a full page of print output with graphs and other complex figures represented thereon.

Full page bit memory controllers can be rather slow devices because it has proved very difficult to transmit data to one position of the full page bit map and to send data from another section of the bit map at the same time. Also, some image generating systems do not transmit data to the bit map serially. With these systems the engine bit map must be fully composed before it is ready to be accessed by the print engine. If only one bit map is provided, it is necessary to follow a pattern of first loading it with pixel data, and then having the print engine access it. This slows down the operation of both the image generator and the print engine since one must remain idle while the other has access to the bit map. Therefore, it is desirable to provide the data controller with at least two full page bit maps so one may be accessed by the image processor while the other is accessed by the print engine.

Another disadvantage of full page bit memory systems is that they have memory elements that usually need to be refreshed. This is because the typical full page bit memory is a dynamic memory, meaning that the electrical charges in it that represents the data tends to decay

over time. This is a problem because data stored early within the print engine will decay and become unuseable before it is accessed by the print engine. Also this decay makes it almost impossible for the print engine to repeatedly access a bit map thereon or so that multiple copies of the page represented thereon can be printed.

A need therefore exists for a means to control the print engine's access to the bit memory system. The print engine should have access to at least two full page bit map memories so it can have access to one while the image generator has access to the other. Also, there should be a means to access the full page maps so data stored therein is frequently refreshed so as to prevent it from decaying and becoming unreadable.

Summary of the Invention

The invention comprises providing a print engine data interface circuit that can be selectively connected to one of a number of full page bit maps that provide the print engine with pixel data. The print engine data interface is designed to access one of the full page bit maps and serially transmit the pixel data contained therein to the print engine. Thus, when two full page bit maps are provided, it is possible to dedicate one of the full page bit maps to the print engine while the other is being loaded with data from the image processor. Both the image processor and the print engine can thus be operated at maximum efficiency in order to generate hard paper copies as fast as possible.

Also, the print engine of this invention is designed to frequently refresh the data stored in the full page bit map it has access to. This keeps the data within the memories in an optimal condition so the full page bit map

may be repeatedly accessed by the print engine to provide multiple copies of the same output.

The print engine drive interface is connected to the print engine, a print bus, and a printer control and status interface. The print bus is connected to at least two full page bit maps The printer control and status interface is connected to both the print engine data interface and the full page bit map memories. It controls the bit map assignments for both the reading to the bit map from the image processor and the access to a bit map by the print engine data interface. The printer control and status interface also directs page geometry parameters to the print engine data interface. The printer control and status interface transmits these control signals in response to initial page parameters supplied to it in the terms of formatting information, and in response to status signals generated by the print engine.

The print engine drive interface includes a set of command and data registers for storing the page geometry parameters transmitted from the printer control and status interface. A scan offset adjustment circuit uses the parameters in the command and data registers to synchronize the retrieval of the pixel data from the full page bit map so that it is synchronous with the demand from the print engine, and to control the length of the memory scan of the memory so it is of an appropriate length to be acceptable with the print engine's requirement for print command data. A bit map sequencer is designed to generate either read/write or refresh control signals to the bit map memory while it is controlled by the print engine data interface. This provides command signals so the memory rows with the full page bit memory are either read or refreshed. The bit

map sequencer is controlled by a refresh and read/write arbitration logic circuit.

The print engine drive interface is also provided with a bit map address control circuit for generating a current data address so the correct data can be retrieved by the bit map sequencer. The retrieved data is read into a parallel to serial data conversion unit for transmission to the print engine.

Brief Description of the Drawing

FIG. 1 is a block diagram of a data processing printer system that incorporates the print engine data interface in accordance with this invention.

FIG. 2 is a block diagram illustrating the principle components of the print engine data interface.

FIGS. 3A through 3C, when assembled, form a schematic diagram of the print engine data interface.

Detailed Description of the Preferred Embodiments

FIG. 1 depicts in block diagram a print system 10 that is connected to a main processor (not illustrated) through a main bus 12 such as an ethernet line. The system is addressed through a host processor 14 that exercises control over the entire print system. A system bus 16 such as a Q-bus connects the system together. The host processor initially determines if the print system is being polled, or accessed, by the main processor. If it is determined that the print system is being accessed the host processor then determines whether the incoming packets of data are formatting data, called font data, or actual composition data. If the incoming data is font data it is passed through a horizontal line processor 20 to a font memory unit 22. If the data is composition data it is passed to an image generator processor 18. A

direct memory access unit 24 serves as a high speed channel to transfer command and data signals to the image generator processor.

The image generator processor responds to a particular packet of composition data by issuing an image command to the horizontal line processor 20. The horizontal line processor in response to the image command, and by reference to the font data generates a full page bit map address where a pixel should be produced. The bit map address is directed along a composition bus 26 to one of two full page bit maps (FPBM) 28 or 30 that the horizontal line processor selectively accesses. The pixel image is then stored in the full page bit map at the address the horizontal line processor generated. When the full page bit map is fully loaded with pixels it is a representation of the page to be produced. This necessitates providing the full page bit maps 28, 30 with a very large amount of memory. In one embodiment of the invention, they are each a 1.25 megabyte array, and each bit within the array represents a potential pixel location.

The full page bit map memories are connected to a print bus 32 that is connected to a print engine data interface (PDI) 34. The print engine data interface is connected to a print engine distribution board 36 that serves as the input-output interface for a print engine 38. The print engine controls the laser and other hardware elements necessary to produce a print document 39.

The transmission of data through the print engine data interface is controlled by a printer control and status interface (PCSI) 40. The printer control and status interface is connected to the host processor by the Q-bus, to the print engine through the distribution

board by a set of command and status lines 42 and to the print engine data interface by scan enable address, and data lines 44, 46 48 respectively, and to the full page bit map by assignment lines 49. The print engine transmits a line sync across a print engine line sync line 50 wherever it is ready to start a new scan line. The line sync line is connected to both the print engine data interface and the printer control and status interface. The printer control and status interface responds to the commands of the host processor 14 by starting and stopping the printer and by selecting the bus assignments of the full page bit map memories. It performs these functions by frequently polling the status of the printer and other elements of the system 10 and communicating their status to the host processor.

The print engine data interface addresses the full page bit memory 28 or 30 that is to be accessed for printing, serially retrieves the pixel data contained therein, and forwards it to the print engine 38 for image processing. The print engine data interface also cyclically refreshes all the data stored in the full page bit memory. This keeps the data fresh and useable by the print engine when it would otherwise decay if the scan line is too short. This also makes it possible to repeatedly scan each full page bit map so multiple copies of the page may be produced without having to spend time re-composing the page each time.

Referring now to FIG. 2 it is seen that the print engine data interface 34 includes a set of command and data registers 52. These registers are designed to store page geometry parameters, specific to the type of print engine and page format the print engine data interface is being used, and print engine command data. These parameters are transferred by the printer control and

status interface to the registers through PCSI address and PCSI data lines 46, 48. The PCSI scan enable command is also forwarded to these registers through the scan enable line 44. These parameters are referenced by a scan offset adjustments logic circuit 54 to adjust to the proper initial address at the beginning of each line scan.

Reading, writing and refreshing of the full bit map memories are controlled by a refresh and read/write arbitration logic circuit 60. This circuit assigns the proper refresh or read/write commands to a bit map sequencer. This enables the bit map sequencer circuit to generate control signals to either refresh the data in the bit map for reading or retrieve it for transmission to the print engine.

A bit map address counter 66 under command of the refresh and read/write arbitration circuit 60 and the bit map sequencer 62, is provided to point to the appropriate address in the full page bit map 28 or 30 so the correct data will be either refreshed or retrieved. The address is transmitted through a set of address lines 56. The retrieved data is read in byte form through a set of eight data lines 68 from the full page bit map. The data is transferred into a parallel-to-serial converter 70 where it is converted into a serial bit stream for transmission to the print engine distribution board through a data output line 162.

The horizontal line processor 20 is connected to the print engine data interface through a refresh line 74, connected to the refresh and read/write arbitration logic. This refresh signal passed through this line is to synchronize the refresh timing when the bit map 28 or 30 accessed by the PDI is not being used to supply print commands to the print engine.

The command and data registers 52 consist of four 8-bit registers 76, 78, 80, and 82 respectively and one D-type flip-flop 84, as shown in Fig. 3. The page parameters of the scan are assigned to the individual registers as follows:

REGISTER	DESCRIPTION	
Register 76	Bits 4-7	High 4 bits of scan offset adjustment
	Bit 3	Print Mode Select (H- Print; L- Print/Erase)
	Bit 2	Test-Enable PDI self-test mode
	Bits 0-1	High 2 bits of byte count per scan line
Register 78	Bits 0-7	Lower 8 bits of scan offset adjustment
Register 80	Bits 0-7	Lower 8 bits of byte count per scan line
Register 82	Bits 0-7	Stored byte pattern to be written back to bit map during print/erase mode

The registers are loaded with geometry parameters from the PCSI through the address and data lines 46 and 48 and the flip flop is triggered by a signal enable from the PCSI through the scan enable line 44. Flip flop 84 is used to generate a page enable signal along the page enable line 86 and is triggered by the line sync signal. The page enable is asserted during the entire frame of a page, is synchronous with the line sync, and thus is used as a system reference signal to enable data transfer.

The scan offset adjustment circuit 54 consists of an offset adjust flip-flop 90, an offset counter 92 and a

pulse stretcher 94. The scan line registration offset adjustment is made at the beginning of each scan line by loading one's complements of offset count from registers 76 and 78 into the offset counter 92 (connection not shown) and setting the offset adjust flip-flop. The offset adjust flip-flop enables the offset counter which counts engine clock pulses received through an engine clock line 96 as the scan progresses. When the total number of counts equals the count stored, the offset counter generates an offset reset signal on an offset reset line 98. The reset line is branched back to the offset adjust flip-flop so the offset adjust flip-flop 90 is reset. The pulse stretcher 94 along with an inverter 100 is used to load the offset counter at the beginning of the line with the scan value. The inverter 100 is used to invert the video clock signal from the print engine so sufficient time is provied to load the offset counter. Alternatively, a comparator can be used to detect the end of the offset, eliminating the need for the pulse stretcher.

The bit map address counter 66 includes a line address counter 101, a column address counter 102 and a column address comparator 104. Each byte, or each image data unit, in the full page bit map is located by row address and column address. As the memory scan of the bit map progresses the line address counter is incremented by the rising edge of the line sync while at the same time the column address counter is incremented by an end R/W signal generated by the bit map sequencer and transmitted over an end R/W line 108. The addresses generated by the counters are transferred to one of the bit maps across the bit map address lines 56. This enables the sequential scanning of the bit map page during the read state. The number of data units to be

read during each scan line is programmable, located in registers 76 and 78, enabling the PDI to adjust the scan through the scan offset adjust circuit 54 to accommodate paper of varying width. The column address comparator 104 detects the end address of each scan line by comparing it to the stored value from register 80. When the end of the scan line is reached the comparator resets a line status flip-flop 110. Since the length of the scan line is programmable it can be used to "image-clip" the length of a page.

The bit map sequencer 62 consists of a memory synchronizer 112 and a sequencer 114. The sequencer 114 is a state machine that samples the input and the present state of the machine to determine its next state and output. The synchronizer is a clocked latch which is used to synchronize the sequencer input signals to prevent meta stable state transitions. The input to the synchronizer is from a refresh request line 116, a print/erase line 118 from register 76 (connection not shown), and a read/write request line 120. The output of the sequencer is two sets of control signals. One set is a set of bit map control signals, outputted along four bit map control lines 122 which are used to access and refresh the bit map. The second set of controls is internal to the PDI and includes the end read/write signal transmitted on the end read/write line 108, an end refresh signal transmitted on an end refresh line 124, an end memory access request signal transmitted on an end memory access line 126, and a write data enable signal asserted on a write data enable line 128.

The arbitration logic unit 60 includes the line status flip-flop 110, a delay flip-flop 130, a multiplexer 132, an AND gate 134, a refresh request flip-flop 136 and a read/write request flip-flop 138. The

multiplexer is a 2 to 1 unit that selects one of the refresher sources between either the horizontal line processor swap request through the horizontal line processor refresh line 74 or the burst refresh through a burst refresh line 140. The line status flip-flop registers the effective data period of the scan line. The output is transmitted along an inhibit refresh line 142 to the AND gate 134 and is used to inhibit refresh requests during implied refreshes. The line status flip-flop 110 may be reset by either the column address comparator 104 or by the line sync signal since they are gated together to the flip-flop through an OR gate 111. The complement of the line status flip-flop is used to activate a pixel counter 144 and the delay flip-flop 130. The output of the delay flip-flop 130 is in turn used to control the start of the memory cycle at each scan line. The delay is inserted to guarantee that the bit map sequencer 62 will always complete the current refresh cycle before any attempted memory scan, and that the scan adjustment between scan lines is uniform.

The refresh request flip-flop 136 is asserted whenever a refresh request is received through refresh line 146 from the AND gate 124. The signal from the refresh request flip-flop is asserted along the refresh request line 116 to the bit map sequencer synchronizer 112. The read/write status flip-flop 138 is asserted when a memory access request is made by a read/write request NAND gate 150 through a read/write request line 148. The flip-flop 138 is reset at the end of the memory cycle by the end memory access signal from the sequencer 114 through the end memory access line 126. The output

of this flip-flop is transmitted to the bit map sequencer synchronizer 112 through the read/write request line 120.

The data conversion logic circuit includes a write data buffer 151, a data buffer 154 and a shift register 156. All three units have the same data width of one data unit. The circuit is synchronized by the pixel counter 144 and NAND gate 150 through the branch of the read/write request line 148. The synchronization is achieved when the pixel counter generates an output signal by counting the print engine clock to a data unit (connection now shown). The signal is further conditioned by logically ANDing the pixel count with that from the delay flip-flop 130 through the NAND gate 150. The resulting signal is a shift load signal triggering the loading of the data unit into the shift register 156 to start the read/write cycle. The data buffer 154 is used to synchronize the timing of the data transfer between the bit map memory and the print engine unit when the individual data units are transferred to the print engine. The data buffer is triggered by a read signal from the read/write sequencer through the read line 158. The write buffer 152 is a tri-state buffer which stores the data pattern to be written back to the bit map memory along the bit map data lines 68 when required by the print erase cycle. The buffer 152 is enabled by the write data enable signal asserted by the sequencer 114 through the write data enable line 128. During the scan process the retrieved data from the full page bit map 28 or 30 is first loaded temporarily into the data buffer 154 through the data lines 68. The data is then loaded into the shift register 156 and shifted out a bit at a time synchronously with the rising edge of the print engine clock. The print engine clock signal is transmitted to the shift register through a print engine

clock line 162 and the data bits are transferred to the print engine through a video shift out line 160.

The PDI also includes a 4 to 2 multiplexer 164 that selects the bit map synchronous signals from either the external print engine or from an internal data source. In this embodiment of the invention the multiplexer accepts either the print engine line sync through the print engine sync line 50 and the print signal engine clock through a print engine clock line 168, or signals from the PCSI through test enable and test clock lines 170, 172 respectively. When the PDI is in the normal operation mode the print engine line sync signal is passed through to the line sync line 88, and the print engine clock signal is passed through to a clock line 96, so as to synchronize the operation of the PDI. The PCSI test lines 170, 172 are provided so the PDI can do a self-test by writing a pattern into one of the bit maps and checking the content through the horizontal line processor without the presence of the print engine.

A 20 MHz clock 174 is provided to run the bit map sequencer. The clock is converted directly to a prescaler 176 that derives a 10 MHz clock signal that is transferred to the multiplexer 164 through a test clock line 166 for the internal test, and a 1.25 MHz through the burst refresh line 140 to the refresh and read/write arbitration circuit 160 to provide a burst refresh signal.

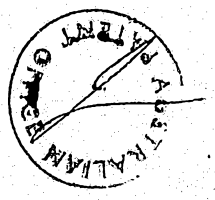
The bit map refresh is achieved by one of three stages of bit map refresh control. The first state, synchronous refresh, occurs whenever the PDI has control of a full page bit map but that bit map is not being accessed by the print engine as a source of print command instructions. In this stage, the refresh commands come from the horizontal line processor through refresh line 74. The second stage refresh is burst mode refresh.

This occurs when the PDI is in the print mode. The refresh is synchronous with the internal 1.25 MHz reference clock.. The burst mode refresh is inhibited during the effective bit map scan, or print engine read, period but remains active throughout the entire page scan period.

The third state refresh is the implied refresh. This refresh takes advantage of the fact that each time a dynamic random access memory cell is accessed the entire row the memory cell is in can be refreshed. By sequentially accessing adjacent row addresses a memory refresh is achieved. The address bus of the PDI is arranged so that the output of the columns address counter is used to linearly address the rows of the bit map memory to achieve the refreshing. The line address counter is used to address columns of bit map memory.

The burst mode refresh is provided because for some paper configurations the scan line width is too short so the entire full page bit map may not be refreshed during an implied refresh. The burst mode refresh periodically has the data refreshed so it will be useable by the print engine. Thus, when one of the full page bit map memories is accessed by the PDI, it is able to both linearly retrieve the pixel data stored therein for transmission to the print engine, and to frequently have the data refreshed, so it remains useable. An advantage of this feature is that the bit map can be repeatedly accessed for printing multiple copies without having to spend time recomposing the page.

It is understood that this description is for the purposes of illustration. Therefore it is intended that all matter contained in the above description or shown in the accompanying drawings be interpreted as illustrative and not limiting.



The Claims defining the Invention are as follows:

1. A print engine data interface for reading pixel image data from a first full page bit map memory and serially transferring the read data to a print engine in response to signals from a horizontal line processor, a printer control and status interface and the print engine, comprising:

(a) a set of command and data registers for storing programmed page format and scan length data from said printer control and status interface;

(b) a scan offset adjustment circuit coupled to receive the page format and scan length data from the command and data registers;

(c) means for periodically generating a burst refresh signal;

(d) an arbitration circuit coupled to detect whether the first full page bit map memory is to be read from/written to or refreshed, said arbitration circuit outputting refresh request signals in response to burst refresh signals to start the refresh cycle and outputting read/write request signals to start the memory cycle of each scan line;

(e) a bit map sequencer coupled to said arbitration circuit for generating read/write or refresh control signals for controlling said first full page bit map memory in dependence on the request signals output by said arbitration circuit;

(f) a bit map memory address counter coupled to said bit map sequencer and to said command and data registers for addressing said first full page bit map memory;

(g) a data conversion circuit coupled to receive data retrieved in parallel from said first full page bit map memory and converting the parallel data into a serial data stream for synchronous reception by the print engine in response to an enabling signal from said arbitration circuit; and

(h) a second full page bit map memory which is loaded with pixel image data while said first full page bit map memory is being read.

whereby the pixel image data stored in said first full page bit map memory is periodically refreshed in response to said burst refresh signals when said print engine data interface is in the print mode.

2. The print engine data interface as defined in claim 1, wherein said second full page bit map memory is coupled to said bit map sequencer and to said data conversion circuit, pixel image data being read from said second full page bit map memory while said first full page bit map memory is being loaded with pixel image data.

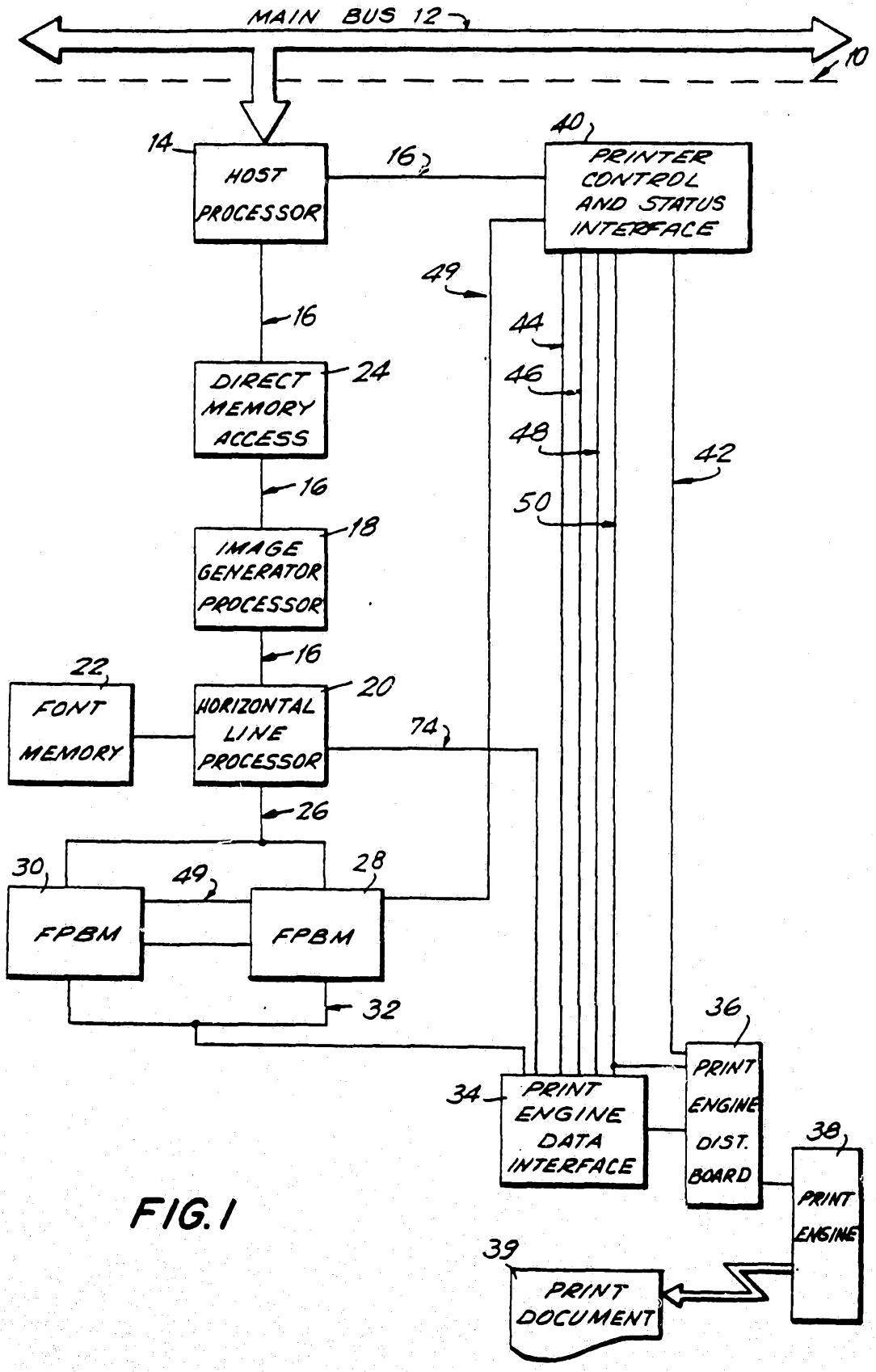
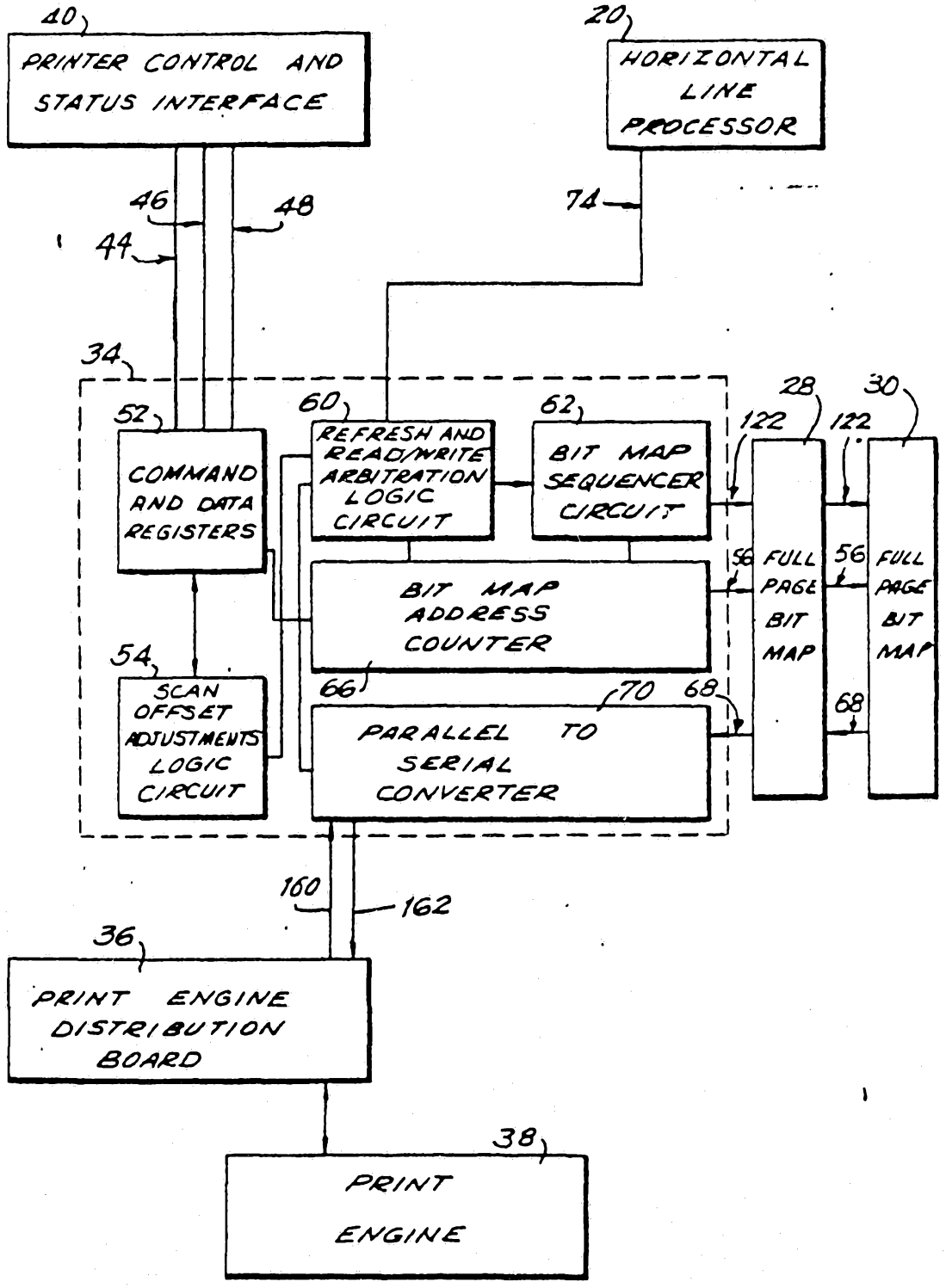

MAIN BUS 12
10
14
HOST PROCESSOR
16
40
PRINTER CONTROL AND STATUS INTERFACE
49
44
46
48
50
42
16
DIRECT MEMORY ACCESS
24
16
IMAGE GENERATOR PROCESSOR
18
16
22
FONT MEMORY
HORIZONTAL LINE PROCESSOR
20
74
26
30
49
28
FPBM
FPBM
32
36
PRINT ENGINE DIST. BOARD
34
PRINT ENGINE DATA INTERFACE
38
PRINT ENGINE
39
PRINT DOCUMENT

FIG. 1

FIG. 2



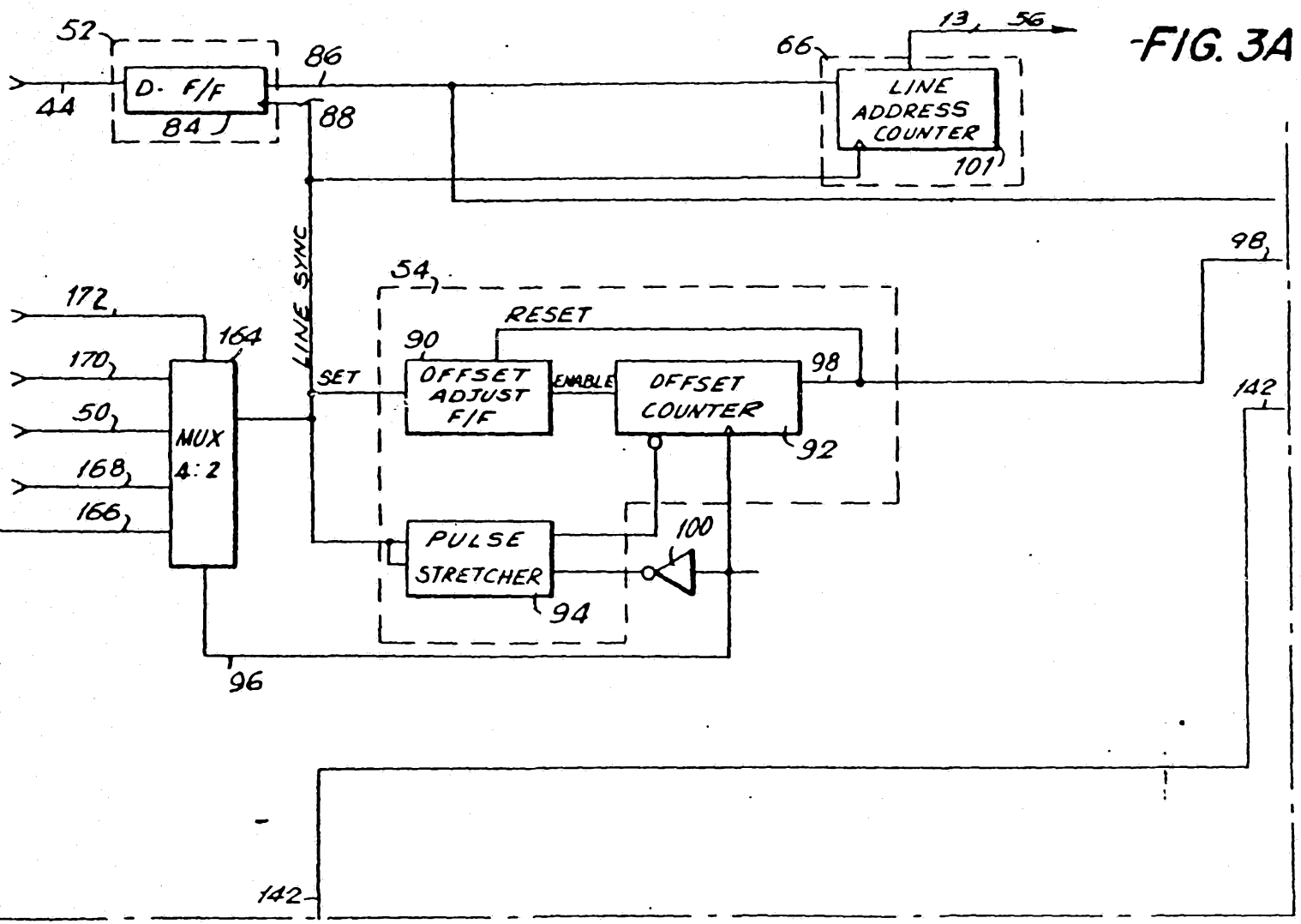
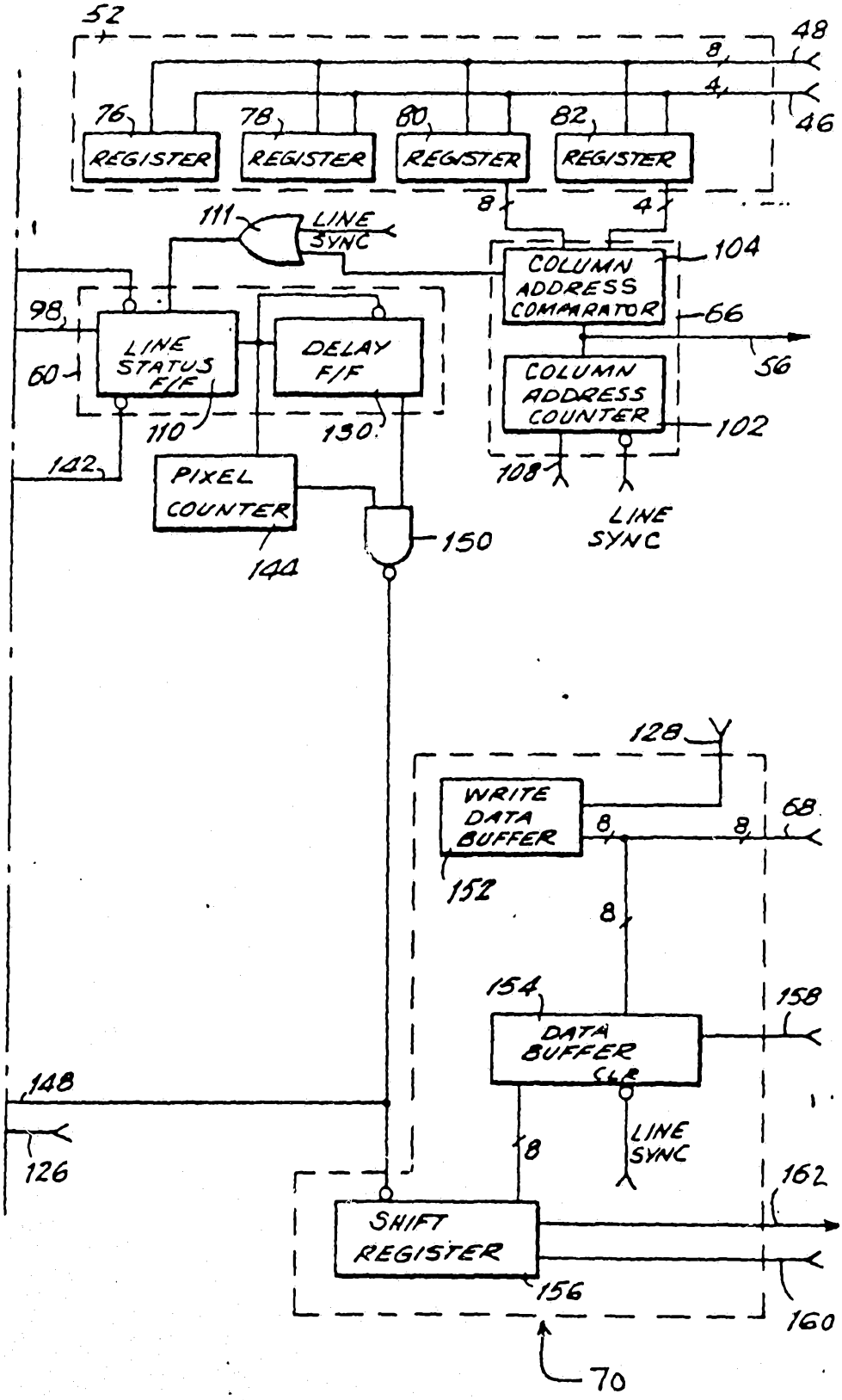

52
D. F/F
84
44
86
88
66
13, 56
LINE ADDRESS COUNTER
101
LINE SYNC
54
RESET
90
OFFSET ADJUST F/F
SET
ENABLE
OFFSET COUNTER
98
92
98
142
172
170
50
168
166
164
MUX 4:2
PULSE STRETCHER
94
100
96
142

FIG. 3A

FIG. 3B


52
48
8
4
46
76
78
80
82
REGISTER
REGISTER
REGISTER
REGISTER
8
4
111
LINE SYNC
104
COLUMN ADDRESS COMPARATOR
66
56
98
60
LINE STATUS F/F
DELAY F/F
110
130
COLUMN ADDRESS COUNTER
102
108
LINE SYNC
142
PIXEL COUNTER
144
150
128
WRITE DATA BUFFER
8
8
68
152
8
154
158
DATA BUFFER
CLR
148
126
8
LINE SYNC
162
SHIFT REGISTER
156
160
70

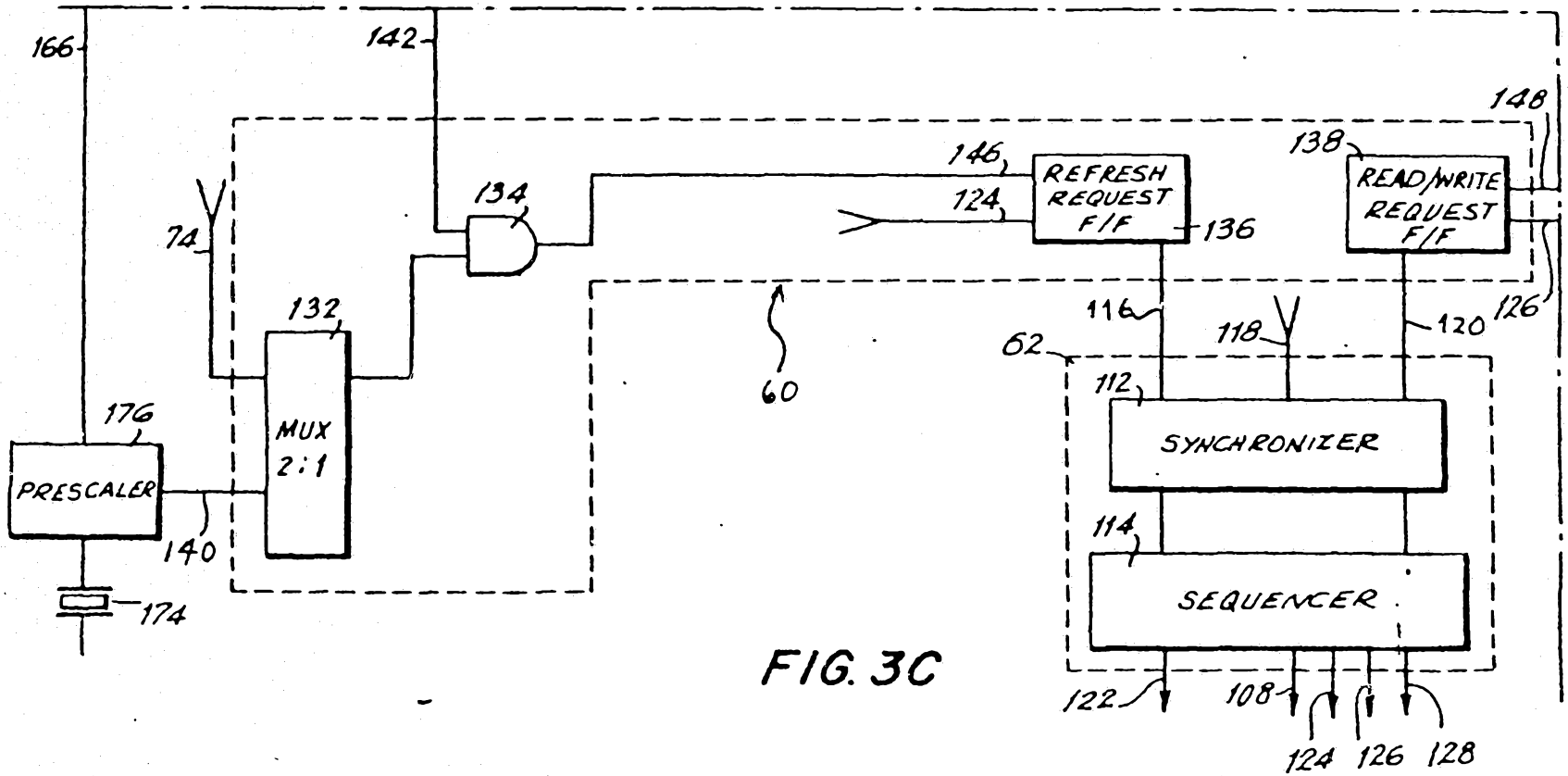


FIG. 3C

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 87/02128

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[4]: G 06 F 3/12

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC[4]	G 06 F 3/12; G 06 K 15/02; G 06 K 15/10; G 06 K 15/12; G 06 K 15/14

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
A,P	EP, A, 0217447 (OCÉ-NEDERLAND B.V.) 8 April 1987 see column 3, lines 21-36; column 5, lines 43-50; column 14, lines 38-42; column 18, lines 42-56; column 21, lines 42-57	1
A	Patent Abstracts of Japan, volume 8, no. 252 (P-314)(1689), 17 November 1984, & JP, A, 59123923 (FUJITSU K.K.) 17 April 1984 see the whole abstract	1
A	US, A, 4300206 (BELLESON et al.) 10 November 1981 see column 1, lines 48-68; figures 5,10	1
A	EP, A2, 0100853 (IBM) 22 February 1984 see page 1, line 21 - page 3, line 16; figures 1,11	1

./.

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
7th December 1987	25 JAN 1988
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	P.F.G. VAN DER PUTTEN

Form PCT/ISA/210 (second sheet) (January 1985)

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category *	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No
A	IBM Techical Disclosure Bulletin, volume 124, no. 2, July 1981, (Armonk, US), T.L. Anderson et al.: "Extended graphics storage and serialization for non-impact printers", pages 1011-1016 see the whole article	1
A	US, A, 4031519 (FINDLEY) 21 June 1977 see figure 5	1

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO. US 8702128 SA 18600

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 06/01/88
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

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		JP-A- 62074162	04-04-87
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		FR-A,B 2395840	26-01-79
		DE-A,B,C 2825321	04-01-79
		JP-A- 54013224	31-01-79
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		NL-A- 7512695	13-05-76
		FR-A,B 2290308	04-06-76
		DE-A,B,C 2550268	13-05-76
		GB-A- 1477427	22-06-77
		CH-A- 600435	15-06-78
		CA-A- 1042354	14-11-78
		CA-A- 1044609	19-12-78
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		SE-A- 7512443	12-05-76
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