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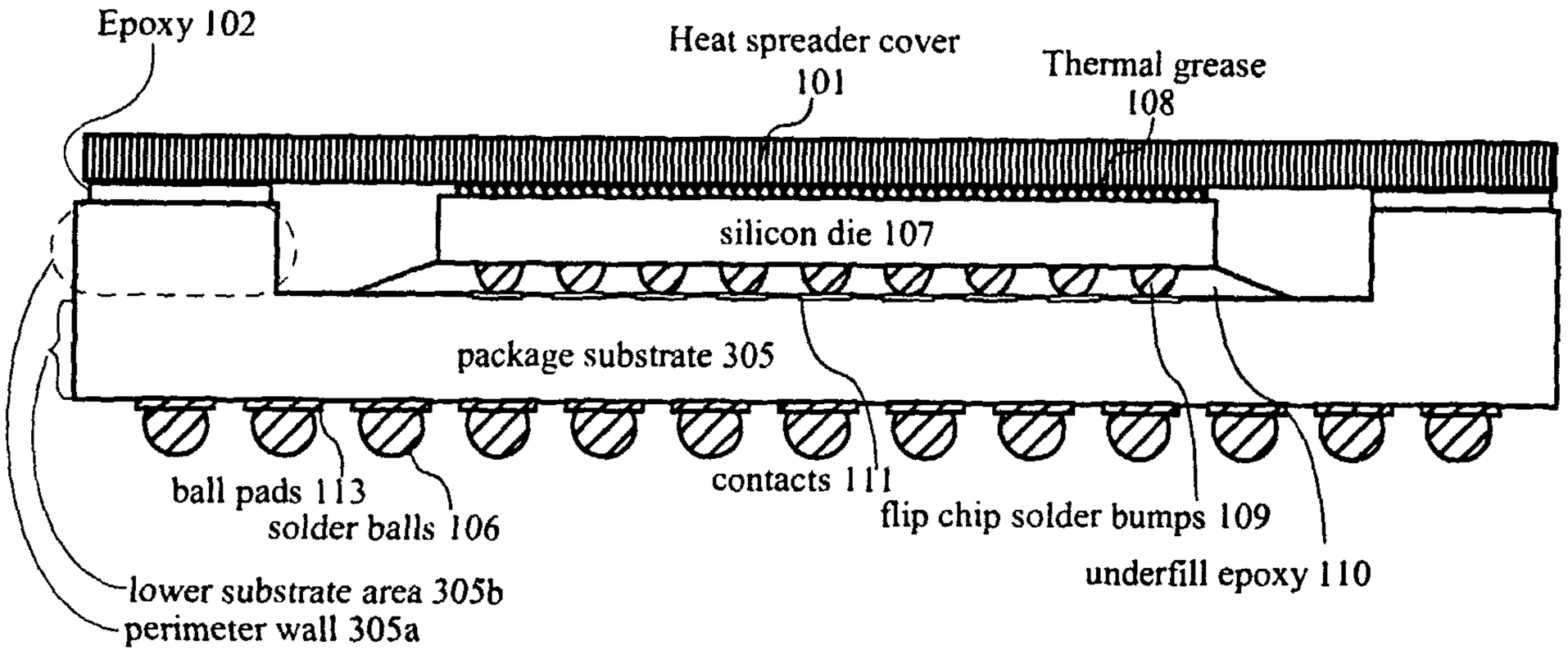


(57) Abrégé/Abstract:
The present invention provides an improved semiconductor flipchip package that includes a central cavity area on the first major side for receiving a flipchip die therein. The package substrate is substantially made from a single material that serves as the support and stiffener and provides within the cavity floor all the connecting points for flipchip interconnection to the silicon die. The integral cavity wall serves as a stiffener member of the package and provides the required mechanical stability of the whole arrangement without the need for a separate stiffener material to be adhesively attached. The cavity walls may contain extra routing metallization to create bypass capacitors to enhance electrical performance. The invention discloses optional methods to cover the silicon die to enhance thermal performance of the package.

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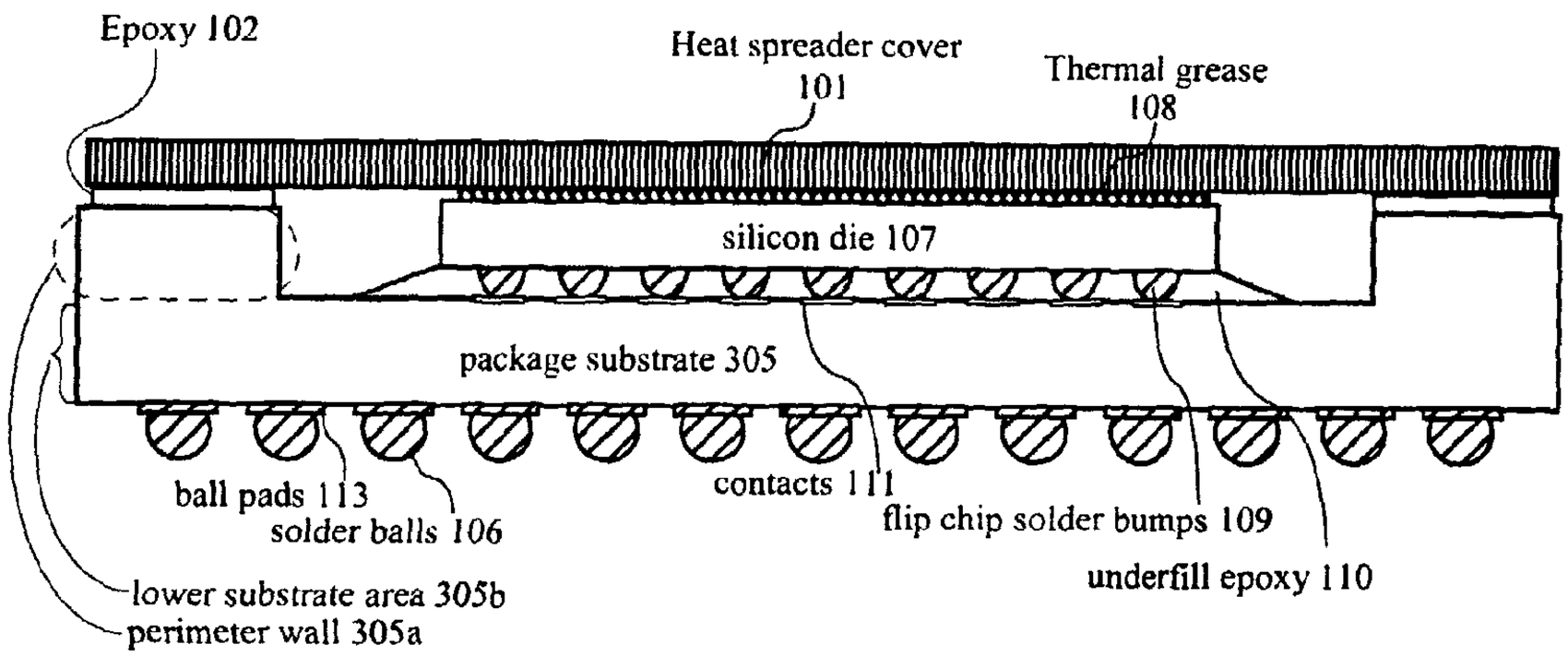


(57) Abstract: The present invention provides an improved semiconductor flipchip package that includes a central cavity area on the first major side for receiving a flipchip die therein. The package substrate is substantially made from a single material that serves as the support and stiffener and provides within the cavity floor all the connecting points for flipchip interconnection to the silicon die. The integral cavity wall serves as a stiffener member of the package and provides the required mechanical stability of the whole arrangement without the need for a separate stiffener material to be adhesively attached. The cavity walls may contain extra routing metallization to create bypass capacitors to enhance electrical performance. The invention discloses optional methods to cover the silicon die to enhance thermal performance of the package.

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# HIGH PERFORMANCE FLIPCHIP PACKAGE THAT INCORPORATES HEAT REMOVAL WITH MINIMAL THERMAL MISMATCH

## FIELD OF THE INVENTION

The invention relates to packaging of integrated circuits, particularly to flipchip-interconnected packaging that minimizes surface mount assembly temperature variations for a wide range of die sizes.

## BACKGROUND OF THE INVENTION

Over the last few years, there has been a surge of activity geared to the use of flipchip interconnection in integrated circuits packages targeted for high performance applications such as networking, storage, and high end CPU computing. There are a number of reasons for this activity in flipchip-interconnected packages. One of the primary drivers spurring this high level of activity is the ability of flipchip interconnection to address pad limitation for these more I/O intensive integrated circuits. A modern integrated circuit die can integrate several million transistors together to form complex systems on a chip. Associated with these complex systems is the need to connect the signals and associated ground and multi-voltage pads from the chip to the supporting package and subsequently to the several hundreds of external connections. Traditional peripheral pad structures run out of room in these devices, making pad array structures used in flipchip interconnection a viable and preferred option.

Another reason flipchip interconnection has become popular for these high performance devices is the added electrical performance afforded by the short I/O interconnects and the ability of flipchip interconnection to support power and ground connections to the precise locations where power and ground connections are needed on the chip.

Multi-layer ceramic substrates, glass-ceramic substrates, and laminated multilayer printed wiring boards (PWB) employing build-up of thin film are among some of the high performance packaging solutions commonly available

today to implement flipchip interconnection. Most of these packages are used in surface mount applications. Packages with flipchip interconnections have to be able to withstand the shock of surface mount assembly temperatures, and have an acceptable board-level reliability for the flipchip joints as well as the external ball joints over the anticipated use conditions.

A flipchip die disposed within a package must be flipped and connected to conductors patterned on the package or substrate through conductive balls or bumps on the active side of the chip in a bump array format covering most of the die's active surface. To extend the fatigue life of the die-to-substrate joints, an underfill material of epoxy is typically dispensed and allowed to cure around the joints to hold the interface together. At this stage, the resulting assembly is commonly referred to as capless, and some end users deploy the device in this capless format. Depending on the end application, various thermal enhancement schemes involving heatsinks, heat spreaders, and combination of encapsulants may be applied. The thermo-mechanical impact of some of these schemes can be challenging due to the number of materials and interfaces involved.

Fig. 1 depicts a cross section of a prior-art flipchip ball-grid-array package using a typical substrate 105 with external solder balls 106 for connecting to an external printed circuit board. Lim et al. in U.S. Patent 6,020,221 discloses this type of structure. The silicon chip or die 107 is connected to substrate 105 by solder bumps 109 formed at the active surface of die 107 before it is separated from the silicon wafer. During assembly, the silicon die with the bumps is put in place with the bumps 109 against array contacts 111 on the upper surface of package substrate 105, preferably by solder reflow, though other attachment methods are possible. The space between the die and the substrate is usually filled with underfill material 110, for example epoxy, through capillary action. The material 110 is then cured in place. The underfill

material is electrically insulative and can be thermally conducting if required.

To maintain substrate flatness and stiffness, a stiffener 103 may be located at the perimeter of substrate 105 and held in place by epoxy 104. Lim et al. in U.S. Patent 6,020,221 also discloses this stiffener feature. In some cases, the stiffener attachment may precede the die mount process. For thermal performance of die 107, a heat spreader or covering heatsink 101 made typically of metal is connected to die 107 with thermal grease 108, and connected to stiffener 103 with epoxy 102. Heat enhanced structures are known. For example, Chia et al. in U.S. Patent 5,568,683 shows a heat-enhanced package. Not shown in Fig. 1 are the electrical connections formed within substrate 105 that connect solder bumps 109 to respective external solder balls 106.

An organic laminate material may be used for substrate 105. Alternatively, as pointed out by Lan Hoang in US Patent No. 6,201,301, other materials such as aluminum nitride, silicon carbide, glass ceramic, and polyimide, etc. may be used for substrate 105. These flipchip package substrates are typically formed in several layers with conductors extending between insulating layers. Traces from the plurality of electrically conducting contact pads 111 on the top surface of the substrate route through electrical vias connecting subsequent layers until the traces end in the corresponding external ball pads 113 at the outer surface opposite the face contacting the die 107. In organic material, several of these layers are laminated together or use sequential build-up technology to form the substrate. In ceramic substrates, the thin ceramic layers with metal circuits on top of them are stacked up and fired at high temperatures to achieve the desired structure. Fujitsu, Kyocera, NTK, 3M (Gore), Unicap, and Ibiden are among manufacturers who offer high performance ceramic as well as laminate ball grid array packages (BGAs).

Fig. 2 shows another prior art package with base substrate 105 sharing similar material characteristics with

the one described in Fig.1. For ease of review, elements having the same structure and function are given the same reference numerals. In the structure depicted in Fig. 2, the base substrate stiffening function is performed by a single piece heat spreader cover 201. The one-piece lid serves the functions of stiffening and heatsinking at the same time.

A problem associated with most of these conventional high performance flipchip packaging structures is that the structure is relatively complex and can be difficult to manufacture. They encompass several different material types that are adhesively bonded to form the package. The thermal interaction between these materials as the structures are exposed to the normal fabrication process temperatures can lead to warpage, lack of planarity and contact issues. Furthermore, normal component mount reflow temperatures and subsequent temperature and power cycles experienced by such complex composite structures during use can lead to thermo-mechanical failures.

A packaged device brings together several materials having different coefficients of thermal expansion (CTE). Among them is the silicon die with CTE between 2.5 and 3 ppm/°C. Substrates can vary from ceramic with CTE around 5.0 ppm/°C to glass-ceramic with CTE typically 8 to 12 ppm/°C to organic laminate with CTE over 16.0 ppm/°C. Encapsulants and underfill based on thermoset epoxy can have CTE around 12 to 18 ppm/°C below their glass transition temperature Tg and much higher numbers such as 50 to 70 ppm/°C above their Tg. Heatsinks and heat spreaders are typically made with copper, having typical CTE values of 16.5 ppm/°C. One of the challenges in modern electronic packaging is to select materials with closely matched CTE over the temperature of interest. This way the normal sources of temperature variations during the component manufacture, testing, reflow onto a board, and subsequent power cycles during use, will minimize CTE-stress-induced failures and thus improve reliability.

The structure of Fig. 1 uses the window stiffener 103 to achieve overall package stiffness. Without it, the substrate 105 is likely to bend as the underfill cools after cure. Though effort is made in material selection to match substrate 105 and stiffener 103 in CTE values, perfect matching is not always possible over the range of temperatures. The cover structure 201 in Fig. 2 serves a similar stiffness function. Again, any variation in expansion differences or a failure in adhesion 104 can lead to loss of function and reliability. It is desirable to minimize the bending of the composite component structure made by die 107 and substrate 105.

## SUMMARY OF THE INVENTION

The present invention is directed to enhancing the structure used in making these packages to make the packages simpler to put together, reduce warpage during assembly, and minimize interfacial stresses without changing base function of the high performance package. The present invention provides an improved semiconductor package that minimizes the number of material types and interfaces required to implement heatsink in a thermally enhanced flipchip BGA package substrate. According to the invention, a single structure incorporating a cavity area for the die serves as both the support substrate and stiffener. The single rigid substrate with a cavity in which the die is mounted with flipchip interconnect addresses the stiffness function with a simple manufacturing step, and more importantly provides perfectly matched CTE between walls and floor of the package, so that it does not cause CTE interfacial reliability problems. Having matched CTE walls and floor of the cavity package allows the use of encapsulants without worrying about in-plane and z-axis CTE differences between the periphery of the cavity floor and the edge of the inner cavity wall.

The connecting points to the external balls end in an array of pads in the cavity area within the boundary of the die. This structural arrangement substantially eliminates

interfacial stresses associated with adhesively attached stiffeners made from heterogeneous materials having different CTEs over the range of operating temperature. The single unitary structure includes conductive wiring layers in which conductors are formed connecting the conductors on the silicon die to conductors such as solder balls external to the package. Several optional top surfaces and encapsulants that can be used with the base are described.

The shape of this single unitary structure allows it to be used as a container or dam for receiving encapsulating material to provide die protection. Again, due to the homogeneous nature of the floor and the walls, this arrangement lends itself to selecting an encapsulant with the appropriate CTE.

Also, as a feature of the invention, because the cavity wall is part of the continuous substrate, it is possible to extend some circuit function into the wall. In particular, plate capacitors in the wall can serve as high frequency bypass capacitors in proximity to the die. The wall of the single unitary structure may include interleaved conductive layers forming one or more chip capacitors for high frequency bypass purposes. When the single unitary structure is formed primarily of material with moderate dielectric constant (5 to 9 ppm/°C) such as ceramic or glass material, conductive and insulating materials may be formed in successive thin layers to create parallel plate capacitors with the ceramic as the dielectric. Placing a capacitor adjacent to the silicon chip provides immediate charge stability to the power and ground voltages experienced by the silicon chip, reducing ground bounce and improving high speed switching characteristics of the integrated circuit device.

## BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1 and 2 represent cross sections of prior art package structures having flat laminated substrates.

Figs. 3-6 represent package structures according to the invention having unitary structures comprising both the package substrate and perimeter walls and having several different arrangements for thermal enhancement.

Fig. 7 represents cross section detail of a package structure according to the invention illustrating how a capacitor is incorporated into the perimeter walls.

DETAILED DESCRIPTION

Fig. 3 shows one embodiment of the invention in which package 305 comprises a unitary structure having a central recessed region surrounded by perimeter walls 305a. Positioned within the central recessed region is silicon die 107 electrically connected to a plurality of contacts 111 in the central recessed region by solder bumps 109 and held in place by underfill epoxy 110. Unlike the prior art structures of Figs. 1 and 2, package 305 is not just flat but incorporates the perimeter walls 305a as a single continuous piece with a lower substrate floor region 305b. The structure itself can have similar material characteristics to those used in prior art structures. A material laminate for package 305 may be procured from Kyocera, Japan as the HiTCE integrated circuit substrate with CTE of 12 ppm/°C. In the package 305, as illustrated, the cavity floor interconnect metal is patterned to define an array of contact pads 111 that correspond to a similar arrangement of bumps 109 on the die 107. The contact pads 111 are preferably copper that is plated with nickel and then gold before the bumps 109 are formed. Vias and traces from the contact pads 111 snake their way through metallization layers and insulating material to the external ball pads 113 for contacting the external balls 106.

Forming the floor or lower substrate layer 305b and stiffening walls 305a of package 305 as a single piece eliminates the thermal mismatch normally associated with traditional metal stiffeners 103 that are adhesively

attached, and eliminates any possibility of delamination that can occur with the structures of Figs.1 and 2.

Several structures for implementing silicon die 107 in package 305 are shown to take advantage of the simpler structure.

In Fig. 3, heat spreader 101, made preferably with a thin compliant metal, is connected to silicon die 107 with thermal grease 108 and attached to the top of walls 305a of package 305 by adhesively tacking in discontinuous sections with epoxy 102 (discontinuous to allow air or trapped moisture to escape during reflow). This produces a thermally enhanced package with a full heatsink.

In Fig. 4, the silicon die 107 is left exposed, but is held and protected by a thermally conductive encapsulant 411. The back of the silicon die 107 is positioned flat with the top of the cavity wall 305a. A lower profile thermally enhanced package results. Also, the encapsulant in this embodiment is in contact with the unitary cavity floor and dam walls, minimizing the chances for dissimilar material expansion differences and potential delamination in that vicinity.

Fig. 5 represents another embodiment in the use of this packaging where heat dissipation may not be the primary objective but the need to cover the silicon die and produce a low profile package may be paramount. In this embodiment, the silicon die 507 is thinned down prior to mounting so that the encapsulant can completely cover the whole die and the adjacent areas. The choice of encapsulant can be tailored to the heat needs of the arrangement. Thus in Fig. 5, die 507 is recessed within package 305, and encapsulant 511 covers both the sides and the exposed surface of die 507.

In Fig. 6, an embedded or drop-in heat spreader 601 covers the exposed surface of die 507, mating with encapsulant 611 to protect die 507 and provide attachment for an external heatsink (not shown) if desired.

Chip Capacitor in Package Wall

Fig. 7 shows a portion of package wall 305a and lower substrate area 305b in greater detail, illustrating some of the electrical connections within package 305. In the embodiment of Fig. 7, the raised perimeter wall region 305a includes one or more chip capacitors. Each capacitor is formed such that each capacitor plate 712 and 713 has a plurality of layers, and the layers of one plate alternate with layers of the other plate, separated by insulation. In Fig. 7, layers 712a, 712b, and 712c of capacitor plate 712 alternate with layers 713a, 713b, and 713c of capacitor plate 713. Placing these layers close together, separated only by thin insulating layers allows the capacitance value to be large. Further, placing the chip capacitor (or capacitors) within the package walls puts the capacitor close to the chip so that it can maintain steady supply voltage in the presence of high speed switching. In particular, the capacitor can accommodate the high speed input/output switching that occurs on a serial input/output bus.

Fig. 7 also shows metallization layers 714 within lower substrate area 305b. Solder balls 106 are joined to ball pads 113, which are connected through vias 716 to conductors 715 in one of the metallization layers 714. The conductors in one metallization layer may be connected through further vias 715 to further conductors and eventually to package contact pads 111 (shown in the earlier figures). Thus electrical connection is made between solder balls 106 external to the package and solder bumps 109 (shown in earlier figures).

CLAIMS

1. A packaged integrated circuit device comprising:

a substrate having a recessed central region surrounded by a raised perimeter, the central region and the perimeter being formed together from the same material, the central region having a plurality of contacts for providing electrical connection from conductors external to the substrate to an integrated circuit device; and

an integrated circuit device formed with contacts on a top surface, flipped, and placed against the central region of the substrate such that the contacts of the integrated circuit device meet the contacts of the central region of the substrate.

2. The packaged integrated circuit device of Claim 1 wherein the contacts of the central region of the substrate are electrically connected to solder balls on an external surface of the packaged integrated circuit device.

3. The packaged integrated circuit device of Claim 1 wherein the substrate is formed primarily from a ceramic material.

4. The packaged integrated circuit device of Claim 3 wherein the ceramic material also includes glass, thereby comprising a glass ceramic material.

5. The packaged integrated circuit device of Claim 1 wherein the contacts of the central region of the substrate comprise solder bumps.

6. The packaged integrated circuit device of Claim 1 further comprising a heat spreader connected to the integrated circuit device with thermal grease.

7. The packaged integrated circuit device of Claim 6 wherein the heat spreader further contacts the raised perimeter

8. The packaged integrated circuit device of Claim 6 wherein the integrated circuit device and the heat spreader are recessed such that an upper surface of the heat spreader is planar with an upper surface of the raised perimeter.

9. The packaged integrated circuit device of Claim 1 wherein the raised perimeter incorporates a capacitor electrically connected to power and ground contacts of the integrated circuit device.

10. An integrated circuit package substrate comprising:

a recessed central region having a plurality of contacts for providing electrical contact to an integrated circuit device; and

a raised peripheral area incorporating at least one capacitor connected to contacts in the recessed central region.

11. The integrated circuit package substrate of Claim 10 wherein the capacitor has a sandwich construction comprising a plurality of ground plates connected to a ground terminal alternating with a plurality of power plates connected to a power terminal, and insulating material is disposed between adjacent plates.

12. The integrated circuit package substrate of Claim 11 wherein the ground and power terminals are connected respectively to ground and power supply terminals of the integrated circuit device.

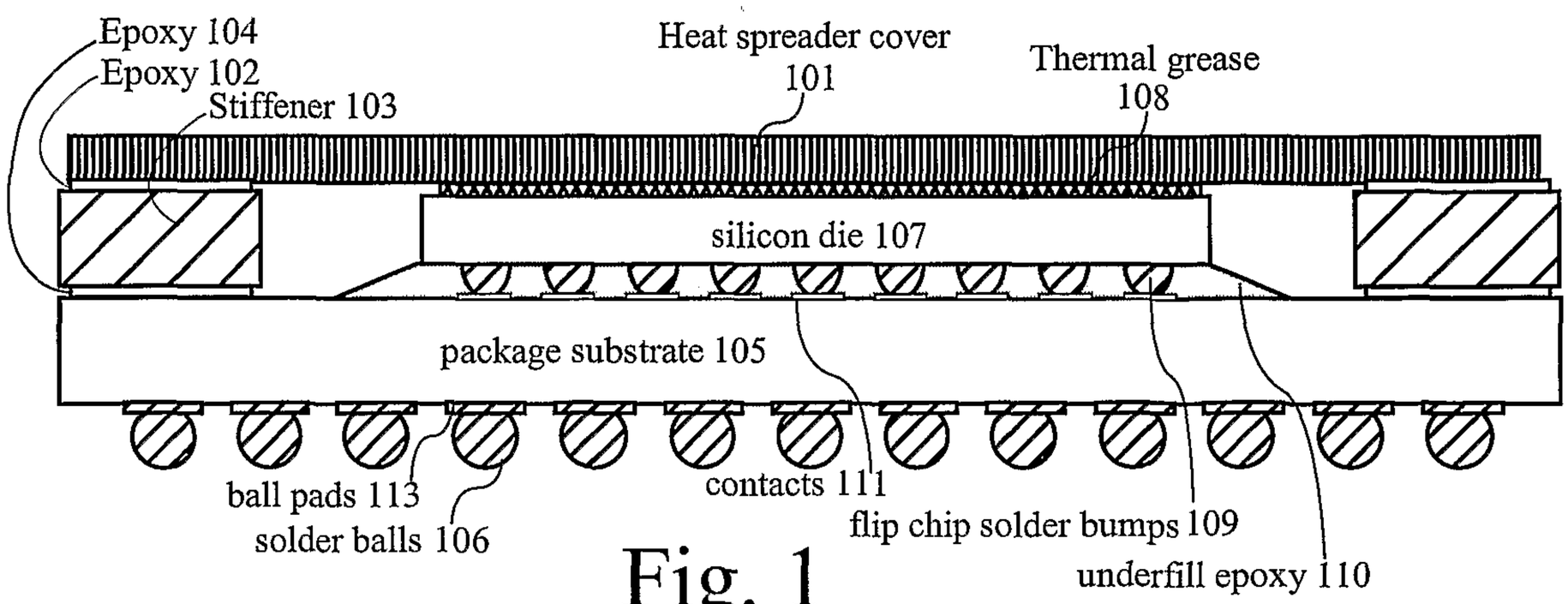



Fig. 1
Prior Art

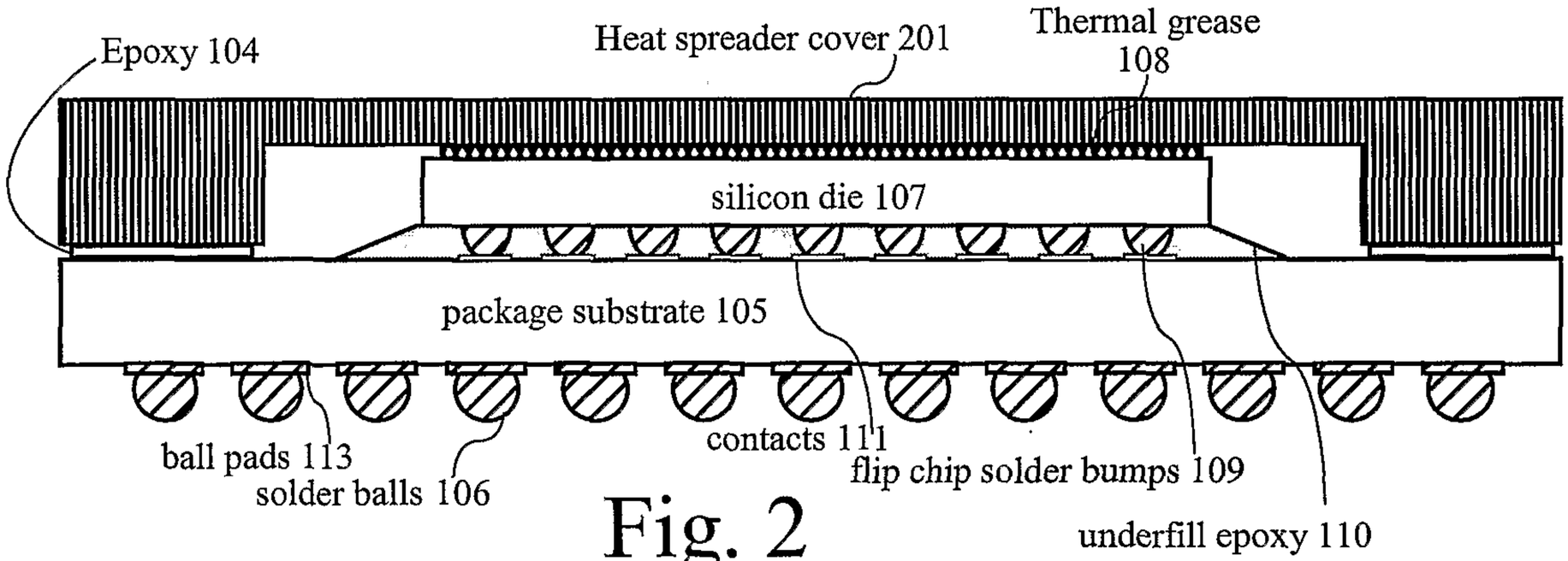



Fig. 2
Prior Art

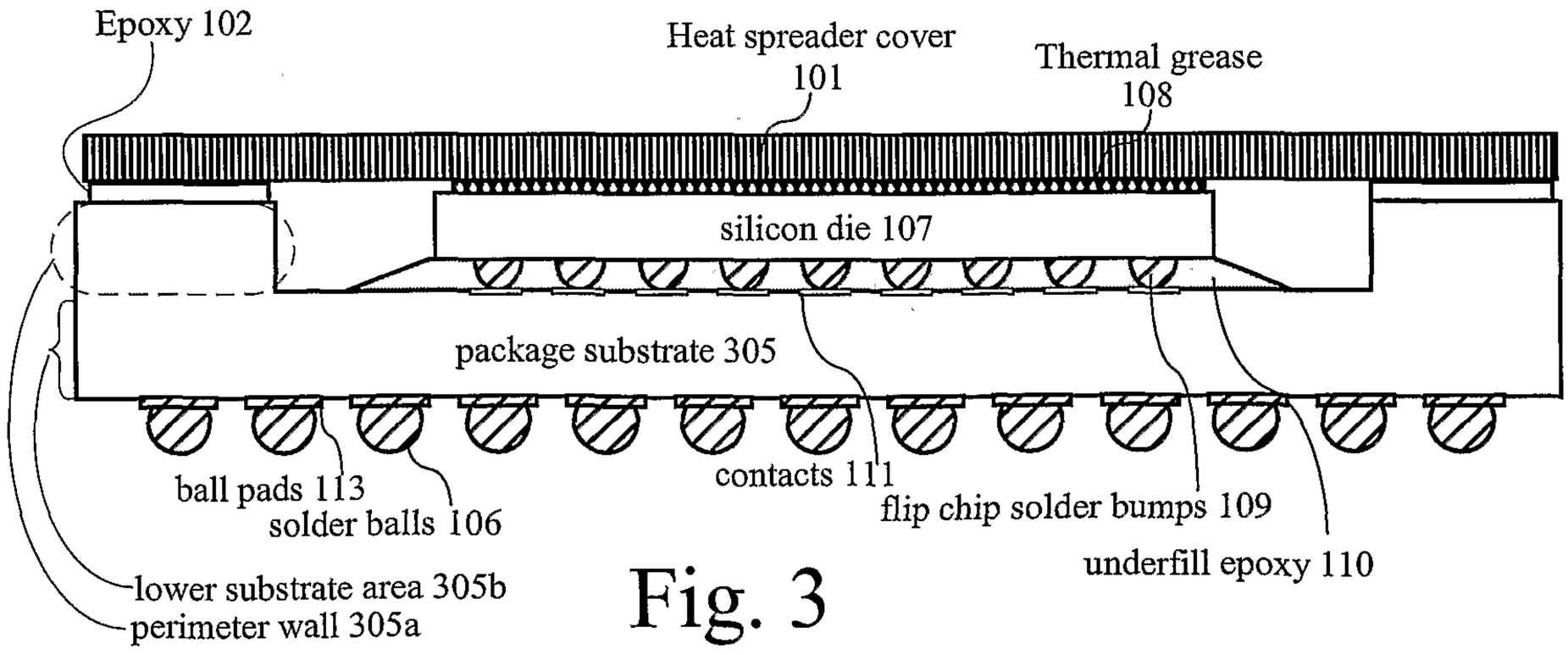



Fig. 3

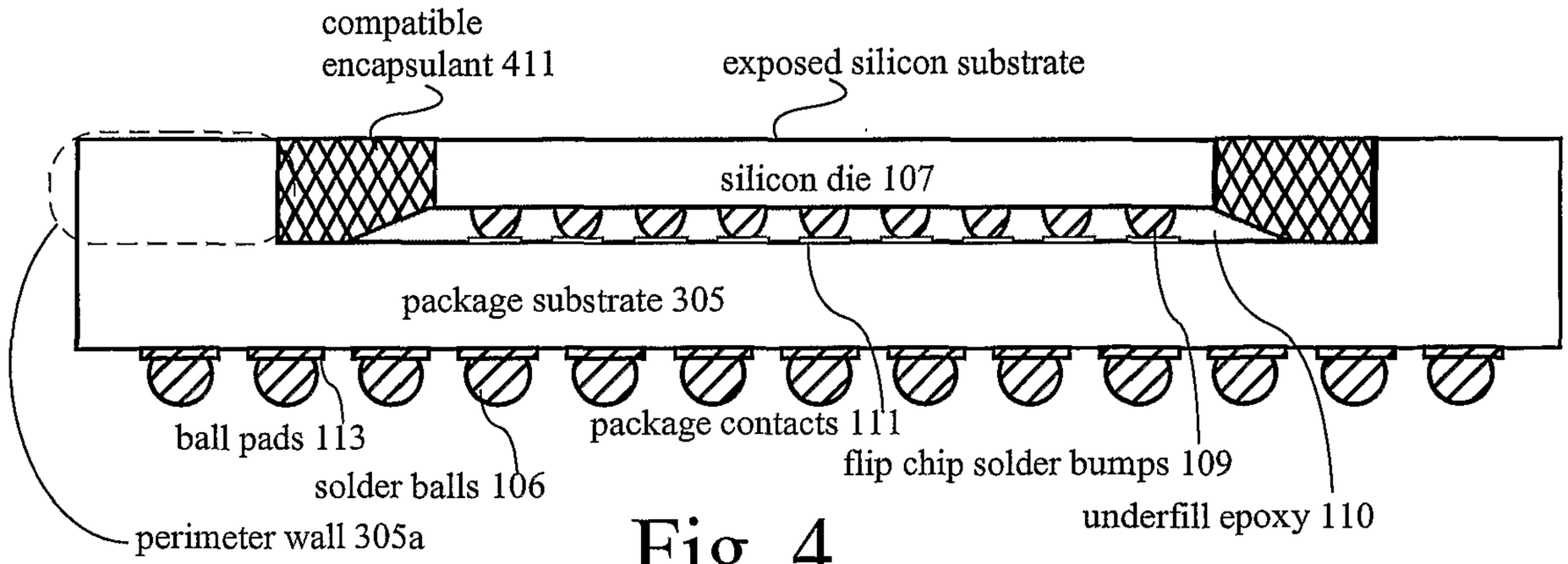



Fig. 4

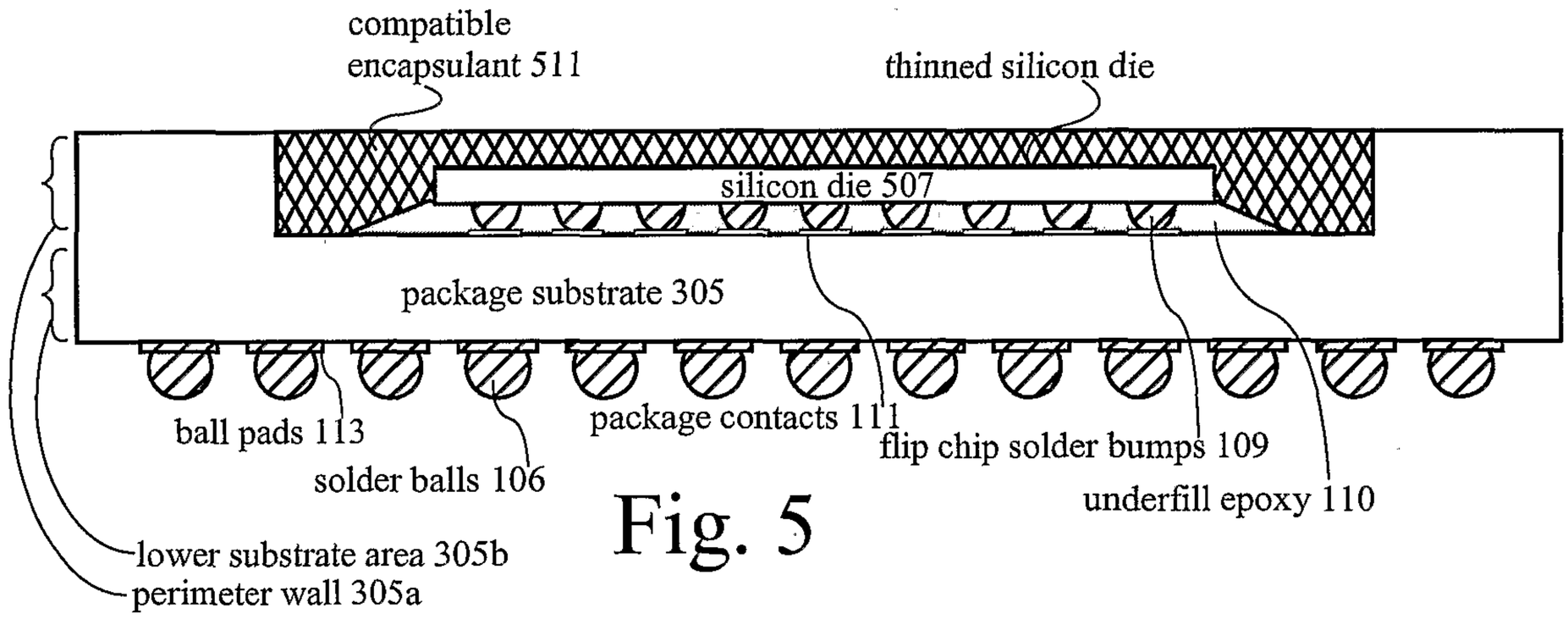



Fig. 5

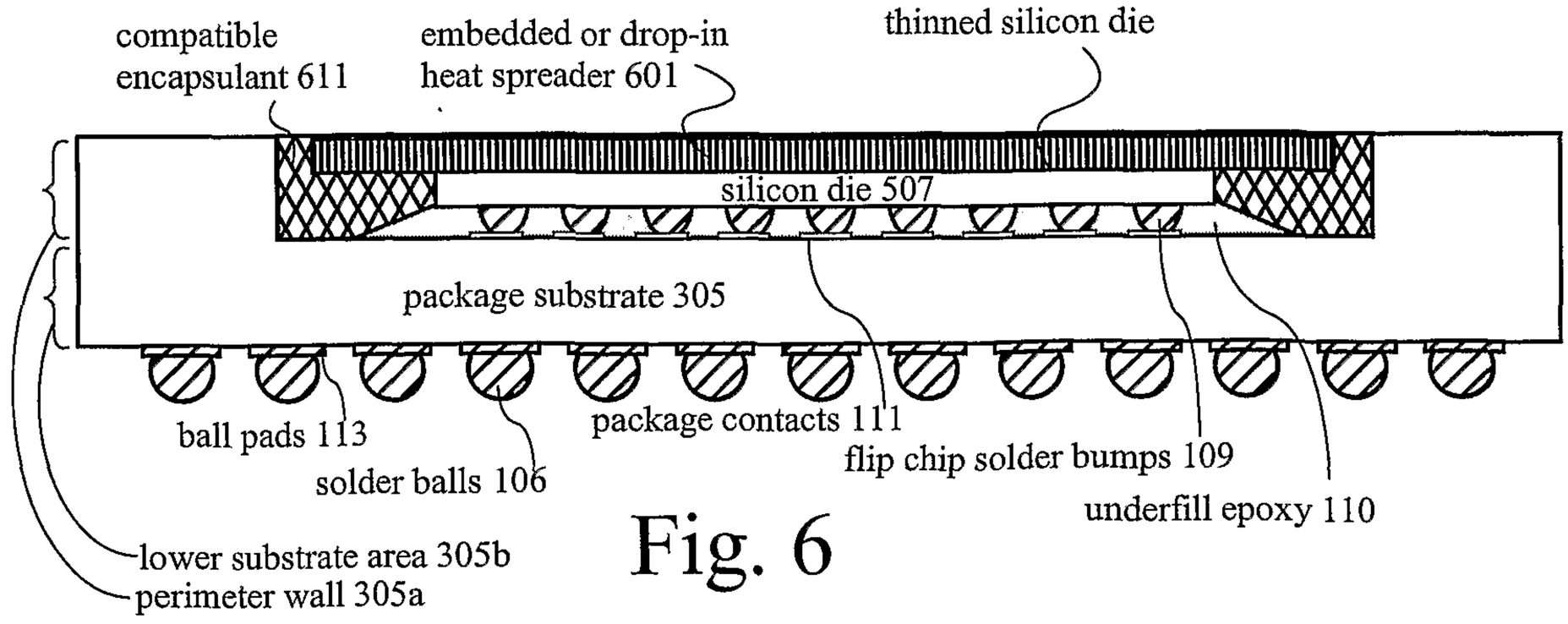



Fig. 6

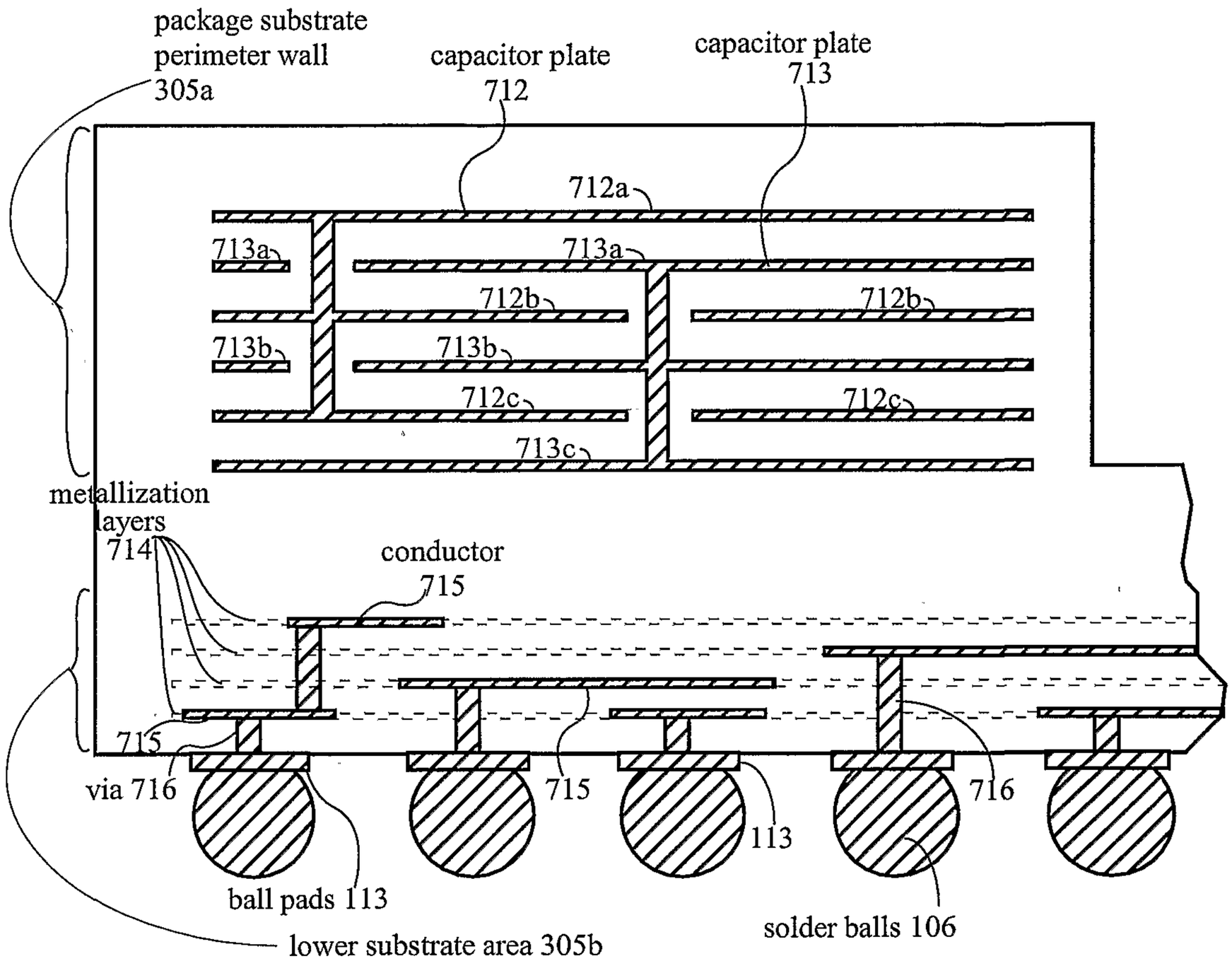
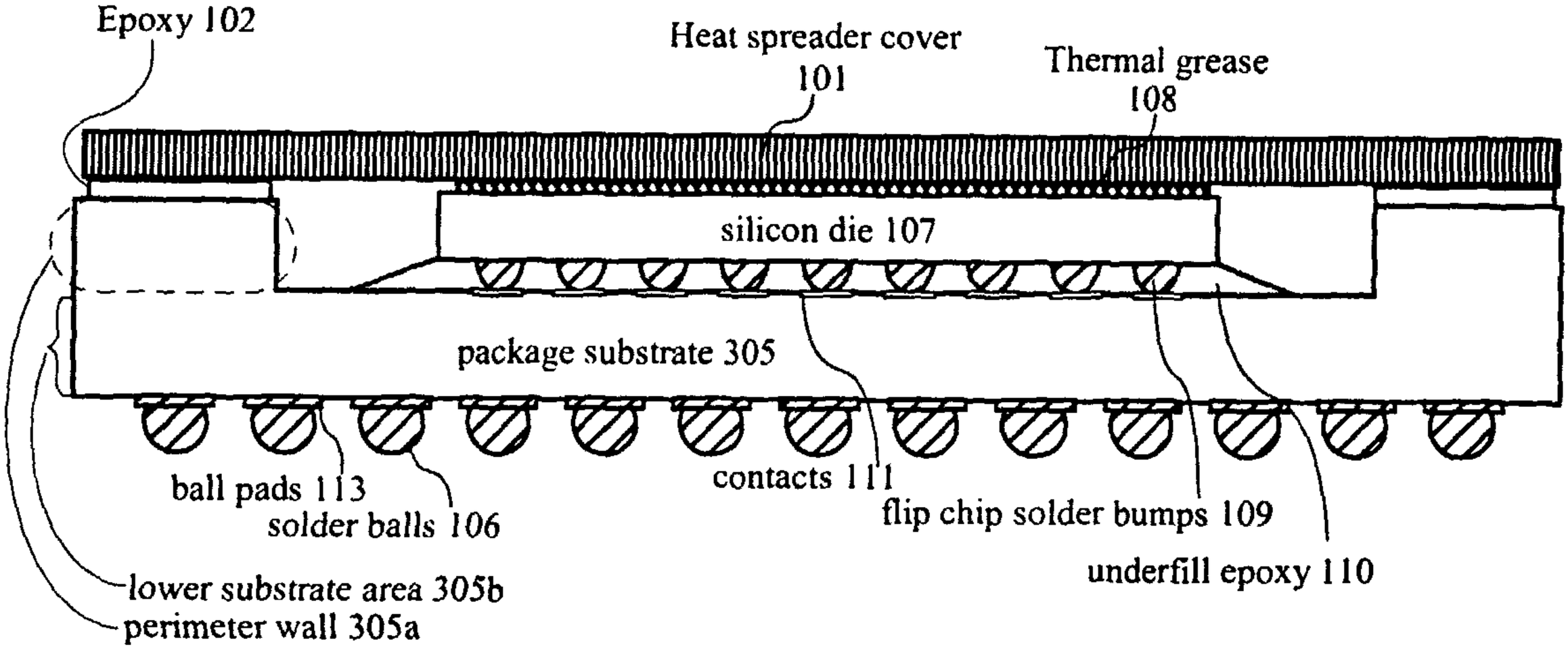

package substrate perimeter wall 305a
capacitor plate 712
capacitor plate 713
712a
713a
713a
712b
712b
713b
713b
712c
712c
713c
metallization layers 714
conductor 715
715
via 716
715
716
113
ball pads 113
solder balls 106
lower substrate area 305b

Fig. 7


Epoxy 102
Heat spreader cover
101
Thermal grease
108
silicon die 107
package substrate 305
ball pads 113
solder balls 106
contacts 111
flip chip solder bumps 109
underfill epoxy 110
lower substrate area 305b
perimeter wall 305a