United States Patent

[11] 3,558,933

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[21] Appl. No. **725,804**
[22] Filed **May 1, 1968**
[45] Patented **Jan. 26, 1971**

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[54] **VOLTAGE VARIABLE DELAY LINE TERMINATION**
5 Claims, 4 Drawing Figs.

[52] **U.S. Cl.** **307/293,** 328/56, 333/18, 333/29
[51] **Int. Cl.** **H03k 5/159**
[50] **Field of Search** 307/293, 320; 328/55, 56; 333/29, 17, 18

[56] **References Cited**
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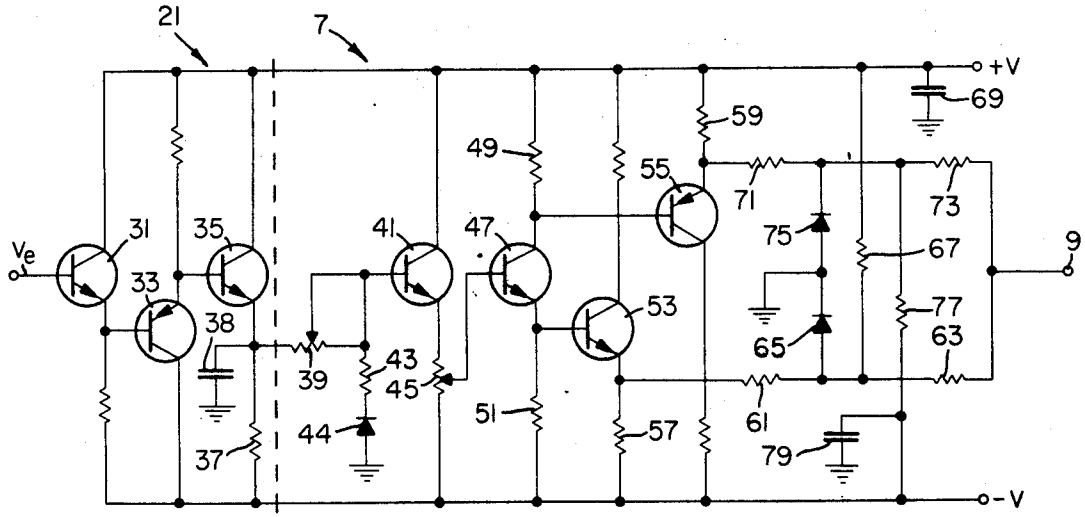
Attorney—Robert G. Clay

ABSTRACT: A voltage variable delay line network in which the delay of the line is dependent upon the bias, and the terminating impedance varies in accordance with the conductive state of a voltage variable termination network responsive to a signal corresponding to the bias.



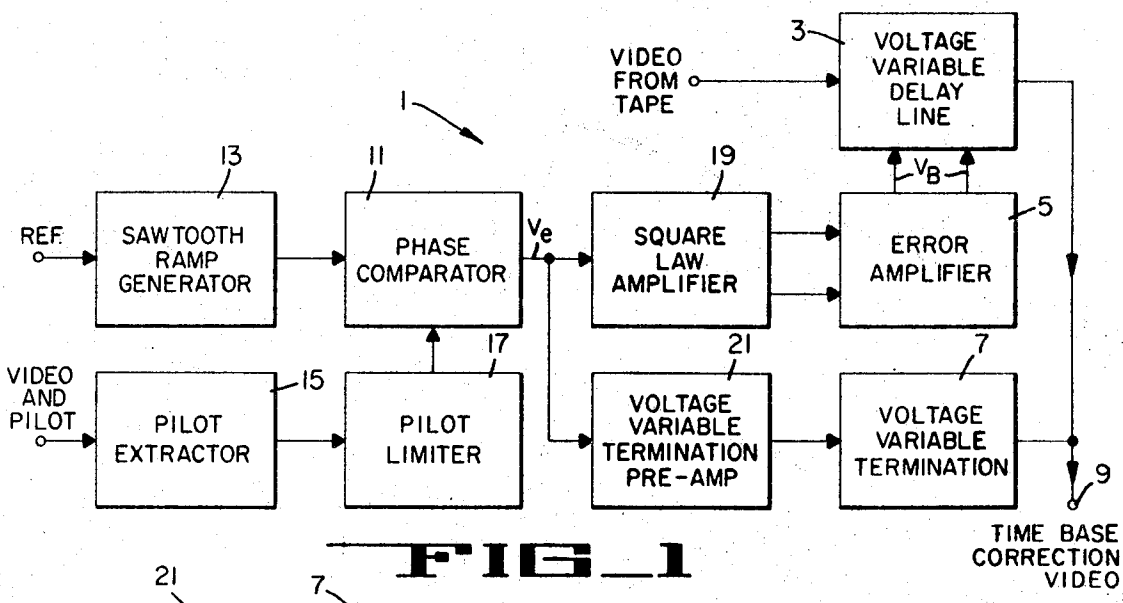


FIG_1

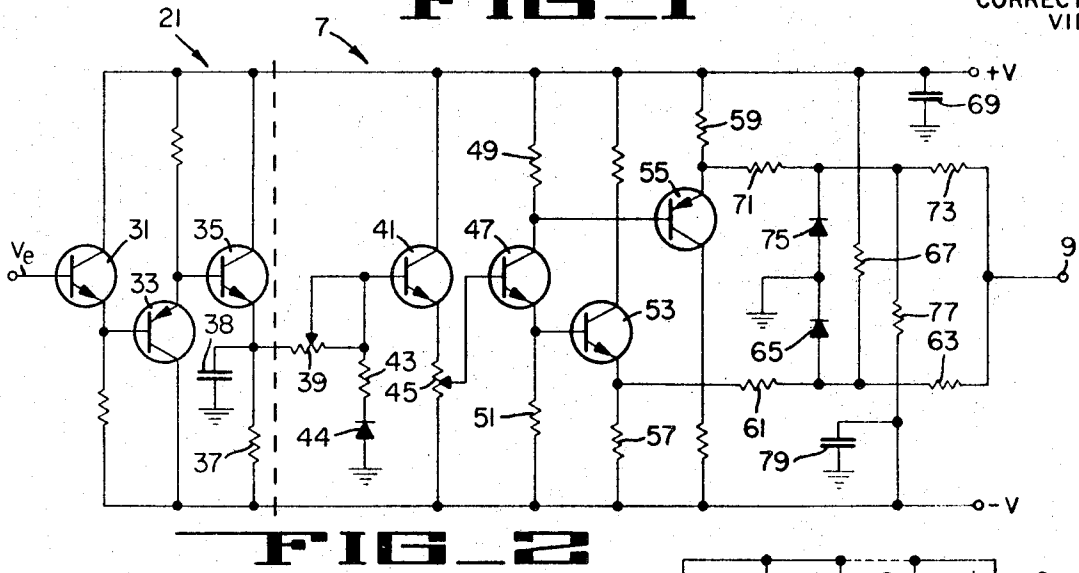


FIG_2

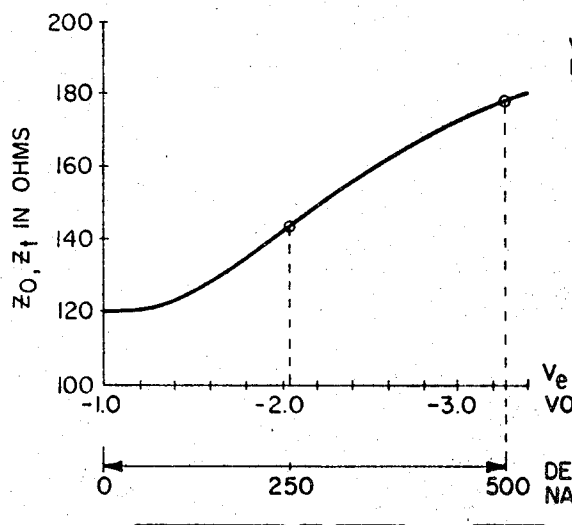


FIG_3

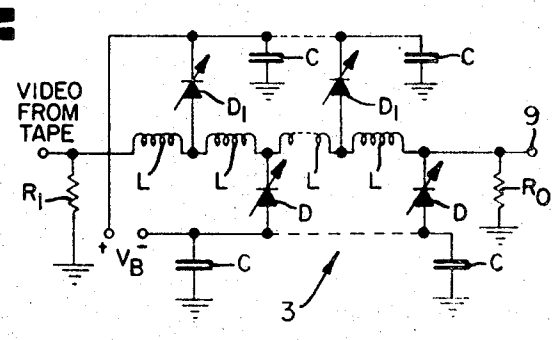


FIG_4

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VOLTAGE VARIABLE DELAY LINE TERMINATION

BACKGROUND OF THE INVENTION

This invention relates to voltage variable delay lines and more particularly to a termination for voltage variable delay lines which automatically provides for correct electrical termination over the line operating range.

Voltage variable delay networks are well known in the electronics art for providing variable time delay of a signal. The delay is varied by varying the bias. Heretofore, it has been common to terminate voltage variable delay lines with resistors of a select value providing correct electrical termination at center bias. However, changes in the bias and delay result in the line being misterminated in proportion to the degree from center the bias has strayed. The mistermination results in a mismatch of the characteristic impedance and the output impedance such that reflected waves exist along the line.

Variable delay lines are known in time base error corrector networks of magnetic tape transports. In the magnetic recording/reproduce art, there is considerable dependence on mechanically moving parts at critical places in the system. The time function of an electrical signal is transformed into a space function. Therefore, most of the parameters defining the mechanical construction and performance of the recorder enter the transfer function from the time domain to the space domain in the storage process. This also affects the reverse process of information retrieval. The end result, without correction or compensation, is that the reproduced information is a time function with spurious variations of the original recorded signal appearing as timing or time-base errors. These spurious transients generated in the recording system are usually of detrimental influence. Consequently, it is necessary to incorporate time-base correction electronics for time-base stability. In time-base correction it has been known to apply the intelligence signal to a voltage variable delay line prior to demodulation. In such systems the voltage variable delay line is biased with an error signal indicative of the degree of time-base error. As the degree of error varies, the bias and degree of mistermination vary and the degree of losses across the line varies. The present invention teaches a method and system in which the intelligence is received by a properly matched voltage variable delay line notwithstanding the degree of time-base error. Accordingly, the losses on the delay line are reduced permitting a more optimum transfer of intelligence power.

SUMMARY OF THE PRESENT INVENTION

The present invention provides for a voltage variable delay network in which variations in the bias are automatically matched by variations in the load impedance of the line. The signals controlling the line bias also control the net line load impedance. Consequently, when the bias voltage changes, there are responsive changes in the delay line characteristic impedance and net load impedance. A control signal is received by a termination network, the conductive state of which is dependent upon the magnitude of the control signal. The network extends to the output of the delay line. Accordingly, as the control signal varies with the bias, the degree of conduction of the network varies and the net line load impedance varies.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram showing a voltage variable termination in conjunction with the present invention as it is employed by a time-base correction network of a magnetic tape transport;

FIG. 2 is a circuit diagram of voltage variable delay line termination network as shown in a block diagram of FIG. 1;

FIG. 3 is a graphical representation of the characteristic and load impedance versus bias of a voltage variable delay line; and

FIG. 4 is a schematic of a double-ended voltage variable delay line which may be used in the embodiment of FIG. 1.

DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1 illustrates in block diagram form a time-base corrector network, referred to by the general reference character 1, presently used in the playback electronics of a pilot stabilized video recorder/reproducer assembly. In such assemblies, a pilot tone, derived from a frequency standard, is combined with the video intelligence before recording. On playback, this pilot tone is extracted, amplified, limited and phase-compared to the frequency standard output. The resulting signal, called the error signal, controls the delay of an electronically variable delay line through which the intelligence signal is passed. By this means, time-base correction of the intelligence signal is accomplished. The use of the pilot signal is only one approach to develop an error signal and those skilled in the art will recognize various other approaches.

More explicitly, the corrector network 1 includes a voltage variable delay line 3 receiving the video signals from the tape. The delay line 3 also receives a variable voltage bias V_B from an error amplifier 5. The output of the delay line 3 is tied to a voltage variable termination network 7 common to an output terminal 9. The bias signal originates at a phase comparator 11 receiving a reference signal and a pilot signal from the tape. The reference signal, e.g. 500 kHz., is received by a sawtooth ramp generator 13 extending to the phase comparator 11. The pilot signals from the tape which are of a frequency coinciding with the reference, e.g. 500 kHz., and combined with the video signal, are received by a pilot extractor 15 adapted to extract the pilot signal from the video information. The pilot signal is received by a pilot limiter 17 which provides the second input signal to the phase comparator 11. The output of the phase comparator 11 represents the phase difference of the two input signals and is in the form of a direct current error signal V_e varying in magnitude in accordance with the phase error. The signal V_e is passed through a square law amplifier 19 and then to the error amplifier 5, which in turn provides the variable voltage bias V_B corresponding to V_e. Commonly, voltage variable delay lines have square law characteristics and the amplifier 19 changes the V_e from linear characteristics to square law characteristics. The amplifiers 5 and 19 are shown as having two output lines to accommodate a double-sided voltage variable delay line, which was incorporated in the present embodiment. The signal V_e also serves as a control signal received by a voltage variable termination preamplifier 21 extending to the voltage variable termination network 7. The network 7 is designed such that proper selection of its operating characteristics provides that for a change in V_e there is a change in its conducting characteristics and the network load on the line 3. The design is such that the characteristic impedance Z_o and terminating impedance Z_t of the line 3 substantially coincide at all bias levels.

FIG. 2 illustrates the circuitry of a voltage variable delay line termination network 7 and associated preamplifier 21. The error signal V_e is received by the preamplifier 21 comprising three emitter followers illustrated as an NPN transistor stage 31, a PNP transistor stage 33 and a NPN transistor stage 35. The emitter of the NPN transistor stage 35 is tied to the input of the network 7 and to a resistance-capacitance network of a resistor 37 and a capacitor 38. The transistor stages 31, 33 and 35 extend across a positive reference source +V and a negative reference source −V. The preamplifier stage 21 is, as shown, included to convert a high impedance source to a low impedance source.

The illustrated voltage variable termination network 7 includes a variable resistance in the form of a potentiometer 39 extending to the input of an emitter follower stage 41 and a resistor-diode network comprising a resistor 43 and diode 44. The resistor-diode network serves as a compensator depending upon the characteristics of the variable voltage delay line 3. As will hereinafter become evident in reference to FIG. 3, the characteristic impedance Z_o of the line 3 may become nonlinear at high bias points. Thus, the resistor-diode network is selected so that the impedance transformation of the termination network 7 takes a shape coinciding with that of the

delay line 3 at high bias. The emitter follower stage 41 includes a potentiometer 45 extending between the base and −V. The wiper arm of the potentiometer 45 is tied to a unit-gain phase splitter comprising an NPN transistor 47 of which the collector extends to +V through a resistor 49 and the emitter to −V through a resistor 51. The emitter of the transistor stage 47 extends to a control valve illustrated as an emitter follower comprising an NPN transistor stage 53. The collector of the transistor stage 47 extends to a control valve illustrated as an emitter follower comprising a second control valve illustrated as a PNP transistor stage 55. The transistors 53 and 55 serve as the input stages of a pair of complementary circuits responsive to drive signals of opposite polarity and the transistor 47 serves as providing the drive signals. The resistors 49 and 51 are selected such that the magnitude of the potentials to the transistors 53 and 55 are always equal to each other, though of opposite polarity. Thus, as one varies in magnitude there is a corresponding change in magnitude of the other. The emitter of the stage 53 extends to the −V through a resistance 57 and the emitter of the stage 55 extends to +V through a resistance 59.

The emitters of the emitter follower stages 53 and 55 also extend to a network comprising precision resistors and diodes which in combination with the potentiometers 39 and 45 determine the terminating impedance Z_t of the delay line 3. The emitter follower stage 53 extends through a first and second precision resistor 61, 63 to the voltage variable delay line or output terminal 9. Intermediate the two resistors 61 and 63 is a unidirectional conducting component in the form of a diode 65 of which the anode is tied to the junction of the resistors and the cathode to a ground reference plane. The junction is also common to a precision resistance 67 extending to +V and through a bypass capacitor 69 to ground. Thus, the diode 65 extends between the two fixed voltage reference levels ground and +V. The emitter follower stage 55 extends to the output terminal 9 through a similar resistor network comprising two precision resistors 71 and 73. The cathode of a unidirectional conducting component in the form of a diode 75 joins the junction of the two resistors 71 and 73 with the anode extending to a ground reference plane. A precision resistor 77, also common to the latter junction, extends to −V and to ground through a bypass capacitor 79. Thus, the diode 75 extends between the two fixed voltage reference levels ground and −V. Accordingly, the two diodes 65 and 75 are prebiased by the respective precision resistors 67 and 77. The resistors 61 and 71, which are of considerably higher value than the load resistors 63 and 73, vary the bias of the diodes 65 and 75 depending upon the conductive state of transistors 53 and 55. This, in turn, is dependent upon the value of the control signal V_e and the settings of the potentiometers 39 and 45. The resistors 61 and 71 may be in the order of approximately ten times greater than their respective associated load resistors 63 and 73, e.g. 1 kilohms to 110 ohms. The resistors 61 and 71 extend to isolate the diodes 65 and 75 from the transistors 53 and 55 such that the diodes 65 and 75 "see" a current source rather than a voltage source.

The diodes 65 and 75, in conjunction with their associated load resistors 63 and 73, provide for a resistance path from the output terminal 9 to ground. The "net resistance" is dependent upon the net bias on the diodes. The two emitter follower stages 53 and 55, being oriented to opposite polarities, control the net bias across the diodes 65 and 75. The potentiometers 39 and 45, respectively, set the maximum and minimum limits of the control signal V_e to which there will be responsive conduction reflected to the output terminal 9. It may be noted that the transistor 41 tends to isolate the potentiometers 39 and 45 from each other allowing adjustment of one without interfering with the other. Potentiometer 39 is adjusted for maximum negative bias and potentiometer 45 for minimum negative bias. This is viewed in delay line terminology as determining the tracking control for tracking the terminating impedance Z_t at the high and low ends which ends are set by the adjustment of the potentiometers 39 and 45. The reference point for determining dynamic range may be selected intermediate the high and low ends. Thus, if the delay line range is from 0 to 500 nanoseconds, the midpoint of 250 nanoseconds may be selected as the reference delay line 3 components may be selected with a dynamic range of ± 250 nanoseconds and the delay line 3 components may be selected such that a 250 nanoseconds delay, the line characteristic impedance Z_o and terminating impedance Z_t are matched.

As the delay varies from the 250 nanosecond reference, one side of the network 7 becomes more or less negative and the other side becomes more or less positive in an equal amount. That is, when the voltage on the emitter of the stage 55 becomes more positive responsive to the control signal V_e, the current through the diode 75 is decreased due to a "bucking effect" of the current through the resistor 71 to the current through the diode 75 supplied by the resistor 77 from −V. At the same time, the emitter of the stage 53 becomes more negative, the current through diode 65 is decreased due to the "-bucking effect" of the current through the resistor 61 to the current of diode 65 supplied by the resistor 67 from +V. When the voltage on the emitter of the stage 55 becomes more negative and the voltage on the emitter of the stage 53 becomes more positive responsive to the control signal V_e, the opposite reaction occurs. In essence, it is believed that both stages 53 and 55 continuously conduct equally, but in opposite phase with the amount of current drawn dependent on the voltage V_e. Thus, as time base error variations are reflected in vibrations of V_e, the network 7 varies the load on the line and thus the net terminating impedance.

FIG. 3 illustrates test results comparing the characteristic impedance Z_o and terminating impedance Z_t with the error voltage and resultant time delay. These results reflect measurements taken from a terminating network of the circuitry of FIG. 2 terminating a double-sided voltage variable delay line similar to that illustrated in FIG. 4. As shown, the impedance Z_o and Z_t vary somewhat linearly over a substantial portion of the curve though there are nonlinearities near the lower and upper magnitudes of error voltage. In the present invention, by varying the load with a change in the conductivity state of the terminating network, the terminating impedance and characteristic impedance vary correspondingly with each other. Consequently, the delay line always appears to be matched.

The voltage variable delay line 3 of FIG. 4 has proven utility in the time-base error corrector networks of video and instrumentation tape transports. Electrically the line appears as a series of inductors L with one end receiving an input signal (video from tape) and the other end tied to the load (output terminal 9). There is an input resistance R_1 extending to ground and an output resistance R_0 extending to ground The junction of successive inductors L joins voltage variable silicon diodes D and D_1. The cathodes of the voltage variable silicon diodes D are common to alternate junctions and the anode of voltage variable silicon diodes D_1 are common to the other junctions. The diodes D_1 extend to a positive bias terminal and the diodes D extend to a negative bias terminal to receive bias potential V_B. The network design provides a push-pull arrangement responsive to the bias signal and has proven beneficial in overcoming superimposition of the bias signal to the information signal along the line. As shown, the information signal from the tape is in frequency modulated form, and bypass capacitors C are incorporated to complete the signal path.

The frequency response and characteristic impedance of this delay line configuration change with the magnitude of the bias signal V_B received by the diodes D and D_1. This variation in the present invention is equalized by incorporating the terminating network 7 of FIG. 2 which tracks the terminating impedance of the delay line in a complementary way to variations in the characteristic impedance.

I claim:

1. A voltage variable delay line having a variable delay responsive to a control signal in combination with a voltage

variable termination network for said line, wherein said network comprises:

a pair of unidirectional conducting components;

prebiasing means connecting each said component between fixed reference potential levels such that each component is prebiased in a forward conducting state;

fixed load resistance means connecting said components in opposite polarity senses to a terminal end of said line to provide a net line termination impedance dependent upon the state of conduction of said components; and

control valve means connected to each said component for varying the bias level thereof to jointly increase or decrease electrical conduction of said components in response to the control signal, said control valve means having adjustment means for presetting maximum and minimum responses of the control valves to the control signal whereby the termination impedance may be adjusted to match a characteristic impedance of the delay line over a range of control signal levels.

2. The combination as defined in claim 1, said control valve means comprising a pair of complementary control valves, each having an output connected to one of said unidirectionally conducting components and said valves being responsive to opposing phase drive signals for jointly increasing or decreasing conduction of said components, and circuit means connected to said control valves providing said drive signals is response to the instantaneous magnitude of said control signal.

3. The combination as defined in claim 2, said components being connected with one set of opposite polarity terminals jointly to a common reference plane and with their other terminals to the respective output of said control valves, said control valves functioning at their outputs to jointly increase or decrease in magnitude but in opposite polarity directions relative to said reference plane in response to variations of said control signal.

4. The combination as defined in claim 3, said circuit means comprising a phase splitter circuit providing said opposing phase drive signals, and said adjustable means for presetting the maximum and minimum responses of said control valve means comprising an emitter follower stage having an input circuit adapted to receive said control signal and including a variable resistance for presetting the termination impedance of said network to a value matching the characteristic impedance of the delay line at one limit of the range of said control signal and said emitter follower stage having an output circuit including a variable potentiometer with the piper arm connected to said phase splitter and being adjustable to preset the termination impedance of said network to a value matching the characteristic impedance of the delay line at the other limit of the range of said control signal.

5. The combination as defined in claim 4, said input circuit of said emitter follower stage further comprising a diode connected to said variable resistance for providing a nonlinear response at the output of said emitter follower stage in response to said control signal, wherein said nonlinear response is adjusted to compensate for a nonlinear relationship between the characteristic impedance of said delay line in its response to said control signal.

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UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,558,933 Dated January 26, 1971

Inventor(s) Henry O. Meyer

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

On the cover page, before the Abstract, insert the followi paragraph -- The invention herein described was ma in the course of or under a contract or subcontrac thereunder with the Department of Defense of the United States. --

Column 2, line 50, delete "network" and insert -- net --

Column 3, line 56, delete "extend" and insert -- tend --

Column 4, lines 4 and 5, delete "line 3 components may be selected"

Column 4, lines 28 and 29, delete "vibrations" and insert -- variations --

Column 5, line 27, delete "is" and insert -- in --

Column 6, line 7, delete "3" and insert -- 2 --

Column 6, line 17, delete "piper" and insert -- wiper --

Signed and sealed this 6th day of June 1972.

(SEAL)
Attest:

EDWARD M.FLETCHER,JR.
Attesting Officer

ROBERT GOTTSCHALK
Commissioner of Patents