



(51) International Patent Classification:

H05K 1/02 (2006.01) H05K 3/40 (2006.01)

H05K 1/11 (2006.01) H05K 1/18 (2006.01)

H05K 3/34 (2006.01)

(21) International Application Number:

PCT/EP2018/083826

(22) International Filing Date:

06 December 2018 (06.12.2018)

(25) Filing Language:

English

(26) Publication Language:

English

(71) Applicant: HELLA GMBH & CO. KGAA [DE/DE];

Rixbecker Straße 75, 59552 Lippstadt (DE).

(72) Inventors: POZZA, Mathieu; 1185 route de Rieumes,

31470 Sainte Foy de Peyrolles (FR). SIGAUD, Laurent;

4 rue du Pr. Pierre Vellas, 31300 Toulouse (FR).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM,

AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH,

GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— of inventorship (Rule 4.17(iv))

Published:

— with international search report (Art. 21(3))

(54) Title: PRINTED CIRCUIT BOARD

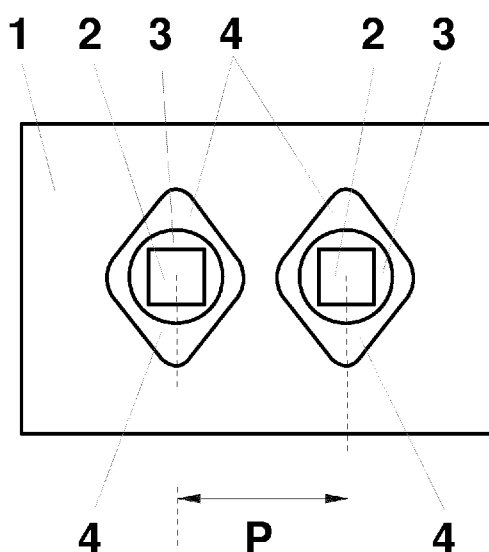


Fig. 1

(57) Abstract: The invention is related to a printed circuit board (PCB) (1) for electrical and/or electronic devices, wherein the PCB (1) comprises at least two adjacent through holes (3) each through hole (3) for receiving a correspondent contact pin (2) of an electrical or electronic component and wherein the through hole (3) is surrounded by a layer (4) of conductive material plated on a surface of the PCB (1). A pitch (P) between through holes (3) shall be reduced without rising the risk for bridging and without negatively affecting the possibility of automatic optical inspection of the readily soldered connection. This is achieved by that the form of the layer (4) is oblong wherein a smaller extension of that form is parallel to a pitch (P) between centres of two adjacent of the through holes (3).

Printed Circuit Board

Description

The invention is related to a printed circuit board (PCB) or electrical and/or electronic devices, wherein the PCB comprises at least two adjacent through holes each through hole for receiving a correspondent contact pin of an electrical or electronic component and wherein the through hole is surrounded by a layer of conductive material plated on the surface of the PCB.

Such PCBs are well known in the art. They are used for building circuits and/or logics by fitting and connecting the components such as for example connectors, resistors and circuits. At least parts of the components have pins that are connected by soldering to the PCB in through holes comprising eyelets. The eyelets known in the art have a circular form.

The readily assembled PCBs are used in devices such as mobile phones, computers and control systems of autocars.

There is a tendency of and a demand for the components and the devices getting smaller and lighter. As a result the distance (pitch) between two adjacent through holes tends to get smaller leading to problems in soldering and automatic inspection when using the known eyelets.

EP 1 174 951 B1 discloses an electrical and mechanical connection between pins of a contact and a PCB. The PCB has through holes for receiving the pins, the holes being surrounded by an annular conductive layer (eyelet). In order to reduce the risk of arcing when applying high voltage a peripheral part of the layer is removed, by that enlarging the distance between two adjacent layers. The layers are circular before and after the removal. Removing the part of the layer is intricate; requirements of area and space remain unchanged.

It is the aim of the invention to provide a PCB where a pitch between through holes can be reduced without rising the risk for solder bridging and without negatively affecting the possibility of automatic optical inspection of the readily soldered connection.

The aim is achieved by an oblong form of the layer (eyelet) wherein a smaller extension of that form is parallel to a pitch between centres of two adjacent of the through holes. By that a distance between adjacent through holes can be reduced without reducing the clearance between edges of two respective layers. The risk of solder bridging remains low.

Furthermore the total area of the layer is not or only marginally reduced resulting in a good quality of soldering and in the possibility to execute automatic optical inspection of the connection.

The dependent claims apply to advantageous embodiments of the invention.

The elliptic, rhombic or rectangular forms are easily to be performed.

Rounded corners of the layer reduce the needs of solder material and in the case of the rhombic form the maximum width of the layer.

The pitch of 2.2 mm is optimal for achieving a good connection and for avoiding solder bridging as well as for allowing automatic optical inspection when reducing the pitch. The reduction is more than 10 % compared to the pitch known in the art.

The invention is explained in more detail in conjunction with the accompanying drawings wherein the only

Figure 1 shows an enlarged plan view of a surface of a part of a PCB.

A printed circuit board (PCB) 1, a small part of which is shown in figure 1 as a front view of a surface, comprises a plurality of electrical leads (not shown) arranged on surfaces of the PCB 1 and/or within the PCB 1. On at least one of the surfaces is ar-

ranged a plurality of electrical and/or electronic components and/or connectors which are selectively connected by the leads. The components and/or connectors are each mounted on the respective surface (surface mounted device SMD) or, as shown in the figure 1, with the aid of contact pins 2 which are plugged in through holes 3 and soldered.

A pitch P, that is a shortest distance of the centres of two adjacent through holes 3, is 2.2 mm. Each through hole 3 is surrounded by a layer 4 of conductive material (eyelet). The layer 4 is plated on that one surface of the PCB 1 where soldering of the respective contact pin 2 is performed. Soldering is for contacting and fastening the contact pins 2 and by that the component and/or the connector to the PCB 1.

The form of the layer 4 (eyelet) is longitudinal, that is: the maximum extension of the form in a first direction is longer than that in a second direction orthogonal to the first one. In short: the length of the layer 4 is greater than its width. The shorter second direction is parallel to the pitch P. By that the area of the layer 4 as well as the distance between two adjacent layers 4 are sufficient large; soldering can be automatically inspected by optical means and the pitch P can be reduced without rising the risk of solder bridging.

The form of the layer 4 according to the example of the figure 1 is rhombic with strongly rounded corners.

The PCB 1 is assembled, soldered and automatically inspected as known in the art.

List of Reference Signs

- 1 Printed circuit board (PCB)
- 2 contact pin
- 3 through hole
- 4 layer
- 5
- P pitch

Claims

1. Printed circuit board (PCB) for electrical and/or electronic devices,
wherein the PCB (1) comprises at least two adjacent through holes (3) each
through hole (3) for receiving a correspondent contact pin (2) of an electrical or
electronic component and
wherein the through hole (3) is surrounded by a layer (4) of conductive material
plated on a surface of the PCB (1),
characterised in that the form of the layer (4) is oblong wherein a smaller extension
of that form is parallel to a pitch (P) between centres of two adjacent of the through
holes (3).
2. The PCB of claim 1, characterised in that the form of the layer (4) is elliptic.
3. The PCB of claim 1, characterised in that the form of the layer (4) is rhombic.
4. The PCB of claim 1, characterised in that the form of the layer (4) is rectangular.
5. The PCB of claim 3 or 4, characterised in that corners of the layer (4) are rounded.
6. The PCB of one of the claims 1 to 4, characterised in that the pitch (P) is 2.2 mm
or less.

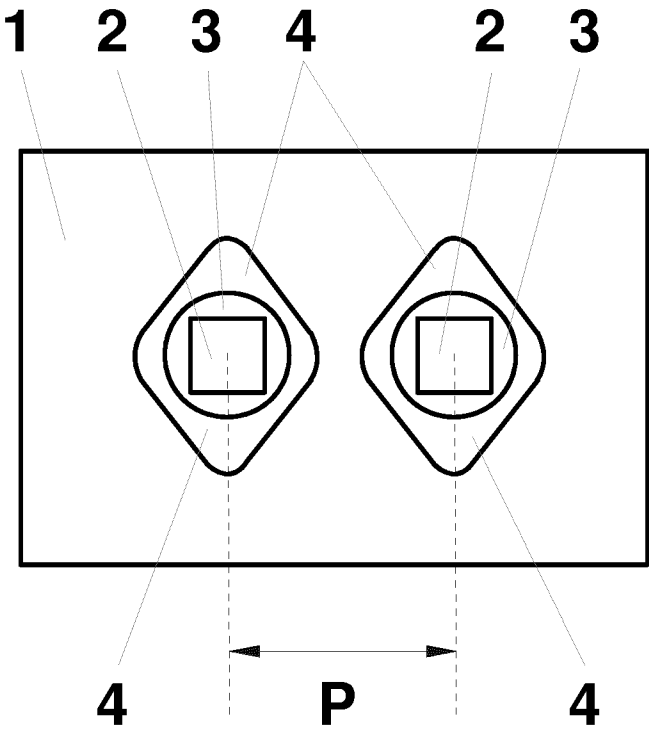


Fig. 1

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2018/083826

A. CLASSIFICATION OF SUBJECT MATTER

INV. H05K1/02 H05K1/11 H05K3/34 H05K3/40
ADD. H05K1/18

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H05K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2017/336584 A1 (ARIGA MAIKO [JP] ET AL) 23 November 2017 (2017-11-23) paragraphs [0023], [0026], [0028], [0030], [0035], [0036], [0040], [0050]; figures 1, 3B	1,2,4-6
X	JP H03 55899 A (IBIDEN CO LTD) 11 March 1991 (1991-03-11) figures 1,3,4,7c	1-3,5,6



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

23 August 2019

Date of mailing of the international search report

29/08/2019

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Tomezak, Alexandre

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2018/083826

Patent document cited in search report	Publication date	Patent family member(s)	Publication date	
US 2017336584	A1	23-11-2017	CN 107251663 A	13-10-2017
			JP W02016129277 A1	24-11-2017
			US 2017336584 A1	23-11-2017
			WO 2016129277 A1	18-08-2016

JP H0355899	A	11-03-1991	NONE	
